STE2004S

102 x 65 single-chip LCD controller/driver

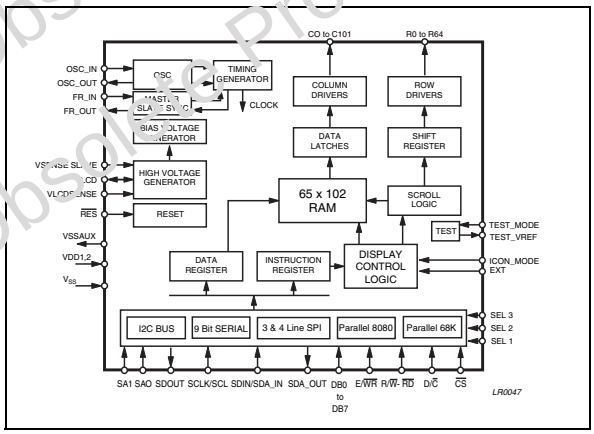
Features

- 102 x 65 bits display data RAM
- Programmable MUX rate
- Programmable frame rate
- X,Y programmable carriage return
- Dual partial display mode
- Row by row scrolling
- N-line inversion
- Automatic data RAM blanking procedure
- Selectable input interface:
  - I^2C Bus Fast and Hs-mode (read and write)
  - 8000 and 8080 Parallel Interfaces (read and write)
  - 3-lines and 4-lines SPI Interface (read and write)
  - 3-lines 9 bit Serial Interface (read and write)
- Fully integrated configurable LCD bias voltage generator with:
  - Selectable multiplication factor (up to 5x)
  - Effective sensing for high precision output
  - Eight selectable temperature compensation coefficients
- CMOS compatible inputs
- Fully integrated oscillator requires no external components
- Designed for chip-on-glass (COG) applications.
- Low power consumption, suitable for battery operated systems
- Logic supply voltage range from 1.7 to 3.6V
- High voltage generator supply voltage range from 1.75 to 4.5V
- Display supply voltage range from 4.5 to 14.5V
- Backward compatibility with STE2001/2/4

Description

The STE2004S is a low power CMOS LCD controller driver. Designed to drive a 65 rows by 102 columns graphic display, it provides all necessary functions in a single chip, including on-chip LCD supply and bias voltages generators, resulting in a minimum of externals components and in a very low power consumption.

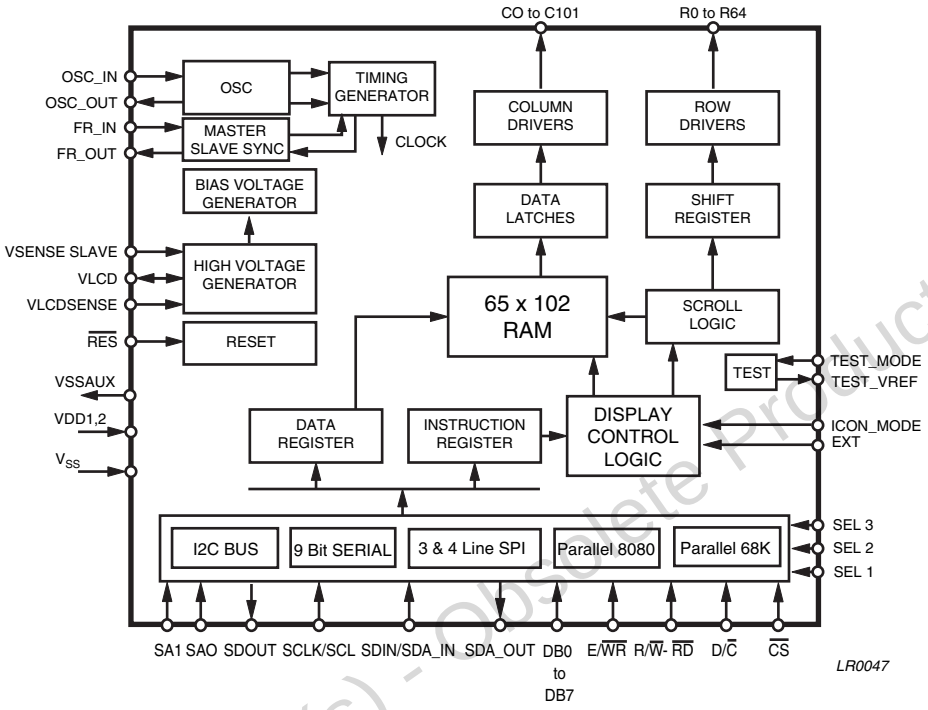
STE2004S features six standard interfaces (3-lines Serial, 3-lines SPI, 4-lines SPI, 68000 Parallel, 8080 parallel and I^2C) for interfacing with the host micro-controller.



Contents

1 Block diagram

Figure 1. STE2004S block diagram



2 Pin description

Table 1. Pin description

<table>
<tr><th>N°</th><th>Pad</th><th>Type</th><th>Function</th></tr>
<tr><td>R0 to R64</td><td>1-6
109-141</td><td>O</td><td>LCD row driver output</td></tr>
<tr><td>C0 to C101</td><td>6-107</td><td>O</td><td>LCD column driver output</td></tr>
<tr><td>V_{SS}</td><td>192-203</td><td>GND</td><td>Ground pads.</td></tr>
<tr><td>V_{DD1}</td><td>156-163</td><td>Supply</td><td>IC positive power supply</td></tr>
<tr><td>V_{DD2}</td><td>164-171</td><td>Supply</td><td>Internal generator supply voltages.</td></tr>
<tr><td>V_{LCD}</td><td>205-209</td><td>Supply</td><td>Voltage multiplier output</td></tr>
<tr><td>$V_{LCDSENSE}$</td><td>204</td><td>Supply</td><td>Voltage multiplier regulation input. V_{LCDOUT} sensing for output voltage fine tuning</td></tr>
<tr><td>V_{SENSE_SLAVE}</td><td>145</td><td>Supply</td><td>Voltage reference for slave charge pump</td></tr>
<tr><td>V_{SSAUX}</td><td>190-177-147</td><td>O</td><td>Ground reference for pins configuration</td></tr>
<tr><td>V_{DD1AUX}</td><td>142</td><td>O</td><td>VDD1 reference for pins configuration</td></tr>
<tr><td>SEL1,2,3</td><td>152
153
154</td><td>I</td><td>Interface mode selection - cannot be left floating
<table>
<tr><th>SEL3</th><th>SEL2</th><th>SEL1</th><th>Interface</th></tr>
<tr><td>GND/VSSAUX</td><td>GND/VSSAUX</td><td>GND/VSSAUX</td><td>I^2C</td></tr>
<tr><td>GND/VSSAUX</td><td>GND/VSSAUX</td><td>VDD1</td><td>SPI 4-Lines 8 bit</td></tr>
<tr><td>GND/VSSAUX</td><td>VDD1</td><td>GND/VSSAUX</td><td>SPI 3-Lines 8 bit</td></tr>
<tr><td>GND/VSSAUX</td><td>VDD1</td><td>VDD1</td><td>Serial 3-Lines 9 bit</td></tr>
<tr><td>VDD1</td><td>GND/VSSAUX</td><td>GND/VSSAUX</td><td>Parallel 8080-series</td></tr>
<tr><td>VDD1</td><td>GND/VSSAUX</td><td>VDD1</td><td>Parallel 68000-series</td></tr>
</table></td></tr>
<tr><td>EXT_SET</td><td>151</td><td>I</td><td>Extended instruction set selection - cannot be left floating
<table>
<tr><th>Ext pad config</th><th>Instruction set selected</th></tr>
<tr><td>GND or VSSAUX</td><td>BASIC</td></tr>
<tr><td>VDD1</td><td>EXTENDED</td></tr>
</table></td></tr>
<tr><td>ICON_MODE</td><td>155</td><td>I</td><td>Extended instruction set selection - cannot be left floating
<table>
<tr><th>Icon mode pad config</th><th>Icon mode status</th></tr>
<tr><td>GND or VSSAUX</td><td>DISBLED</td></tr>
<tr><td>VDD1</td><td>ENABLED</td></tr>
</table></td></tr>
<tr><td>SDOUT</td><td>180</td><td>O</td><td>Serial and SPI data output - if unused must be left floating</td></tr>
<tr><td rowspan="2">SDIN - SDAIN</td><td rowspan="2">179</td><td>I</td><td>SDIN - Serial and SPI interface data input - cannot be left floating</td></tr>
<tr><td>I</td><td>SDAIN - I^2C bus data in - cannot be left floating</td></tr>
</table>

Table 1. Pin description (continued)

<table>
<tr><th>N°</th><th>Pad</th><th>Type</th><th>Function</th></tr>
<tr><td rowspan="2">SCLK - SCL</td><td rowspan="2">181</td><td>I</td><td>SCLK - Serial and SPI interface clock - cannot be left floating</td></tr>
<tr><td>I</td><td>SCL - I^2C bus clock - cannot be left floating</td></tr>
<tr><td>SDA_OUT</td><td>178</td><td>O</td><td>I^2C Bus data out - if unused must be left floating</td></tr>
<tr><td>SA0</td><td>149</td><td>I</td><td>I^2C slave address BIT 0 - cannot be left floating</td></tr>
<tr><td>SA1</td><td>148</td><td>I</td><td>I^2C slave address BIT 1- cannot be left floating</td></tr>
<tr><td>DB0 to DB7</td><td>182-189</td><td>I/O</td><td>Parallel interface 8 bit data bus - cannot be left floating</td></tr>
<tr><td rowspan="2">R/$\overline{W}$ - $\overline{RD}$</td><td rowspan="2">175</td><td>I</td><td>R/$\overline{W}$ - 68000 Series Parallel interface read and write control input - cannot be left floating</td></tr>
<tr><td>I</td><td>$\overline{RD}$ - 8080 Series Parallel interface read enable clock input - cannot be left floating</td></tr>
<tr><td>E / $\overline{WR}$</td><td>176</td><td>I</td><td>E - 68000 Series Parallel interface read and write clock input - cannot be left floating</td></tr>
<tr><td>E / $\overline{WR}$</td><td>176</td><td>I</td><td>$\overline{WR}$ - 8080 Series Parallel interface - write enable clock input - cannot be left floating</td></tr>
<tr><td>RES</td><td>172</td><td>I</td><td>Reset input. Active Low.</td></tr>
<tr><td>D/$\overline{C}$</td><td>174</td><td>I</td><td>Interface data/command selector- cannot be left floating</td></tr>
<tr><td>CS</td><td>173</td><td>I</td><td>Serial and Parallel interfaces ENABLE. When Low the incoming data are clocked In. Cannot be left floating</td></tr>
<tr><td>TEST_MODE</td><td>191</td><td>I</td><td>Test Pad - 50 kohm internal pull-down must be connected to VSS/VSSAUX</td></tr>
<tr><td>TEST_VREF</td><td>146</td><td>O</td><td>Test Pad - must be left floating</td></tr>
<tr><td>OSCIN</td><td>144</td><td>I</td><td>Oscillator Input:
<table>
<tr><th>OSC_IN</th><th>Configuration</th></tr>
<tr><td>High</td><td>Internal oscillator enabled</td></tr>
<tr><td>Low</td><td>Internal oscillator disabled</td></tr>
<tr><td>External Oscillator</td><td>Internal oscillator disabled</td></tr>
</table></td></tr>
<tr><td>OSCOUT</td><td>210</td><td>O</td><td>Internal/external oscillator out - if unused must be left floating</td></tr>
<tr><td>FR_OUT</td><td>211</td><td>O</td><td>Master slave frame inversion synchronization - f unused must be left floating</td></tr>
<tr><td>FR_IN</td><td>143</td><td>I</td><td>Master slave frame inversion synchronization - cannot be left floating</td></tr>
<tr><td>M/$\overline{S}$</td><td>100</td><td>I</td><td>Master/slave configuration bit:- cannot be left floating
<table>
<tr><th>M/$\overline{S}$ PIN</th><th>OSC_OUT</th><th>FR_OUT</th><th>FR_IN</th><th>Charge Pump</th></tr>
<tr><td>High</td><td>ENABLED</td><td>Enabled</td><td>Disabled</td><td>AuxVsense disabled</td></tr>
<tr><td>Low</td><td>ENABLED</td><td>Enabled</td><td>Enabled</td><td>Charge pump in slave mode or ext power</td></tr>
</table></td></tr>
</table>

Figure 2. Chip mechanical drawing

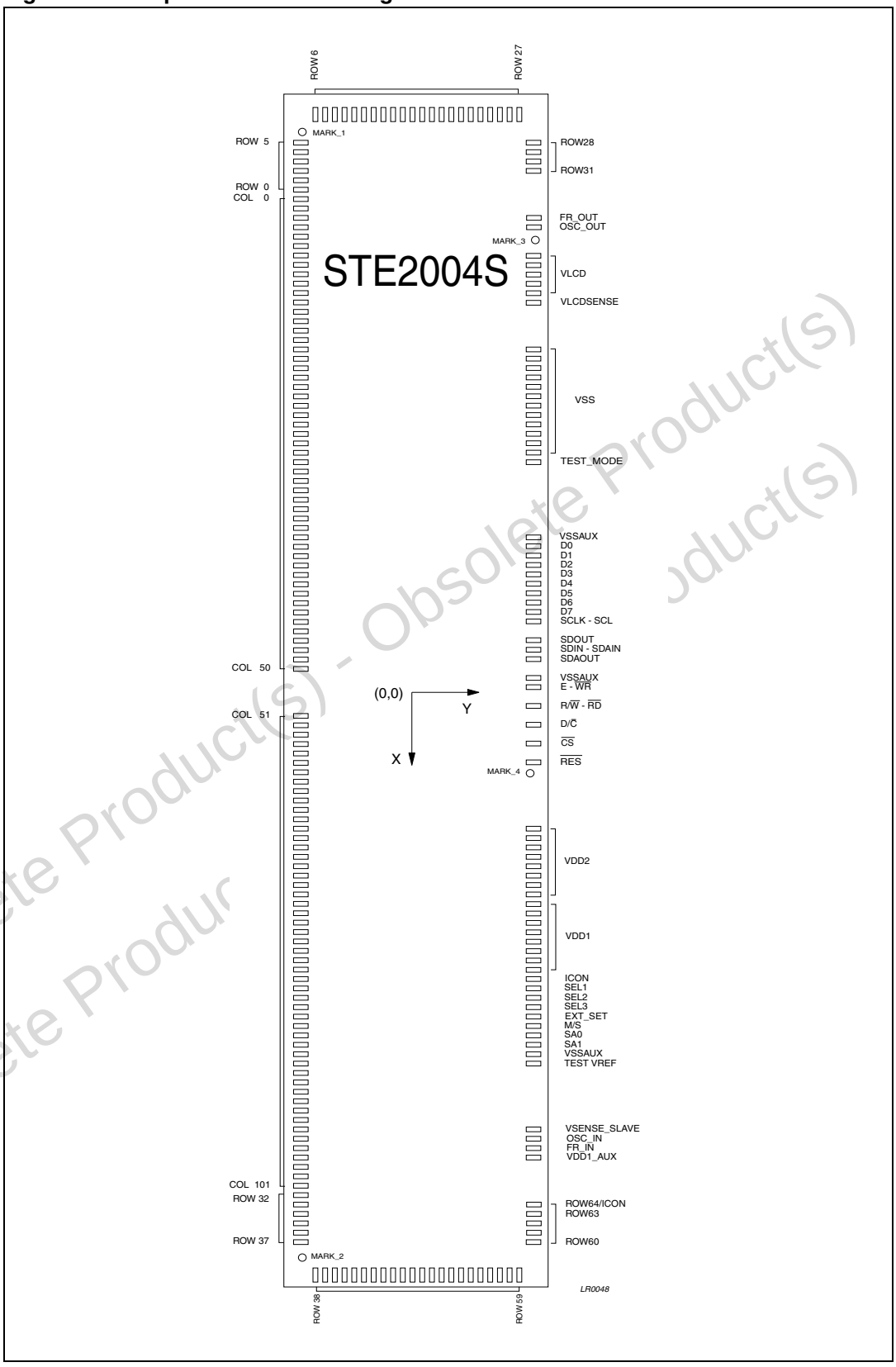
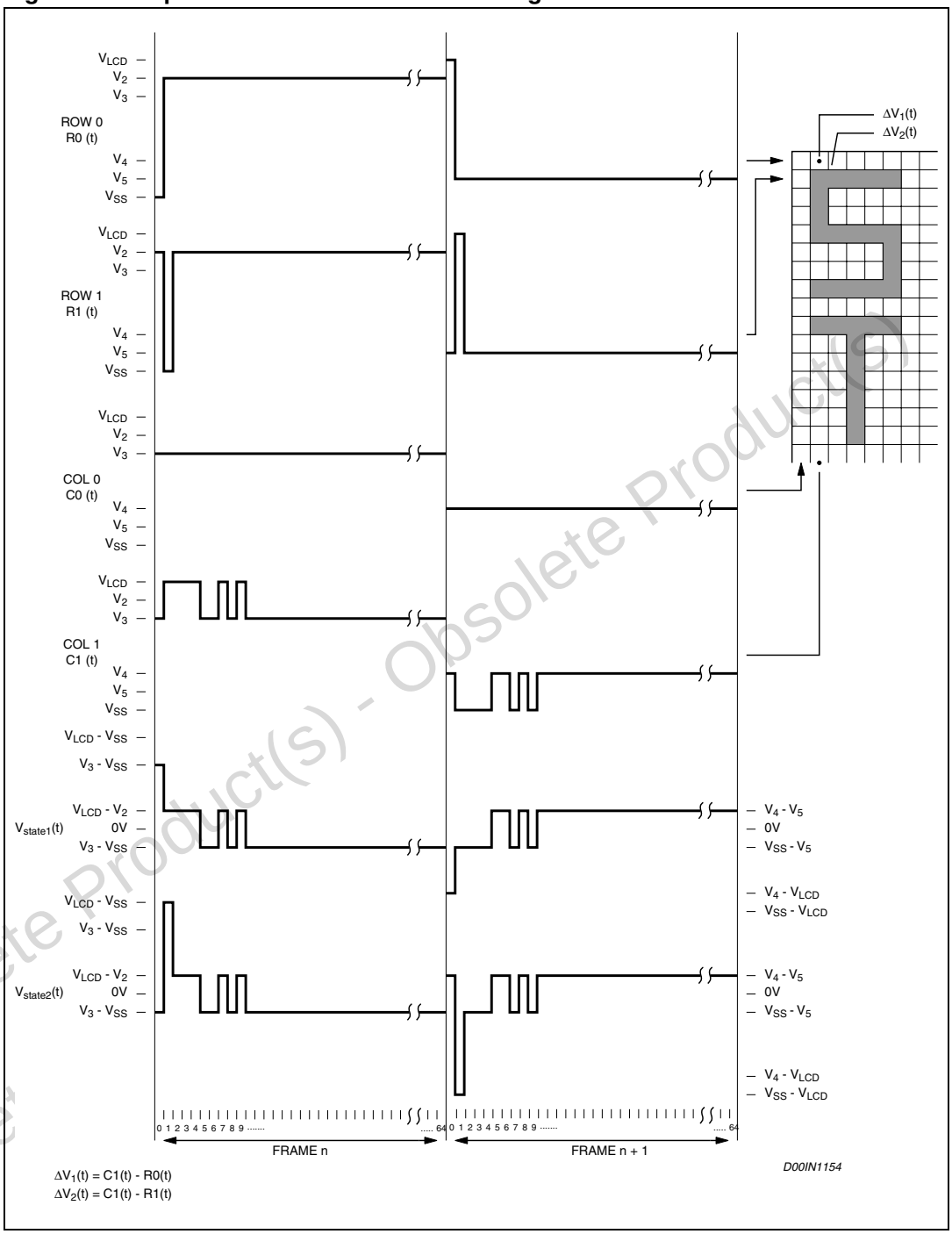


Figure 3. Improved ALTH and PLESKO driving method



3 Circuit description

3.1 Supplies voltages and grounds

V_{DD2} supplies voltages to the internal voltage generator (see below). If the internal voltage generator is not used, this should be connected to V_{DD1} pad. V_{DD1} supplies the rest of the IC. V_{DD1} supply voltage could be different form V_{DD2}.

$$V_{DD2} \geq \frac{2 \cdot VLCD}{(n+4)} + 200mV$$

3.2 Internal supply voltage generator

The IC has a fully integrated (no external capacitors required) charge pump for the liquid crystal display (LCD) supply voltage generation. The multiplying factor can be programmed to be: Auto, X5, X4, X3, X2, using the 'set CP multiplication' command. If auto is set, the multiplying factor is automatically selected to have the lowest current consumption in every condition, allowing an input voltage that changes over time and a constant V_{LCD} voltage. The output voltage (V_{LCD}) is tightly controlled through the $V_{LCDSENSE}$ pad. For this voltage, eight different temperature coefficients (TC, rate of change with temperature) can be programmed using the bits TC1, TC0, T2, T1, T0, to ensure there is no contrast degradation over the LCD operating range.

An external supply could be connected to V_{LCD} to supply the LCD without using the internal generator. In such event the internal voltage generator must be programmed to zero (PRS = [0;0], Vop = 0 - reset condition) and the charge pump (CP[0;0]) set to 5x or quto mode.

3.3 Oscillator

A fully integrated oscillator (requires no external components) is present to provide the clock for the display system. When used the OSC pad must be connected to V_{DD1} pad. An external oscillator could be used and fed into the OSC pin. If an external oscillator is used, it must be always present when STE2004S is not in power down mode. An oscillator out is provided on the OSCOUT Pad to cascade two or more drivers.

3.4 Master/slave mode

STE2004S supports the master slave working mode for both control logic and charge pump. This function allows to drive matrix such as 204x65 or 102x130 using two synchronized STE2004S and the internal charge pump of both devices.

If M/$\overline{S}$ is connected to VDD1, the driver is configured to work in master mode. When STE2004S is in master mode, the Vsense_Slave pin is disabled and the VLCD value can be controlled using Vop bits. The master time generator outputs the relevant timing references on FR_OUT and OSC_OUT.

If M/$\overline{S}$ is connected to GND, the driver is configured to work in slave mode. When STE2004S is in slave mode, the VLCD configuration set by Vop registers and the thermal compensation slope set by TC register, are neglected. The VLCD value generated is equal to the voltage value present on the Vsense_Slave pin so the slave configuration can follow

the master configuration. The only recognized configuration is Vop=0 that forces the charge pump to be in off state whatever is the value of Vsense_aux.

To synchronize the master and slave timing circuits, the slave driver FR_IN pad must be connected to master driver FR_OUT pad, and slave driver OSC_IN pad must be connected to the master driver OSC_OUT Pad (*Figure 4.*). This connection ensures a synchronization at both frame level (R0 on the master is driven together with the Slave R0 driver) and at oscillator level (same frame frequency on the master and on the slave). If the synchronization at frame level is not required, FR_IN pin must be connected toVDD1 or to VDD1_aux (*Figure 5.*).

During the power up procesure, the master device must be forced to exit from power down before the slave device. To enter into PowerDown mode, the slave device must be forced into power down state before master device.

Figure 4. Master slave logic connection with frame synchronization

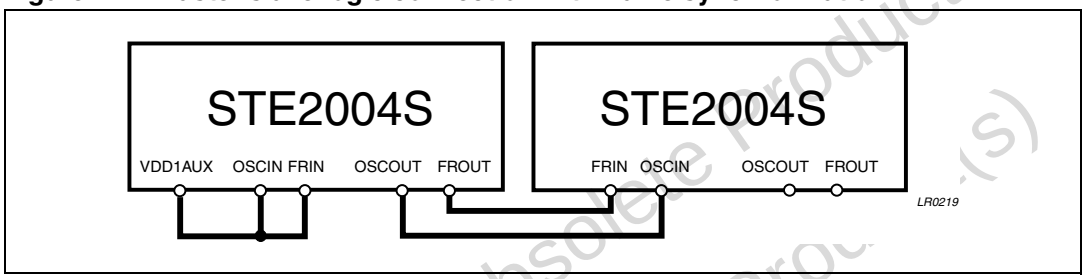
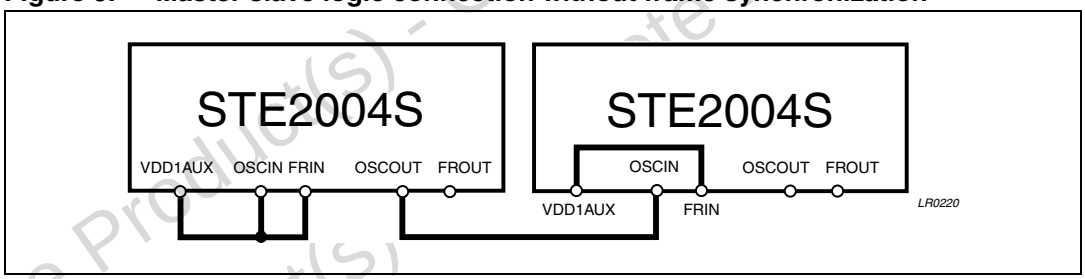


Figure 5. Master slave logic connection without frame synchronization

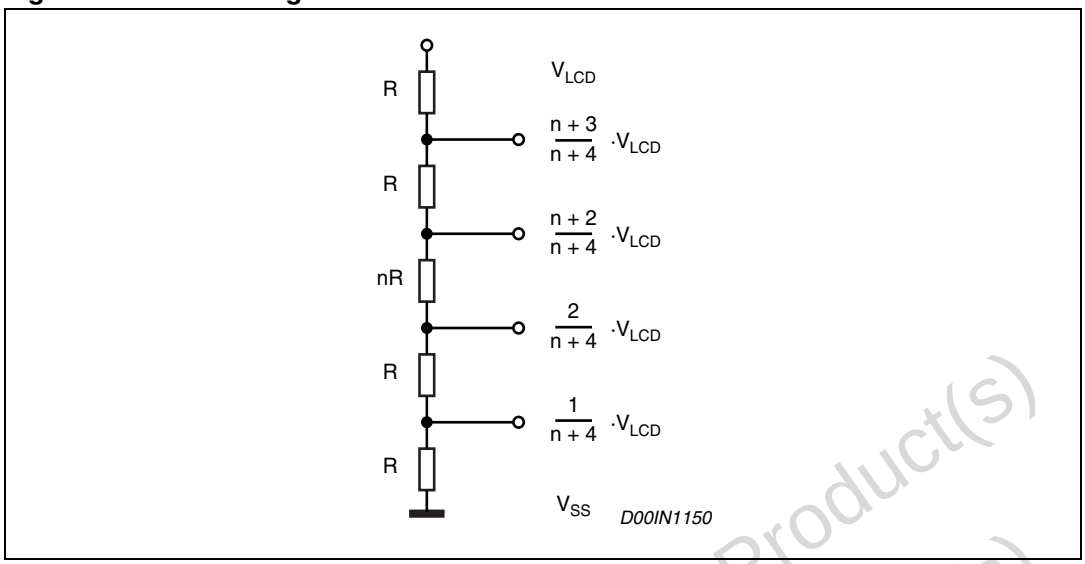


3.5 Bias levels

To properly drive the LCD, six (Including VLCD and VSS) different voltage (Bias) levels are generated. The ratios among these levels and VLCD, should be selected according to the MUX ratio (m). They are established according to the following (*Figure 6.*)

$$V_{LCD}, \frac{n+3}{n+4} V_{LCD}, \frac{n+2}{n+4} V_{LCD}, \frac{2}{n+4} V_{LCD}, \frac{1}{n+4} V_{LCD}, V_{SS}$$

Figure 6. Bias level generator



providing an 1/(n+4) ratio, with n calculated from:

$$n = \sqrt{m} - 3$$

For m = 65, n = 5, a 1/9 ratio is set.

For m = 49, n =4, a 1/8 ratio is set.

The STE2004S provides three bits (BS0, BS1, BS2) for programming the bias ratio as shown below:

Table 2. Bias ratio programmable bits

BS2	BS1	BS0	n
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

The following table shows the bias level for m = 65 and m = 49:

Table 3. Bias level m=65 and m=49

Symbol	m = 65 (1/9)	m = 49 (1/8)
V1	V_{LCD}	V_{LCD}
V2	8/9*V_{LCD}	7/8*V_{LCD}
V3	7/9*V_{LCD}	6/8*V_{LCD}
V4	2/9*V V_{LCD}	2/8*V_{LCD}
V5	1/9 *V_{LCD}	1/8*V_{LCD}
V6	V_{SS}	V_{SS}

3.6 LCD voltage generation

The LCD voltage at reference temperature (To = 27°C) can be set using the VOP register content according to the following formula:

$$V_{LCD}(T=To) = V_{LCD}o = (Ai+V_{OP} \cdot B) \qquad (i=0,1,2)$$

with the following values:

Table 4. LCD voltage generation

Symbol	Value	Unit	Note
Ao	2.95	V	PRS = [0;0]
A1	6.83	V	PRS = [0;1]
A2	10.71	V	PRS = [1;0]
B	0.0303	V	
To	27	°C	

Note that the three PRS values produce three adjacent ranges for VLCD. If the V_{OP} register and PRS bits are set to zero the internal voltage generator is switched off.

The proper value for the VLCD is a function of the liquid crystal threshold voltage (Vth) and of the multiplexing rate. A general expression for this is:

$$V_{LCD} = \frac{1+\sqrt{m}}{\sqrt{2 \cdot \left(1-\frac{1}{\sqrt{m}}\right)}} \cdot V_{th}$$

For MUX Rate m = 65 the ideal V_{LCD} is:

$$V_{LCD(to)} = 6.85 \cdot V_{th}$$

than:

$$V_{op} = \frac{(6.85 \cdot V_{th} - A_i)}{0.03}$$

3.7 Temperature coefficients

As the viscosity, and therefore the contrast, of the LCD are subject to change with temperature, the LCD voltage must be varied with temperature. STE2004S provides eight different temperature coefficients to change the VLCD in a linear fashion against temperature. selectable through T2, T1 and T0 bits. Only four of the temperature coefficients are available through the basic instruction set.

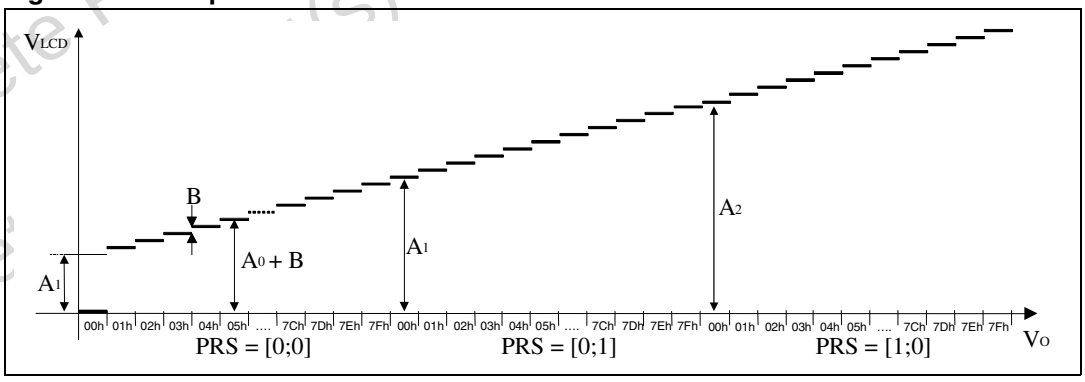
Table 5. Temperature coefficients with basic instruction set

NAME	TC1	TC0	Value	Unit
TC0	0	0	$-0.0 \cdot 10^{-3}$	1/ °C
TC2	0	1	$-0.7 \cdot 10^{-3}$	1/°C
TC3	1	0	$-1.05 \cdot 10^{-3}$	1/°C
TC6	1	1	$-2.1 \cdot 10^{-3}$	1/°C

Table 6. Temperature coefficients

NAME	T2	T1	T0	Value	Unit
TC0	0	0	0	$-0.0 \cdot 10^{-3}$	1/ °C
TC1	0	0	1	$-0.35 \cdot 10^{-3}$	1/°C
TC2	0	1	0	$-0.7 \cdot 10^{-3}$	1/°C
TC3	0	1	1	$-1.05 \cdot 10^{-3}$	1/°C
TC4	1	0	0	$-1.4 \cdot 10^{-3}$	1/°C
TC5	1	0	1	$-1.75 \cdot 10^{-3}$	1/°C
TC6	1	1	0	$-2.1 \cdot 10^{-3}$	1/°C
TC7	1	1	1	$-2.3 \cdot 10^{-3}$	1/°C

Figure 7. Temperature coefficients



Finally, the V_{LCD} voltage at a given (T) temperature can be calculated as:

$$V_{LCD}(T) = V_{LCD}o \cdot [1 + (T\text{-}To) \cdot TC]$$

3.8 Display data RAM

The STE2004S, provides an 102X65 bits static RAM to store display data. This is organized into 9 (Bank0 to Bank8) banks with 102 bytes. One of these banks can be used for icons. RAM access is accomplished in either one of the bus interfaces provided (see below). Allowed addresses are X0 to X101 (Horizontal) and Y0 to Y8 (Vertical).

There are four address mode provided to write to RAM:

- Normal Horizontal (MX=0 and V=0), having the column with address X= 0 located on the left of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer jumps to the following bank and X restarts from X=0. (*Figure 8.*)
- Normal Vertical (MX=0 and V=1), having the column with address X= 0 located on the left of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), X address pointer jumps to next column and Y restarts from Y=0 (*Figure 9*).
- Mirrored Horizontal (MX=1 and V=0), having the column with address X= 0 located on the right of the memory map. The X pointer is increased after each byte written. After the last column address (X=X-Carriage), Y address pointer jumps to the next bank and X restarts from X=0 (*Figure 10.*).
- Mirrored Vertical (MX=1 and V=1), having the column with address X= 0 located on the right of the memory map. The Y pointer is increased after each byte written. After the last Y bank address (Y=Y-Carriage), the X pointer jumps to next column and Y restarts from Y=0 (*Figure 11.*).

After the last allowed address (X;Y)=(X-Carriage; Y-Carriage), the address pointers always jumps to the cell with address (X;Y) = (0;0) (*Figure 12. Figure 13. Figure 14. Figure 15.*).

Data bytes in the memory could have the MSB either on top (D0 = 0, *Figure 16.*) or on the bottom (D0=1, *Figure 17.*).

The STE2004S also allows the normal output address to be altered. The display is mirrored along the X axis if a logic one MY bit is set. Only the memory read process is altered, the content is not affected in memory.

When **ICON MODE=1** the icon row is not mirrored with MY and is not scrolled.

When **ICON MODE=0** the icon row is like an other graphic line and is mirrored and scrolled.

When the partial display mode is disabled, there are three multiplex ratios available (MUX 33, MUX 49 and MUX 65). Only a subset of writable rows are output on row drivers in MUX 33,49 and 65 modes.

When **Y-Carriage<MUX/8**, if MUX 49 is selected only the first 49 memory rows are visualized; if MUX 33 selected, only the first 33 memory rows. The unused output row and column drivers must be left floating.

When **Y-Carriage<=MUX/8** the icon bank is located to BANK 8 in MUX 65 Mode, to BANK6 in MUX 49 Mode, and to BANK 4 in MUX 33 Mode.

In MUX 33 and MUX 49 modes and **Y-Carriage>MUX/8**, only lines 33 and 49 are visualized.

The lines of DDRAM connected on the output drivers using the scrolling function (Range: 0-Y-Carriage*8) are selectable. When **Y-Carriage>MUX/8** lines, the icon row is moved in DDRAM to the first row of the bank, corresponding to the Y-CARRIAGE Return value, being always connected on the same output Driver.

When **MY=0**, the icon Row is output on R64 in MUX 65 mode, on R56 in MUX 49, and on R48 in MUX33.

When **MY=1**, and **ICON MODE=0**, the icon Row is output on R0 whatever the MUX rate.

Figure 8. Automatic data RAM writing sequence with V=0 and data RAM normal format (MX=0)[a]

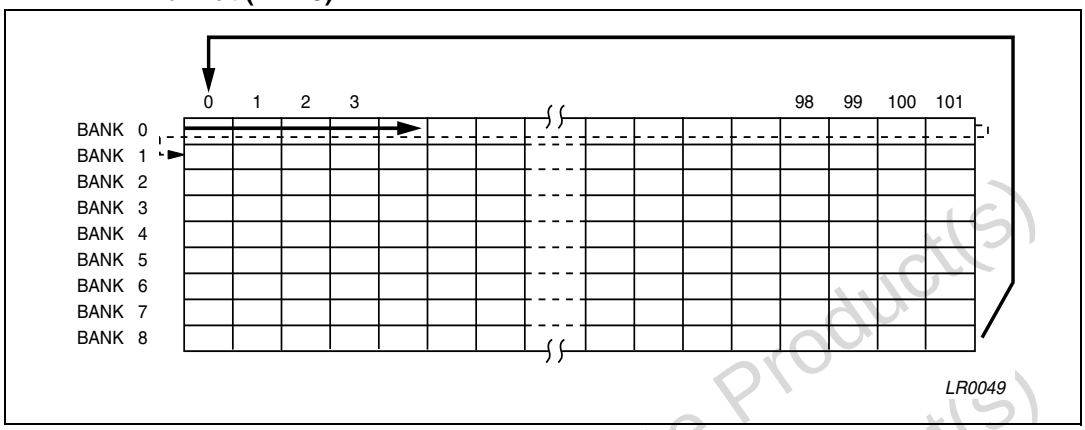
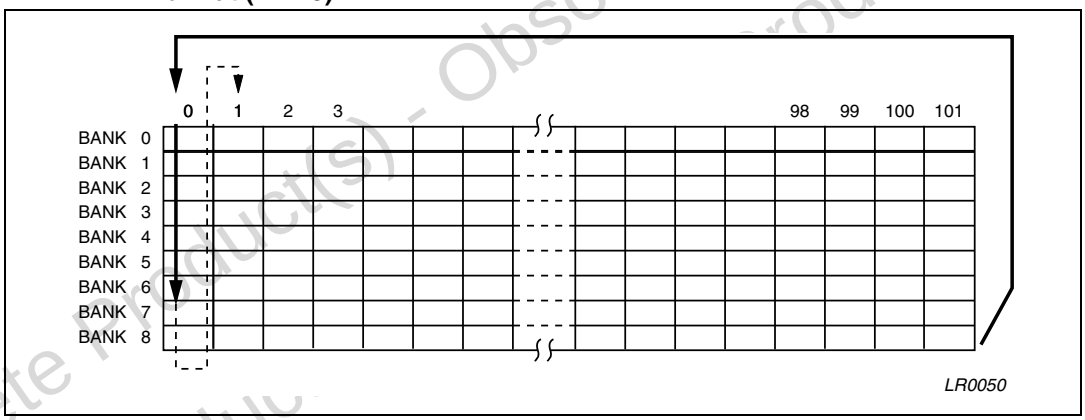


Figure 9. Automatic data RAM writing sequence with V=1 and data RAM normal format (MX=0)[a]



a. X Carriage=101; Y-Carriage = 8

Figure 10. Automatic data RAM writing sequence with V=0 and data RAM mirrored format (MX=1)[a]

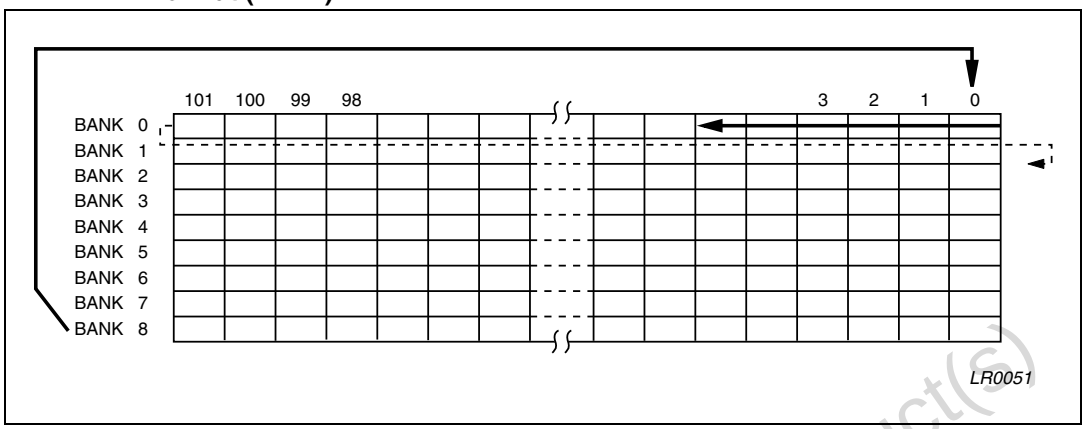


Figure 11. Automatic data RAM writing sequence with V=1 and data RAM mirrored format (MX=1)[a]

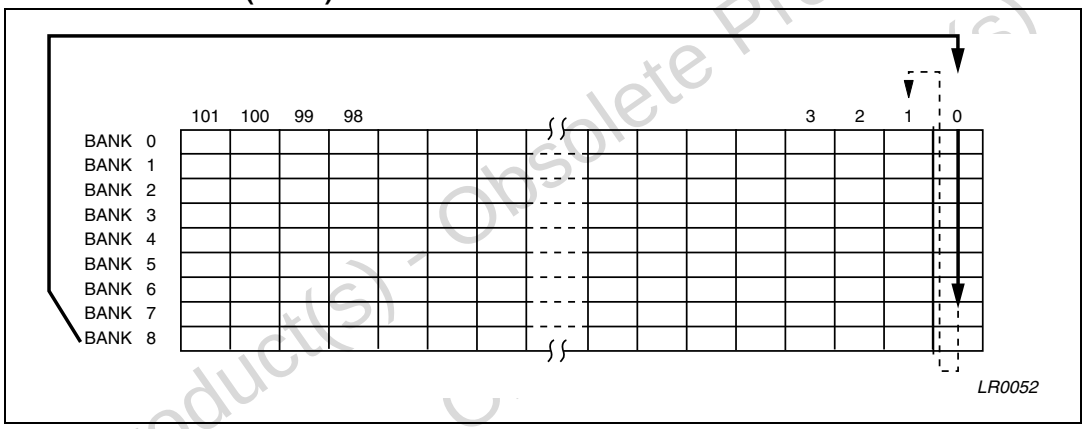


Figure 12. Automatic data RAM writing sequence with X-Y carriage return (V=0; MX=0)

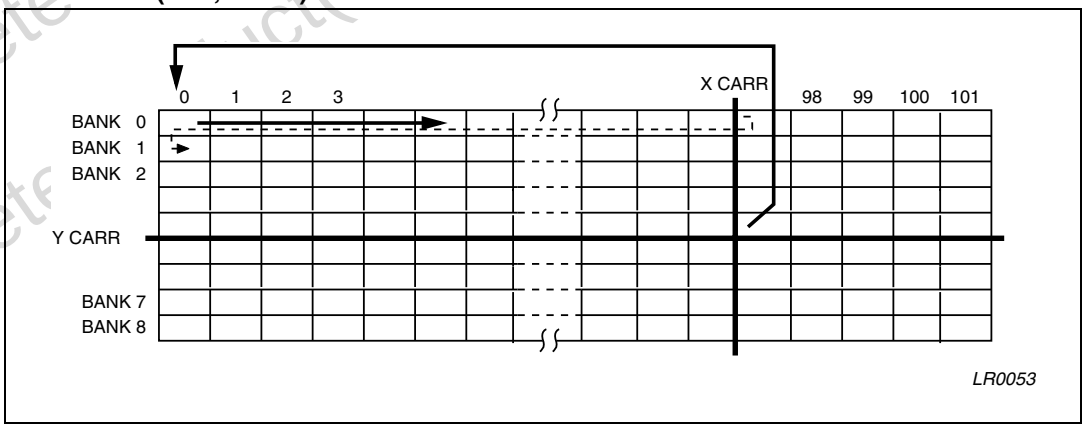


Figure 13. Automatic data RAM writing sequence with X-Y carriage return (V=1; MX=0)

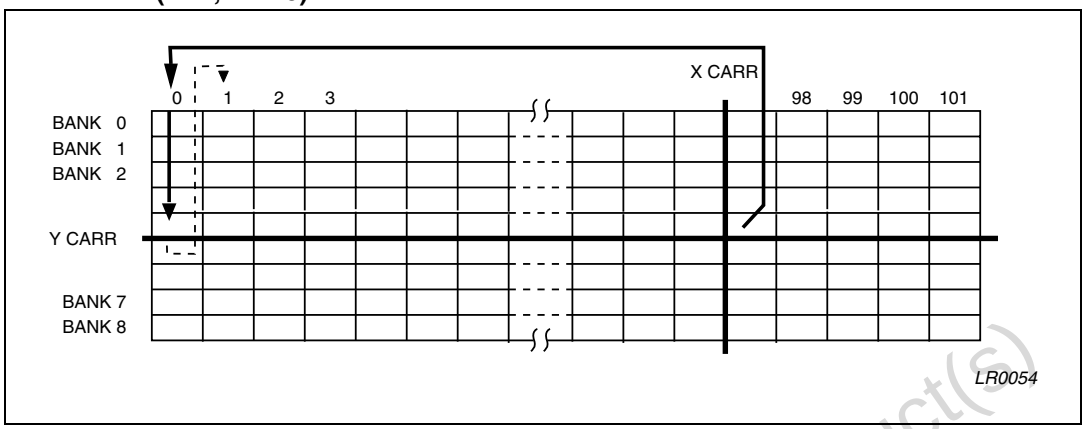


Figure 14. Automatic data RAM writing sequence with X-Y carriage return (V=0; MX=1)

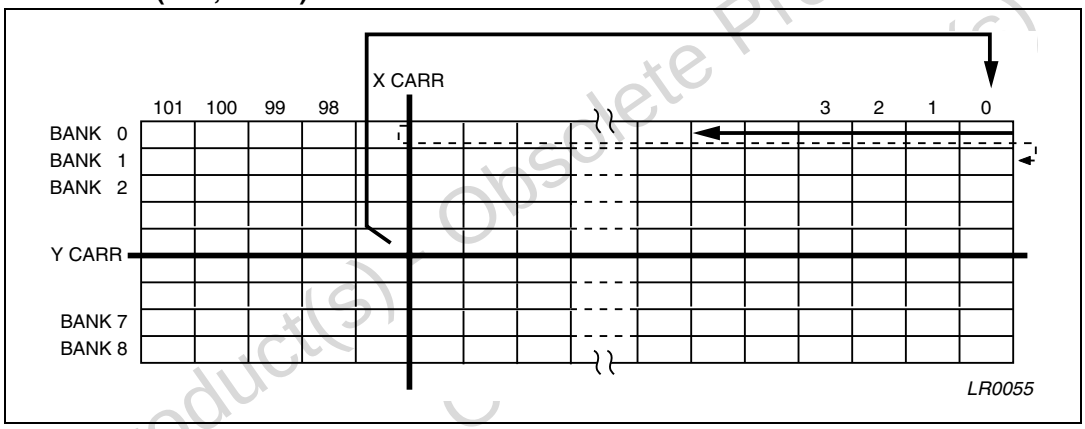


Figure 15. Automatic data RAM writing sequence with X-Y carriage return (V=1; MX=1)

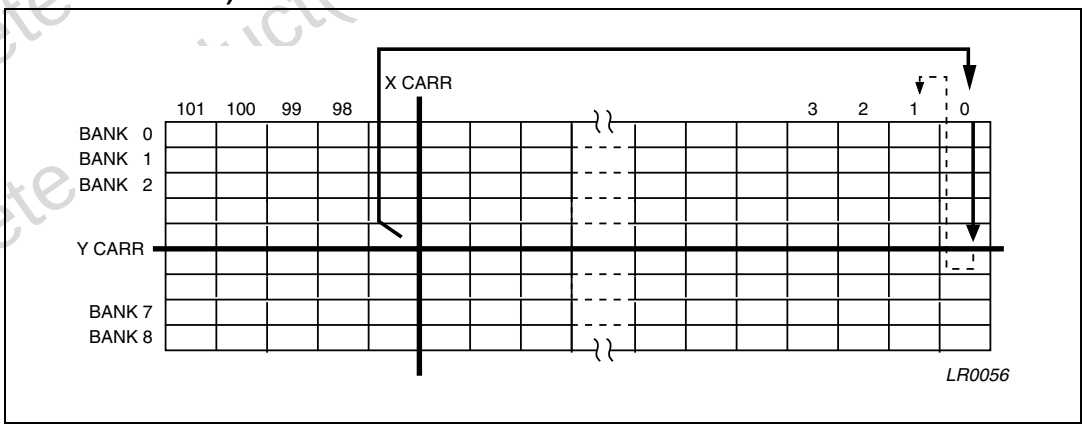


Figure 16. Data RAM Byte organization with D0 = 0

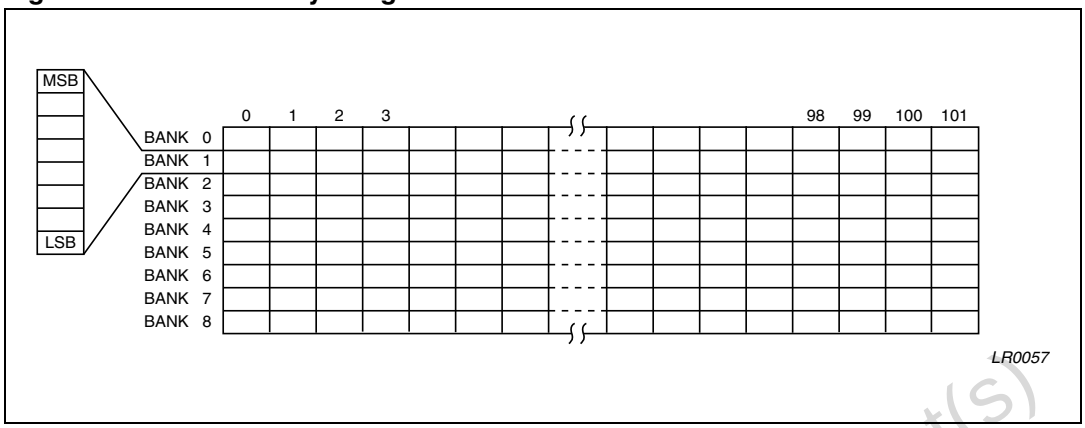


Figure 17. Data RAM byte organization with D0 = 1

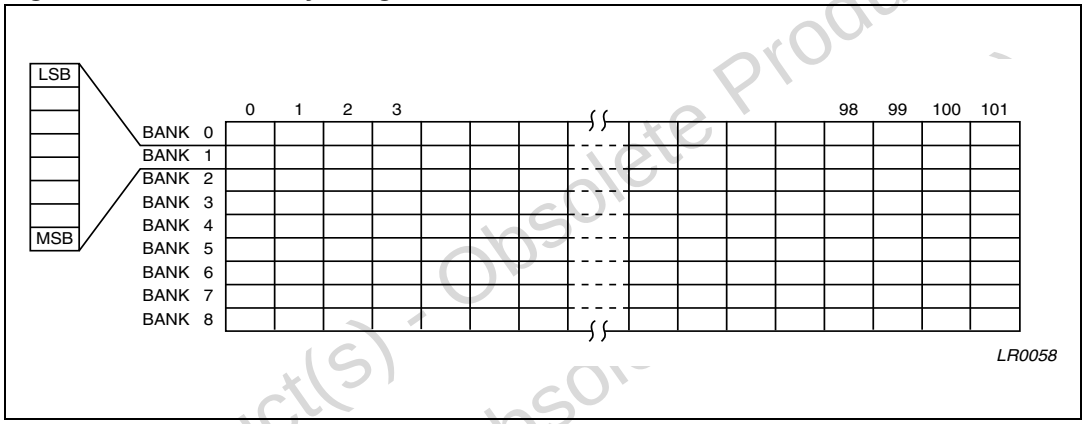


Figure 18. Memory rows vs. row drivers mapping ICON_MODE=1 and MUX 65

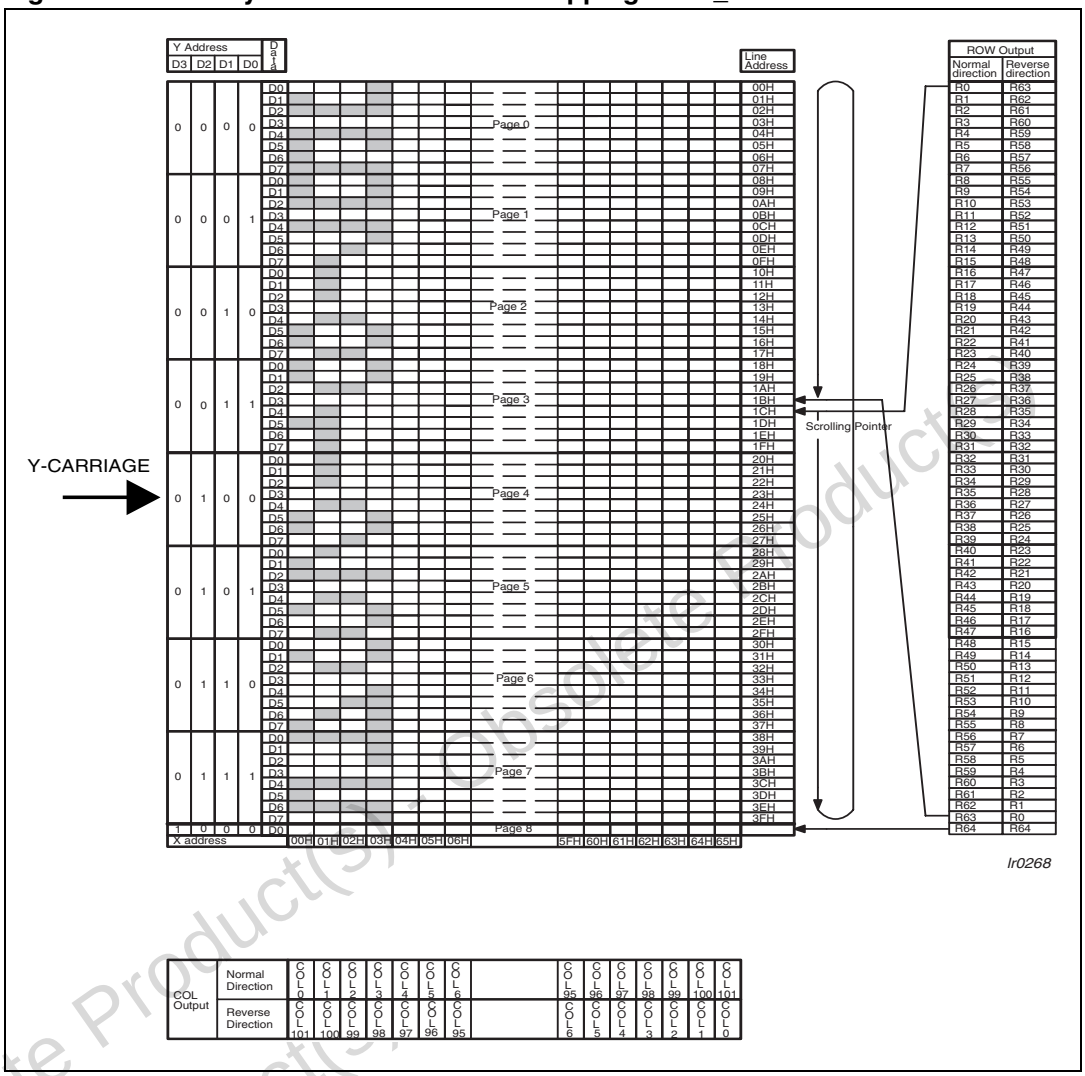


Figure 19. Memory rows vs. row drivers mapping ICON_MODE=0 and MUX 65

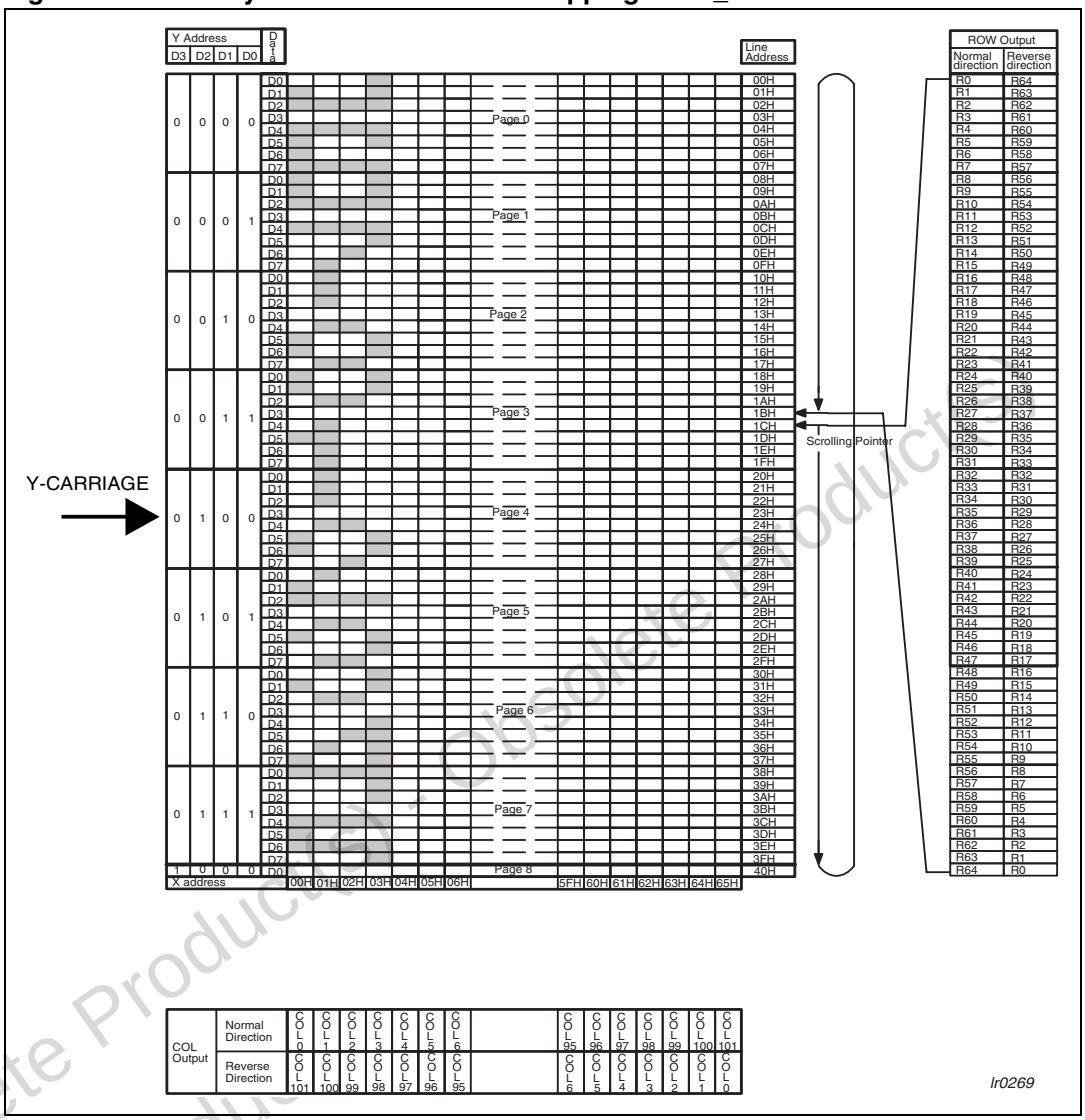


Figure 20. Memory rows vs. Row drivers mapping ICON_MODE=1, Y-Carriage<=6 and MUX 49

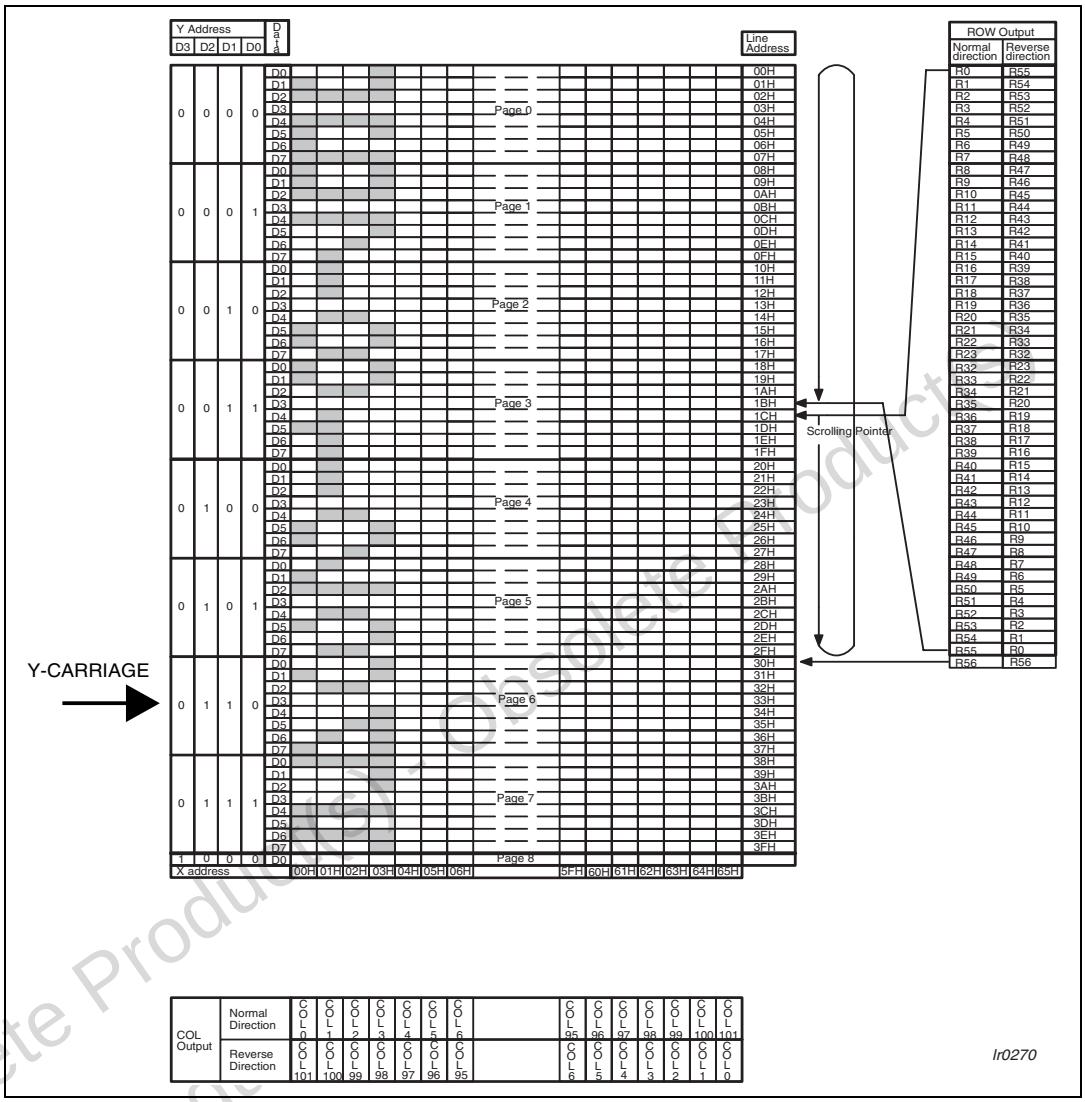


Figure 21. Memory rows vs. row drivers ;apping ICON_MODE=0, Y-Carriage<=6 and MUX 49

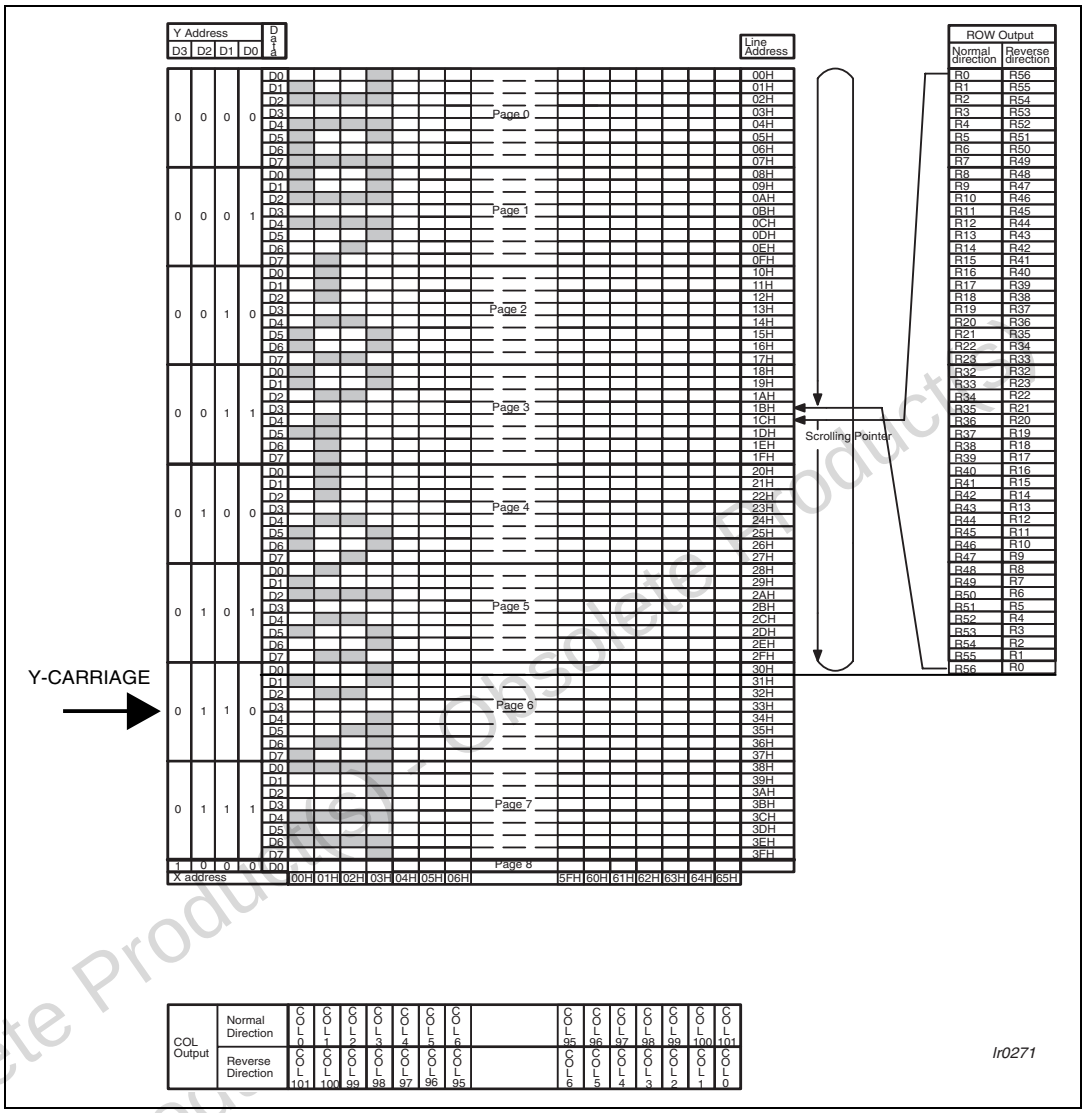


Figure 22. Memory rows vs. row drivers mapping ICON_MODE=0, Y-carriage=7, scrolling pointer>07h and MUX 49

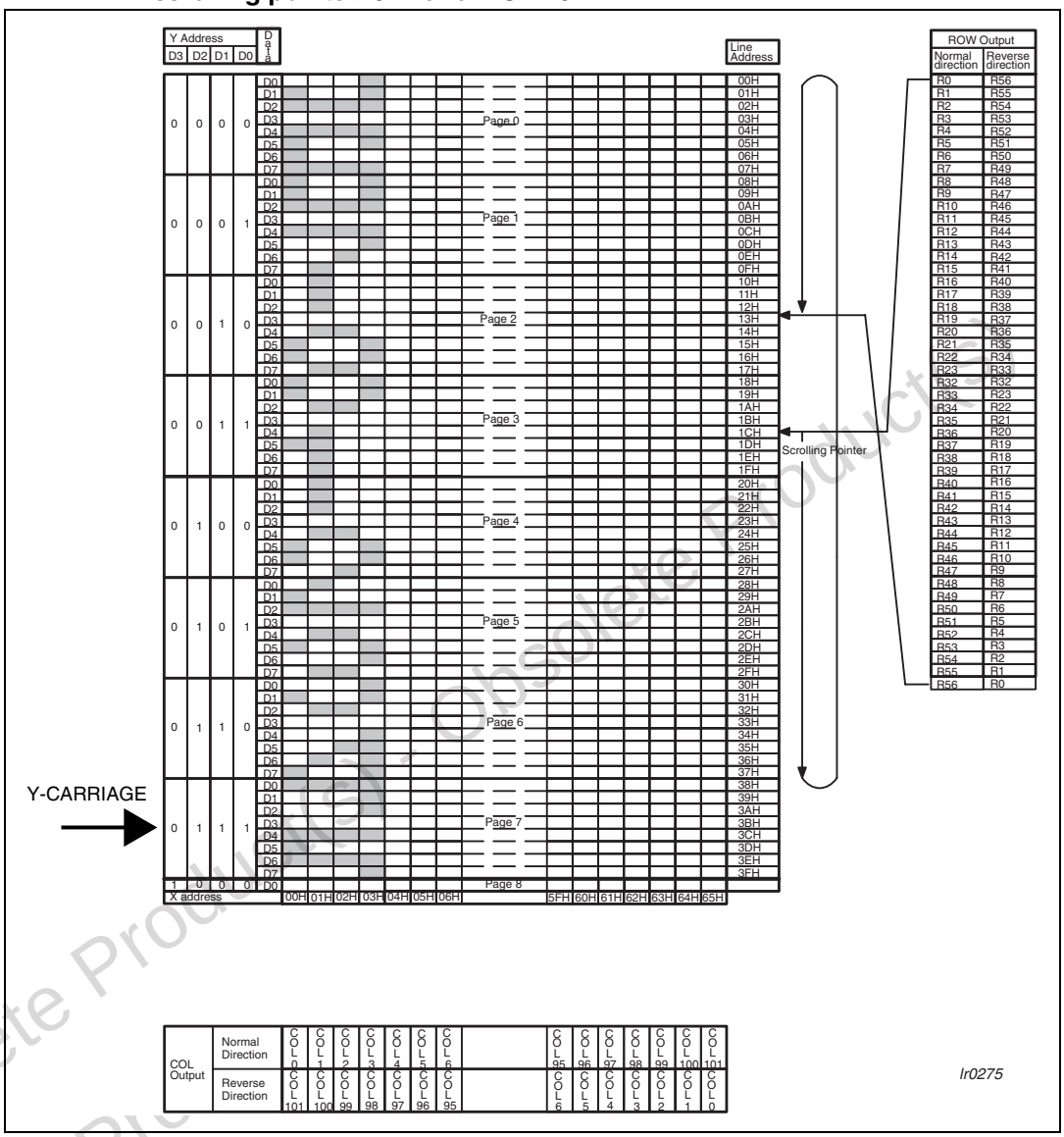


Figure 23. Memory rows vs. row drivers mapping ICON_MODE=1, Y-Carriage=7, scrolling pointer>07h and MUX 49

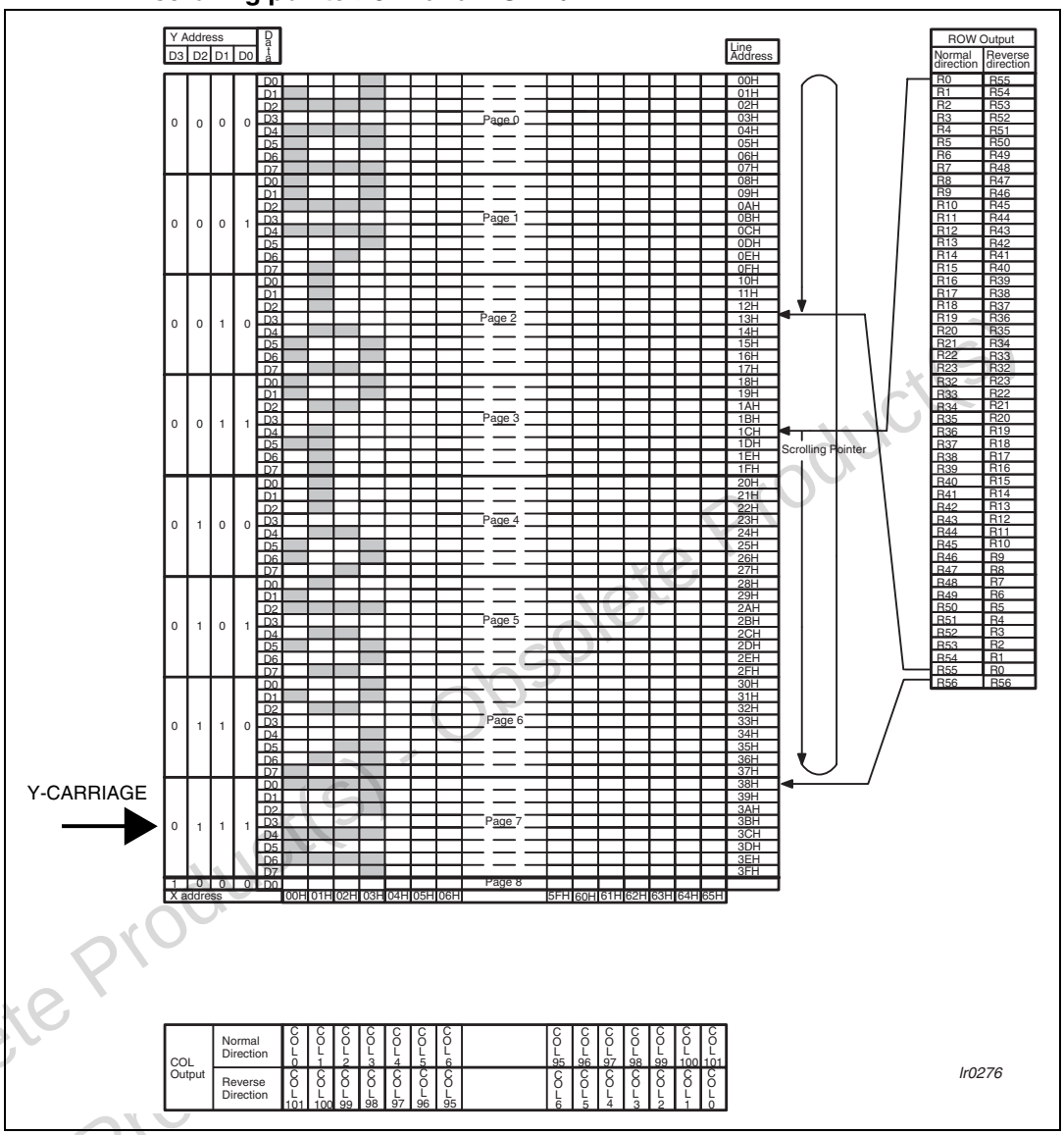


Figure 24. Memory rows vs. row drivers mapping ICON_MODE=1, Y-carriage=8, Scrolling pointer<10h and MUX 49

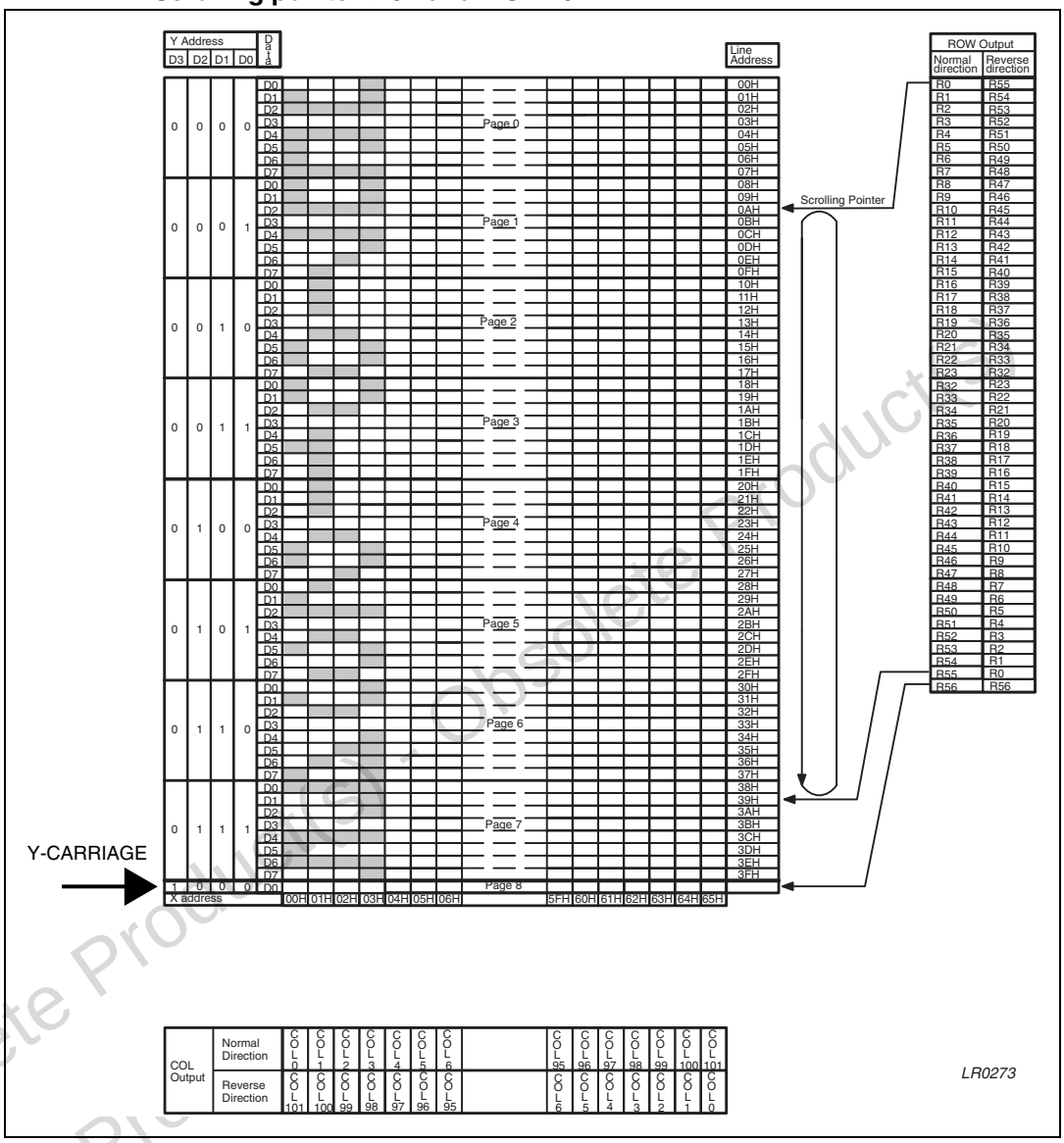


Figure 25. Memory rows vs. row drivers mapping ICON_MODE=0, Y-carriage=8, Scrolling pointer<10h and MUX 49

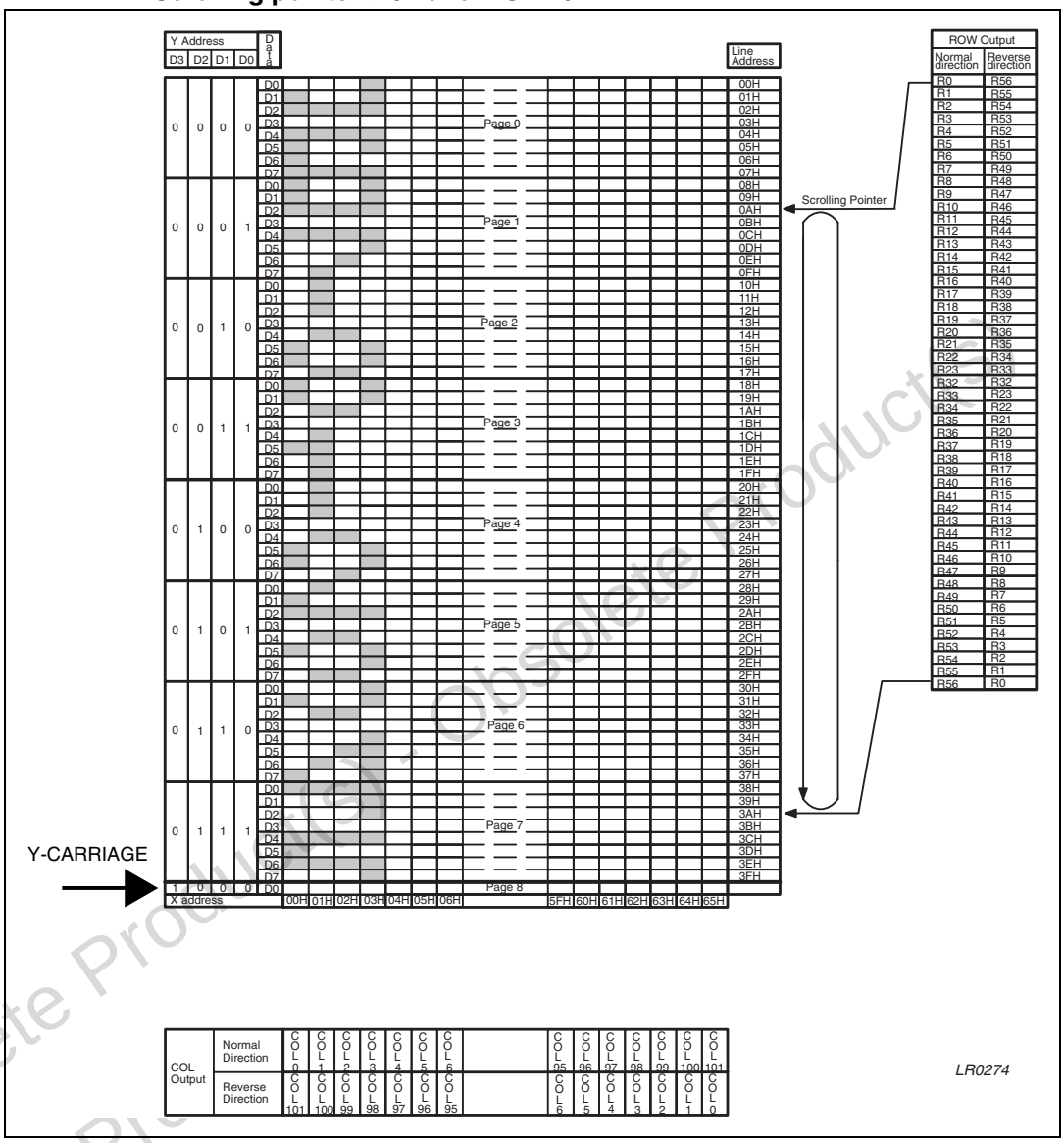


Figure 26. Memory rows vs. row drivers mapping ICON_MODE=1, Y-carriage<=4 and MUX33

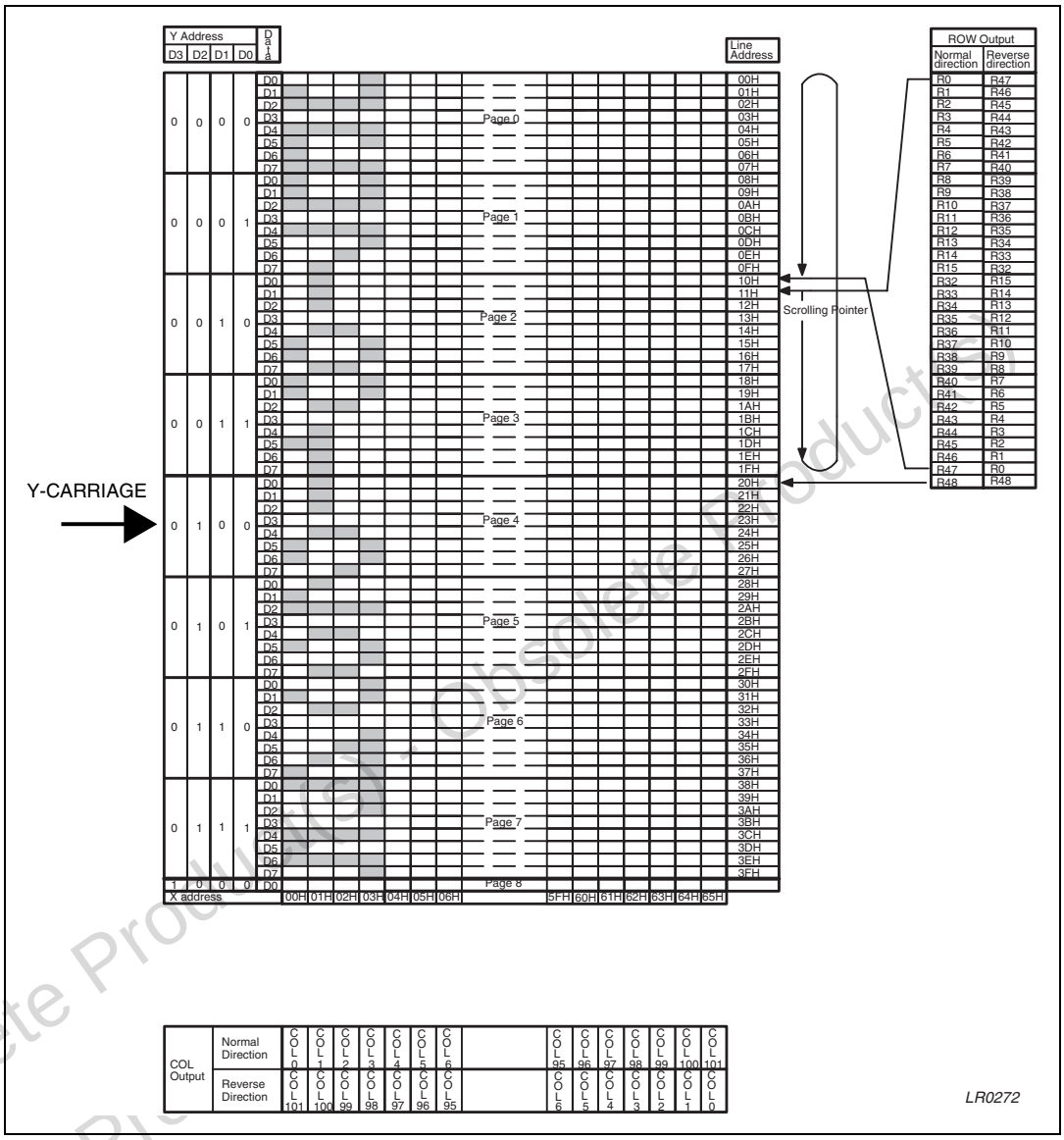


Figure 27. Memory rows vs. row drivers mapping ICON_MODE=0, Y-carriage<=4 and MUX 33

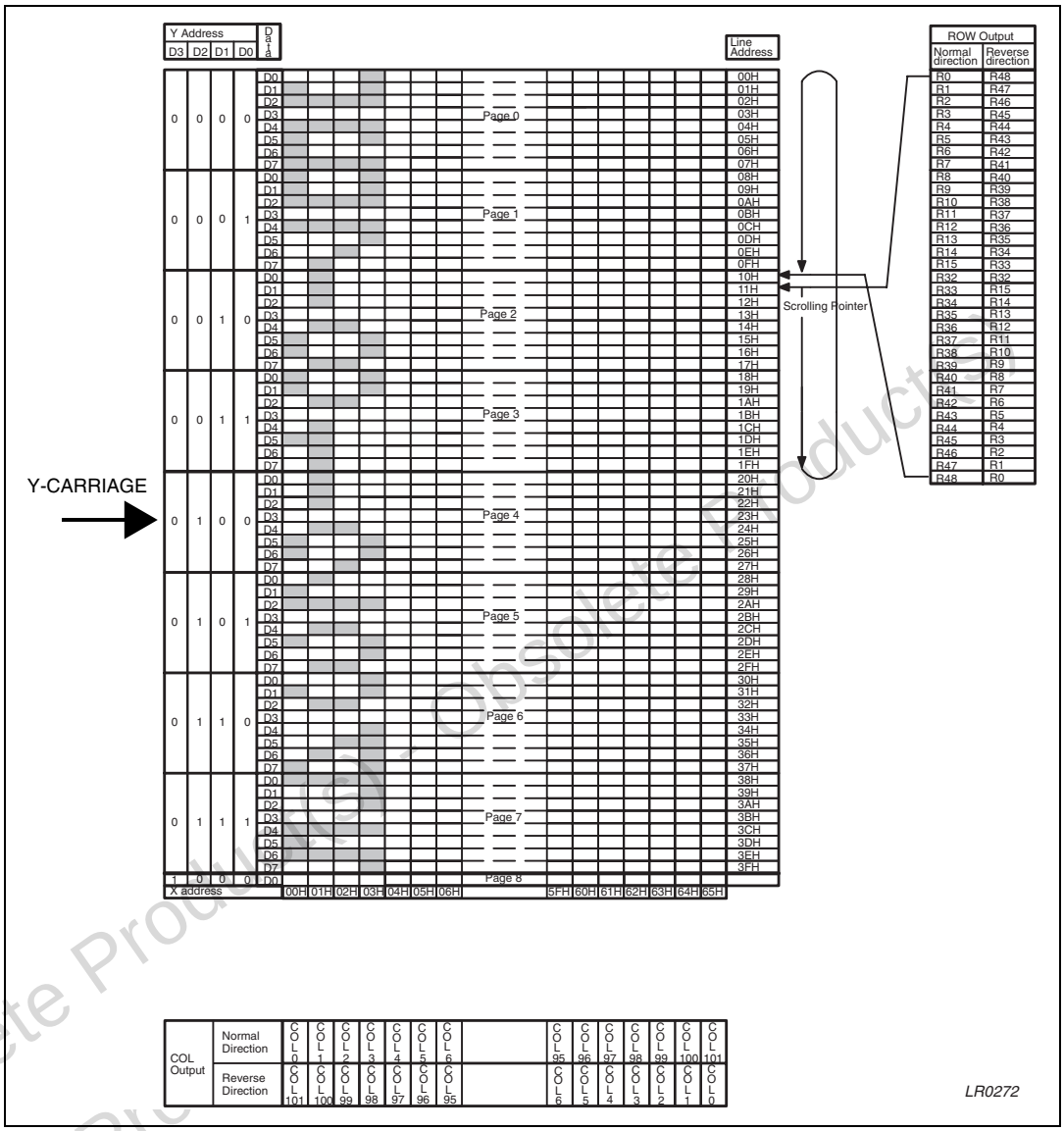


Figure 28. Row drivers vs. LCD panel interconnection in MUX65 mode

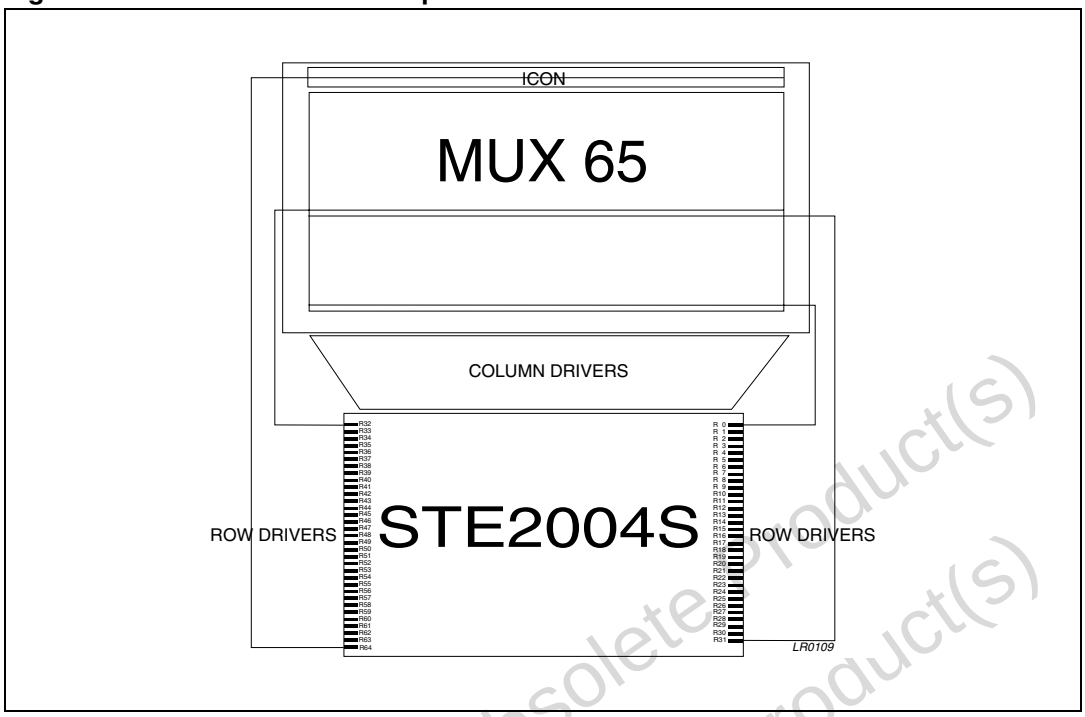


Figure 29. Row drivers vs. LCD panel interconnection in MUX49 mode

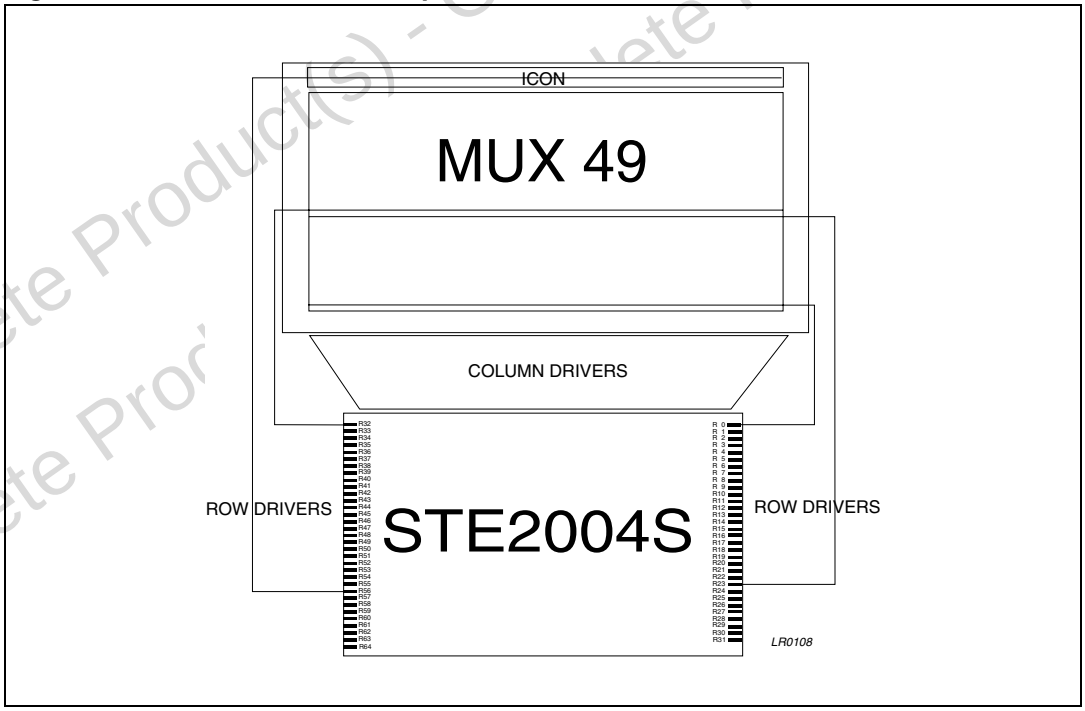
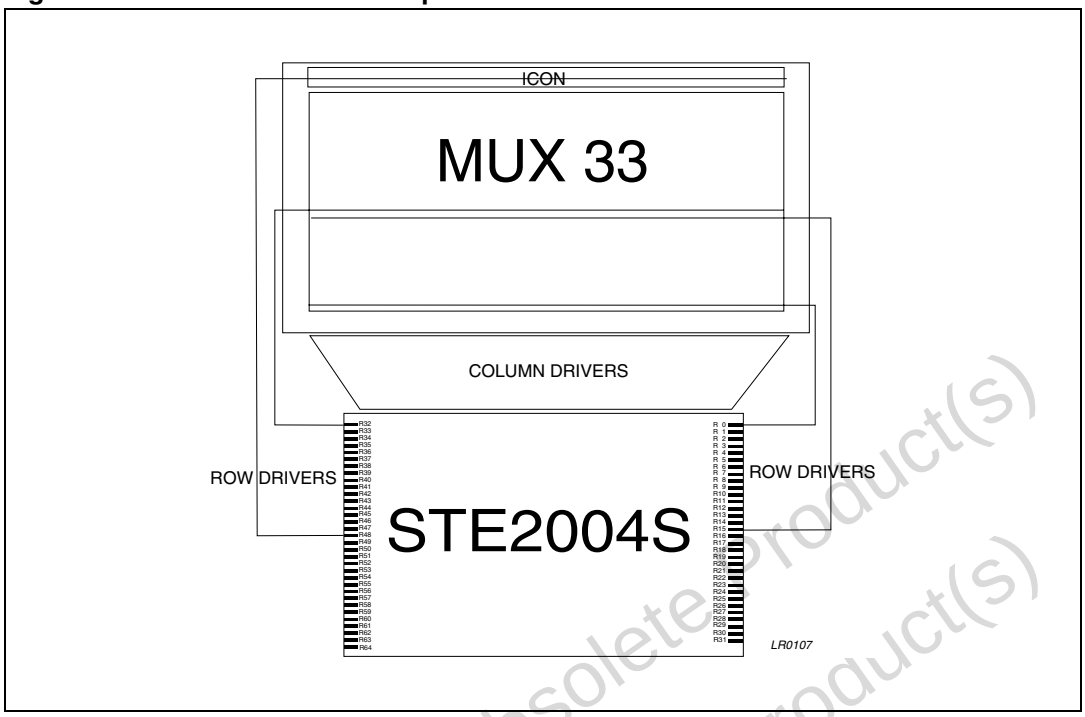


Figure 30. Row drivers vs. LCD panel interconnection in MUX33 mode



4 Bus interfaces

To provide the widest flexibility and ease of use the STE2004S features six different methods for interfacing the host controller. To select the desired interface the SEL1, SEL2 and SEL3 pads need to be connected to a logic LOW (connect to GND) or a logic HIGH (connect to VDD). All the I/O pins of the unused interfaces must be connected to GND.

All interfaces work while the STE2004S is in power down.

Table 7. Bus interfaces

SEL3	SEL2	SEL1	Interface	Note
0	0	0	I^2C	Read and write; fast and high speed mode
0	0	1	SPI 4 lines 8 bit	Read and write
0	1	0	SPI 3 lines 8 bit	Read and write
0	1	1	Serial 3 lines 9 bit	Read and write
1	0	0	Parallel 8080-series	Read and write
1	0	1	Parallel 68000-series	Read and write

4.1 I^2C Interface

The I^2C interface is a fully complying I^2C bus specification, selectable to work in both Fast (400kHz Clock) and High Speed Mode (3.4MHz).

This bus is intended for communication between different LCs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

BUS not busy: Both data and clock lines remain High.

Start Data Transfer: A change in the state of the data line, from High to Low, while the clock is High, define the START condition.

Stop Data Transfer: A Change in the state of the data line, from low to High, while the clock signal is High, defines the STOP condition.

Data Valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and the stop conditions is not

limited. The information is transmitted byte-wide and each receiver acknowledges with the ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the signals is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves"

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA_IN line during the acknowledge clock pulse. Of course, setup and hold time must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Connecting SDA_IN and SDA_OUT together the SDA line become the standard data line. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the STE2004S will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

To be compliant with the I^2C-bus Hs-mode specification the STE2004S is able to detect the special sequence "S00001xxx". After this sequence no acknowledge pulse is generated.

Since no internal modification are applied to work in Hs-mode, the device is able to work in Hs-mode without detecting the master code.

Figure 31. Bit transfer and start,stop conditions definition

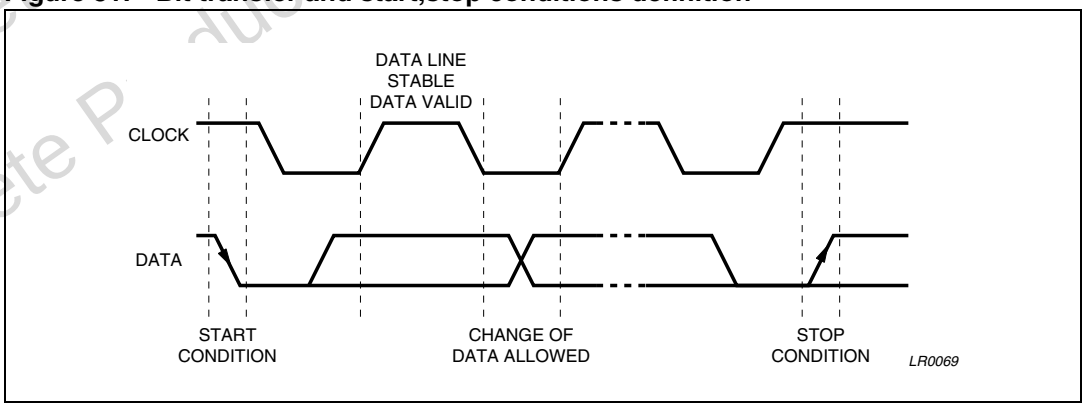
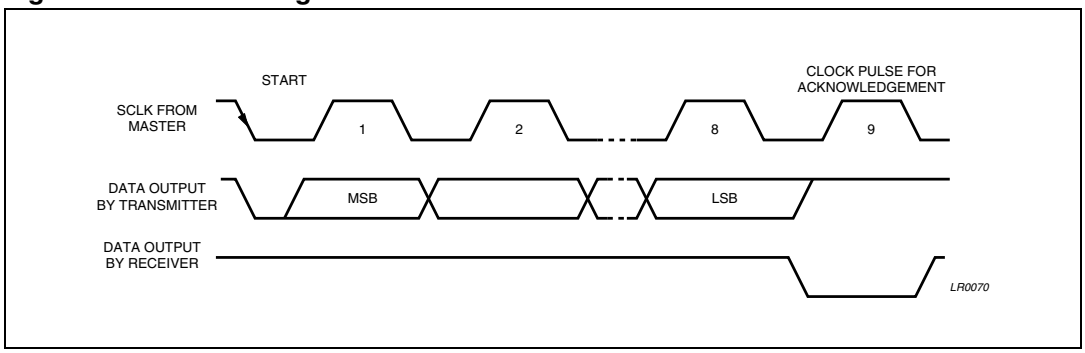


Figure 32. Acknowledgment on the I²C-bus



4.1.1 Communication protocol

The STE2004S is an I²C slave. The access to the device is bi-directional as data write and status read are allowed.

The STE2004S has four device addresses. All have the first 5 bits (01111) in common. The two least significant bit of the slave address are set by connecting the SA0 and SA1 inputs to a logic 0 or logic 1.

To start the communication between the bus master and the slave LCD driver, the master must initiate a START condition. Following this, the master sends an 8-bit byte, on the SDA bus line (most significant bit first). This consists of the 7-bit device select code, and the 1-bit read/write designator (R/$\overline{W}$).

All slaves with the corresponding address acknowledge in parallel, while the rest ignore the I²C-bus transfer.

Writing mode

When the R/W bit is set to logic 0, the STE2004S is set to be a receiver. After the slaves acknowledge, one or more command word follows to define the status of the device.

A command word is composed of three bytes. The first is a control byte which defines the Co and D/$\overline{C}$ values, the second and third are data bytes. The Co bit is the command MSB and defines whether this command is followed by two data bytes and and another command word, or if a stream of data follows (Co = 1 Command word, Co = 0 Stream of data). The D/$\overline{C}$ bit defines whether the data byte is a command or RAM data (D/$\overline{C}$ = 1 RAM Data, D/$\overline{C}$ = 0 Command).

If Co =1 and D/$\overline{C}$ = 0, the incoming data byte is decoded as a command, and if Co =1 and D/$\overline{C}$ =1, the following data byte is stored in the data RAM at the location specified by the data pointer.

Every byte of a command word must be acknowledged by all addressed units.

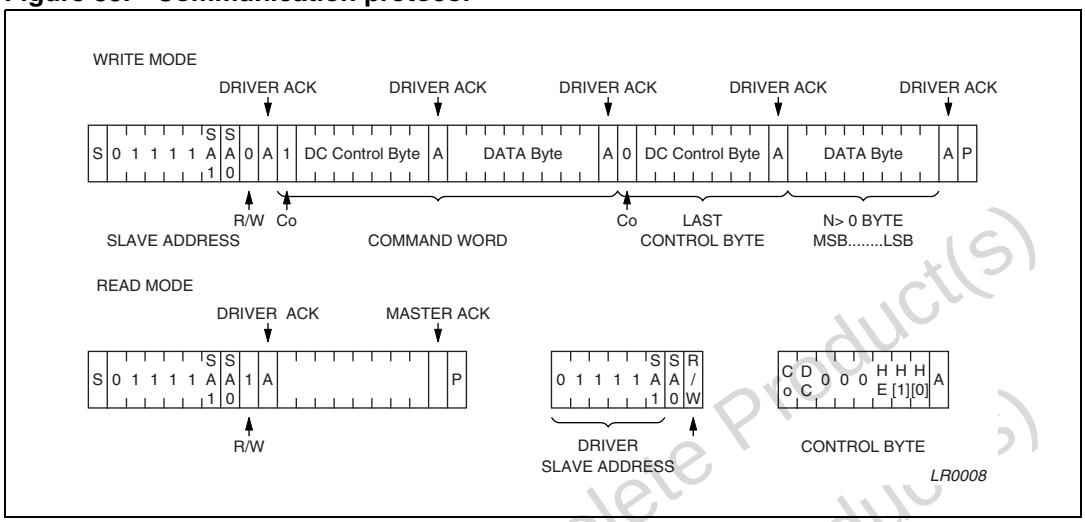
After the last control byte, if D/$\overline{C}$ is set to a logic 1, the incoming data bytes are stored inside the STE2004S display RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.

Every byte must be acknowledged by all addressed units.

Reading mode

If the R/W bit is set to logic 1 the chip outputs data immediately after the slave address. If the D/C bit during the last write access is set to a logic 0, the byte read is the status byte.

Figure 33. Communication protocol



4.2 Serial interfaces

STE2004S can feature three different serial synchronized interfaces with the host controller. It is possible to select a 3-lines SPI, a 4-lines SPI or 3-line 9 bits serial interface.

4.2.1 4-lines SPI interface

The STE2004S 4-lines serial interface is a bidirectional link between the display driver and the application supervisor. It consists of four lines: one/two for data signals (SDIN, SOUT), one for clock signals (SCLK), one for the peripheral enable ($\overline{CS}$) and one for mode selection (SD/$\overline{C}$).

The serial interface is active only if the $\overline{CS}$ line is set to a logic 0. When $\overline{CS}$ line is high the serial peripheral power consumption is zero. While $\overline{CS}$ pin is high the serial interface is kept in reset. The STE2004S is always a slave on the bus and receives the communication clock on the SCLK pin from the master.

Information is exchanged byte-wide. During data transfer, the data line is sampled on the positive SCLK edge.

SD/$\overline{C}$ line status indicates whether the byte is a command (SD/$\overline{C}$ =0) or a data (SD/$\overline{C}$ =1); SD/$\overline{C}$ line is read on the eighth SCLK clock pulse during every byte transfer.

If $\overline{CS}$ stays low after the last bit of a command/data byte, the serial interface expects the MSB of the next byte at the next SCLK positive edge.

A reset pulse on $\overline{RES}$ pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared.

If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the serial interface is ready to receive data.

Throughout SDOUT, the driver I^2C slave address or the status byte can be read. The command sequence to read the I^2C slave address or the status byte is shown in *Figure 34.*, *Figure 35.*,

Figure 36.. SDOUT is in high impedance in steady state and during data write. It is possible to short circuit SDOUT and SDIN and read the I2C address or status byte without any additional lines.

Figure 34. 4-lines serial bus protocol - one byte transmission

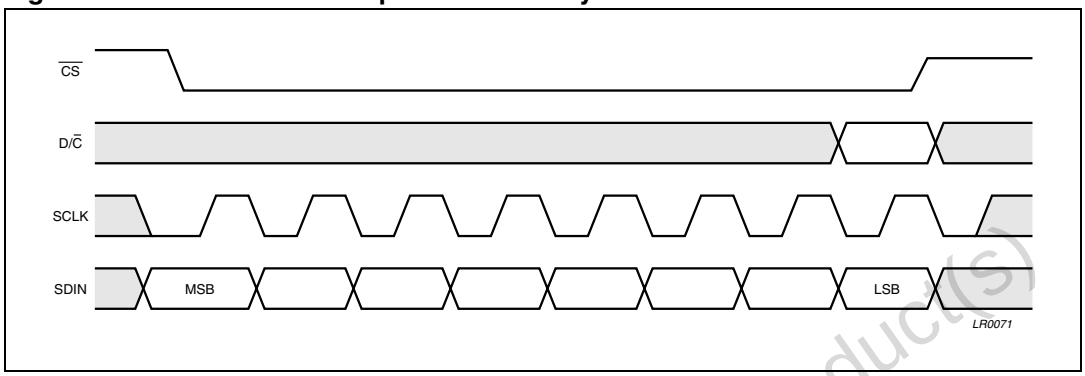


Figure 35. 4-lines serial bus protocol - several byte transmission

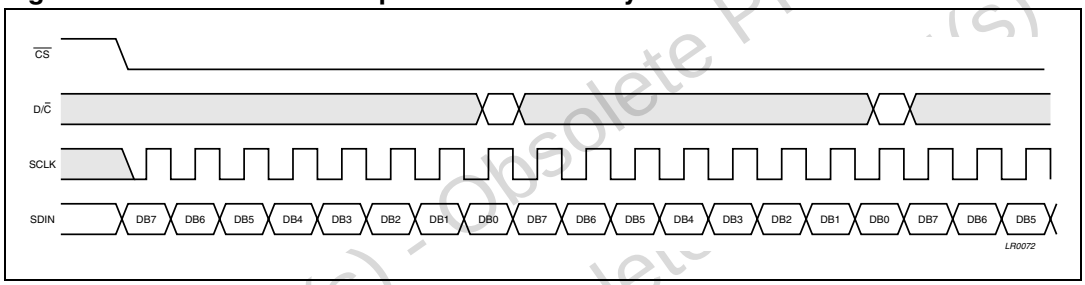


Figure 36. 4-lines serial bus protocol - I2C address or status byte read

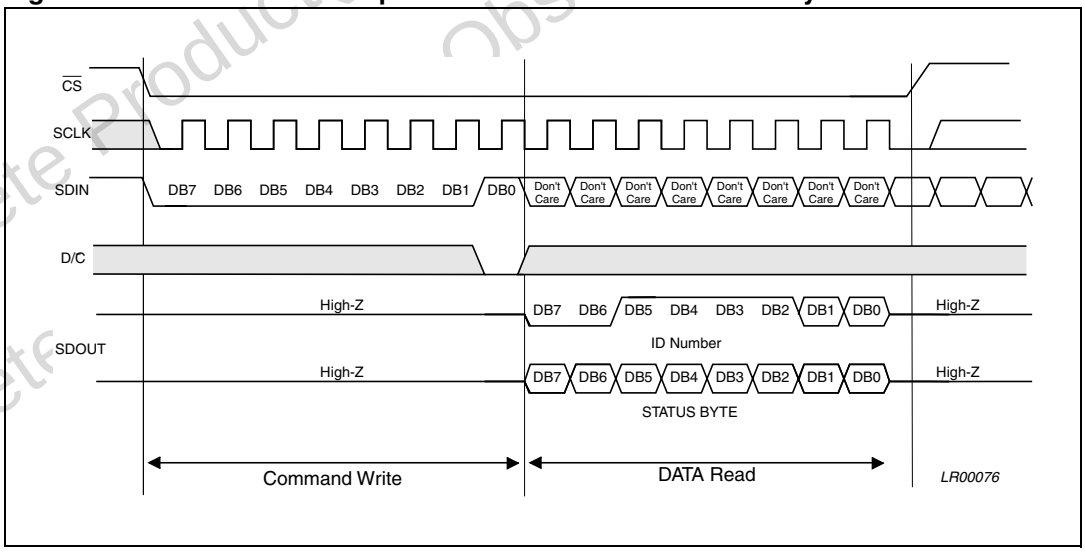
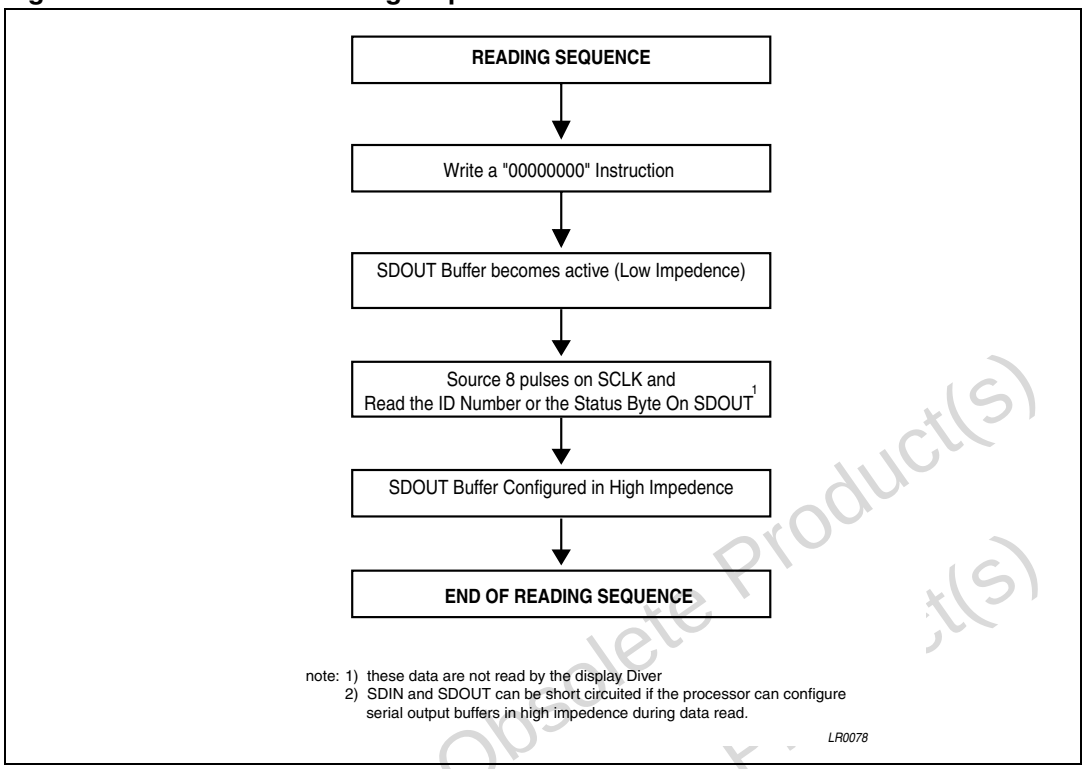


Figure 37. 4-lines SPI reading sequence



4.2.2 3-lines SPI interface

The STE2004S 3-lines serial interface is a bidirectional link between the display driver and the application supervisor.

It consists of three lines: one/two for data signals (SDIN,SDOUT), one for clock signals (SCLK) and one for peripheral enable ($\overline{CS}$).

If the R/W bit is set to logic 0 the STE2004S is set to be a receiver. One or more command words follow to define the status of the device.

A command word is composed by two bytes. The first is a control byte which defines Co, D/$\overline{C}$, R/W H[1;0] and HE values, the second is a data byte (*Figure 38.*). The Co bit is the command MSB and defines whether the command is followed by one data byte and an other command word, or if it is followed by a stream of commands, or a steam of DDRAM data (Co = 1 Command word, Co = 0 Stream of data). The D/$\overline{C}$ bit defines whether the data byte is a command or DDRAM data (D/$\overline{C}$ = 1 RAM Data, D/$\overline{C}$ = 0 Command). The H[1;0] bits define the instruction Set Page if HE bit =1. If HE bit is set to 0, H[1;0] values are neglected and it is possible to update the instruction set page number using only the related instruction in the instruction set.

If Co =1 and D/$\overline{C}$ = 0, the incoming data byte is decoded as a command, and if Co =1 and D/$\overline{C}$ =1, the following data byte is stored in the data RAM at the location specified by the data pointer.

After the last control byte, if D/$\overline{C}$ is set to a logic 1, the incoming data bytes are stored inside the STE2004S display data RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.

Throughout SDOUT can be read the driver I^2C slave address or the status byte. The command sequence that allows to read I^2C slave address or the status byte is shown in *Figure 39.* and *Figure 40.*.

If the R bit is set to logic 0 and D/C=0, the I^2C slave address is read. If the R bit is set to logic 1 and D/C=0, the the I^2C slave address is read. SDOUT is in high impedance in steady state and during data write.

It is possible to short circuit SDOUT and SDIN and read the I^2C address or status byte without any additional line.

Figure 38. 3-lines serial interface protocol in writing mode

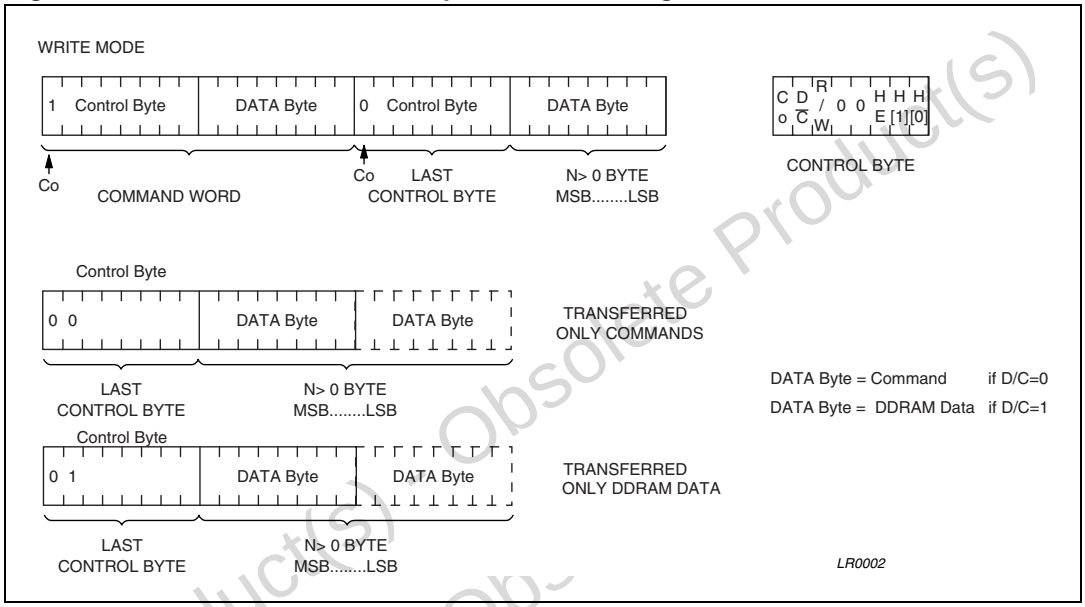


Figure 39. 3-lines SPI interface protocol in reading mode

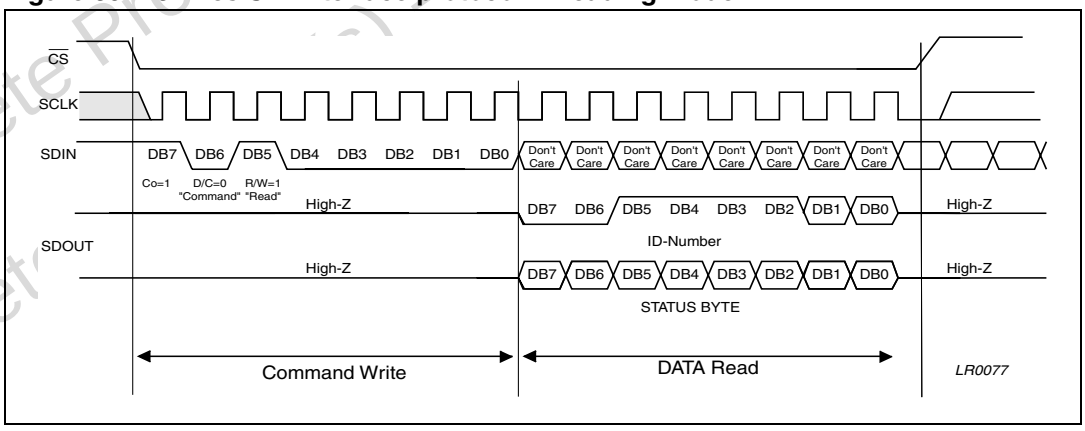
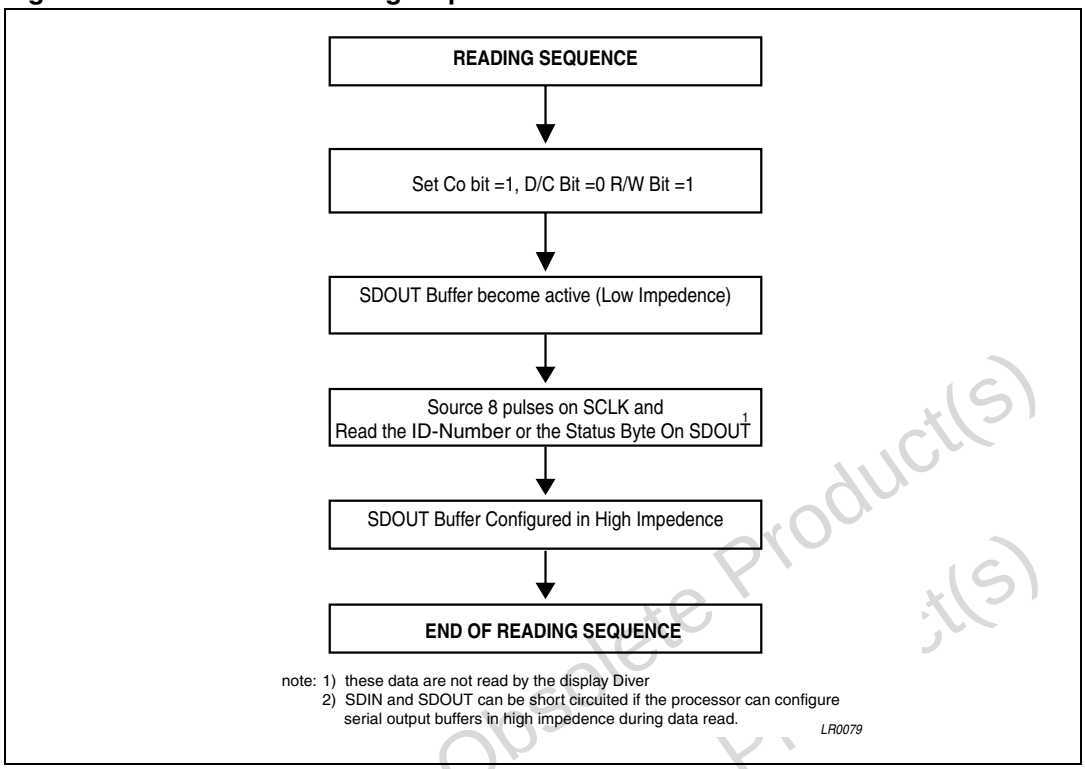


Figure 40. 3-lines SPI reading sequence



4.2.3 3-lines 9 bits serial interface

The STE2004S 3-lines serial interface is a bidirectional link between the display driver and the application supervisor.

It consists of three lines: one/two for data signals (SDIN, SDOUT), one for clock signals (SCLK) and one for peripheral enable ($\overline{CS}$).

The serial interface is active only if the $\overline{CS}$ line is set to a logic 0. When $\overline{CS}$ line is high the serial peripheral power consumption is zero. While $\overline{CS}$ pin is high the serial interface is kept in reset.

The STE2004S is always a slave on the bus and receives the communication clock on the SCLK pin from the master.

Information is exchanged word-wide. The word is composed of 9 bits. The first bit is named SD/$\overline{C}$ and indicates whether the following byte is a command (SD/$\overline{C}$ =0) or data byte (SD/$\overline{C}$ =1). During data transfer, the data line is sampled on the positive SCLK edge.

If $\overline{CS}$ stays low after the last bit of a command/data byte, the serial interface expects the SD/$\overline{C}$ bit of the next word at the next SCLK positive edge. A reset pulse on $\overline{RES}$ pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared. If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the serial interface is ready to receive data.

Throughout SDOUT, only the driver I^2C slave address or the status byte can be read. The command sequence that the I^2C slave address or status byte to be read is shown in *Figure 43.* and *Figure 44.*. SDOUT is in high impedance in steady state and during data write.

It is possible to short circuit SDOUT and SDIN, and read the I^2C address or status byte without any additional line.

Figure 41. 3-lines serial bus protocol - one byte transmission

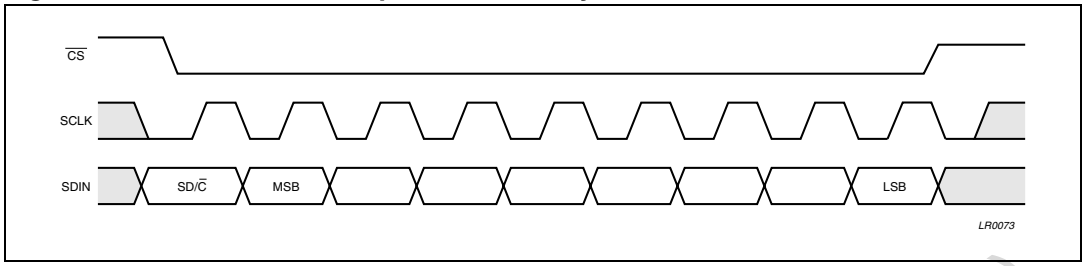


Figure 42. 3-lines serial bus protocol - several byte transmission

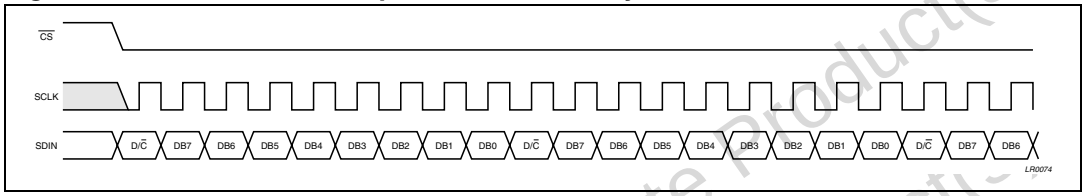


Figure 43. 3-lines serial interface protocol in Reading Mode

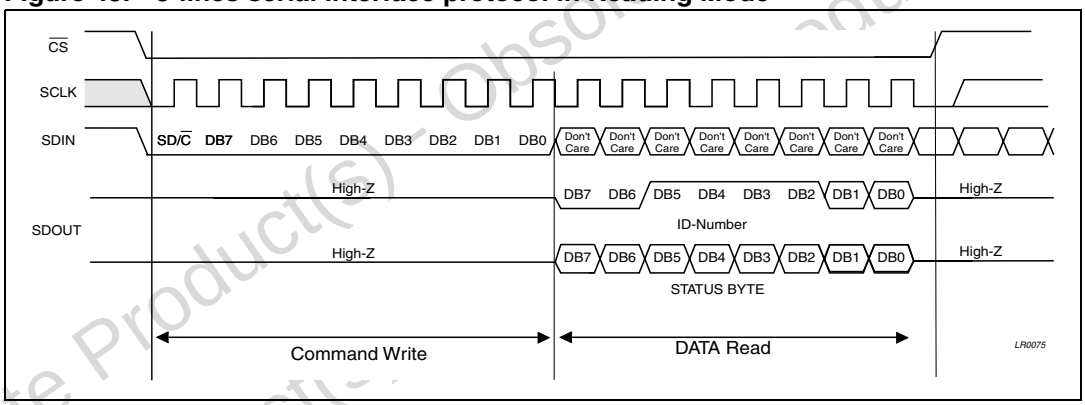
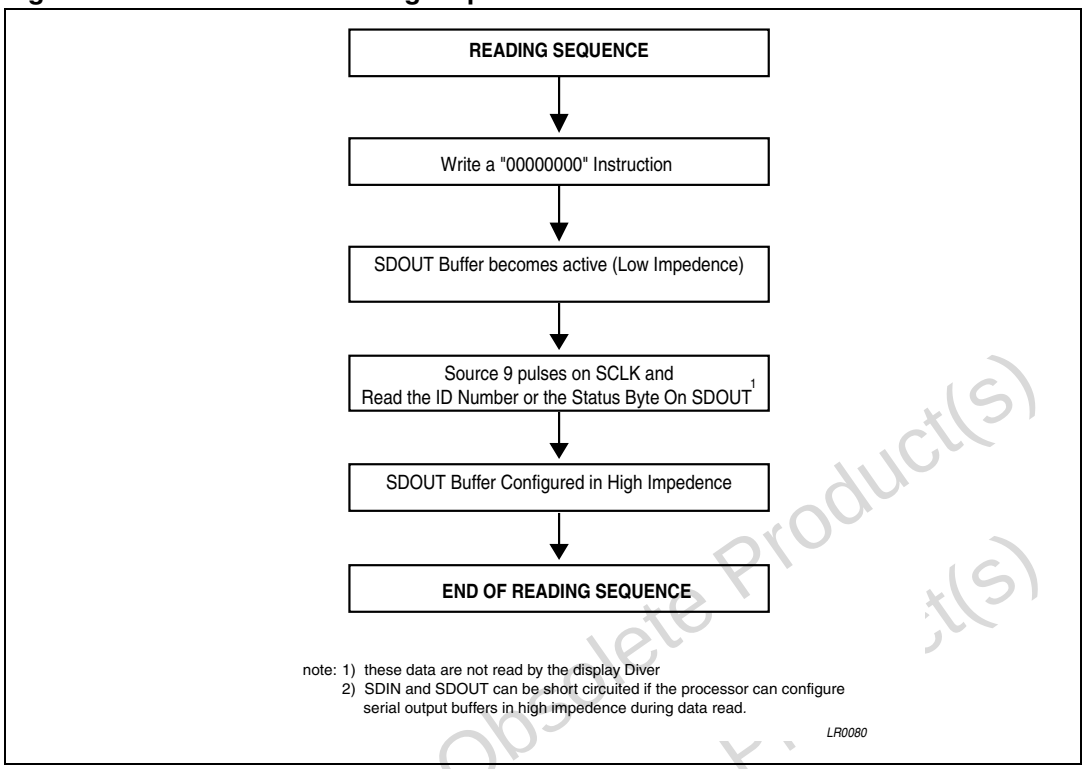


Figure 44. 3-lines serial reading sequence



4.3 Parallel interface

The STE2004S selectable parallel interfaces are 68000-series and 8080-series. They are both an 8-bits bi-directional link between the display driver and the application supervisor.

Both parallel interfaces can be read the I^2C driver slave address or the status byte.

4.3.1 68000-series parallel interface

If $\overline{CS}$ is low after the positive edge of $\overline{RES}$, the 68000 parallel interface is ready to receive or transmit data.

While $\overline{CS}$ pin is high the 68000 parallel interface is kept in reset.

Write mode

If R/W line is set to 0, data is latched on the E falling edge.

Read mode

When R/W line is set to 1, data is output on the D0-D7 bus on the E rising edge. The data bus is set in high impedance mode when E is set to logic 0.

The I2C address or status byte is output on D0-D7 bus, according to R bit value.

Figure 45. 68000-series parallel interface protocol - one byte transmission

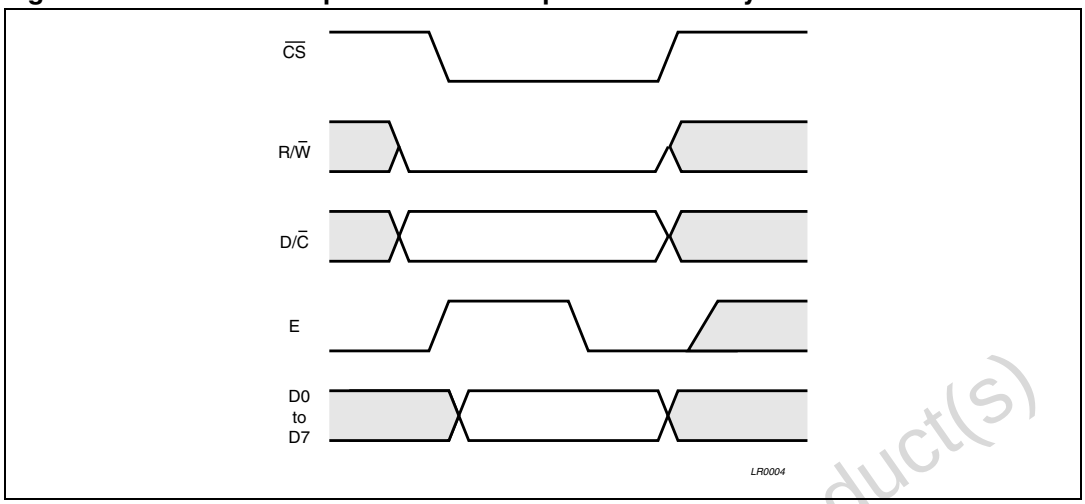


Figure 46. 68000-series parallel interface bus protocol - several bytes transmission

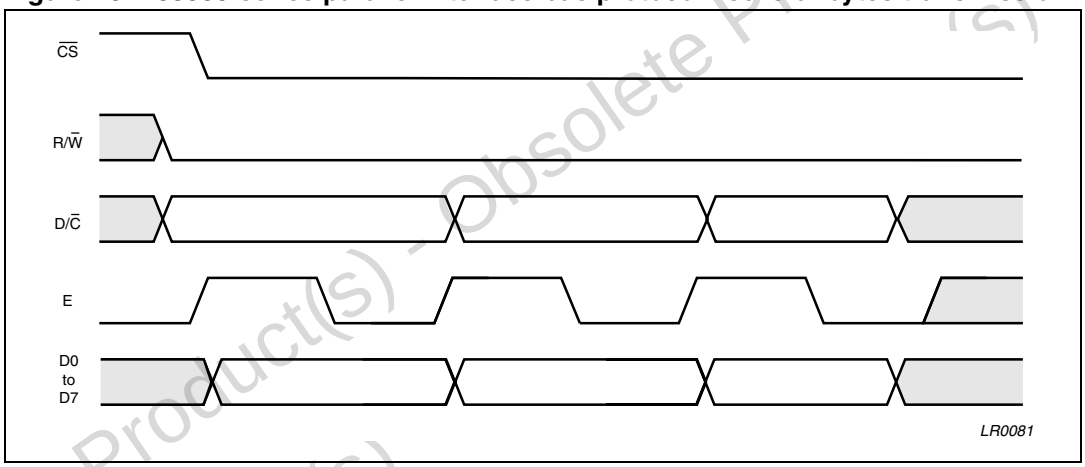


Figure 47. 68000-series parallel interface protocol in reading mode

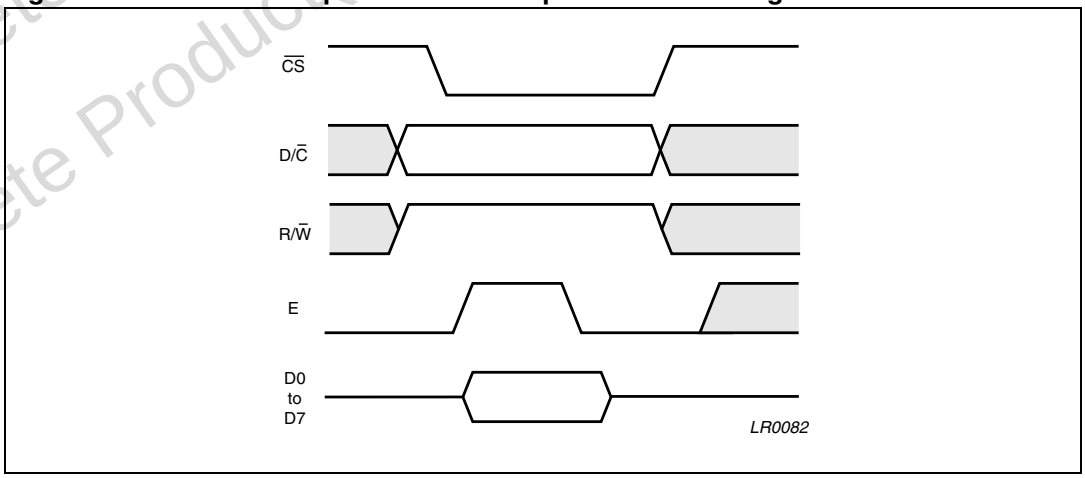
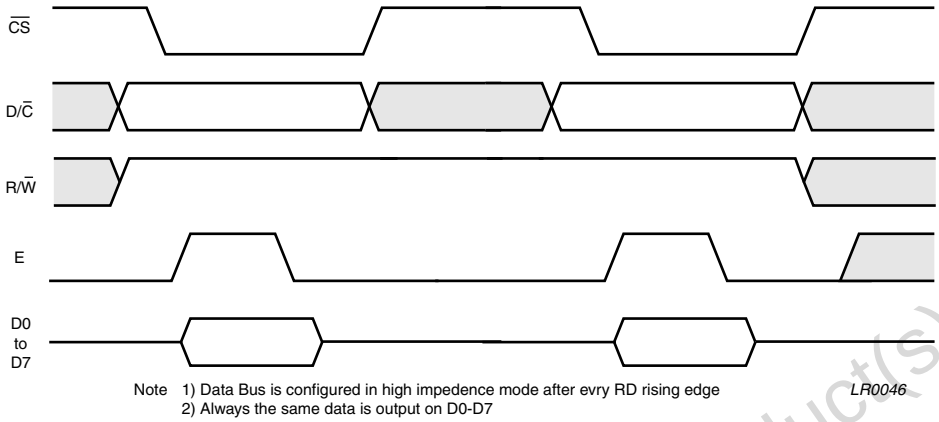


Figure 48. 68000-series parallel interface protocol in reading mode (several bytes)



Note 1) Data Bus is configured in high impedence mode after evry RD rising edge
2) Always the same data is output on D0-D7

4.3.2 8080-series parallel interface

If CS is low after the positive edge of RES, the 8080 parallel interface is ready to receive or transmit data. While CS pin is high the 8080 parallel interface is kept in reset.

Write mode

Data are latched on WR rising edge.

Read mode

Data is output on the D0-D7 bus on the RD rising edge. The data bus is set in high impedance mode when RD is set to logic 1.

The I2C address or status byte is output on D0-D7 bus, accordingly to R bit value.

Figure 49. 8080-series parallel bus protocol - one byte transmission

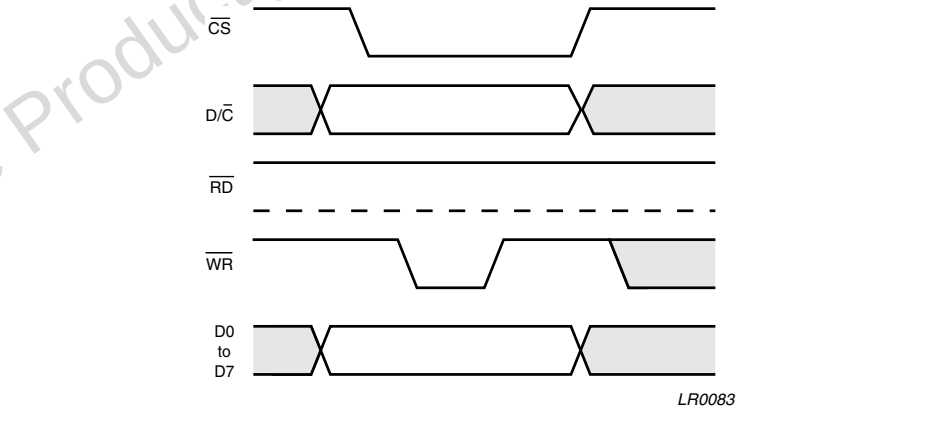


Figure 50. 8080-series parallel bus protocol - several bytes transmission

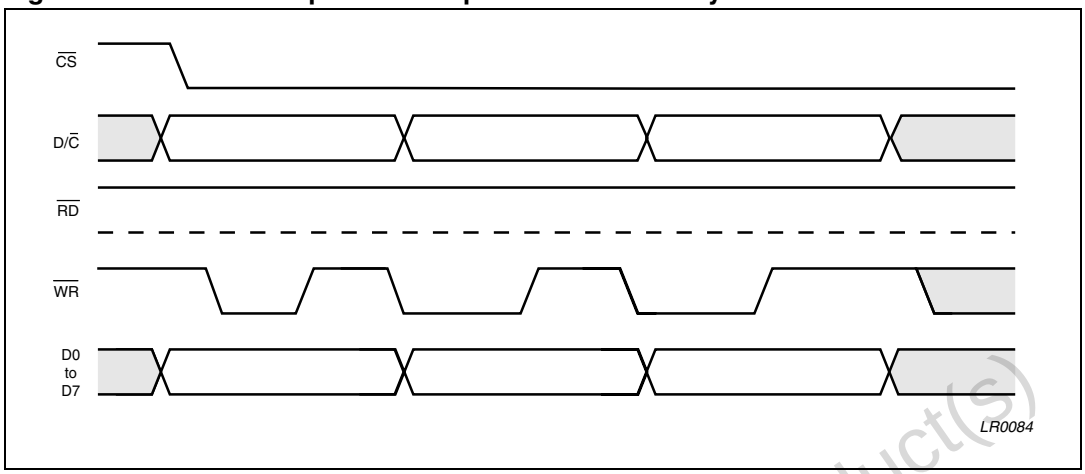


Figure 51. 8080-series parallel interface protocol in reading mode

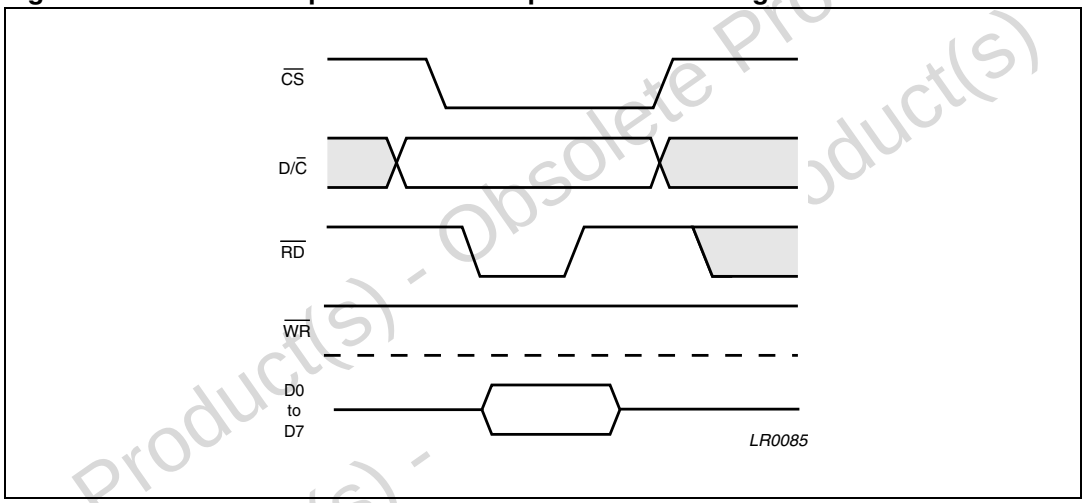
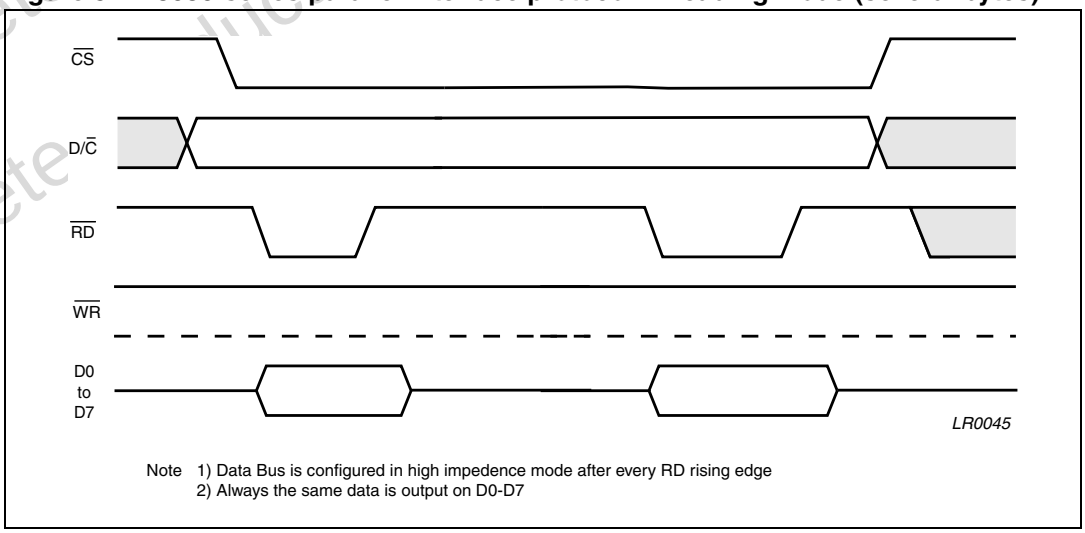


Figure 52. 8080-series parallel interface protocol in reading mode (several bytes)



Note 1) Data Bus is configured in high impedence mode after every RD rising edge
2) Always the same data is output on D0-D7

5 Instruction set

Two different instructions formats are provided:

- With D/$\overline{C}$ set to LOW : commands are sent to the control circuitry.
- With D/$\overline{C}$ set to HIGH : the data RAM is addressed.

Two different instruction sets are embedded: the STE2001-like instruction set and the extended instruction set. To select the STE2001-like instruction set, the EXT pad must be connected to a logic LOW (connect to GND). To select the extended instruction set, the EXT pad must be connected to a logic HIGH (connect to VDD1).

The instruction syntax is summarized in *Table 8.* (basic-set) and *Table 9.* (extended set).

Table 8. STE2001/2-like instruction set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H=0 or H=1											
Read command	0	0	0	0	0	0	0	0	0	0	Read I^2C address or status byte (with 3-lines serial and 4-lines SPI only)
Function set	0	0	0	0	1	MX	MY	PD	V	H[0]	Power down management; entry mode;
Status byte	0	1	PD	BSY	0	D	E	MX	MY	DO	(I^2C interface only)
ID code	0	1	0	0	1	1	1	1	ID1	ID0	
Write data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data to RAM
H=0											
Memory blank	0	0	0	0	0	0	0	0	0	1	Starts memory blank procedure
Scroll	0	0	0	0	0	0	0	0	1	DIR	Scrolls by one row up or down
V_{LCD} range setting	0	0	0	0	0	0	0	1	0	PRS[0]	V_{LDC} programming range selection
Display control	0	0	0	0	0	0	1	D	0	E	Select display configuration
Set CP factor	0	0	0	0	0	1	0	S2	S1	S0	Charge pump multiplication factor
Set RAM Y	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set horizontal (Y) RAM address
Set RAM X	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set vertical (X) RAM address

Table 8. STE2001/2-like instruction set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H=1											
Checker board	0	0	0	0	0	0	0	0	0	1	Starts checker board procedure
Duty	0	0	0	0	0	0	0	0	1	MUX	Selects duty factor
TC select	0	0	0	0	0	0	0	1	TC1	TC0	Set temperature coefficient for V_{LDC}
Data order	0	0	0	0	0	0	1	DO	0	0	
Bias ratios	0	0	0	0	0	1	0	BS2	BS1	BS0	Set desired bias ratios
Reserved	0	0	0	1	X	X	X	X	X	X	Not to be used
Set V_{OP}	0	0	1	OP6	OP5	OP4	OP3	OP2	OP1	OP0	V_{OP} register write instruction

Table 9. Extended instruction set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H independent instructions											
Read command	0	0	0	0	0	0	0	0	0	0	Read I^2C address or status byte (with 3-lines serial and 4-lines SPI only)
	0	0	0	0	1	MX	MY	PD	H[1]	H[0]	Page selector, power down management; entry mode
Status byte	0	1	PD	BSY	0	D	E	MX	MY	DO	
ID code	0	1	0	0	1	1	1	1	ID1	ID0	
Write data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Writes data to RAM
H=[0;0] RAM commands											
Memory blank	0	0	0	0	0	0	0	0	0	1	Starts memory blank procedure
Scroll	0	0	0	0	0	0	0	0	1	DIR	Scrolls by one row up or down
V_{LCD} range setting	0	0	0	0	0	0	0	1	PRS[1]	PRS[0]	V_{LDC} programming range selection
Display control	0	0	0	0	0	0	1	D	0	E	Select display configuration
Set CP factor	0	0	0	0	0	1	0	S2	S1	S0	Charge pump multiplication factor
Set RAM Y	0	0	0	1	0	0	Y3	Y2	Y1	Y0	Set horizontal (Y) RAM address
Set RAM X	0	0	1	X6	X5	X4	X3	X2	X1	X0	Set vertical (X) RAM address

Table 9. Extended instruction set

Instruction	D/$\overline{C}$	R/$\overline{W}$	B7	B6	B5	B4	B3	B2	B1	B0	Description
H=[0;1]											
Checker board	0	0	0	0	0	0	0	0	0	1	Starts checker board procedure
	0	0	0	0	0	0	0	0	1	V	Vertical addressing mode
TC select	0	0	0	0	0	0	0	1	TC1	TC0	Set temperature coefficient for V_{LDC}
Data order	0	0	0	0	0	0	1	DO	0	0	MSB position
Bias ratios	0	0	0	0	0	1	0	BS2	BS1	BS0	Set desired bias ratios
Read mode,	0	0	0	1	0	0	R	0	0	0	
Set V_{OP}	0	0	1	OP6	OP5	OP4	OP3	OP2	OP1	OP0	V_{OP} register write instruction
H=[1;0]											
Driver control	0	0	0	0	0	0	0	0	0	1	Software reset
Display control	0	0	0	0	0	0	0	0	1	PE	Partial enable
	0	0	0	0	0	0	0	1	FR1	FR0	Frame rate control
	0	0	0	0	0	0	1	0	M[1]	M[0]	MUX ratio
Partial mode	0	0	0	0	0	1	0	PDC2	PDC1	PDC0	Partial display config
	0	0	0	1	PDY5	PDY4	PDY3	PDY2	PDY1	PDY0	1st Sector start address
	0	0	1	PDY6	PDY5	PDY4	PDY3	PDY2	PDY1	PDY0	2nd Sector start address
H=[1;1]											
	0	0	0	0	0	0	0	0	0	1	Scrolling pointer reset
	0	0	0	0	0	0	0	0	1	X	Not used
	0	0	0	0	0	0	0	1	X	X	Not used
	0	0	0	0	0	0	1	T2	T1	T0	Set temperature coefficient for V_{LDC}
	0	0	0	0	0	1	NW3	NW2	NW1	NW0	N-Line inversion
	0	0	0	1	0	0	YC-3	YC-2	YC-1	YC-0	Y carriage return
	0	0	1	XC-6	XC-5	XC-4	XC-3	XC-2	XC-1	XC-0	X carriage return

Table 10. Explanations of Table 8 and Table 9 symbols

Bit	0	1	Reset state
DIR	Scroll by one down	Scroll by one up	
H[0]	Select page 0	Select page 1	0
PD	Device fully working	Device in power down	1
V	Horizontal addressing	Vertical addressing	0
MX	Normal X axis addressing	X axis address is mirrored.	0
MY	Image is displayed not vertically mirrored	Image is displayed vertically mirrored	0
DO	MSB on TOP	MSB on BOTTOM	0
PE	Partial Display disabled	Partial Display enabled	0
MUX	MUX 65 mode	MUX 33 mode	0
R	Read ID-Number / I2C address	Read status byte	0

Table 11. Page selection

H[1]	H[0]	Description	Reset state
0	0	Page 0	Page 0
0	1	Page 1	
1	0	Page 2	
1	1	Page 3	

Table 12. Display mode

D	E	Description	Reset state
0	0	Display blank	E=0 D=0
0	1	Qll display segments on	
1	0	Normal mode	
1	1	Inverse video mode	

Table 13. Frame rate control

FR[1]	FR[0]	Description	Reset state
0	0	65Hz	75Hz
0	1	70Hz	
1	0	75Hz	
1	1	80Hz	

Table 14. Vlcd range selection

PRS[1]	PRS[0]	Description	Reset state
0	0	2.94	
0	1	6.78	
1	0	10.62	
1	1	10.62	

Table 15. Multiplexing ratio

M[1]	M[0]	Description	Reset state
0	0	49	01
0	1	65	
1	0	33	
1	1	Not Allowed	

Table 16. Temperature coefficient (T0, T1, T2)

T2	T1	T0	Description	Reset state
0	0	0	VLCD temperature coefficient 0	000
0	0	1	VLCD temperature coefficient 1	
0	1	0	VLCD temperature coefficient 2	
0	1	1	VLCD temperature coefficient 3	
1	0	0	VLCD temperature coefficient 4	
1	0	1	VLCD temperature coefficient 5	
1	1	0	VLCD temperature coefficient 6	
1	1	1	VLCD temperature coefficient 7	

Table 17. Temperature coefficient (TC0, TC1)

TC1	TC0	Description	Reset state
0	0	VLCD temperature coefficient 0	00
0	1	VLCD temperature coefficient 2	
0	1	VLCD temperature coefficient 3	
1	1	VLCD temperature coefficient 6	

Table 18. Charge pump multiplication factor

CP2	CP1	CP0	Description	Reset state
0	0	0	Multiplication factor X2	000
0	0	1	Multiplication factor X3	
0	1	0	Multiplication factor X4	
0	1	1	Multiplication factor X5	
1	0	0	Not used	
1	0	1	Not used	
1	1	0	Not used	
1	1	1	Automatic	

Table 19. Bias ratio

BS2	BS1	BS0	Description	Reset state
0	0	0	Bias ratio equal to 7	000
0	0	1	Bias ratio equal to 6	
0	1	0	Bias ratio equal to 5	
0	1	1	Bias ratio equal to 4	
1	0	0	Bias ratio equal to 3	
1	0	1	Bias ratio equal to 2	
1	1	0	Bias ratio equal to 1	
1	1	1	Bias ratio equal to 0	

Table 20. Y Carriage return register

Y-C[3]	Y-C[2]	Y-C[1]	Y-C[0]	Description	Reset state
0	0	0	0	Y-CARRIAGE =0	1000
0	0	0	1	Y-CARRIAGE =1	
0	0	1	0	Y-CARRIAGE =2	
0	0	1	1	Y-CARRIAGE =3	
0	1	0	0	Y-CARRIAGE =4	
.	.	.	.		
0	1	1	0	Y-CARRIAGE =6	
0	1	1	1	Y-CARRIAGE =7	
1	0	0	0	Y-CARRIAGE =8	

Table 21. Partial display configuration

PD2	PD1	PD0	Section 1	Section 2	Reset state
0	0	0	0	8 + Icon row	000
0	0	1	8	0 + Icon row	
0	1	0	8	8 + Icon row	
0	1	1	0	16 + Icon row	
1	0	0	16	0 + Icon row	
1	0	1	8	16 + Icon row	
1	1	0	16	8 + Icon row	
1	1	1	16	16 + Icon row	

Table 22. N-Line inversion

NW3	NW2	NW1	NW0	Description	Reset state
0	0	0	0	0-Line inversion (Frame inversion)	0000
0	0	0	1	2-Line inversion	
0	0	1	0	3-Line inversion	
0	0	1	1	4-Line inversion	
:	:	:	:	:	
1	1	1	0	15-Line inversion	
1	1	1	1	16-Line inversion	

5.1 Reset (RES)

At power-on, all internal registers are configured with the default value. The RAM content is not defined. A reset pulse on the RES pad (active low) re-initializes the internal registers content see *Table 10.* All on-going communication with the host controller is interrupted if a reset pulse is applied. After the power-on, the software reset instruction can be used to re-load the reset configuration into the internal registers.

The default configuration is:

- Horizontal addressing (V = 0)
- Normal instruction set (H[1:0] = 0)
- Normal display (MX = MY = 0)
- Display blank (E = D = 0)
- Address counter X[6: 0] = 0 and Y[4: 0] = 0
- Temperature coefficient (TC[1: 0] = 0)
- Bias system (BS[2: 0] = 0)
- Multiplexing ratio (M[1:0]=0 - MUX 65)
- Frame rate (FR[1:0]="75Hz")
- Power down (PD = 1)
- Dual partial display disabled (PE=0)
- V_{OP}=0
- Y-CARRIAGE=8
- X-CARRIAGE=101

A memory blank instruction can be used to clear the DDRAM content.

5.2 Power down (PD = 1)

At power down, all LCD outputs are kept at V_{SS} (display off). Bias generator and V_{LCD} generator are off (V_{LCDOUT} output is discharged to V_{SS}, and then V_{LCDOUT} can be disconnected). The internal oscillator is in off state. An external clock can be provided. The RAM contents is not cleared.

5.3 Memory blanking procedure

This instruction fills the memory with "blank" patterns, in order to delete patterns randomly generated in memory when starting up the device. It substitutes (102X8) single "write" instructions. The procedure can only be programmed if:

PD bit = 0

No instruction can be programmed for a period equivalent to 102X8 internal write cycles (102X8X1/fclock). The start of the memory blanking procedure is between one and two fclock cycles from the last active edge (E falling edge for the parallel interface, last SCLK rising edge for the serial and SPI interfaces, last SCL rising edge for the I^2C interface).

5.4 Checker board procedure

This instruction fills the memory with "checker-board" pattern, allowing developers to create a complex module test configuration using one instruction. It can only be programmed if:

PD bit = 0

No instruction can be programmed for a period equivalent to 102X8 internal write cycles (102X8X1/fclock). The start of checker-board procedure is between one and two fclock cycles from the last active edge (E falling edge for the parallel interface, last SCLK rising edge for the serial and SPI interfaces, last SCL rising edge for the I^2C interface).

5.5 Scrolling function

The STE2004S can scroll the graphics display in units of raster-rows. The scrolling function changes the correspondence between the rows of the logical memory map and the output row drivers. The scroll function does not affect the data ram contentm it is only related to the visualization process. The information output on the drivers is related to the row reading sequence (the 1st row read is output on R0, the 2nd on R1 and so on). Scrolling means reading the matrix starting from a row that is sequentially increased or decreased. After every scrolling command the offset between the memory address and the memory scanning pointer is increased or decreased by one. The offset range changes in accordance with MUX Rate. After 64th/65th scrolling commands in MUX 65 mode, or after the 48th/49th scrolling commands in MUX 49 mode, or after 32nd/33rd scrolling command in MUX 33 mode, the offset between the memory address and the memory scanning pointer is again zero (Cyclic Scrolling).

A Reset Scrolling Pointer instruction can be executed to force the offset between the memory address and the memory scanning pointer to zero.

If ICON MODE =1, the Icon Row is not scrolled. If ICON MODE=0 the last row is like a general purpose row and it is scrolled as other lines.

If the DIR bit is set to a logic 0, the offset register is increased by one and the raster is scrolled from top down. If the DIR bit is set to a logic 1, the offset register is decreased by one and the raster is scrolled from bottom-up.

Table 23. Scrolling function

MUX Rate	Icon mode	Description	Icon row driver with MY=0
MUX 33	1	Icon row not scrooled	R48
MUX 33	0	33 line graphic matrix	R48
MUX 49	1	Icon row not scrooled	R56
MUX 49	0	49 line graphic matrix	R56
MUX 65	1	Icon row not scrooled	R64
MUX 65	0	65 line graphic matrix	R64

5.6 Dual partial display

If the PE bit is set to a logic one the dual partial display mode is enabled. There are eight partial display modes available. The offset of the two partial display zones is row by row programmable. The icon row is accessed last in each partial display frame.

Two sets of register for the HV-generator parameters are provided (PRS[1:0], Vop[6:0], BS[2:0], CP[2:0]), allowing normal mode and partial display mode to be switched using one instruction. The HV generator is automatically reconfigured using the parameters related to the enabled mode. The parameters of the two sets of registers with the same function are located in the same position of the instruction set. The registers related to the normal mode are accessible when normal mode (PE=0) is selected, the others are accessible when the partial display mode is enabled (PE=1). To setup the PRS[1:0], Vop[6:0], BS[2:0], CP[2:0] values, follow the instruction flow proposed in *Figure 54.* To setup partial display sectors start qddress and partial display mode no particular instruction flow has to be followed.

Figure 53. Dual partial display enabling instruction flow

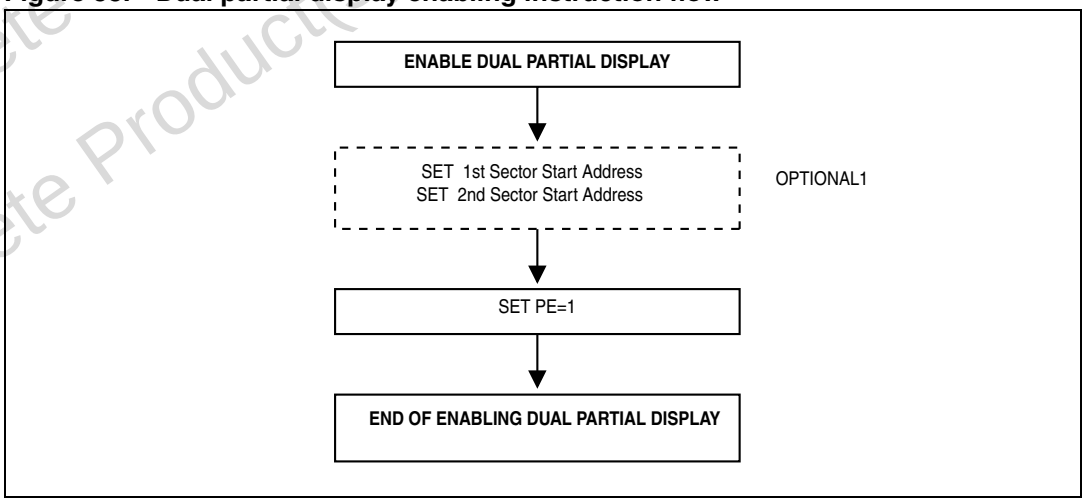


Figure 54. Dual partial display mode configuration or duty change

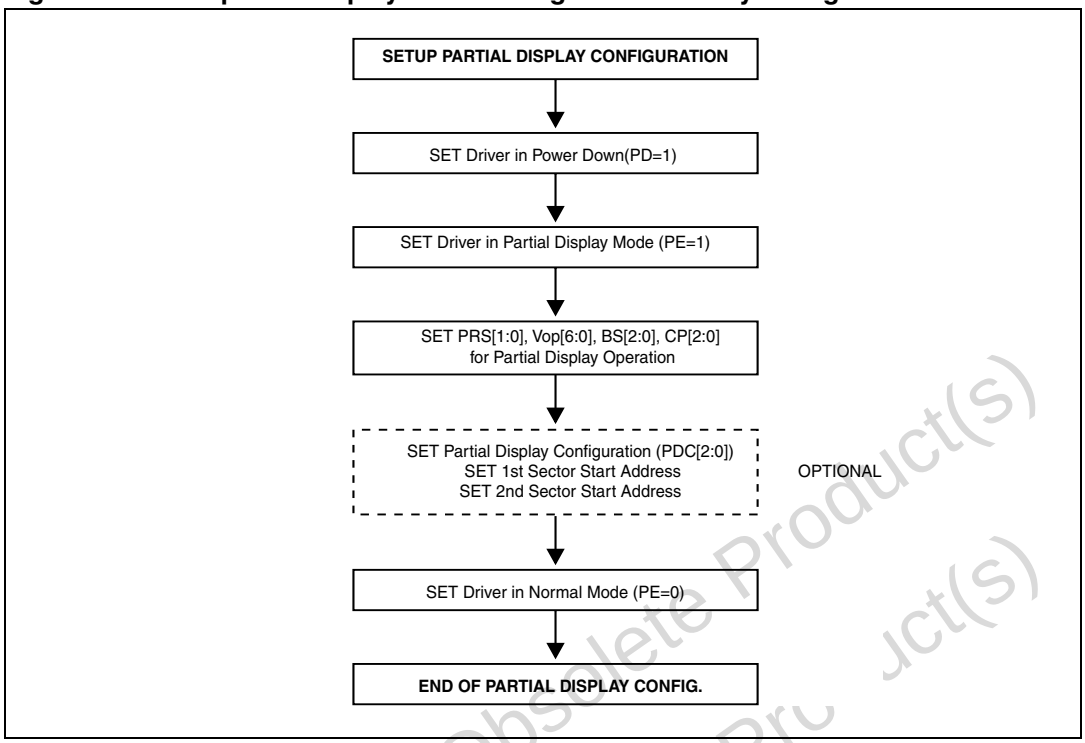


Table 24. Partial display configurations

PDC2	PDC1	PDC0	Section 1	Section2	Reset state
0	0	0	0	8 + Icon Row	000
0	0	1	8	0 + Icon Row	
0	1	0	8	8 + Icon Row	
0	1	1	0	16 + Icon Row	
1	0	0	16	0 + Icon Row	
1	0	1	8	16 + Icon Row	
1	1	0	16	8 + Icon Row	
1	1	1	16	16 + Icon Row	

6 ID-number

The STE2004S lets you program a driver identification number (ID-Number), so more than one LCD module with different configuration parameters can be managed on one platform.

There are four programmable device ID-numbers: 00111100, 00111101, 0011110 and 0011111. All have the first 6 bits (001111) in common. The two least significant bits can be used to connect the SA0 and SA1 inputs to a VSS or VDD1.

The driver ID-number can be read through all communication interfaces. The way to read the ID-number changes according the interface selected. The readout protocol for each interface is described in *Chapter 4*.

Figure 55. I2C interface interconnection in master/ slave mode

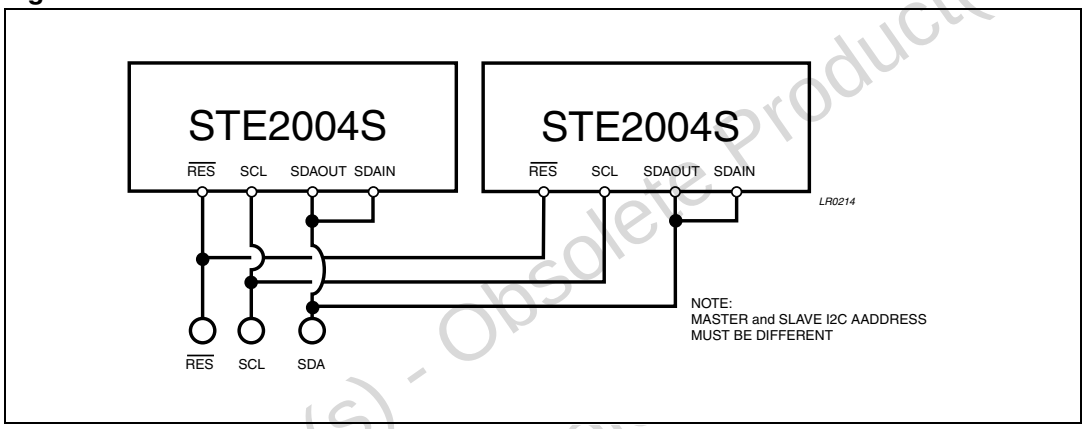


Figure 56. I3-lines SPI and 3-lines serial interfaces interconnection in master slave mode

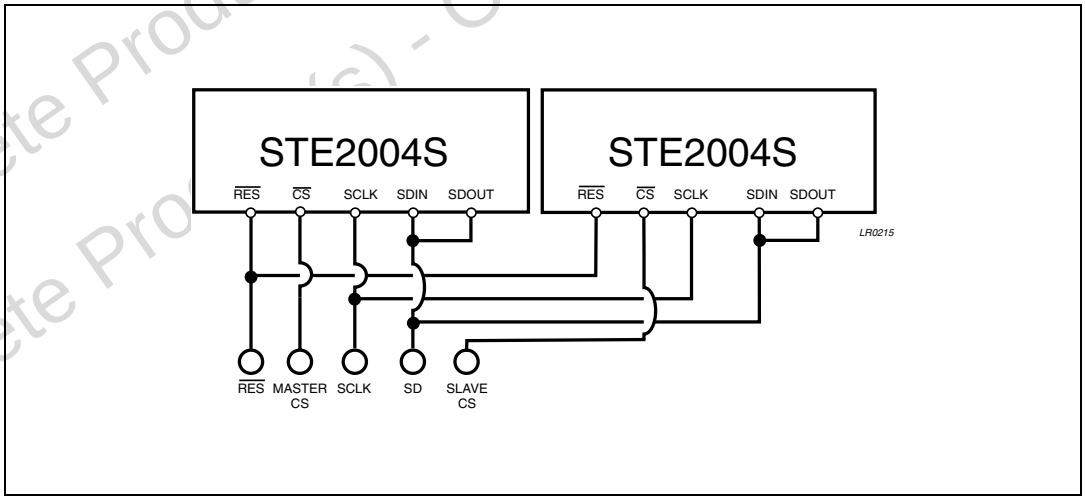


Figure 57. 4-lines SPI interface interconnection in master slave mode

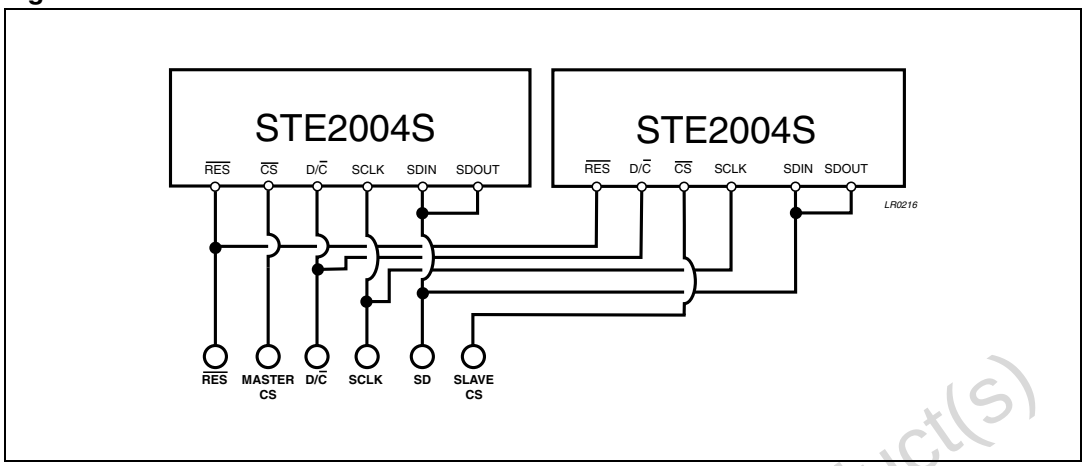


Figure 58. 8080-series and 68000-series interface interconnection in master slave mode

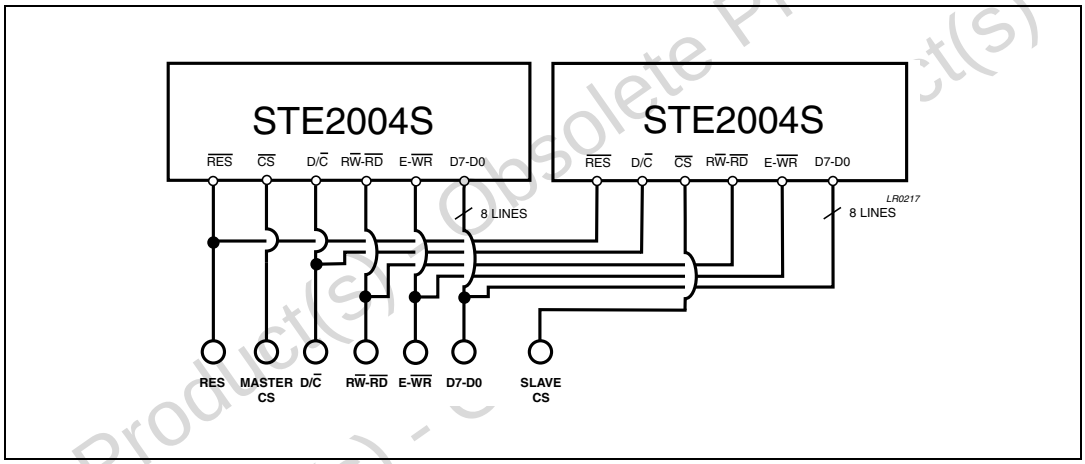


Figure 59. Host processor interconnection with I2C interface

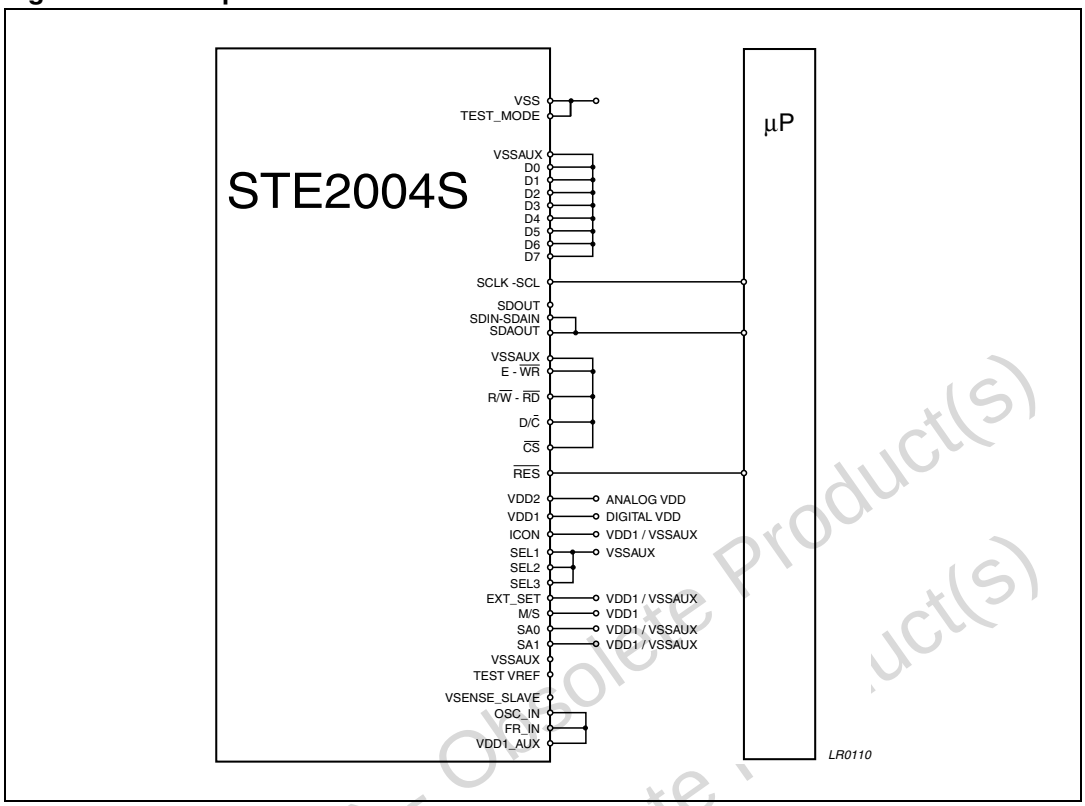


Figure 60. Host processor interconnection with 4-line SPI interface

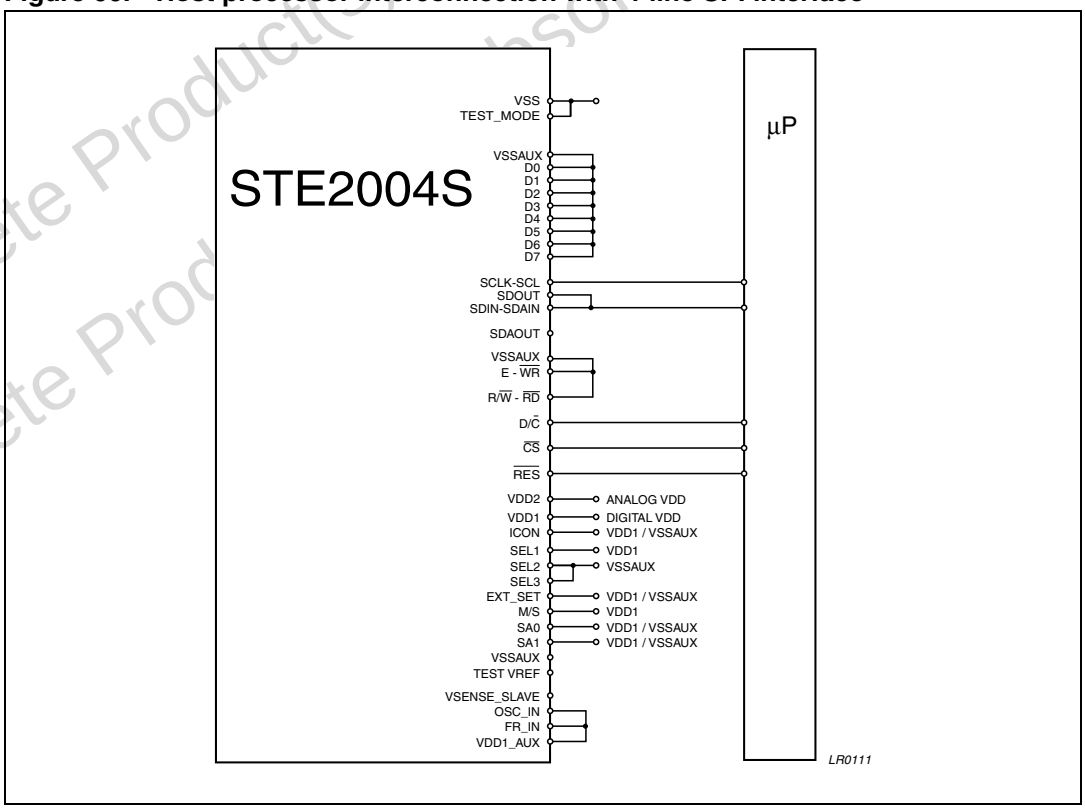


Figure 61. Host processor interconnection with 3-line SPI interface

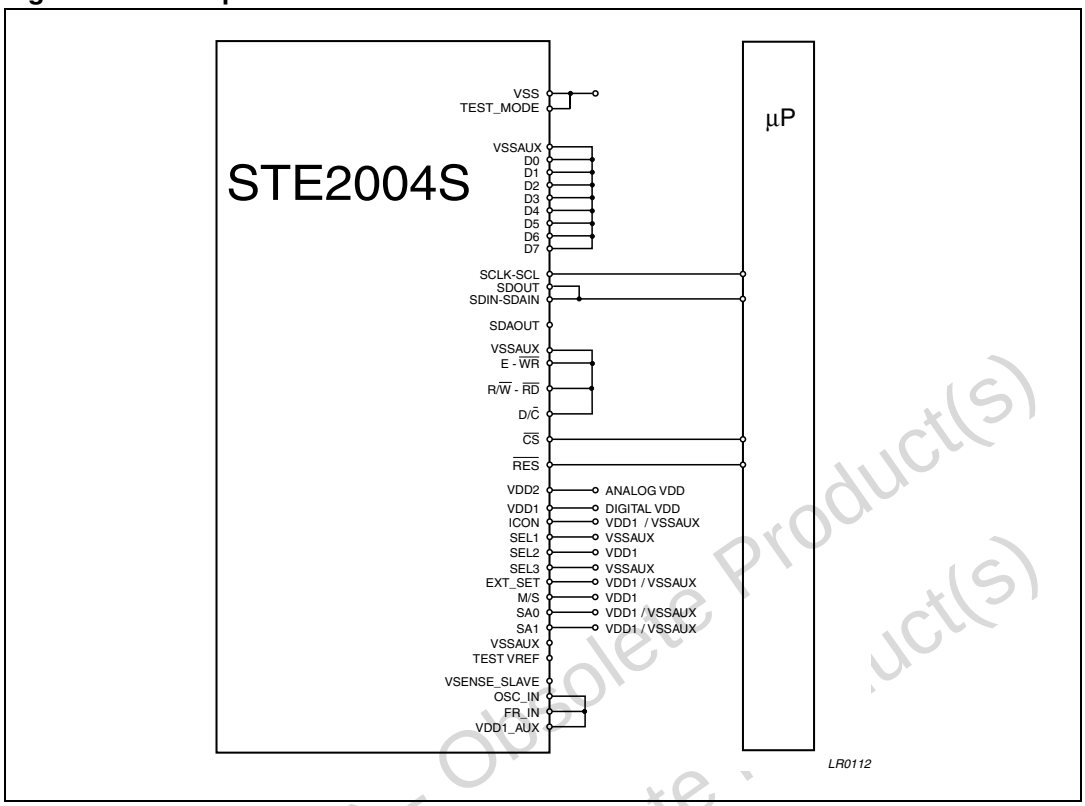


Figure 62. Host processor interconnection with 3-line serial interface

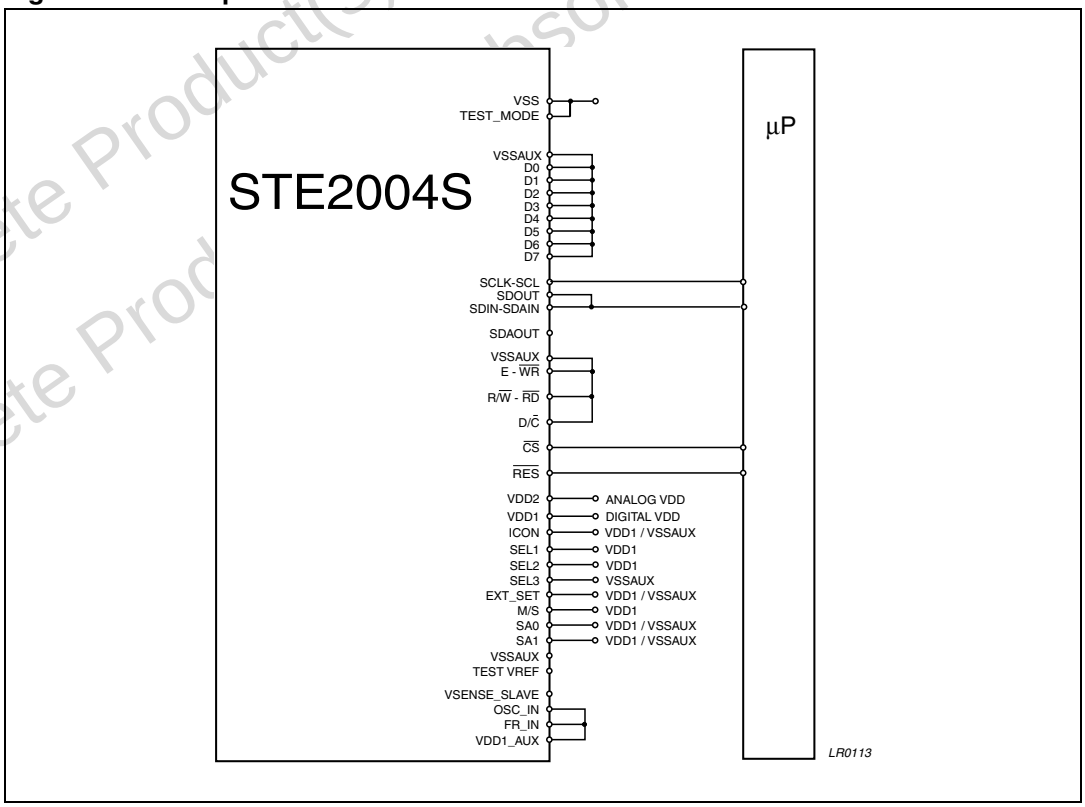


Figure 63. Host processor interconnection with 8080-series parallel interface

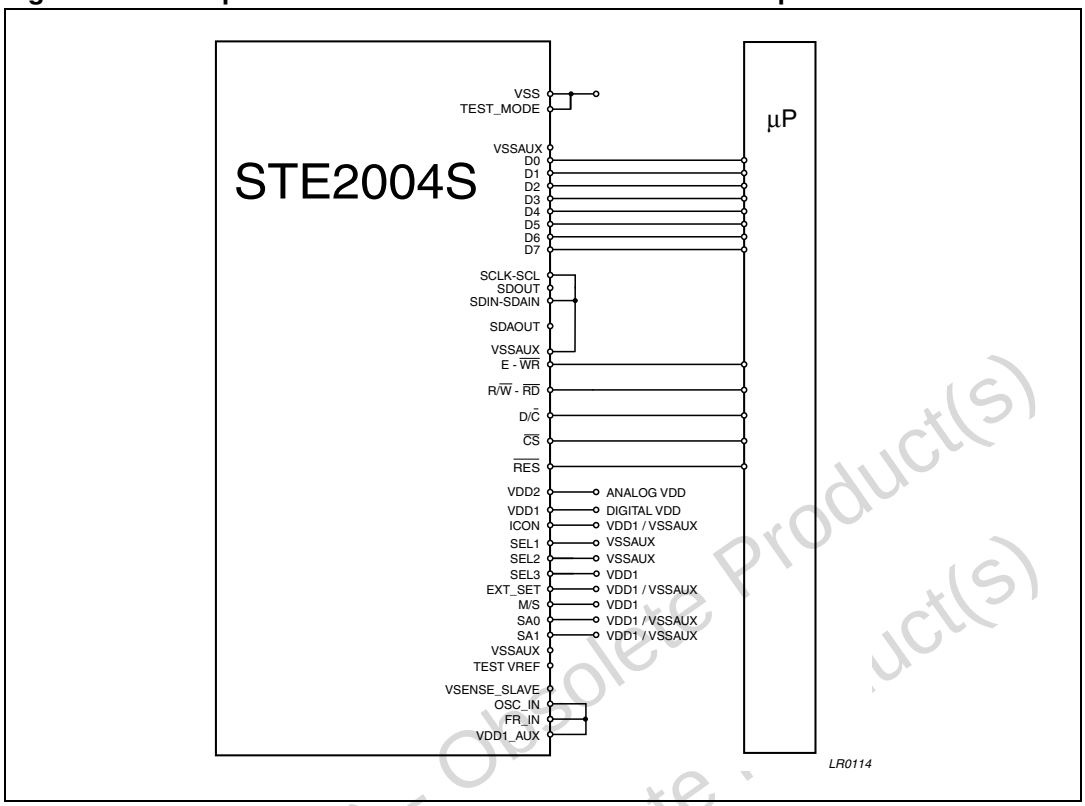


Figure 64. Host processor interconnection with 6800

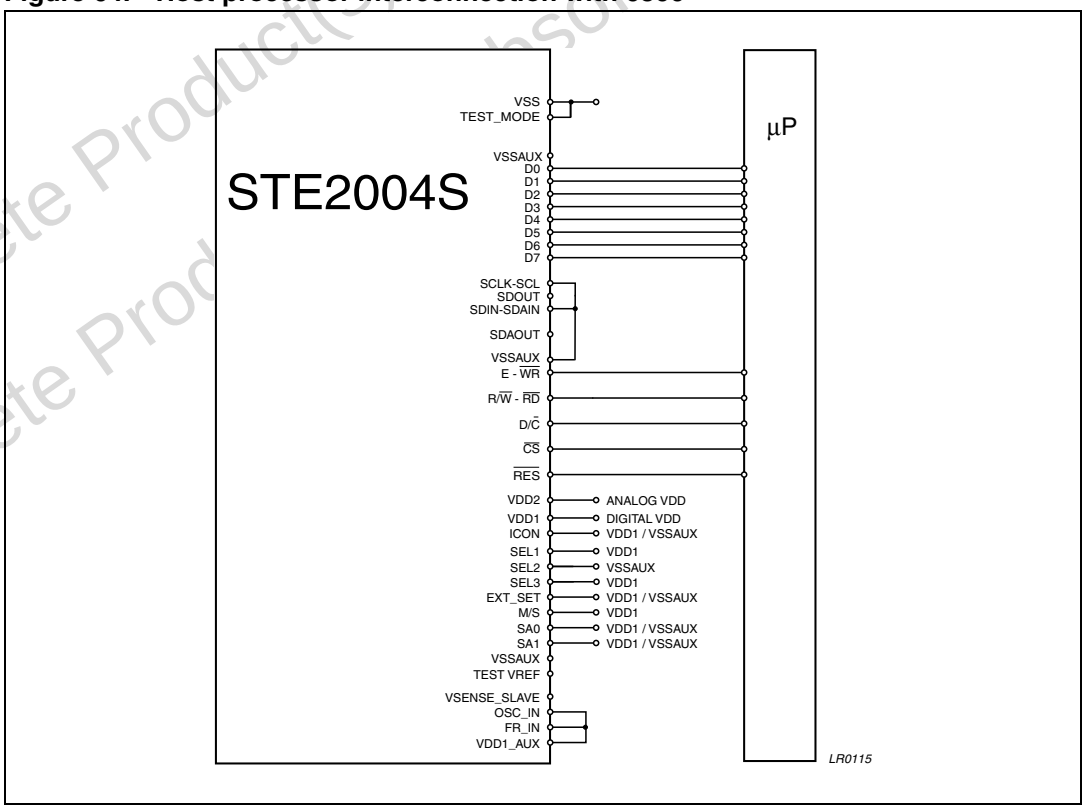


Figure 65. Application schematic using the internal LCD voltage generator and two separate supplies

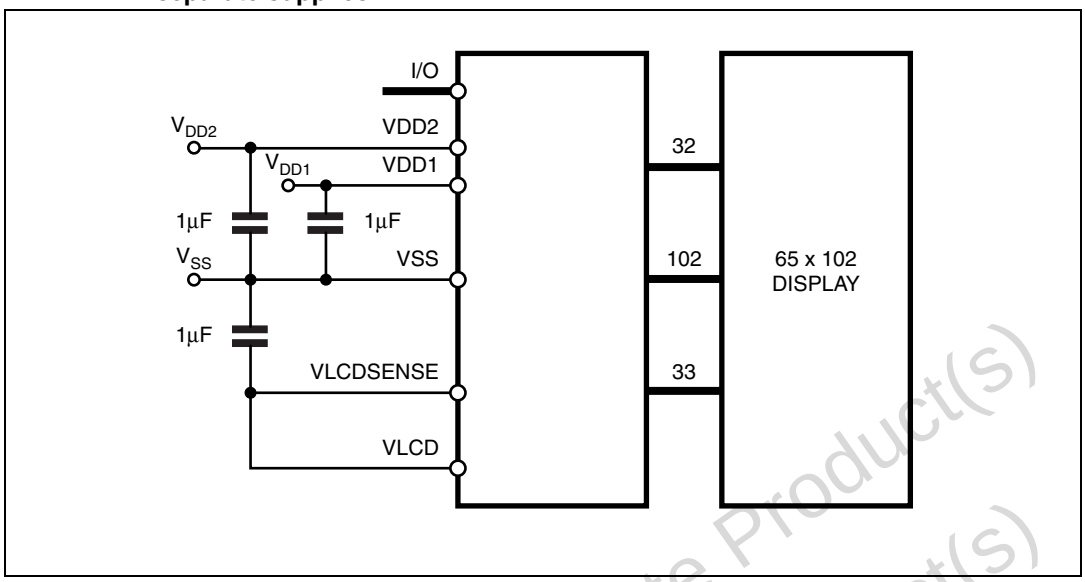


Figure 66. Application schematic using the internal LCD voltage generator and a single supply

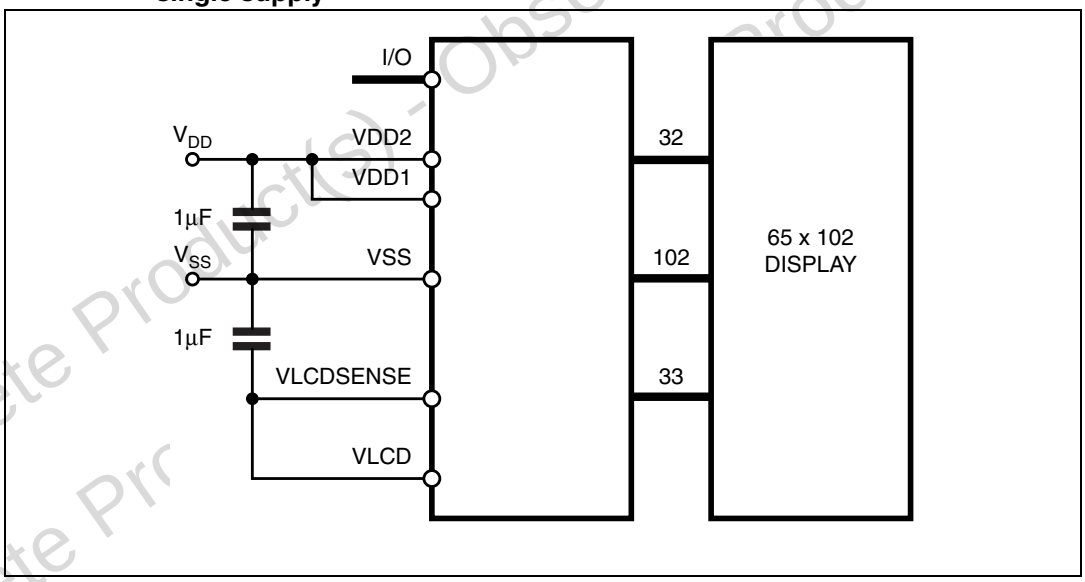


Figure 67. Power-ON timing diagram

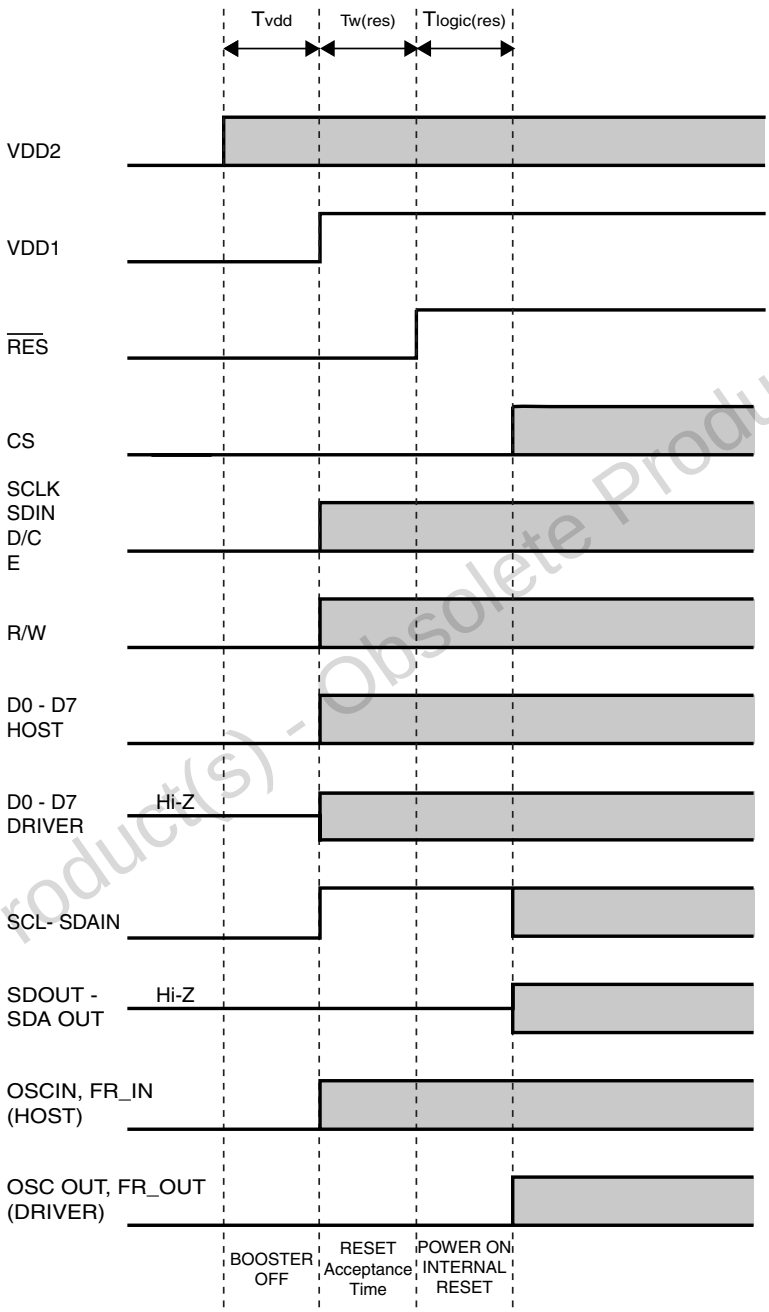


Figure 68. Power-OFF timing diagram

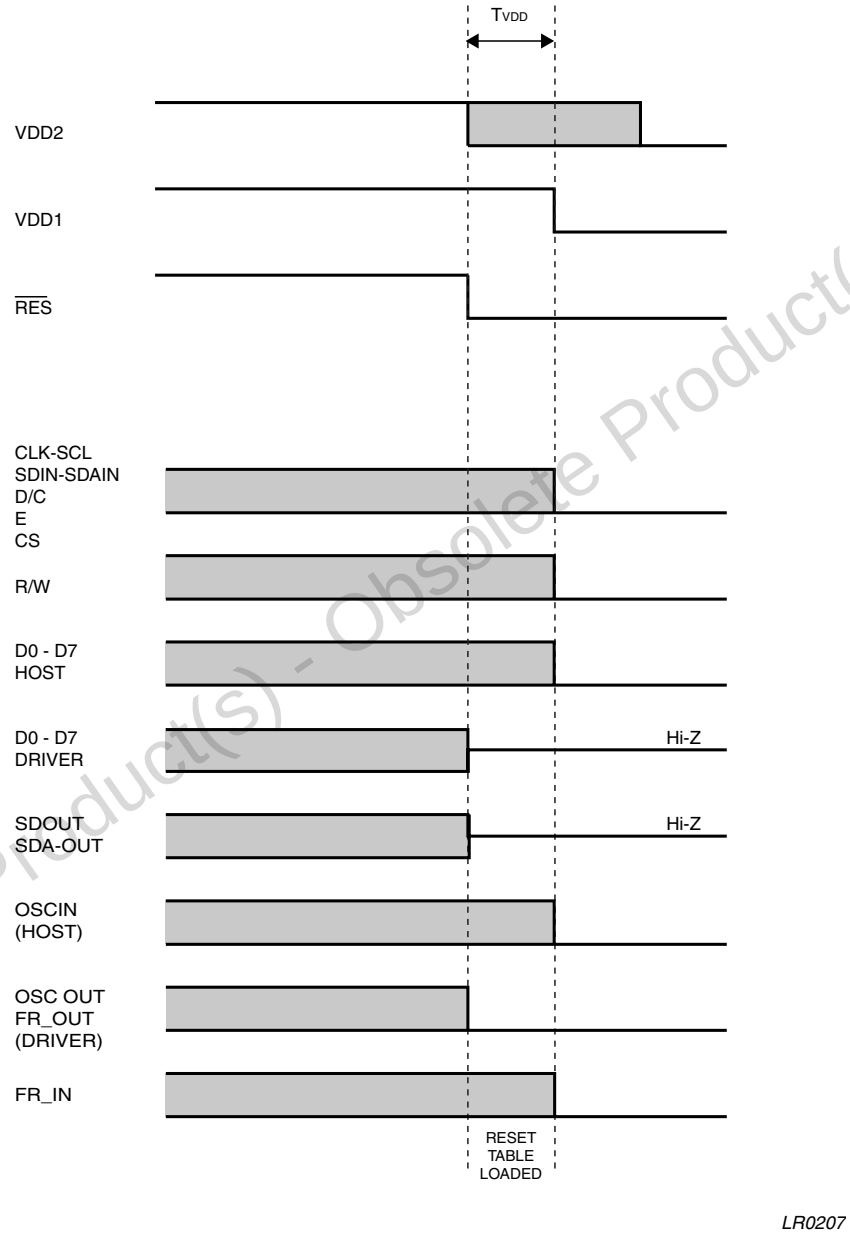


Figure 69. Initialization with built-in booster

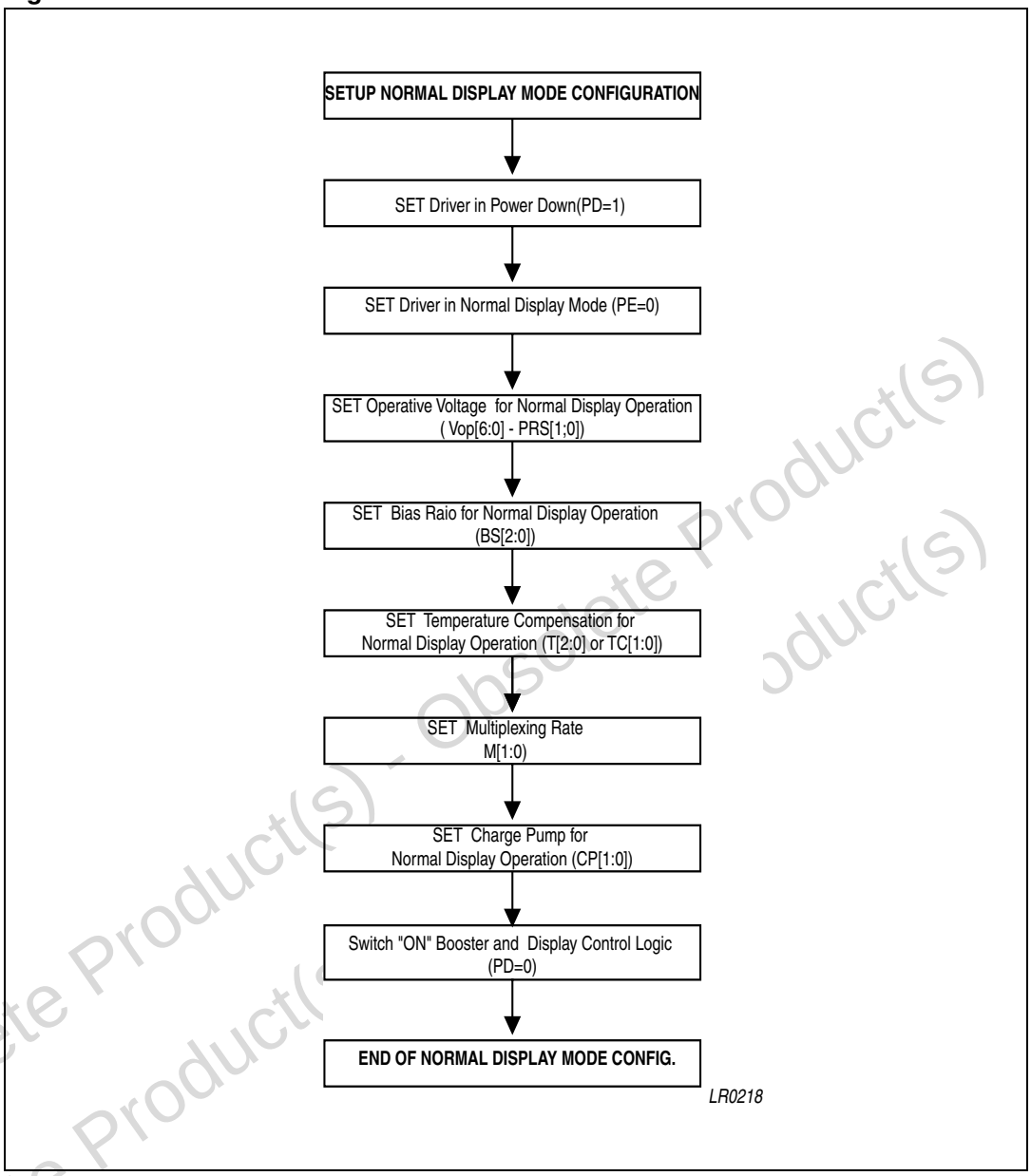


Figure 70. Data RAM to display mapping

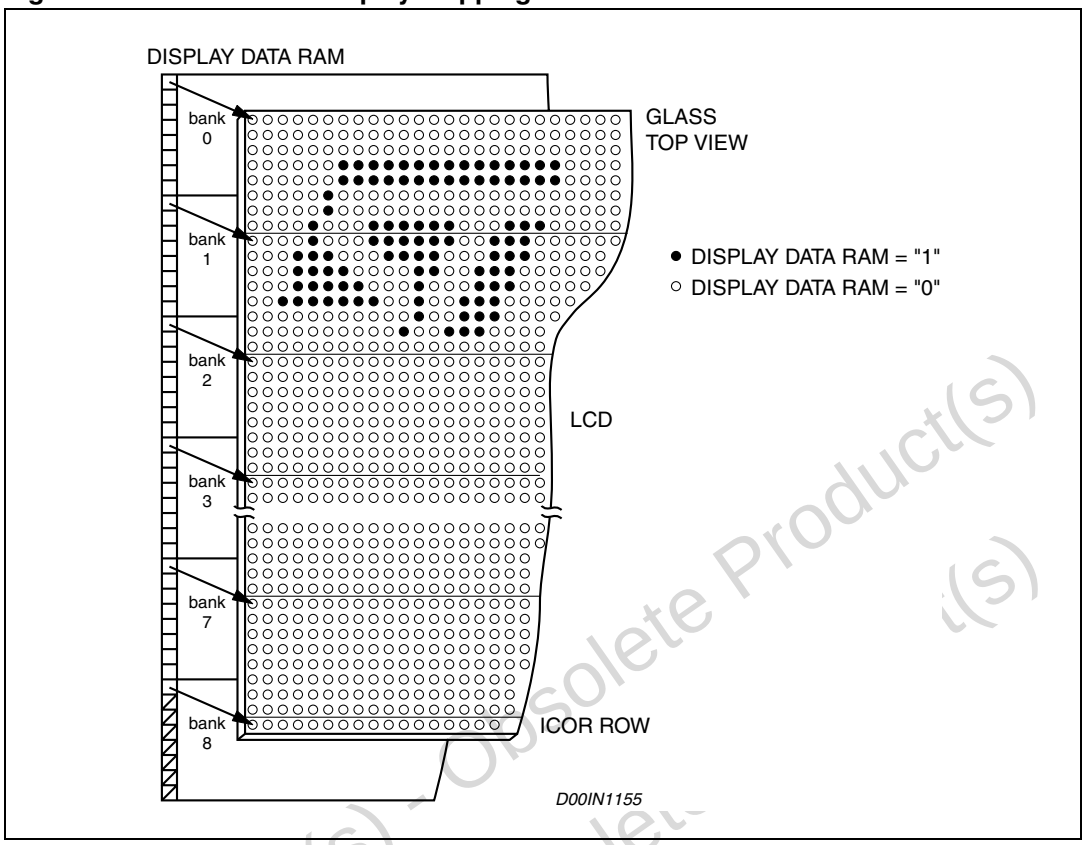


Table 25. Test pin configuration

Test Pin	Pin Configuration
TEST_VREF	OPEN
TEST_MODE	GND

7 Electrical characteristics

7.1 Absolute maximum ratings

Table 26. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD1}	Supply voltage range	- 0.5 to + 5	V
V_{DD2}	Supply voltage range	- 0.5 to + 7	V
V_{LCD}	LCD supply voltage range	- 0.5 to + 15	V
I_{SS}	Supply current	- 50 to +50	mA
V_i	Input voltage (all input pads)	-0.5 to V_{DD1} + 0.5	V
I_{in}	DC input current	- 10 to + 10	mA
I_{out}	DC output current	- 10 to + 10	mA
P_{tot}	Total power dissipation (T_j = 85°C)	300	mW
P_o	Power dissipation per output	30	mW
T_j	Operating junction temperature(1)	-25 to + 85	°C
T_{stg}	Storage temperature	- 65 to 150	°C

1. Device behavior and characterization are measured over this temperature range during internal qualification of the product. During production testing, however, device performance is measured at a fixed ambient temperature - typically 25°C.

7.2 DC operation

VDD1 = 1.7 to 3.6 V; VDD2 = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =25°C; unless otherwise specified.

Table 27. DC operation

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltages						
V_{DD1}	Supply voltage(1)		1.7		3.6	V
					V_{DD2}	V
V_{DD2}	Supply voltage	LCD voltage internally generated	1.75		4.5	V
V_{LCD}	LCD supply voltage	LCD voltage supplied externally	4.5		14.5	V
	LCD supply voltage	Internally generated(2)	4.5		14.5	V
$I(V_{DD1})$	Supply current	V_{DD1} = 2.8V; V_{LCD} = 10V; f_{sclk} = 0; Parallel Port (3) (5)	15	20	40	µA
	Supply current write mode	V_{DD2} = 2.8V; V_{LCD} = 10V; f_{sclk} = 1Mhz; OSC_IN=GND(3)		100	200	µA

Table 27. DC operation (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I(V_{DD2})$	Voltage generator supply current	with V_{OP} = 0 and PRS = [0:0] with external V_{LCD} (4)			5	µA
		V_{DD2} = 2.8V; V_{LCD} = 10V; f_{sclk}=0; no display load; 5x charge pump (5)(3) (6)		60	150	µA
$I(V_{DD1,2})$	Total supply current	V_{DD2} = 2.8V; V_{LCD} = 10V; 5x charge pump; f_{sclk} = 0; no display load (5) (3) (6)		80	190	µA
		Power down mode with internal or external VLCD (7)		3	15	µA
$I(V_{LDCIN})$	External LCD supply voltage current	V_{DD} =2.8V; V_{LCD} =10V; no display load; f_{sclk} = 0; (3)			25	µA
Logic outputs						
V_{0H}	High logic level output voltage	IOH=-500µA	$0.8V_{DD1}$		V_{DD1}	V
V_{OL}	Low logic level output voltage	IOL=+500µA	V_{SS}		$0.2V_{DD1}$	V
Logic inputs						
V_{IL}	Logic low voltage level		V_{SS}		$0.3\ V_{DD1}$	V
V_{IH}	Logic high voltage level		$0.7\ V_{DD1}$		V_{DD2}	V
I_{in}	Input current	V_{in} = V_{SS1} or V_{DD1}	-1		1	µA
Logic inputs/outputs						
V_{IL}	Logic low voltage level		V_{SS}		$0.3\ V_{DD1}$	V
V_{IH}	Logic high voltage level		$0.7\ V_{DD1}$		V_{DD1} + 0.5	V

Table 27. DC operation (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Column and row driver						
R_{row}	ROW output resistance			3K	5K	kohm
R_{col}	Column output resistance			5K	10K	kohm
V_{col}	Column bias voltage accuracy	No load	-50		+50	mV
V_{row}	Row bias voltage accuracy		-50		+50	mV
LCD supply voltage						
V_{LCD}	LCD supply voltage accuracy; internally generated	V_{DD} = 2.8V; V_{LCD} = 10V; fsclk=0; no display load(5)(3) (6) (8) VOP=69h, PRS=2Hex(9)	-2		+2	%
TC0	Temperature coefficient			$-0.0 \cdot 10^{-3}$		1/°C
TC1				$-0.35 \cdot 10^{-3}$		1/°C
TC2				$-0.7 \cdot 10^{-3}$		1/°C
TC3				$-1.05 \cdot 10^{-3}$		1/°C
TC4				$-1.4 \cdot 10^{-3}$		1/°C
TC5				$-1.75 \cdot 10^{-3}$		1/°C
TC6				$-2.1 \cdot 10^{-3}$		1/°C
TC7				$-2.3 \cdot 10^{-3}$		1/°C

1. VDD1<=VDD2
2. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.
3. When f_{sclk} = 0 there is no interface clock.
4. If external V_{LCD}, the display load current is not transmitted to I_{DD}
5. Internal clock
6. Tolerance depends on the temperature; (typically zero at T_{amb} = 25°C), maximum tolerance values are measured at the temperature range limit.
7. Power-down mode. During power-down all static currents are switched-off.
8. For TC0 to TC7
9. Data byte writing mode

7.3 AC operation

VDD1 = 1.7 to 3.6 V; VDD2 = 1.75 to 4.5 V; Vss1,2 = 0V; VLCD = 4.5 to 15 V; Tamb =25°C; unless otherwise specified.

Table 28. AC operation

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Internal oscillator (*Figure 71*)						
F_{OSC}	Internal oscillator frequency	V_{DD} = 2.8V	61	72	83	kHz
F_{EXT}	External oscillator frequency		20		100	kHz
F_{FRAME}	Frame frequency	fosc or fext = 72 kHz(1)		75		Hz
$T_{w(RES)}$	$\overline{RES}$ LOW pulse width		5			µs
	Reset pulse rejection				1	µs
$T_{LOGIC (RES)}$	Internal logic reset time				5	µs
T_{VDD}	VDD1 vs. VDD2 Delay		0			µs
I^2C bus interface (*Figure 72*)(2) (3)						
F_{SCL}	SCL clock frequency	Fast mode	DC		400	kHz
		High speed mode; Cb=100pF (max);(4) V_{DD1}=2	DC		3.4	MHz
		High speed mode; Cb=400pF (max)(4); V_{DD1}=2	DC		1.7	MHz
		Fast Mode (4);V_{DD1}=1.7V			400	KHz
$T_{SU;STA}$	Set-up time (repeated) START condition	Cb = 100pF(5) (6)	160			ns
$T_{HD;STA}$	Hold time (repeated) START condition	Cb = 100pF(5) (6)	160			ns
T_{LOW}	Low period of SCLH clock	Cb = 100pF(5) (6)	160			ns
T_{HIGH}	High period of SCLH clock	Cb = 100pF(5) (6)	160			ns
$T_{SU;DAT}$	Data set-up time	Cb = 100pF(5) (6)	60			ns
$T_{HD;DAT}$	Data hold time	Cb = 100pF(5) (6)	10			ns
$T_{r;CL}$	Rise time of SCLH signal	Cb = 100pF(5) (6)	10			ns
$T_{r;CL1}$	Rise time of SCLH signal after a repeated START condition and aftyer an acknowledge bit	Cb = 100pF(5) (6)	10			ns
$T_{f;CL}$	Fall time of SCLH signal	Cb = 100pF(5) (6)	10			ns

Table 28. AC operation

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{r;DA}$	Rise time of SCLH signal	Cb = 100pF(5) (6)	10			ns
$T_{f;DA}$	Fall time of SDAH signal	Cb = 100pF(5) (6)	10		80	ns
$T_{r;DA}$	Rise time of SDAH signal	Cb = 400pF(5) (6)	20			ns
$T_{f;DA}$	Fall time of SDAH signal	Cb = 400pF(5) (6)	20		160	ns
$T_{SU;STO}$	Setup time for STOP condition	Cb = 100pF(5) (6)	160			ns
Cb	Capacitive load for SDAH and SCLH		100		400	pF
Cb	Capacitive load for SDAH +SDA line and SCLH +SCL line				400	pF
Parallel interface (*Figure 73*, *Figure 74*)						
T_{CYC}	System cycle time	V_{DD1} = 1.7V; read and write	125			ns
T_{CLW}	Control low pulse width (WR)		20			ns
T_{CHW}	Control high pulse width (WR)		75			ns
T_{CLR}	Control low pulse width (RD)		40			ns
T_{CHR}	Control high pulse width (RD)		55			ns
T_{EWHW}	Enable high pulse width (Write)		60			ns
T_{EWLW}	Enable low pulse width (Write)		60			ns
T_{EWHR}	Enable high pulse width (Read)		60			ns
T_{EWLR}	Enable low pulse width (Read)		60			ns
$T_{SU(A)}$	Address set-up time		10			ns
$T_{H(A)}$	Address hold time		10			ns
T_{SU1}	Data set-up time		30			ns
T_{H1}	Data hold time		30			ns
T_{SU2}	Read access time				40	ns
T_{H2}	Output disable time		0		30	ns

Table 28. AC operation

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Serial interface (*Figure 75*)						
F_{SCLK}	Clock frequency	V_{DD1} = 1.7V;	8			MHz
T_{CYC}	Clock cycle SCLK		125			ns
T_{PWH1}	SCLK pulse width HIGH		60			ns
T_{PWL1}	SCLK pulse width LOW		60			ns
T_{S2}	$\overline{CS}$ setup time	V_{DD1} = 1.7V	40			ns
T_{H2}	$\overline{CS}$ hold time	V_{DD1} = 1.7V	50			ns
T_{PWH2}	$\overline{CS}$ minimum high time	V_{DD1} = 1.7V	50			ns
T_{S3}	SD/$\overline{C}$ setup time		30			ns
T_{H3}	SD/$\overline{C}$ hold time		30			ns
T_{S4}	SDIN setup time		30			ns
T_{H4}	SDIN hold time		40			ns
T_{S5}	SDOUT access time				30	ns
T_{H5}	SDOUT disable time vs. SCLK		0		20	ns
T_{H6}	SDOUT disable time vs. CS		0		20	ns

1. $F_{frame} = \frac{f_{osc}}{960}$
2. For bus line loads Cb between 100 and 400pF the timing parameters must be linearly interpolated
3. Trise and Tfall (30%-70%) -10ns
4. C_{VLCD} is the filtering capacitor on VLCD
5. All timing values are valid within the operating supply voltage and ambient temperature ranges and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}
6. Cb is the capacitive load for each bus line.

Figure 71. Reset timing diagram

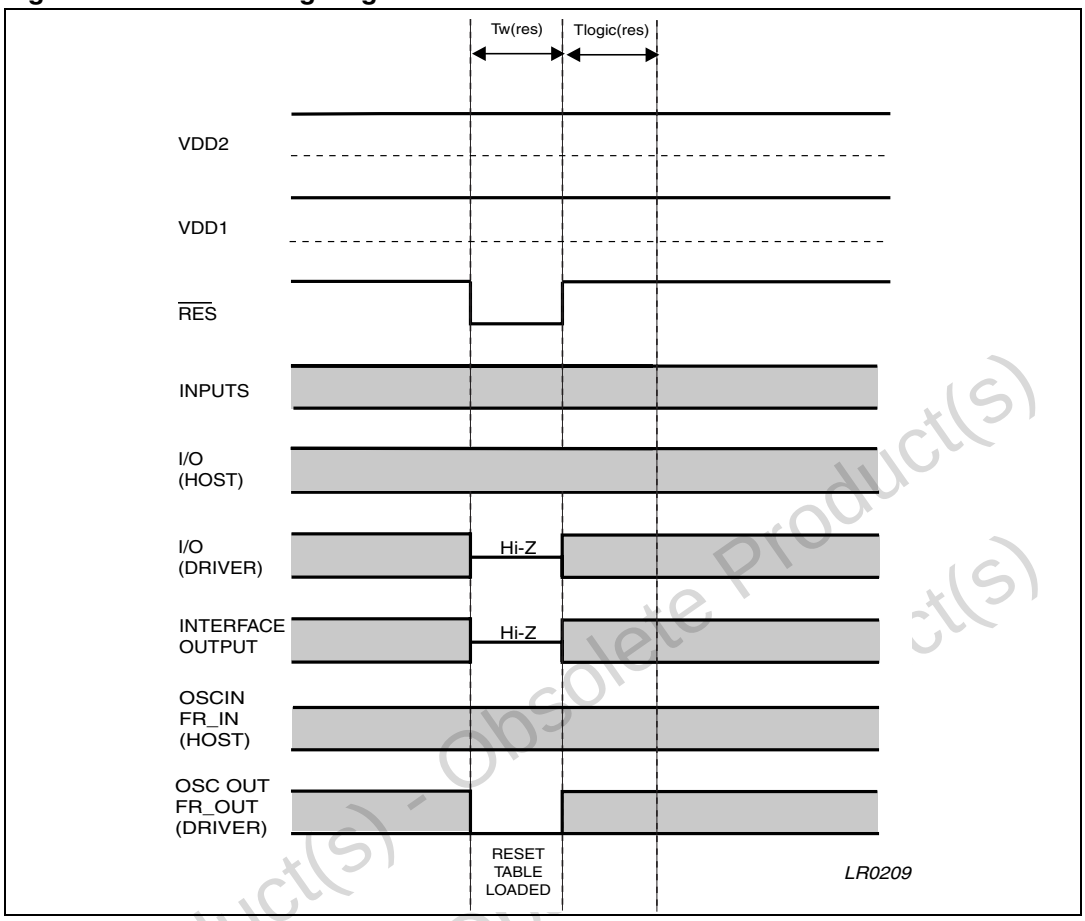


Figure 72. I²C-bus timings

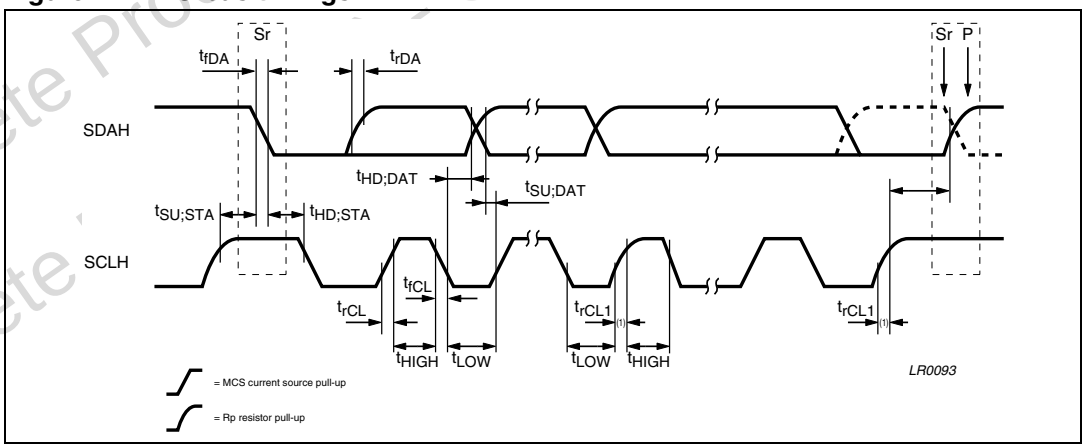


Figure 73. 68000-series parallel interface timing

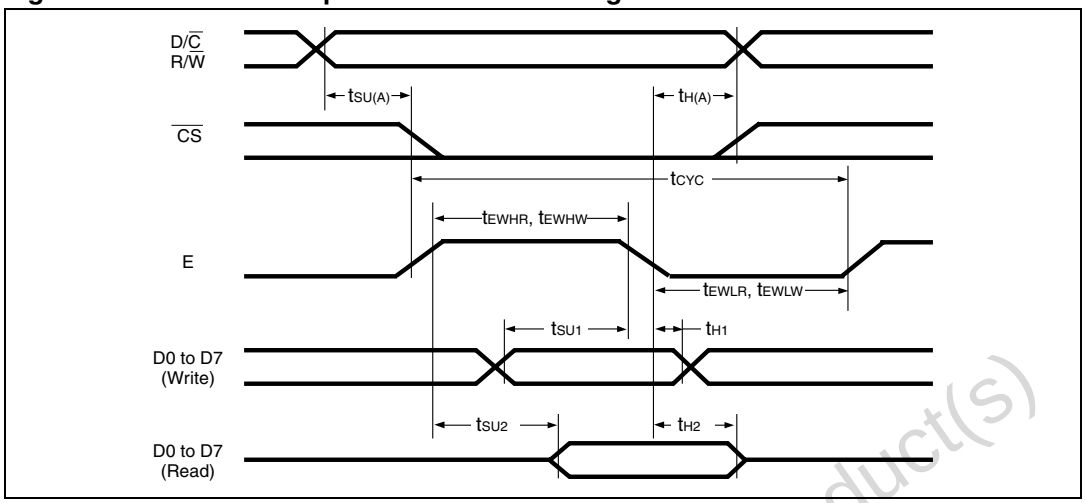


Figure 74. 8080-series parallel interface timing

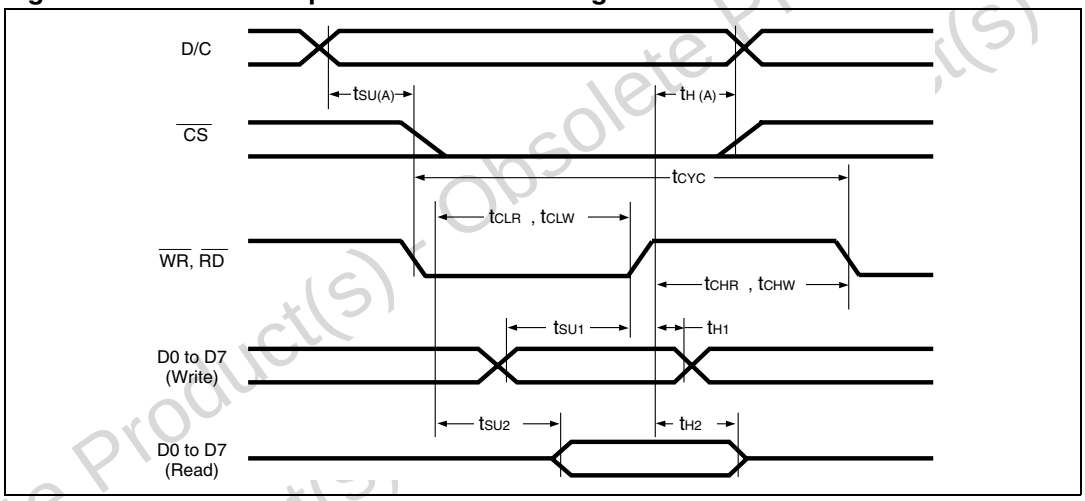
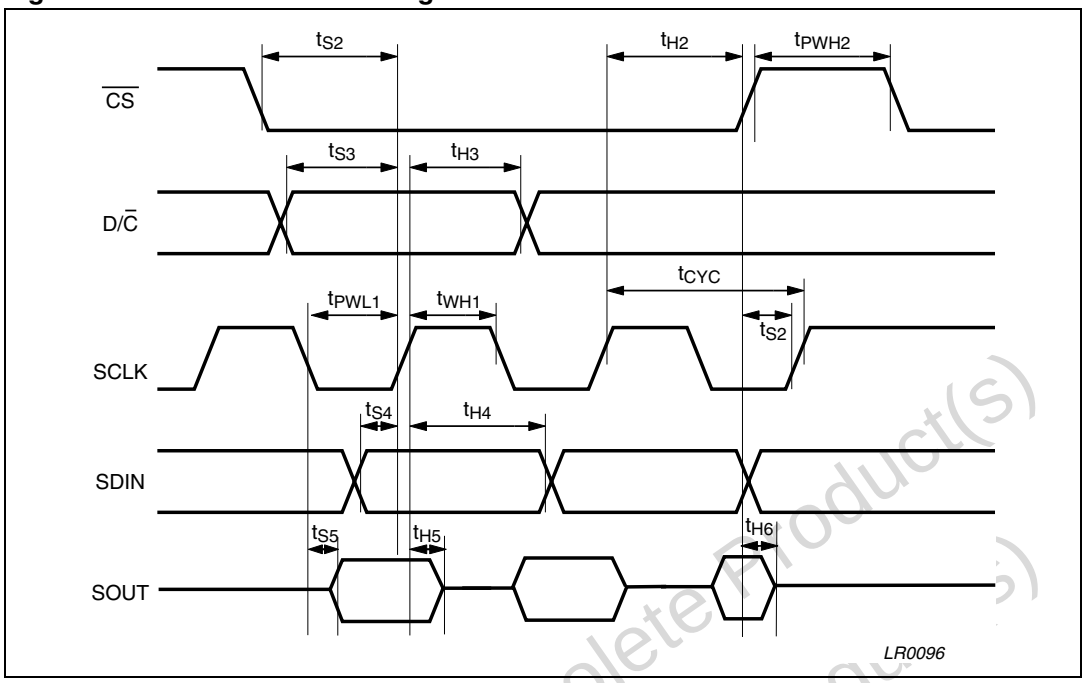


Figure 75. Serial interface timing



8 Pad coordinates

See *Table 29: Pad coordinates* and *Table 30: Alignment marks coordinates*.

Table 29. Pad coordinates

N°	Name	Pad placements	
		X	Y
1	R5	-2632.5	-532.8
2	R4	-2587.5	-532.8
3	R3	-2542.5	-532.8
4	R2	-2497.5	-532.8
5	R1	-2452.5	-532.8
6	R0	-2407.5	-532.8
7	C0	-2362.5	-532.8
8	C1	-2317.5	-532.8
9	C2	-2272.5	-532.8
10	C3	-2227.5	-532.8
11	C4	-2182.5	-532.8
12	C5	-2137.5	-532.8
13	C6	-2092.5	-532.8
14	C7	-2047.5	-532.8
15	C8	-2002.5	-532.8
16	C9	-1957.5	-532.8
17	C10	-1912.5	-532.8
18	C11	-1867.5	-532.8
19	C12	-1822.5	-532.8
20	C13	-1777.5	-532.8
21	C14	-1732.5	-532.8
22	C15	-1687.5	-532.8
23	C16	-1642.5	-532.8
24	C17	-1597.5	-532.8
25	C18	-1552.5	-532.8
26	C19	-1507.5	-532.8
27	C20	-1462.5	-532.8
28	C21	-1417.5	-532.8
29	C22	-1372.5	-532.8
30	C23	-1327.5	-532.8
31	C24	-1282.5	-532.8
32	C25	-1237.5	-532.8
33	C26	-1192.5	-532.8
34	C27	-1147.5	-532.8
35	C28	-1102.5	-532.8
36	C29	-1057.5	-532.8
37	C30	-1012.5	-532.8
38	C31	-967.5	-532.8
39	C32	-922.5	-532.8
40	C33	-877.5	-532.8
41	C34	-832.5	-532.8
42	C35	-787.5	-532.8
43	C36	-742.5	-532.8
44	C37	-697.5	-532.8
45	C38	-652.5	-532.8
46	C39	-607.5	-532.8
47	C40	-562.5	-532.8
48	C41	-517.5	-532.8
49	C42	-472.5	-532.8
50	C43	-427.5	-532.8
51	C44	-382.5	-532.8
52	C45	-337.5	-532.8
53	C46	-292.5	-532.8
54	C47	-247.5	-532.8
55	C48	-202.5	-532.8
56	C49	-157.5	-532.8
57	C50	-112.5	-532.8
58	C51	112.5	-532.8
59	C52	157.5	-532.8
60	C53	202.5	-532.8
61	C54	247.5	-532.8
62	C55	292.5	-532.8
63	C56	337.5	-532.8
64	C57	382.5	-532.8
65	C58	427.5	-532.8
66	C59	472.5	-532.8

Table 29. Pad coordinates

N°	Name	Pad placements	
		X	Y
67	C60	517.5	-532.8
68	C61	562.5	-532.8
69	C62	607.5	-532.8
70	C63	652.5	-532.8
71	C64	697.5	-532.8
72	C65	742.5	-532.8
73	C66	787.5	-532.8
74	C67	832.5	-532.8
75	C68	877.5	-532.8
76	C69	922.5	-532.8
77	C70	967.5	-532.8
78	C71	1012.5	-532.8
79	C72	1057.5	-532.8
80	C73	1102.5	-532.8
81	C74	1147.5	-532.8
82	C75	1192.5	-532.8
83	C76	1237.5	-532.8
84	C77	1282.5	-532.8
85	C78	1327.5	-532.8
86	C79	1372.5	-532.8
87	C80	1417.5	-532.8
88	C81	1462.5	-532.8
89	C82	1507.5	-532.8
90	C83	1552.5	-532.8
91	C84	1597.5	-532.8
92	C85	1642.5	-532.8
93	C86	1687.5	-532.8
94	C87	1732.5	-532.8
95	C88	1777.5	-532.8
96	C89	1822.5	-532.8
97	C90	1867.5	-532.8
98	C91	1912.5	-532.8
99	C92	1957.5	-532.8

N°	Name	Pad placements	
		X	Y
100	C93	2002.5	-532.8
101	C94	2047.5	-532.8
102	C95	2092.5	-532.8
103	C96	2137.5	-532.8
104	C97	2182.5	-532.8
105	C98	2227.5	-532.8
106	C99	2272.5	-532.8
107	C100	2317.5	-532.8
108	C101	2362.5	-532.8
109	R32	2407.5	-532.8
110	R33	2452.5	-532.8
111	R34	2497.5	-532.8
112	R35	2542.5	-532.8
113	R36	2587.5	-532.8
114	R37	2632.5	-532.8
115	R38	2773.8	-472.5
116	R39	2773.8	-427.5
117	R40	2773.8	-382.5
118	R41	2773.8	-337.5
119	R42	2773.8	-292.5
120	R43	2773.8	-247.5
121	R44	2773.8	-202.5
122	R45	2773.8	-157.5
123	R46	2773.8	-112.5
124	R47	2773.8	-67.5
125	R48	2773.8	-22.5
126	R49	2773.8	22.5
127	R50	2773.8	67.5
128	R51	2773.8	112.5
129	R52	2773.8	157.5
130	R53	2773.8	202.5
131	R54	2773.8	247.5
132	R55	2773.8	292.5

Table 29. Pad coordinates

N°	Name	Pad placements	
		X	Y
133	R56	2773.8	337.5
134	R57	2773.8	382.5
135	R58	2773.8	427.5
136	R59	2773.8	472.5
137	R60	2632.5	532.8
138	R61	2587.5	532.8
139	R62	2542.5	532.8
140	R63	2497.5	532.8
141	R64/ICON	2452.5	532.8
142	VDD1 AUX	2227.5	532.8
143	FR IN	2182.5	532.8
144	OSC IN	2137.5	532.8
145	Vsns_Slave	2092.5	532.8
146	TEST_VREF	1777.5	532.8
147	VSSAUX	1732.5	532.8
148	SA1	1687.5	532.8
149	SA0	1642.5	532.8
150	M/S	1597.5	532.8
151	EXT_SET	1552.5	532.8
152	SEL3	1507.5	532.8
153	SEL2	1462.5	532.8
154	SEL1	1417.5	532.8
155	ICON	1372.5	532.8
156	VDD1	1327.5	532.8
157	VDD1	1282.5	532.8
158	VDD1	1237.5	532.8
159	VDD1	1192.5	532.8
160	VDD1	1147.5	532.8
161	VDD1	1102.5	532.8
162	VDD1	1057.5	532.8
163	VDD1	1012.5	532.8
164	VDD2	967.5	532.8
165	VDD2	922.5	532.8
166	VDD2	877.5	532.8
167	VDD2	832.5	532.8
168	VDD2	787.5	532.8
169	VDD2	742.5	532.8
170	VDD2	697.5	532.8
171	VDD2	652.5	532.8
172	_RES	337.5	532.8
173	-CS	247.5	532.8
174	D/C	157.5	532.8
175	RW-RD	67.5	532.8
176	E-WR	-22.5	532.8
177	VSSAUX	-67.5	532.8
178	SDA_OUT	-157.5	532.8
179	SDIN_SDAIN	-202.5	532.8
180	SDOUT	-247.5	532.8
181	SCLK_SCL	-337.5	532.8
182	D7	-382.5	532.8
183	D6	-427.5	532.8
184	D5	-472.5	532.8
185	D4	-517.5	532.8
186	D3	-562.5	532.8
187	D2	-607.5	532.8
188	D1	-652.5	532.8
189	D0	-697.5	532.8
190	VSSAUX	-742.5	532.8
191	TEST_MODE	-1102.5	532.8
192	VSS	-1147.5	532.8
193	VSS	-1192.5	532.8
194	VSS	-1237.5	532.8
195	VSS	-1282.5	532.8
196	VSS	-1327.5	532.8
197	VSS	-1372.5	532.8
198	VSS	-1417.5	532.8

Table 29. Pad coordinates

N°	Name	Pad placements	
		X	Y
199	VSS	-1462.5	532.8
200	VSS	-1507.5	532.8
201	VSS	-1552.5	532.8
202	VSS	-1597.5	532.8
203	VSS	-1642.5	532.8
204	VLCD_SNS	-1867.5	532.8
205	VLCD	-1912.5	532.8
206	VLCD	-1957.5	532.8
207	VLCD	-2002.5	532.8
208	VLCD	-2047.5	532.8
209	VLCD	-2092.5	532.8
210	OSC_OUT	-2227.5	532.8
211	FR_OUT	-2272.5	532.8
212	R31	-2497.5	532.8
213	R30	-2542.5	532.8
214	R29	-2587.5	532.8
215	R28	-2632.5	532.8
216	R27	-2773.8	472.5
217	R26	-2773.8	427.5
218	R25	-2773.8	382.5
219	R24	-2773.8	337.5
220	R23	-2773.8	292.5
221	R22	-2773.8	247.5
222	R21	-2773.8	202.5
223	R20	-2773.8	157.5
224	R19	-2773.8	112.5
225	R18	-2773.8	67.5
226	R17	-2773.8	22.5
227	R16	-2773.8	-22.5
228	R15	-2773.8	-67.5
229	R14	-2773.8	-112.5
230	R13	-2773.8	-157.5
231	R12	-2773.8	-202.5
232	R11	-2773.8	-247.5
233	R10	-2773.8	-292.5
234	R9	-2773.8	-337.5
235	R8	-2773.8	-382.5
236	R7	-2773.8	-427.5
237	R6	-2773.8	-472.5

1. I^2C bus AC characteristics are tested by correlation

Table 30. Alignment marks coordinates

Marks	X	Y
mark1	-2780.55	-539.55
mark2	2780.55	-539.55
mark3	-2160.0	539.55
mark4	484.89	539.55

Figure 76. Alignment marks dimensions

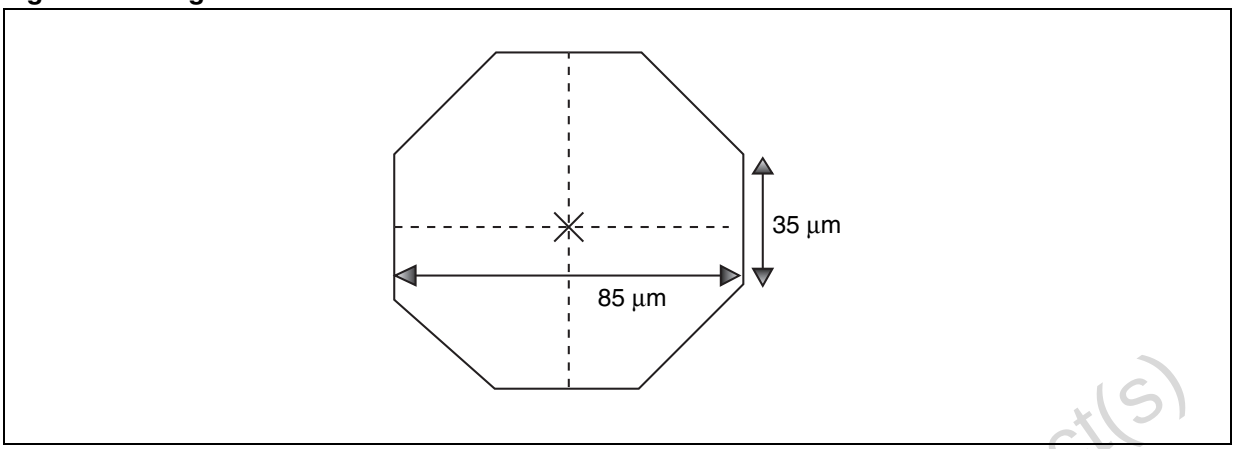


Table 31. Bumps

	Dimensions
Bumps size	28µmX97µmX17.5µm
Pad size	35µm X 104µm
Pad pitch	45µm
Spacing between bumps	17µm

Table 32. Die mechanical dimensions

Die Size (X x Y)	5.815mm x 1.333mm
Wafers thickness	500µm

9 Ordering information

Table 33. Ordering information

Part numbers	Type
STE2004S DIE2	Bumped dice on waffle pack

10 Revision history

Table 34. Document revision history

Date	Revision	Changes
24-Jan-2006	1	Initial release.
12-Dec-2006	2	– Junction temperature range in *Table 26: Absolute maximum ratings* set to: -25 to + 85 and added a footnote. – Globally set T_{amb} = 25°C – Moved Table 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20 from *Chapter 6: ID-number* to *Chapter 5: Instruction set* where Table 8 and Table 9 are referenced. – Ordering information moved from cover page to *Chapter 9*.
31-Jan-2007	3	Added *Chapter 1: Block diagram* and corrected the document title.

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