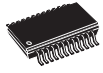
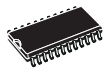


## Low voltage 16-bit constant current LED sink driver



QSOP-24



SO-24



TSSOP-24

TSSOP-24  
(exposed pad)

### Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial data IN/parallel data OUT
- Can be driven by a 3.3 V microcontroller
- Output current: 5 to 100 mA
- Max clock frequency 30 MHz
- ESD protection: 2 kV HBM, 200 V MM

### Description

The **STP16CP05** is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The **STP16CP05** contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs.

The output current setup time is 40 ns (typ.), thus improving the system performance.

The LEDs' brightness can be controlled by using an external resistor to adjust the **STP16CP05** output current.

The **STP16CP05** guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V micro controller.

Maturity status link

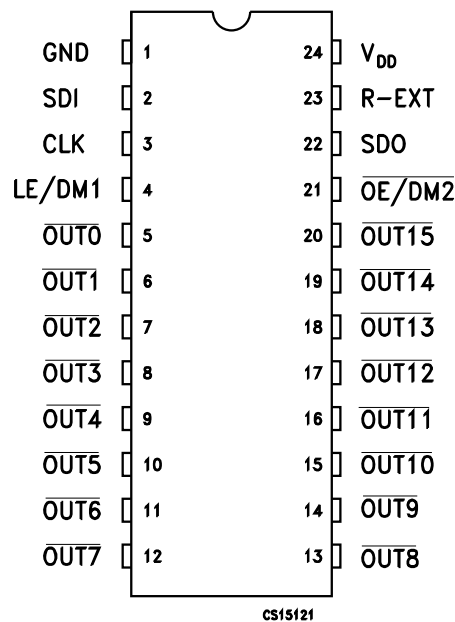
[STP16CP05](#)

# 1 Summary description

**Table 1. Typical current accuracy**

Output voltage	Current accuracy		Output current	V <sub>DD</sub>	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1.5 %	± 5 %	20 to 100 mA	3.3 V to 5 V	25 °C

## 1.1 Pin connection and description

**Figure 1. Pin connection**


GIPD280920150957MT

*Note:* The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

**Table 2. Pin description**

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{\text{OE/DM2}}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V <sub>DD</sub>	Supply voltage terminal

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	0 to 7	V
$V_O$	Output voltage	-0.5 to 20	V
$I_O$	Output current	100	mA
$V_I$	Input voltage	-0.4 to $V_{DD}$	V
$I_{GND}$	GND terminal current	1600	mA
$f_{CLK}$	Clock frequency	50	MHz
$T_J$	Junction temperature range	-40 to +170	°C

### 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit	
$T_{OPR}$	Operating temperature range	-40 to +125	°C	
$T_{STG}$	Storage temperature range	-55 to +150	°C	
$R_{thJA}$	Thermal resistance junction-ambient <sup>(1)</sup>	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24 exposed pad <sup>(2)</sup>	37.5	°C/W
		QSOP-24	55	°C/W

1. According with JEDEC standard 51-7.

2. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

## 2.3 Recommended operating conditions

@  $T_A = 25\text{ }^\circ\text{C}$

**Table 5. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage		3.0	-	5.5	V
$V_O$	Output voltage			-	20	V
$I_O$	Output current	OUTn	3	-	100	mA
$I_{OH}$	Output current	SERIAL-OUT		-	+1	mA
$I_{OL}$	Output current	SERIAL-OUT		-	-1	mA
$V_{IH}$	Input voltage		$0.7 V_{DD}$	-	$V_{DD}$	V
$V_{IL}$	Input voltage		-0.3	-	$0.3 V_{DD}$	V
$t_{wLAT}$	LE/DM1 pulse width	$V_{DD} = 3.0\text{ V to }5.0\text{ V}$	6	-		ns
$t_{wCLK}$	CLK pulse width		8	-		ns
$t_{wEN}$	$\overline{OE}/\overline{DM2}$ pulse width		100	-		ns
$t_{SETUP(D)}$	Setup time for DATA		5	-		ns
$t_{HOLD(D)}$	Hold time for DATA		3	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		18	-		ns
$f_{CLK}$	Clock frequency		Cascade operation $V_{DD} = 5\text{ V}^{(1)}$		-	30

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

### 3 Electrical characteristics

$V_{DD} = 3.3\text{ V to }5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 6. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input voltage high level		$0.7 V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3 V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 20\text{ V}$			1	$\mu\text{A}$
$V_{OL}$	Output voltage (serial-OUT)	$I_{OL} = 1\text{ mA}$			0.4	V
$V_{OH}$	Output voltage (serial-OUT)	$I_{OH} = -1\text{ mA}$	$V_{DD}-0.4\text{V}$			V
$I_{OL1}$	Output current	$V_O = 0.3\text{ V}$ , $R_{ext} = 4.2\text{ k}\Omega$	4.25	5	5.75	mA
$I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{ext} = 1\text{ k}\Omega$	19	20	21	
$I_{OL3}$		$V_O = 1.3\text{ V}$ , $R_{ext} = 200\ \Omega$	96	100	104	
$\Delta I_{OL1}$	Output current error between bit (all output ON)	$V_O = 0.3\text{ V}$ , $R_{ext} = 4.2\text{ k}\Omega$		$\pm 5$	$\pm 8$	%
$\Delta I_{OL2}$		$V_O = 0.3\text{ V}$ , $R_{ext} = 1\text{ k}\Omega$		$\pm 1.5$	$\pm 3$	
$\Delta I_{OL3}$		$V_O = 1.3\text{ V}$ , $R_{ext} = 200\ \Omega$		$\pm 1.2$	$\pm 3$	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	$\text{k}\Omega$
$R_{SIN(down)}$	Pull-down resistor		100	200	400	$\text{k}\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{ext} = 1\text{ k}\Omega$ , OUT 0 to 15 = OFF		4		mA
$I_{DD(OFF2)}$		$R_{ext} = 250\ \Omega$ , OUT 0 to 15 = OFF		11.2		
$I_{DD(ON1)}$	Supply current (ON)	$R_{ext} = 1\text{ k}\Omega$ , OUT 0 to 15 = ON		4.5		
$I_{DD(ON2)}$		$R_{ext} = 250\ \Omega$ , OUT 0 to 15 = ON		11.7		
Thermal	Thermal protection			170		$^\circ\text{C}$

$V_{DD} = 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 7. Switching characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{PLH1}$	Propagation delay time, CLK-OUT <sub>n</sub> , LE/DM1 = H, OE/DM2 = L	$V_{DD} = 3.3\text{ V}$	-	45	74	ns
		$V_{DD} = 5\text{ V}$	-	24	38	
$t_{PLH2}$	Propagation delay time, LE/DM1-OUT <sub>n</sub> , OE/DM2 = L	$V_{DD} = 3.3\text{ V}$	-	48	77	ns
		$V_{DD} = 5\text{ V}$	-	27	46	
$t_{PLH3}$	Propagation delay time, OE/DM2-OUT <sub>n</sub> , LE/DM1 = H	$V_{DD} = 3.3\text{ V}$	-	75	128	ns
		$V_{DD} = 5\text{ V}$	-	43	64	
$t_{PLH}$	Propagation delay time, CLK-SDO	$V_{DD} = 3.3\text{ V}$	-	19	28	ns
		$V_{DD} = 5\text{ V}$	-	11	16.5	
$t_{PHL1}$	Propagation delay time, CLK-OUT <sub>n</sub> , LE/DM1 = H, OE/DM2 = L	$V_{DD} = 3.3\text{ V}$	-	15	23	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{OUTn}$ , LE/DM1 = H, $\overline{OE}/DM2 = L$	$V_{IH} = V_{DD}$ $V_{IL} = GND$ $C_L = 10$ pF $I_O = 20$ mA $V_L = 3.0$ V $R_{ext} = 1$ K $\Omega$ $R_L = 60$ $\Omega$	$V_{DD} = 5$ V	-	10	14	ns
$t_{PHL2}$	Propagation delay time, LE/DM1- $\overline{OUTn}$ , $\overline{OE}/DM2 = L$		$V_{DD} = 3.3$ V	-	13	18.5	
			$V_{DD} = 5$ V	-	9	12	ns
$t_{PHL3}$	Propagation delay time, $\overline{OE}/DM2$ - $\overline{OUTn}$ , LE/DM1 = H		$V_{DD} = 3.3$ V	-	17	24.5	
			$V_{DD} = 5$ V	-	14	19.5	ns
$t_{PHL}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3$ V	-	23	35	
			$V_{DD} = 5$ V	-	14	21	ns
$t_{ON}$	Output rise time 10~90% of voltage waveform		$V_{DD} = 3.3$ V	-	35	68	
			$V_{DD} = 5$ V	-	21	31.5	ns
$t_{OFF}$	Output fall time 90~10% of voltage waveform		$V_{DD} = 3.3$ V	-	10.5	15	
		$V_{DD} = 5$ V	-	11	15.5	ns	
$t_r$	CLK rise time <sup>(1)</sup>		-		5000	ns	
$t_f$	CLK fall time <sup>(1)</sup>		-		5000	ns	

1. In order to achieve high cascade data transfer, please consider  $t_r/t_f$  timings carefully.

## 4 Equivalent circuit of inputs and outputs

Figure 2.  $\overline{OE}/DM2$  terminal

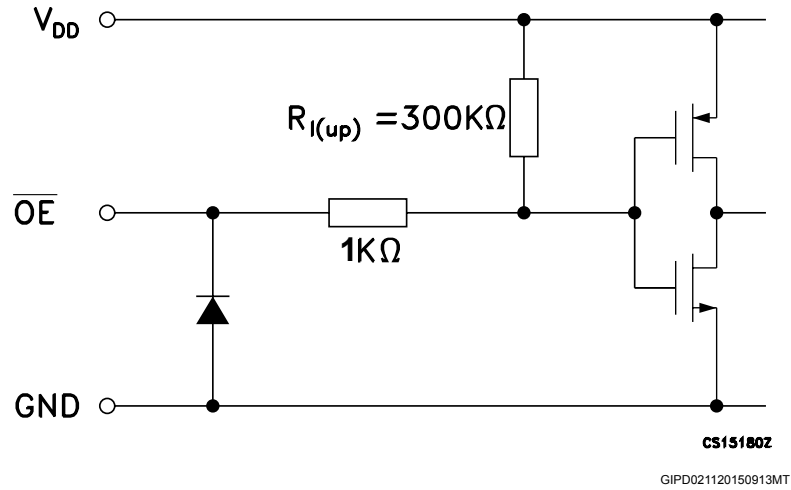


Figure 3. LE/DM1 terminal

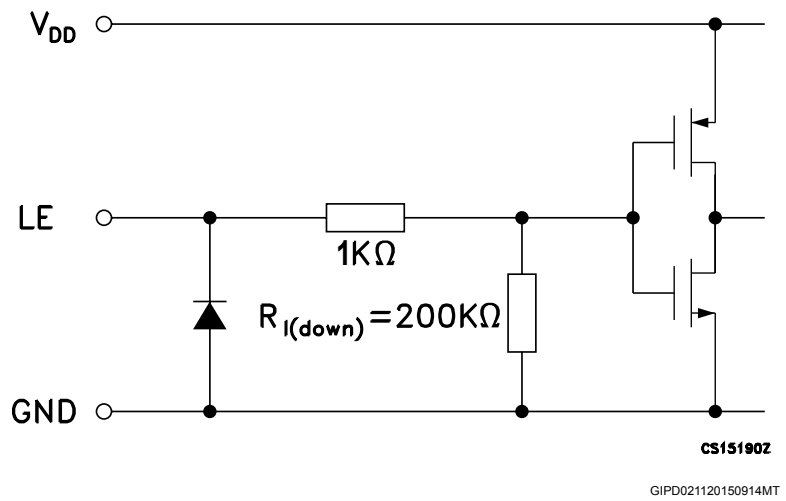
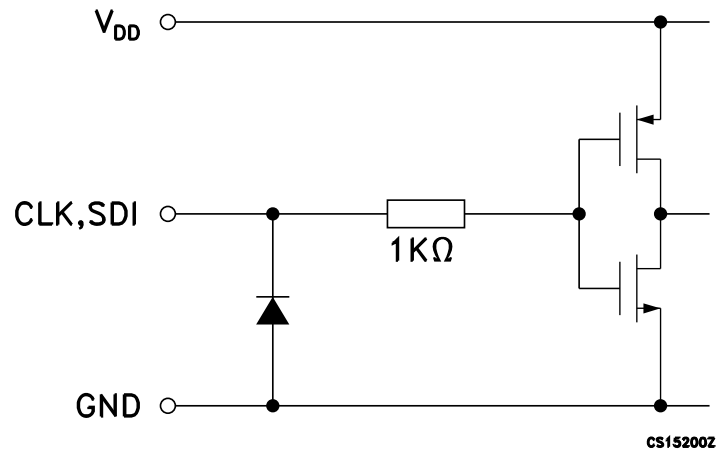
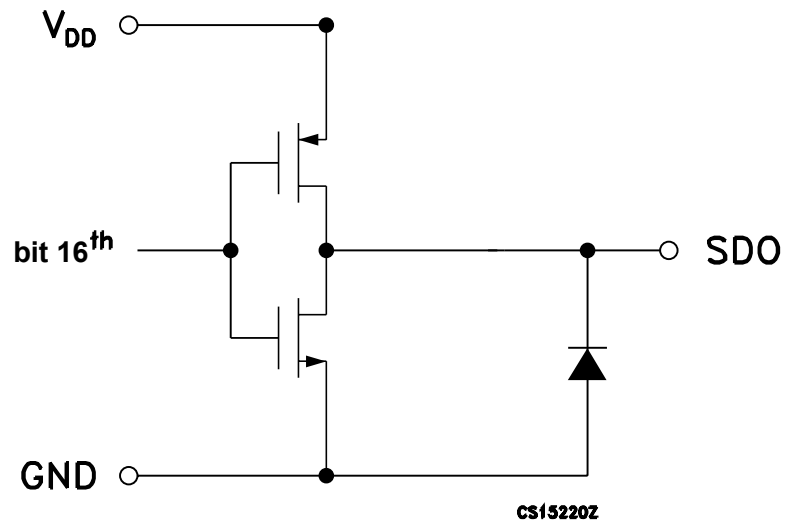


Figure 4. CLK, SDI terminal



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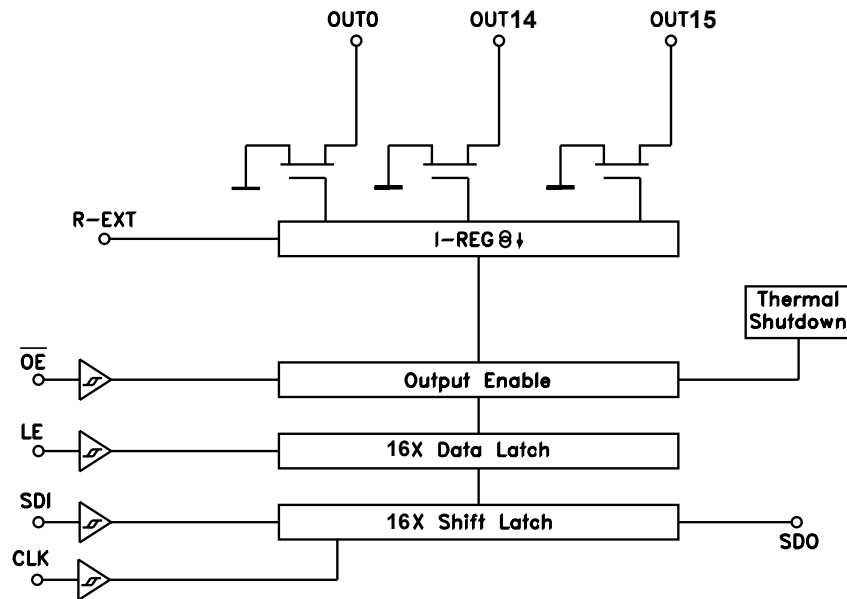
Figure 5. SDO terminal



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Figure 6. Block diagram



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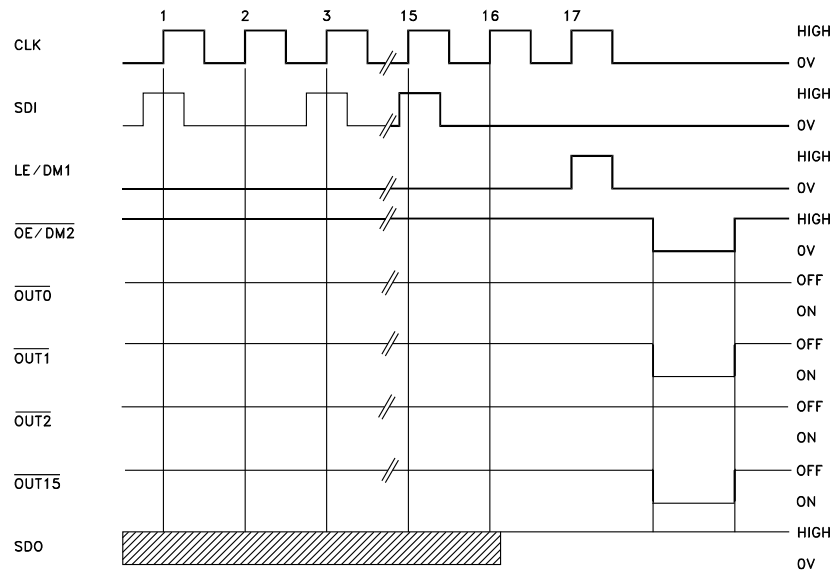
## 5 Timing diagrams

Table 8. Truth table

CLOCK	LE/DM1	OE/DM2	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
	H	L	Dn	Dn ..... Dn - 7 ..... Dn - 15	Dn - 15
	L	L	Dn + 1	No change	Dn - 14
	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn - 13	Dn - 13
	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn - 13	Dn - 13
	X	H	Dn + 3	OFF	Dn - 13

Note:  $OUTn = ON$  when  $Dn = H$   $OUTn = OFF$  when  $Dn = L$ .

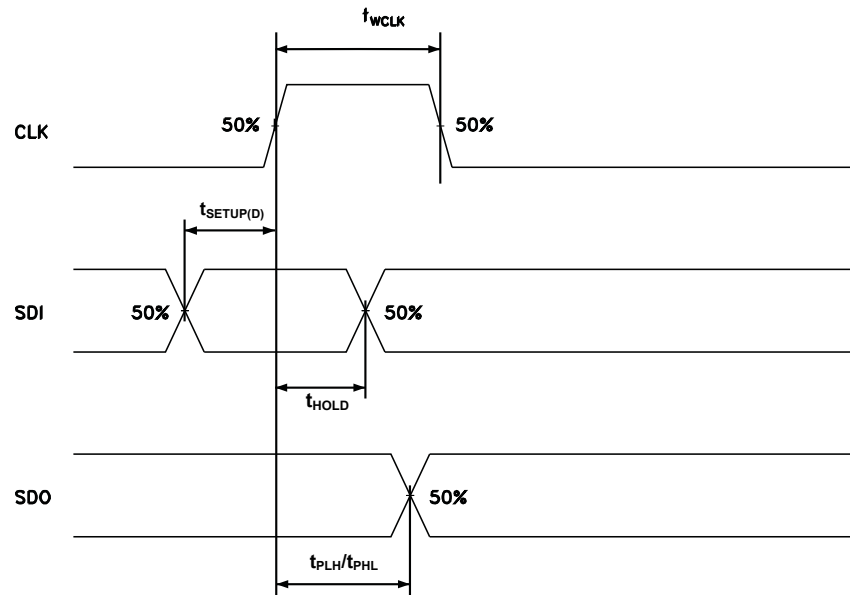
Figure 7. Timing diagram



GIPD300920151126MT

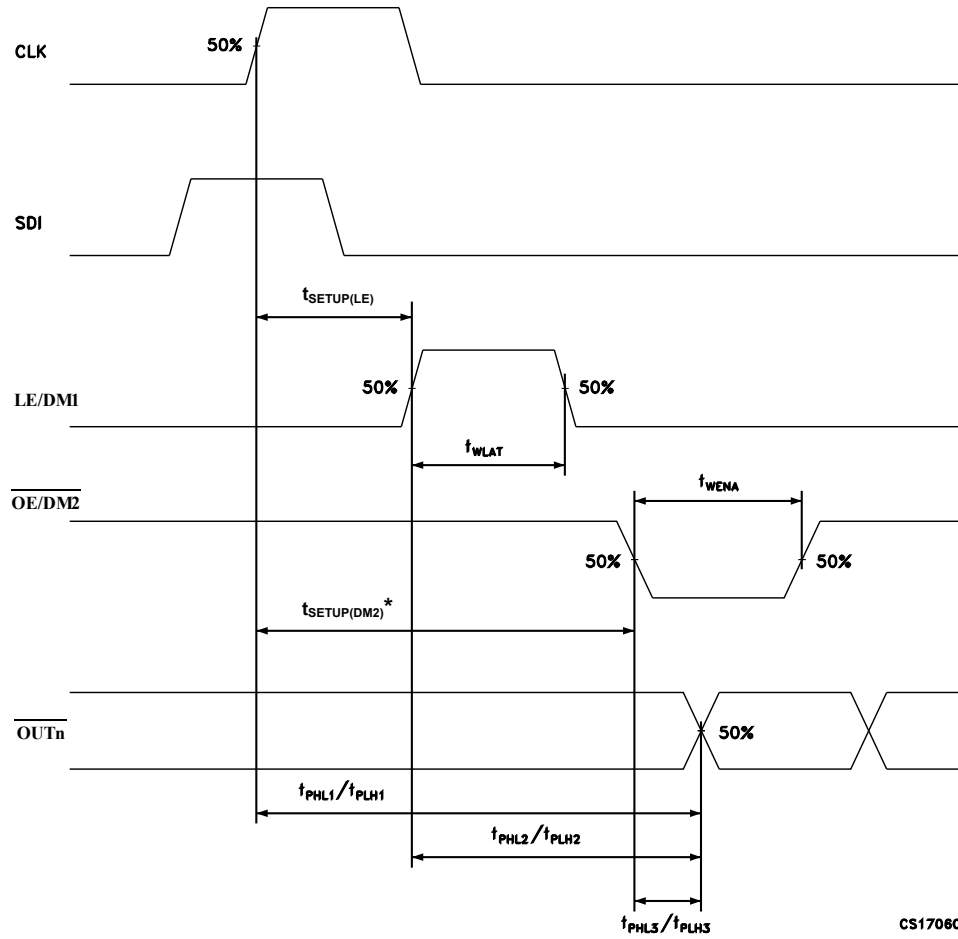
Note: 1 Latch and output enable terminals are level-sensitive and are not synchronized with rising or falling edge of CLK signal. 2 When LE/DM1 terminal is low level, the latch circuit holds previous set of data. 3 When LE/DM1 terminal is high level, the latch circuit refreshes new set of data from SDI chain. 4 When OE/DM2 terminal is at low level, the output terminals Out 0 to Out 15 respond to data in the latch circuits, either '1' for ON or '0' for OFF. 5 When OE/DM2 terminal is at high level, all output terminals are switched OFF.

Figure 8. Clock, serial-in, serial-out



AMG130220170701MT

Figure 9. Clock, serial-in, latch, enable, outputs

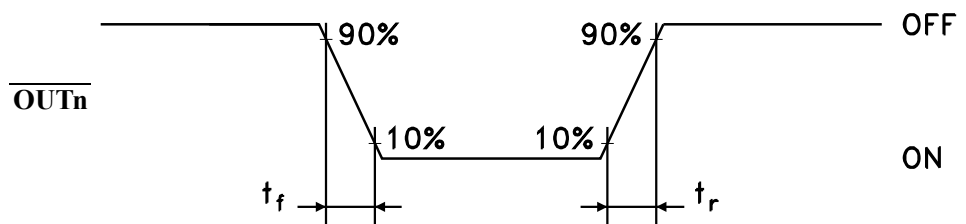


CS17060

\* Only for detection feature.

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Figure 10. Outputs

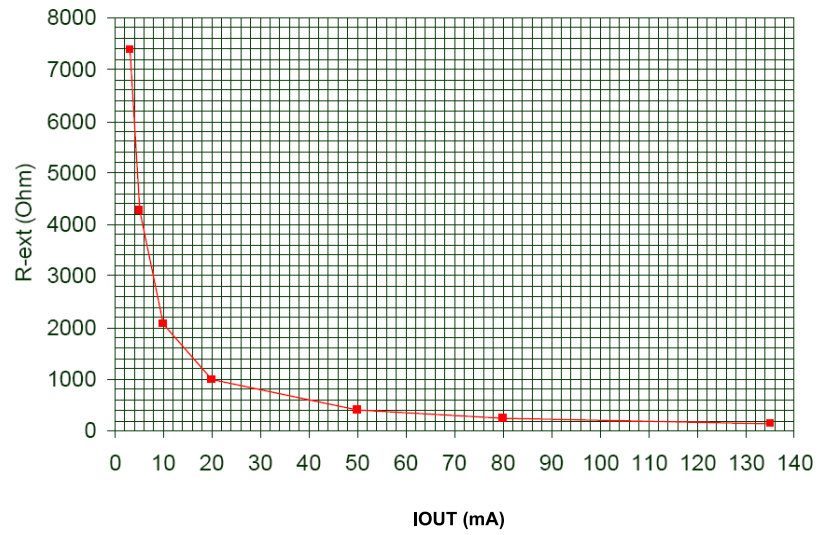


CS17070

GIPD300920151146MT

## 6 Typical characteristics

Figure 11. Output current- $R_{EXT}$  resistor

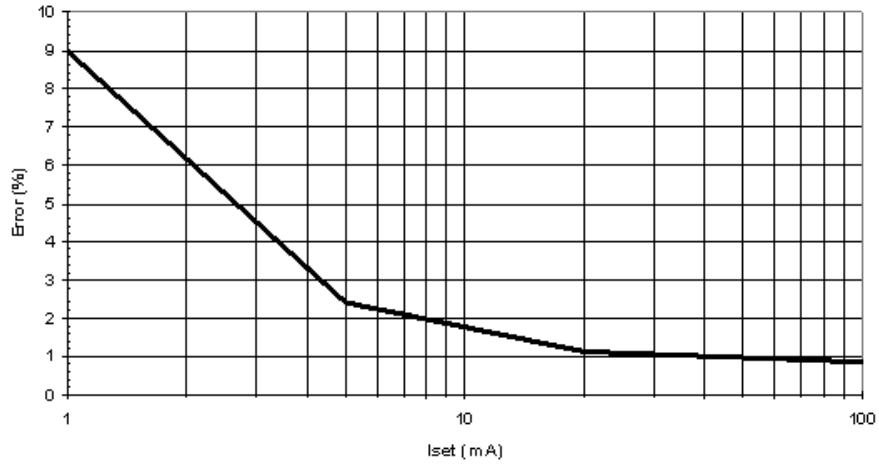


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Table 9. Output current- $R_{EXT}$  resistor

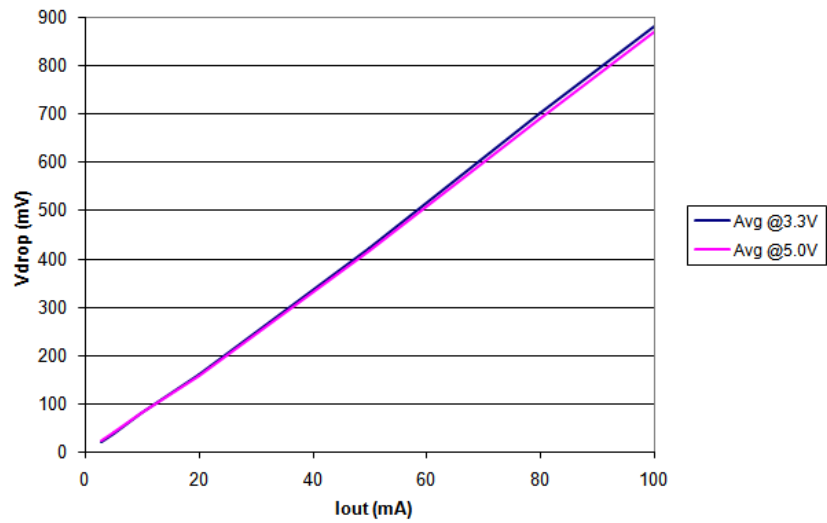
R-EXT ( $\Omega$ )	Output current (mA)
7370	3
4270	5
2056	10
1006	20
382	50
251	80
200	100

**Figure 12. Output current vs  $\pm \Delta I_{OL}(\%)$   $T_A = 25^\circ C$**



GIPD051020151346MT

**Figure 13.  $I_{SET}$  vs drop out voltage ( $V_{drop}$ )  $T_A = 25^\circ C$**

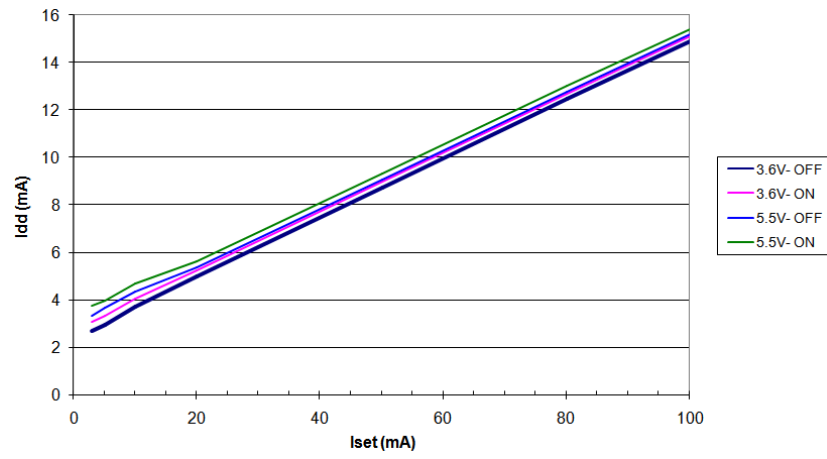


GIPD051020151348MT

**Table 10.  $I_{SET}$  vs. dropout voltage ( $V_{drop}$ )**

Iout (mA)	Avg (mV) @ 3.3 V	Avg (mV) @ 5.0 V
3	20	22
5	37	40
10	79	79
20	160	158
50	422	415
80	700	690
100	880	870

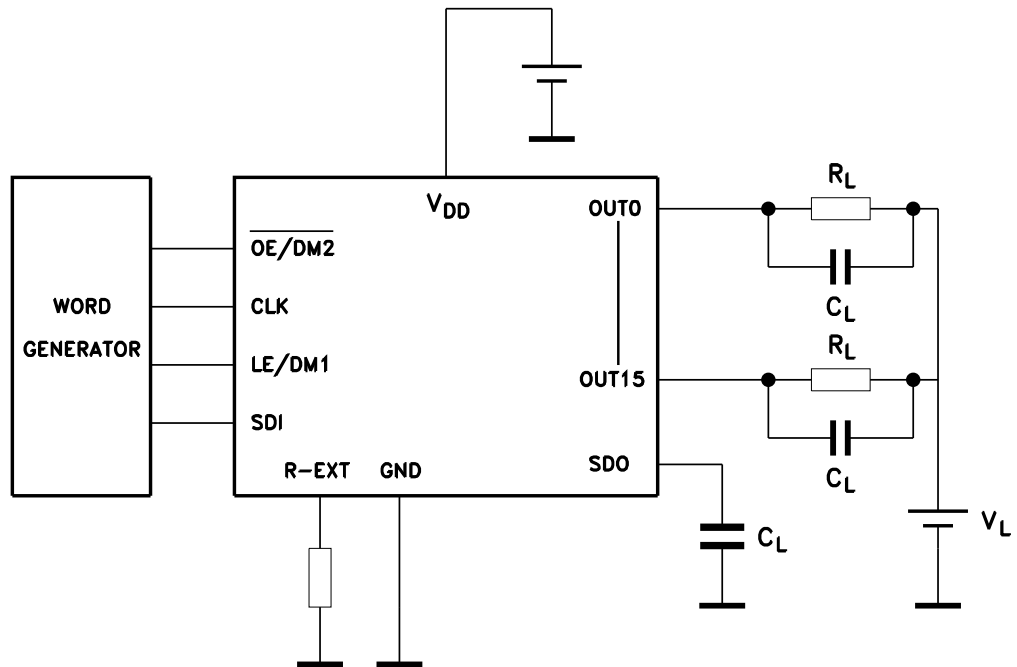
Figure 14.  $I_{DD}$  ON/OFF,  $T_A = 25\text{ }^\circ\text{C}$



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## 7 Test circuit

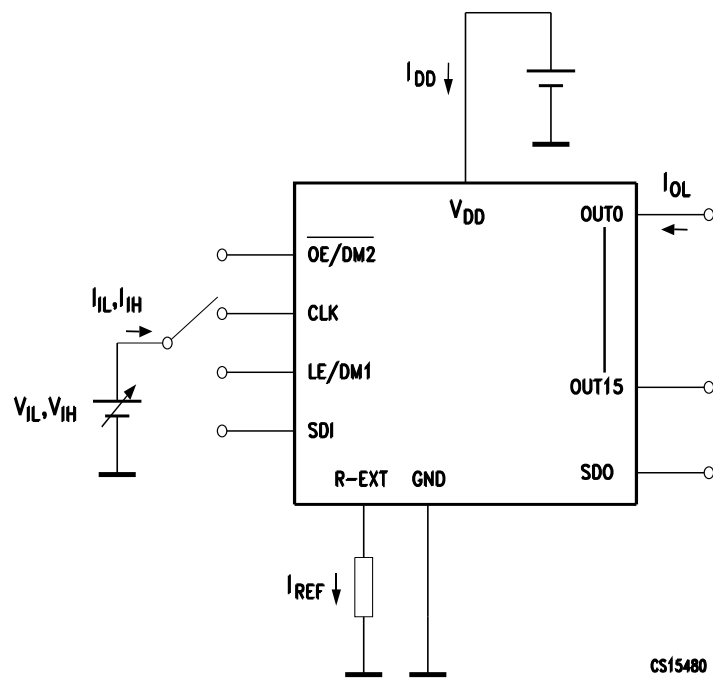
Figure 15. DC characteristic



CS15470

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Figure 16. AC characteristic

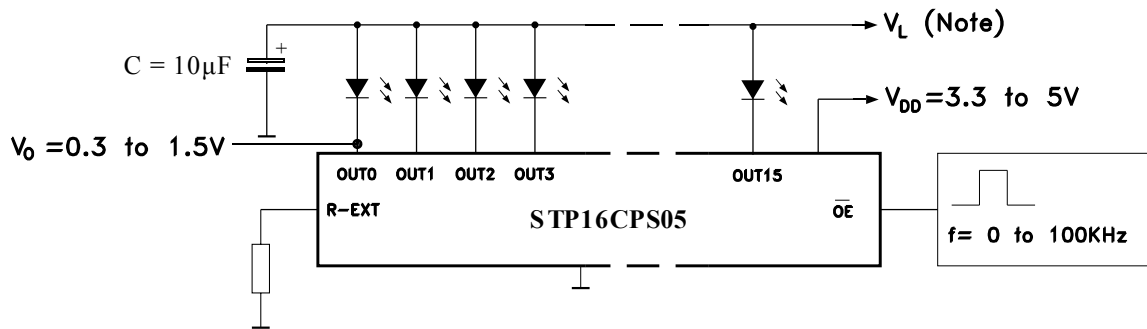


CS15480

GIPD051020151411MT



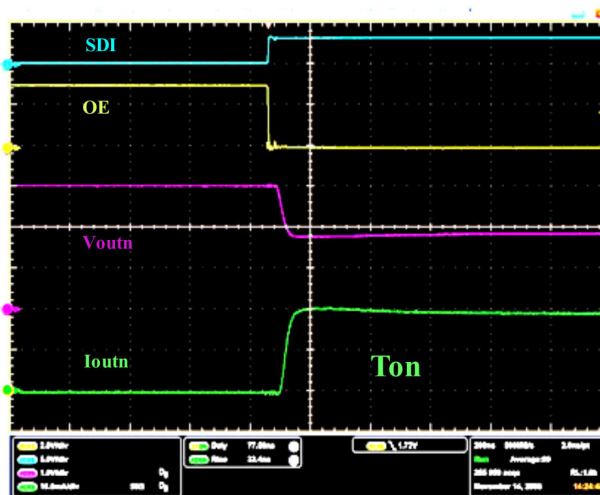
Figure 17. Typical application schematic



GIPD051020151415MT

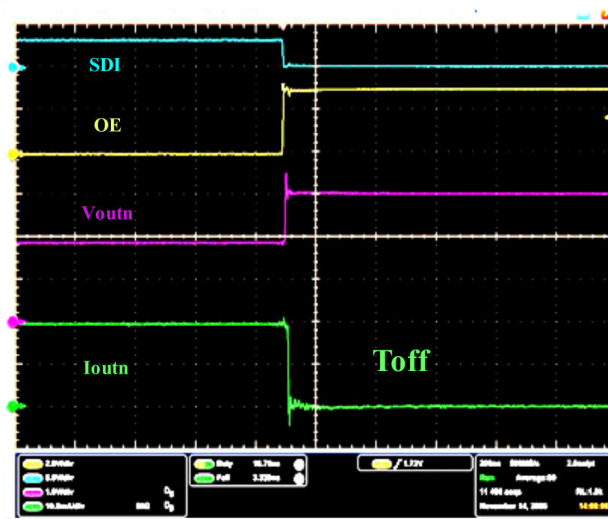
Note:  $V_L$  will be determined by the  $V_F$  of the LEDs. Test condition: temp. = 25 °C,  $V_{DD}$  = 3.0 V,  $V_{IN}$  =  $V_{DD}$ ,  $C_L$  = 10 pF, freq. = 1 MHz, Ch1 =  $\overline{OE}/DM2$ , Ch2 = SDI, Ch3 =  $V_{OUT}$ , Ch4 =  $I_{OUT}$

Figure 18. Turn ON output current setup



GIPD081020151217MT

Figure 19. Turn OFF output current setup



GIPD081020151225MT

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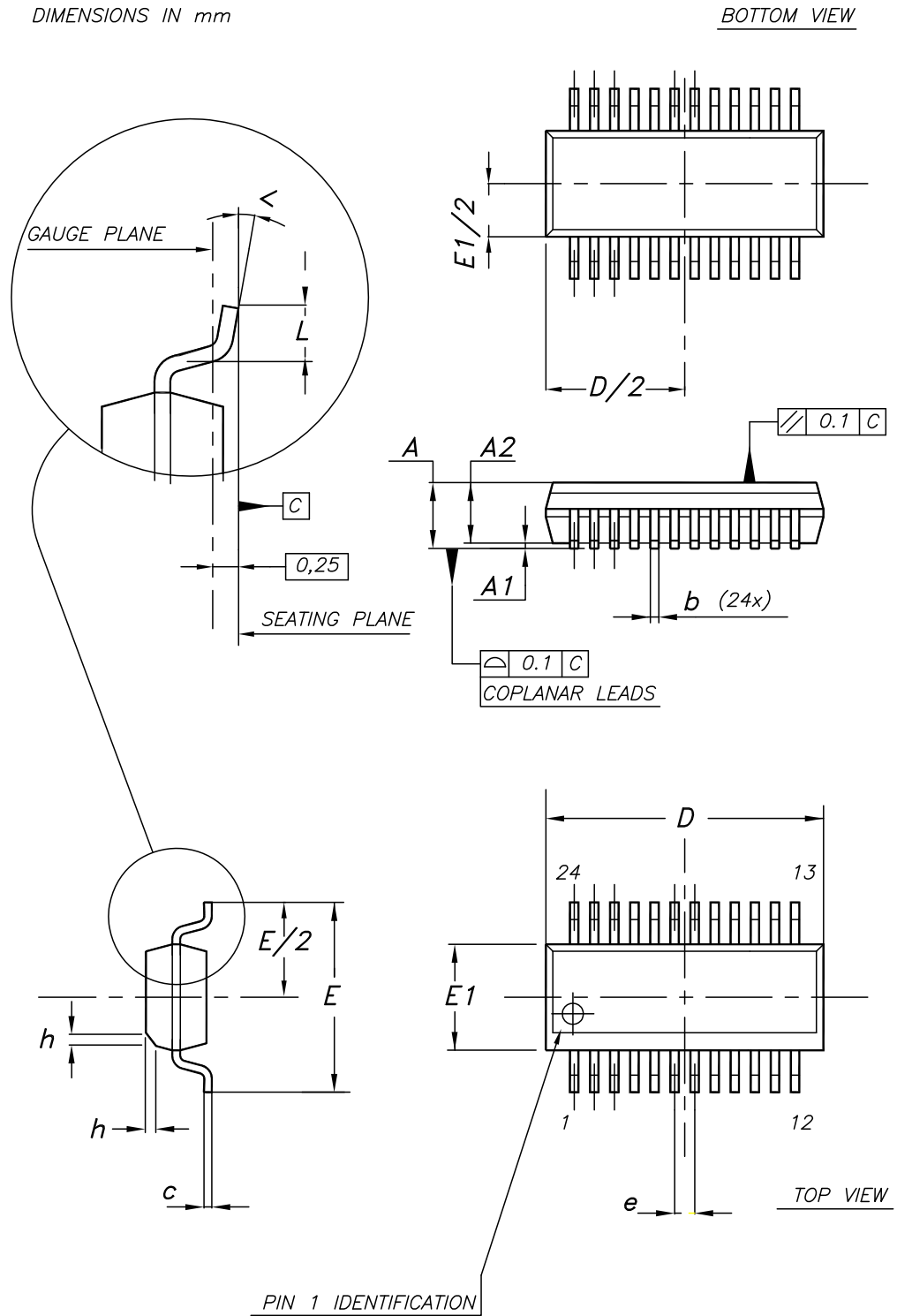
## 8 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 8.1 QSOP-24 package information

Figure 20. QSOP-24 package outline

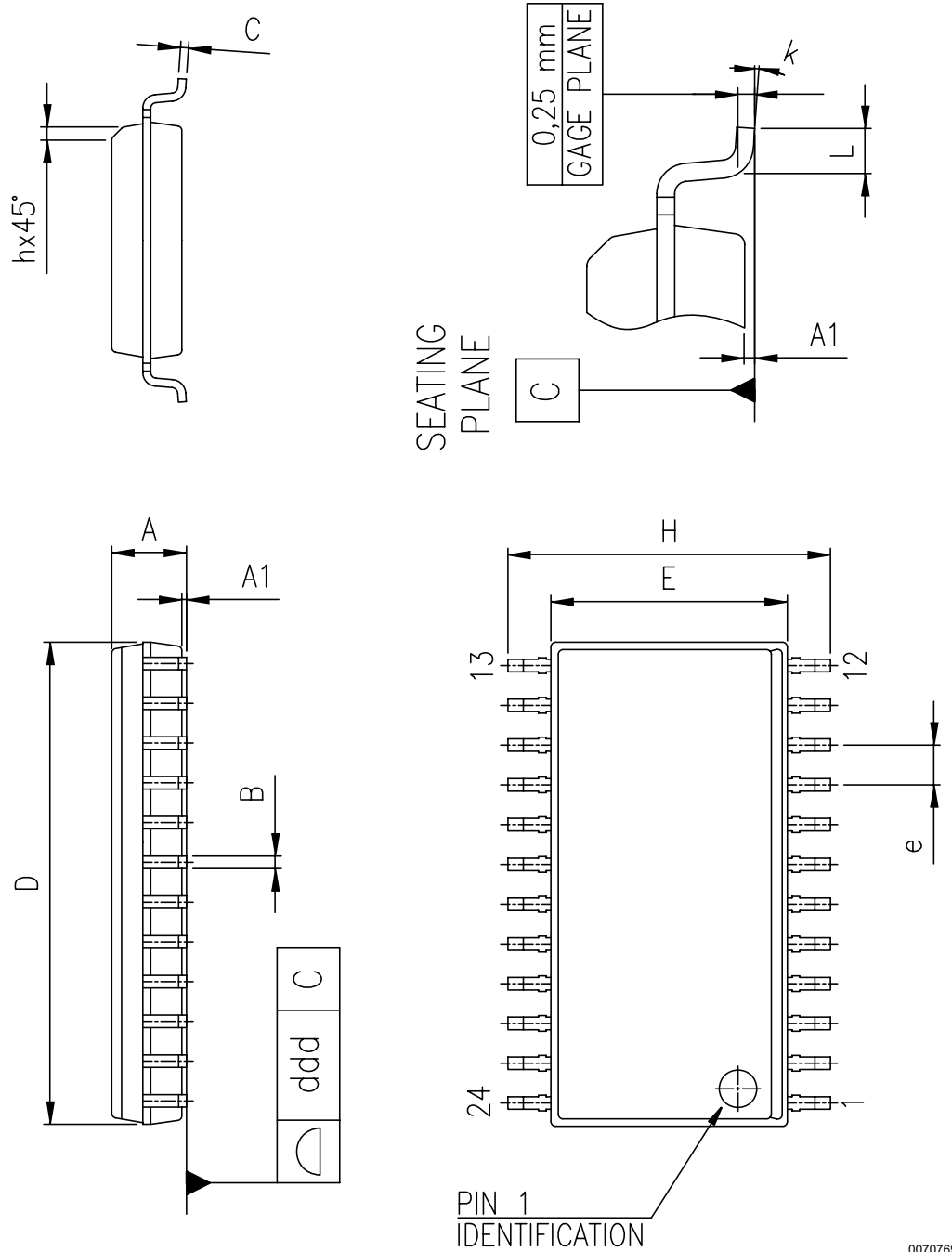


**Table 11. QSOP-24 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

8.2 SO-24 0070769 package information

Figure 21. SO-24 package outline

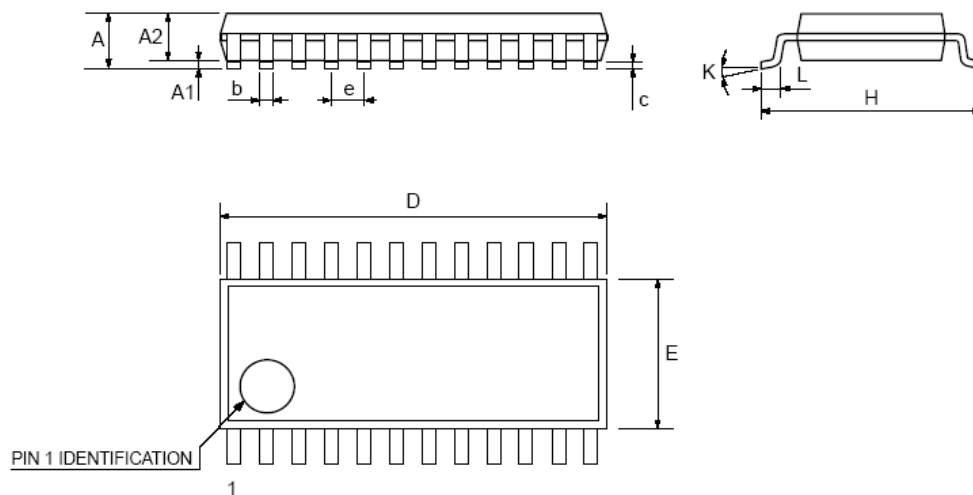


0070769

**Table 12. SO-24 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

### 8.3 TSSOP24 package information

**Figure 22. TSSOP24 package outline**


7047476B

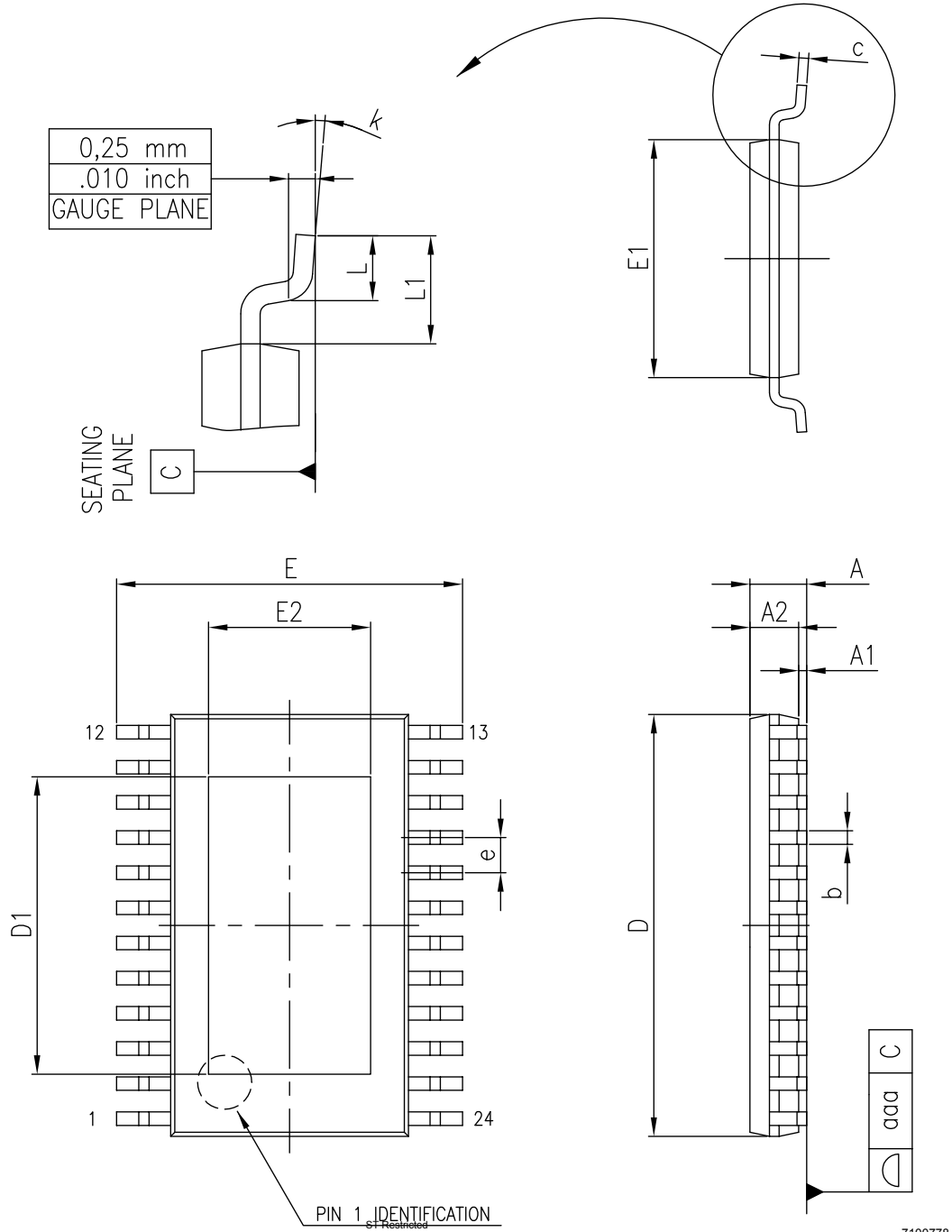
**Table 13. TSSOP24 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70



### 8.4 TSSOP24 exposed pad package information

Figure 23. TSSOP24 exposed pad package outline



**Table 14. TSSOP24 exposed pad mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e			
L	0.45	0.60	0.75
L1		1.00	
K	0		8
aaa			0.10

## 8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 24. TSSOP24, TSSOP24 exposed pad and SO-24 reel outline

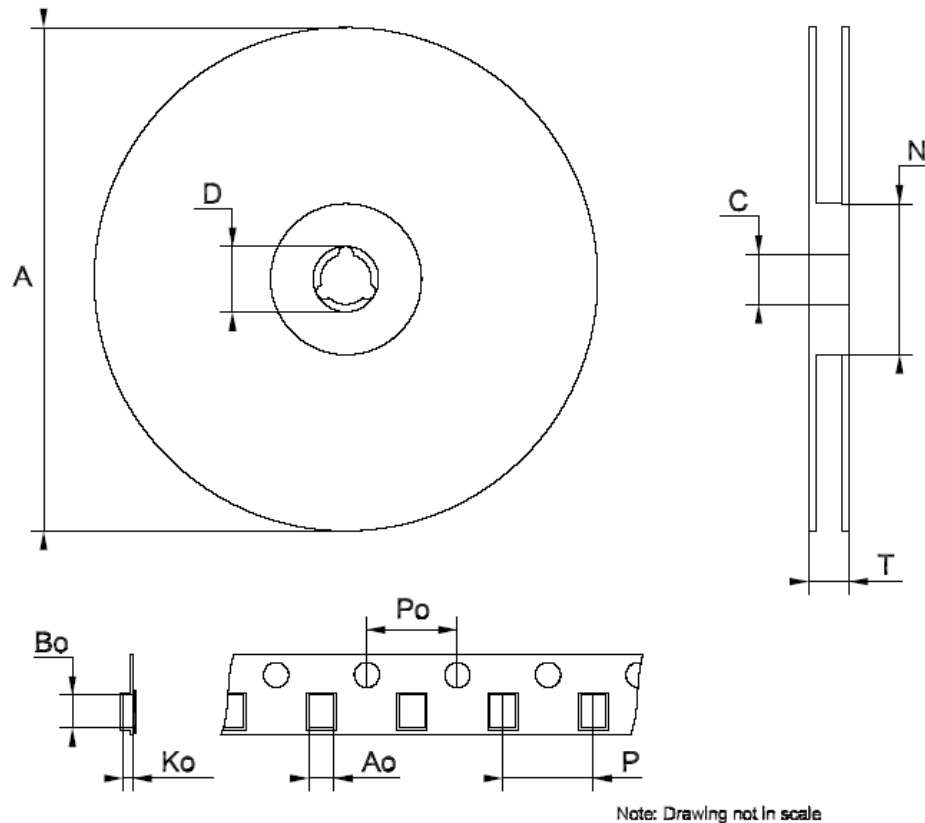


Table 15. TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	330	-	331
C	13.0	-	14.0
D	18.7	-	
N	100	-	
T	16.5	-	18.5
Ao	6.85	-	7.05
Bo	8.20	-	8.40
Ko	1.5	-	1.7
Po	3.9	-	4.1
P	7.9	-	8.1

**Table 16. SO-24 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

## 9 Device summary

Table 17. Device summary

Order code	Package	Packing
STP16CP05MTR	SO-24	1000 parts per reel
STP16CP05TTR	TSSOP24	2500 parts per reel
STP16CP05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CP05PTR	QSOP-24	2500 parts per reel

## Revision history

**Table 18. Document revision history**

Date	Revision	Changes
28-Jul-2006	1	First release
21-Dec-2006	2	Final datasheet
17-May-2007	3	Updated Table 7 on page 6
10-Jul-2007	4	Updated Table 9: Truth table on page 10
12-Mar-2008	5	Updated Table 15: TSSOP24 exposed-pad on page 23, added QSOP-24 Table 12 and Figure 2 on page 19
07-May-2008	6	Updated Section 5 on page 10
03-Dec-2008	7	Updated cover page, Table 6 on page 5, Table 7 on page 6, Table 8 on page 7, Figure 2 on page 13, Table 10 on page 13, Figure 2, 2, and Figure 2 on page 15
12-May-2009	8	Updated cover page, Table 6 on page 5, Table 7 on page 6, Table 8 on page 7
22-Oct-2009	9	Updated Note: on page 3
20-Jan-2010	10	Updated Table 5 on page 4
18-Jun-2014	11	Updated Section 8: Package mechanical data and Section 9: Packaging mechanical data.
01-Apr-2016	12	Updated <i>Table 12: "QSOP-24 mechanical data"</i> . Minor text changes.
08-Mar-2017	13	Updated SDO terminal, Clock, serial/in, serial/out and Clock, serial/in, latch, enable, outputs. Minor text changes.
21-Feb-2024	14	Updated <a href="#">Table 15. TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data.</a>

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