

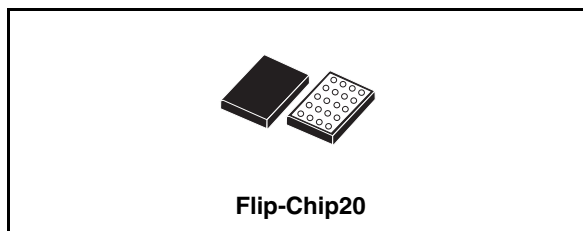


# STSLVDSP27

## 8-bit low voltage serializer with 1.8V high speed dual differential line drivers and embedded DPLL

### Features

- Sub-low voltage differential signaling:  
 $V_{OD} = 150\text{mV}$  with  $R_T = 100\Omega$ ,  $C_L = 10\text{pF}$
- Clock range: 4 to 27 MHz in parallel mode,  $\text{BYP} = \text{Gnd}$
- Operative frequency serial mode,  $\text{BYP} = V_{DD}$ ;  
DIN0 to DOUT, CLKIN to CLKOUT,  
 $f_{OPR} = 1$  to 208 MHz max
- Embedded DPLL requires no external components
- Output voltage rise and fall times  
 $t_{rVOD} = t_{fVOD} = 610\text{ps}$  typ at  $f_{OPR} = 208\text{MHz}$
- High speed propagation delay times  
 $t_{pLH} \sim t_{pHL} = 2.1\text{ns}$  typ at  $V_{DD} = 3.0\text{V}$ ;  $V_{IO} = 1.8\text{V}$
- Operating voltage range:  
 $V_{DD} (\text{OPR}) = 2.5\text{V}$  to  $3.6\text{V}$   
 $V_{IO} (\text{OPR}) = 1.65\text{V}$  to  $1.95\text{V}$
- High impedance on driver outputs  
 $I_{OZ} = 1\mu\text{A}$  max;  $\text{EN} = \text{Gnd}$ ;  $V_O = \text{Gnd}$  or  $V_{IO}$
- Low voltage CMOS input threshold  
(DIN0-DIN7, CLKIN, EN, BYP, DV0, DV1)  
 $V_{IL} = 0.3 \times V_{DD}$  max;  $V_{IH} = 0.7 \times V_{DD}$  min
- 3.6V tolerant on all inputs  
(DIN0-DIN7, CLKIN, EN, BYP, DV0, DV1)
- Lead-free Flip-Chip package
- SMIA CCP1 (MIPI CSI-1) compatible PHY



serializer IC is provided with two power supply rails,  $V_{DD}$  and  $V_{IO}$ . The first supply is related to the logic levels of the input data (DIN0-DIN7, CLKIN) and Enables (EN, BYP, DV0, DV1) pins.  $V_{IO}$  provides the power supply to the output current drivers in the device.  $V_{IO}$  is always expected to be a nominal 1.8V.  $V_{DD}$  depends on the application, but will always be equal to or higher than  $V_{IO}$ . In order to minimize static current consumption, it is possible to shut down the transmitters when the interface is not used by setting a power-down (EN) pin. This operation reduces the maximum current consumption to 20 $\mu\text{A}$ , making this device ideal for portable applications like mobile phones and portable battery equipment. Simplified functionality can be reached using the BYP select pin, which disables the internal DPLL circuitry. When this pin is High the device can work with serialized signals from DIN0 input only. A synchronous CLKIN signal must be provided and it will be put-out using sub-LVDS level by CLKOUT port; the sub-LVDS data will be put-out by DOUT port at a maximum frequency of 208Mhz. This innovative device provides an optimized high-speed link solution from different CMOS sensor devices (parallel or serial outputs) to more advanced graphic controllers in mobile phone applications. All inputs and outputs are equipped with protection circuits against static discharge, providing ESD immunity from transient excess voltage. The STSLVDSP27 is designed for operation over the commercial temperature range -40°C to 85°C.

### Description

The STSLVDSP27 is an 8:1 bit serializer with embedded DPLL. The dual differential line drivers implement the electrical characteristics of sub-low voltage differential signaling (subLVDS), bringing out the serialized data and related synchronous clock signal. The STSLVDSP27

### Order code

| Part number   | Temperature range | Package                   | Packaging           |
|---------------|-------------------|---------------------------|---------------------|
| STSLVDSP27BJR | -40 to 85 °C      | Flip-Chip20 (Tape & Reel) | 3000 parts per reel |

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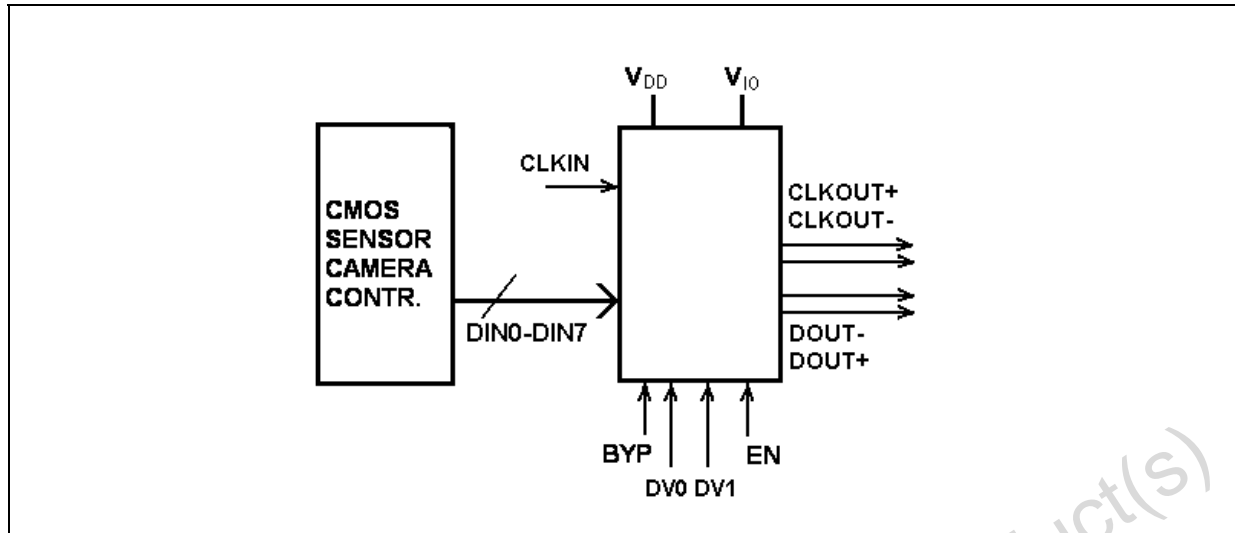
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Obsolete Product(s) - Obsolete Product(s)

# 1 Block diagram

Figure 1. Simplified block diagram typical application



## 2 Pin configuration

Figure 2. Pin configuration and logic diagram (Top view - Bumps are on the other side)

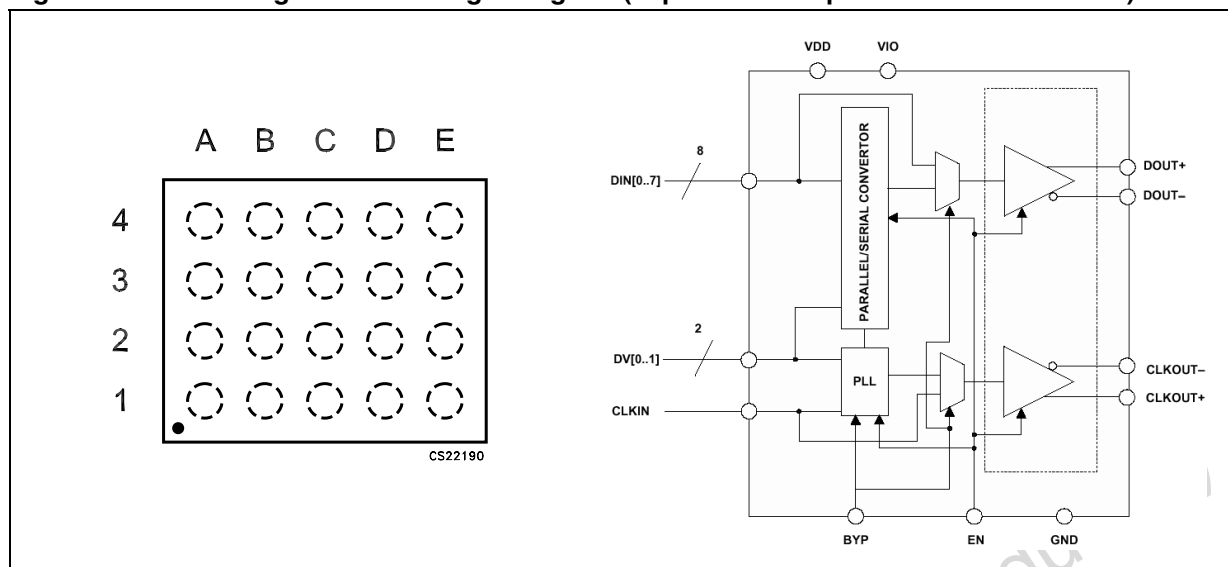


Table 1. Pin description

| PIN N°                     | Symbol           | Name and function                 |
|----------------------------|------------------|-----------------------------------|
| B1                         | DIN0             | CMOS parallel/serial data inputs  |
| A1, A2, A3, A4, B4, C4, D4 | DIN1-DIN7        | CMOS parallel data inputs         |
| D1, C1                     | DOUT+, DOUT-     | SubLVDS driver data outputs       |
| B3                         | CLKIN            | CMOS parallel/serial clock input  |
| D3, C3                     | CLKOUT+, CLKOUT- | SubLVDS driver clock outputs      |
| C2, D2                     | DV0, DV1         | CMOS data valid inputs            |
| B2                         | GND              | Ground                            |
| E1                         | V <sub>DD</sub>  | Main power supply voltage         |
| E2                         | V <sub>IO</sub>  | SubLVDS bus output supply voltage |
| E3                         | EN               | CMOS main chip enable input       |
| E4                         | BYP              | CMOS by-pass select input         |

**Table 2. Truth table (bypass functionality: DIN0 => DOUT, CLKIN => CLKOUT; main chip Enable<sup>(1)</sup> functionality)**

| Controls |     | Input |     |      |        |       | Differential outputs |       |         |         |
|----------|-----|-------|-----|------|--------|-------|----------------------|-------|---------|---------|
| EN       | BYP | DV0   | DV1 | DIN0 | DIN1-7 | CLKIN | DOUT+                | DOUT- | CLKOUT+ | CLKOUT- |
| L        | X   | X     | X   | X    | X      | X     | Z                    | Z     | Z       | Z       |
| H        | H   | X     | X   | L    | X      | L     | L                    | H     | L       | H       |
| H        | H   | X     | X   | L    | X      | H     | L                    | H     | H       | L       |
| H        | H   | X     | X   | H    | X      | L     | H                    | L     | L       | H       |
| H        | H   | X     | X   | H    | X      | H     | H                    | L     | H       | L       |

1. All differential outputs are put in high impedance vs gnd only; the internal DPLL circuit is put in shutdown mode to obtain minimum power consumption.

Note:  $n:0..1$ ; Z = High Impedance, X = Don't care

**Table 3. Truth table (data valid functionality)**

| Controls |     | Input              |                    |      |        |       | Differential outputs |       |         |         |
|----------|-----|--------------------|--------------------|------|--------|-------|----------------------|-------|---------|---------|
| EN       | BYP | DV0 <sup>(1)</sup> | DV1 <sup>(1)</sup> | DIN0 | DIN1-7 | CLKIN | DOUT+                | DOUT- | CLKOUT+ | CLKOUT- |
| H        | L   | L                  | X                  | X    | X      | X     | H                    | L     | H       | L       |
| H        | L   | X                  | L                  | X    | X      | X     | H                    | L     | H       | L       |

1. An AND gate is designed on Data Valid Inputs (DV0, DV1) to enable the standard functionality; only when the DV0=DV1="H" the device will work according to description in main page

Note:  $n:0..1$ ; Z = High Impedance, X = Don't care

### 3 Maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol    | Parameter   | Value                      | Unit               |
|-----------|---|----------------------------|--------------------|
| $V_{DD}$  | Supply voltage  | -0.5 to 4.6                | V                  |
| $V_{IO}$  | SubLVDS bus supply voltage  | -0.5 to 4.6                | V                  |
| $V_I$     | DC input voltage (DIN0-DIN7, BYP, CLKIN, EN, DV0, DV1)  | -0.5 to 4.6                | V                  |
| $V_O$     | DC output voltage (DOUT+,DOUT-,CLKOUT+,CLKOUT-)   | -0.5 to ( $V_{IO} + 0.5$ ) | V                  |
| ESD       | Electrostatic discharge protection<br>IEC61000-4-2 Contact R = 330 $\Omega$ , C = 150pF (All Pins vs GND) | $\pm 2$                    | KV                 |
| $T_{STG}$ | Storage temperature range   | -65 to +150                | $^{\circ}\text{C}$ |

*Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.*

**Table 5. Recommended operating conditions**

| Symbol          | Parameter  | Min. | Typ. | Max. | Unit               |
|-----------------|--|------|------|------|--------------------|
| $V_{DD}$        | Main supply voltage <sup>(1)</sup> <sup>(2)</sup>                                | 2.5  | 3.0  | 3.6  | V                  |
| $V_{IO}$        | SubLVDS bus supply voltage   | 1.65 | 1.80 | 1.95 | V                  |
| $V_{DD\_NOISE}$ | Peak-to-peak permitted main supply voltage noise <sup>(2)</sup>                  |      |      | 100  | mV                 |
| $R_T$           | Termination resistance (per pair differential output line)                       | 80   | 100  | 120  | $\Omega$           |
| $C_L$           | Termination capacitance (per line vs GND Pin)                                    |      | 10   |      | pF                 |
| $T_A$           | Operating ambient temperature range  | -40  |      | 85   | $^{\circ}\text{C}$ |
| $T_J$           | Operating junction temperature range   | -40  |      | 125  | $^{\circ}\text{C}$ |
| $t_R, t_F$      | Rise and fall time (DIN0-DIN7, BYP, CLKIN, EN, DV0, DV1; 10% to 90%; 90% to 10%) |      |      | 10   | ns                 |

1.  $V_{DD}$  Main supply voltage in serial mode (BYP =  $V_{DD}$ ) can be reduced down to 1.65V for typical 1.8V input signals

2.  $V_{DD}$  Main supply voltage in parallel mode (BYP = GND) can reach 2.5V when  $V_{DD\_NOISE} = 100\text{mV}$  and  $V_{DD} = 2.55\text{V}$

## 4 Electrical characteristics

**Table 6. Electrical characteristics** (over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.0\text{V}$ ,  $V_{IO} = 1.8\text{V}$ )

| Symbol          | Parameter   | Test conditions  | Min.             | Typ.       | Max.             | Unit     |
|-----------------|---|--|------------------|------------|------------------|----------|
| $V_{CM}$        | Common mode output voltage ( <i>Figure 3.</i> )   | $R_T = 100\Omega \pm 1\%$  | $V_{IO}/2 - 0.1$ | $V_{IO}/2$ | $V_{IO}/2 + 0.1$ | V        |
| $V_{CM(SS)}$    | Common mode output voltage change between logic state ("L" and "H") ( <i>Figure 5.</i> )              | $R_T = 100\Omega \pm 1\%$  | -20              |            | 20               | mV       |
| $V_{CM(PP)}$    | Common mode peak-to-peak output voltage change between logic state ("L" and "H") ( <i>Figure 5.</i> ) | $R_T = 100\Omega \pm 1\%$  | -40              |            | 40               | mV       |
| $ V_{OD} $      | Differential output voltage ( <i>Figure 3.</i> )  | $R_T = 100\Omega \pm 1\%$  | 100              | 150        | 200              | mV       |
| $\Delta V_{OD}$ | Differential output voltage change between logic state ("L" and "H")                                  | $R_T = 100\Omega \pm 1\%$  | -20              |            | 20               | mV       |
| $DC_{VOD}$      | Clock duty cycle@208MHz differential output voltage CLKOUT+, CLKOUT-, DOUT+, DOUT-                    | $R_T = 100\Omega \pm 1\%$ $BYP = V_{DD}$ ; $EN = V_{DD}$<br>$f_{CLKIN} = 208\text{MHz}$ , $f_{DIN0} = 208\text{MHz}$ | 45               | 50         | 55               | %        |
| $I_{IO}$        | Driver output current CLKOUT+, CLKOUT-, DOUT+, DOUT-  | $R_T = 100\Omega \pm 1\%$  | 1                | 1.5        | 2                | mA       |
| $R_O$           | Driver output impedance (Single ended) CLKOUT+, CLKOUT-, DOUT+, DOUT- ( <i>Figure 8.</i> )            | $V_{CM} = V_{IO}/2 + 100\text{mV}$ and $V_{IO}/2 - 100\text{mV}$   | 40               | 100        | 140              | $\Omega$ |
| $D_{RO}$        | Driver output impedance mismatch between $R_{ODOUT+}$ , $R_{OCLKOUT}$                                 |  |                  |            | 10               | %        |

**Table 6. Electrical characteristics** (over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.0\text{V}$ ,  $V_{IO} = 1.8\text{V}$ )

| Symbol     | Parameter  | Test conditions  | Min.                | Typ. | Max.                | Unit          |
|------------|--|--|---------------------|------|---------------------|---------------|
| $I_S$      | Supply current ( $I_{IO} + I_{DD}$ )                                 | EN= $V_{DD}$ , BYP= $V_{DD}$ or GND,<br>DIN0-DIN7= $V_{DD}$ or GND<br>No load ( $R_T = \infty$ )   |                     |      | 15                  | mA            |
|            |  | EN= $V_{DD}$ , BYP= $V_{DD}$ or GND,<br>DIN0-DIN7= $V_{DD}$ or GND<br>$R_T = 100\Omega \pm 1\%$  |                     |      | 15                  |               |
|            |  | EN= $V_{DD}$ , BYP= $V_{DD}$ (DPLL="OFF")<br>$R_T = 100\Omega \pm 1\%$ , $C_L = 10\text{pF}$ per line,<br>DV0=DV1= $V_{DD}$ ,<br>$f_{DIN0}$ and CLKIN = 208 MHz<br>( $V_{IL}$ and $V_{IH}$ levels)                                 |                     |      | 12                  |               |
|            |  | EN= $V_{DD}$ , BYP=Gnd(DPLL="ON") $R_T$<br>= $100\Omega \pm 1\%$ , $C_L = 10\text{pF}$ per line,<br>DV0 = DV1 = $V_{DD}$ , $f_{CLKOUT} = 160\text{MHz}$<br>$f_{DIN0-DIN7,CLKIN} = 22\text{MHz}$<br>( $V_{IL}$ and $V_{IH}$ levels) |                     |      | 20                  |               |
| $I_{SOFF}$ | Shutdown supply current<br>( $I_{IO} + I_{DD}$ )                     | EN = GND, $V_{DD} = 2.7\text{V}$ to $3.6\text{V}$<br>$V_{IO} = 1.65\text{V}$ to $1.95\text{V}$<br>DIN0-DIN7, CLKIN, BYP = GND or<br>$V_{DD}$   |                     |      | 20                  | $\mu\text{A}$ |
| $V_{IH}$   | High level input voltage<br>(DIN0-DIN7, BYP, CLKIN,<br>EN, DV0, DV1) | $V_{DD} = 2.7\text{V}$ to $3.6\text{V}$ ,<br>$V_{IO} = 1.65\text{V}$ to $1.95\text{V}$   | $0.7 \times V_{DD}$ |      | 3.6                 | V             |
| $V_{IL}$   | Low level input voltage<br>(DIN0-DIN7, BYP, CLKIN,<br>EN, DV0, DV1)  | $V_{DD} = 2.7\text{V}$ to $3.6\text{V}$ ,<br>$V_{IO} = 1.65\text{V}$ to $1.95\text{V}$   | 0                   |      | $0.3 \times V_{DD}$ | V             |
| $I_{IH}$   | High level input current<br>(DIN0-DIN7, BYP, CLKIN,<br>EN, DV0, DV1) | $V_{IH} = 0.7 \times V_{DD}$   |                     |      | $\pm 1$             | $\mu\text{A}$ |
| $I_{IL}$   | Low level input current<br>(DIN0-DIN7, BYP, CLKIN,<br>EN, DV0, DV1)  | $V_{IL} = 0.3 \times V_{DD}$   |                     |      | $\pm 1$             | $\mu\text{A}$ |
| $I_{OZ}$   | High impedance output<br>current CLKOUT+, CLKOUT-,<br>DOUT+, DOUT-   | $V_O = 0$ or $V_{CC}$  |                     |      | $\pm 1$             | $\mu\text{A}$ |

**Table 7. Serial switching characteristics** (DPLL = "OFF",  $R_T = 100\Omega \pm 1\%$ ,  $C_L = 10\text{pF}$ , over recommended operating conditions unless otherwise noted. Typical values are referred to  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.0\text{V}$ ,  $V_{IO} = 1.8\text{V}$ )

| Symbol      | Parameter   | Test Conditions   | Min. | Typ. | Max. | Unit          |
|-------------|---|---|------|------|------|---------------|
| $t_{rVOD}$  | Rise time differential output voltage (20% to 80%) (Figure 4.)                                  | $t_{rDIN} = 4.9\text{ns}$ (10% to 90%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$   | 400  | 610  | 1000 | ps            |
| $t_{fVOD}$  | Fall time differential output voltage (80% to 20%) (Figure 4.)                                  | $t_{fDIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$   | 400  | 610  | 1000 | ps            |
| $t_{PLHD}$  | Differential propagation delay time (DIN to DOUT) (Low to High) (Note: 1) (Figure 4.)           | $t_{rDIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$  | 1.0  | 2.1  | 2.8  | ns            |
| $t_{PHLD}$  | Differential propagation delay time (DIN to DOUT) (Low to High) (Note: 1) (Figure 4.)           | $t_{rDIN} = 4.2\text{ns}$ (10% to 90%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$   | 1.0  | 2.1  | 2.8  | ns            |
| $t_{EN}$    | Enable delay time (EN to DOUT: $t_{PLZ}$ , $t_{PHZ}$ ) (Figure 7.)                              | $t_{rEN} = 2.0\text{ns}$ (10% to 90%);<br>$t_{fEN} = 2.0\text{ns}$ (90% to 10%)   |      |      | 20   | $\mu\text{s}$ |
| $t_{DIS}$   | Disable delay time (EN to DOUT: $t_{PLZ}$ , $t_{PHZ}$ ) (Figure 7.)                             | $t_{rEN} = 2.0\text{ns}$ (10% to 90%);<br>$t_{fEN} = 2.0\text{ns}$ (90% to 10%)   |      |      | 1000 | ns            |
| $f_{OPR}$   | Operating frequency serial mode without DPLL  | $\text{BYP} = V_{DD}$<br>$t_{rDIN0,CLKIN} = 1\text{ns}$ (10% to 90%);<br>$t_{fDIN0,CLKIN} = 1\text{ns}$ (90% to 10%)<br>$f_{DIN0,CLKIN} = 208\text{MHz}$<br>$\text{PulseWidth}_{DIN0,CLKIN} = 2.4\text{ns}$ | 1    |      | 208  | MHz           |
| $t_{SKEW1}$ | Differential skew between signals on each differential pair ( $t_{PLHD} - t_{PHLD}$ )           | $t_{rDIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$  |      |      | 150  | ps            |
| $t_{SKEW2}$ | Channel to channel skew between any two signals on each different differential pair (Figure 6.) | $t_{rDIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$  |      |      | 200  | ps            |

Note: 1 50%  $V_{DIN}$  to 50%  $V_{DOUT}$

**Table 8. Parallel switching characteristics** (DPLL = "ON",  $R_T = 100\Omega \pm 1\%$ ,  $C_L = 10\text{pF}$ , over recommended operating conditions unless otherwise noted. Typical values are referred to  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.0\text{V}$ ,  $V_{IO} = 1.8\text{V}$ )

| Symbol        | Parameter  | Test Conditions  | Min. | Typ. | Max. | Unit          |
|---------------|--|--|------|------|------|---------------|
| $t_{rVOD}$    | Rise time differential output voltage (20% to 80%) (Figure 4.)                                       | $t_{rDIN} = 4.9\text{ns}$ (10% to 90%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$  | 400  | 610  | 1000 | ps            |
| $t_{fVOD}$    | Fall time differential output voltage (80% to 20%) (Figure 4.)                                       | $t_{fDIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN} = 10\text{MHz}$ , $\text{PulseWidth}_{DIN} = 50\text{ns}$  | 400  | 610  | 1000 | ps            |
| $t_{PLHDIN0}$ | Differential propagation delay time DIN0 (CLKIN to DOUT) (Low to High) (Note 2) (Figure 10.)         | $t_{rDIN0-DIN7,CLKIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 22\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$        |      | 8    |      | ns            |
| $t_{PHLDIN0}$ | Differential propagation delay time DIN0 (CLKIN to DOUT) (High to Low) (Note 2) (Figure 10.)         | $t_{rDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 22\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$        |      | 8    |      | ns            |
| $t_{PLHDIN7}$ | Differential propagation delay time DIN7 (CLKIN to DOUT) (Low to High) (Note 2) (Figure 10.)         | $t_{rDIN0-DIN7,CLKIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 22\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$        |      | 53   |      | ns            |
| $t_{PHLDIN7}$ | Differential propagation delay time DIN7 (CLKIN to DOUT) (High to Low) (Note 2) (Figure 10.)         | $t_{rDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 10\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$        |      | 53   |      | ns            |
| $t_{OCD}$     | Differential propagation delay time (CLKIN to DOUT first positive edge) (Low to High) (Figure 10.)   | $t_{rDIN0-DIN7,CLKIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 10\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$        |      | 11   |      | ns            |
| $t_{SU\_CLK}$ | Set-up time (DIN0-DIN7, DV to CLKIN) (LH or HL to positive CLKIN edge) (Figure 11.)                  | $t_{rDIN0-DIN7,CLKIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 4$ to $22\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$ | 12   |      |      | ns            |
| $t_{H\_CLK}$  | Hold time (CLKIN to DIN0-DIN7, DV) (positive CLKIN edge to LH or HL DIN, DV transition) (Figure 11.) | $t_{rDIN0-DIN7,CLKIN} = 4.9\text{ns}$ (10% to 90%);<br>$t_{fDIN0-DIN7,CLKIN} = 4.2\text{ns}$ (90% to 10%);<br>$f_{DIN0-DIN7,CLKIN} = 4$ to $22\text{MHz}$ ,<br>$\text{PulseWidth}_{DIN} = 50\text{ns}$ | 10   |      |      | ns            |
| $t_{EN}$      | Enable delay time (EN to DOUT: $t_{PLZ}$ , $t_{PHZ}$ ) (Figure 7.)                                   | $t_{rEN} = 2.0\text{ns}$ (10% to 90%);<br>$t_{fEN} = 2.0\text{ns}$ (90% to 10%)  |      |      | 20   | $\mu\text{s}$ |
| $t_{DIS}$     | Disable delay time (EN to DOUT: $t_{PLZ}$ , $t_{PHZ}$ ) (Figure 7.)                                  | $t_{rEN} = 2.0\text{ns}$ (10% to 90%);<br>$t_{fEN} = 2.0\text{ns}$ (90% to 10%)  |      |      | 1000 | ns            |
| $f_{OPR}$     | Operating frequency parallel mode with DPLL  | BYP = GND, $f_{DIN0-DIN7,CLKIN} = 4$ to $27\text{MHz}$ $\text{PulseWidth}_{DIN0,CLKIN} = 50\%$<br>$t_{rDIN0,CLKIN} = 3\text{ns}$ (10% to 90%);<br>$t_{fDIN0,CLKIN} = 3\text{ns}$ (90% to 10%)          | 4    |      | 27   | MHz           |

**Table 8. Parallel switching characteristics** (DPLL = "ON",  $R_T = 100\Omega \pm 1\%$ ,  $C_L = 10\text{pF}$ , over recommended operating conditions unless otherwise noted. Typical values are referred to  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 3.0\text{V}$ ,  $V_{IO} = 1.8\text{V}$ )

| Symbol              | Parameter   | Test Conditions  | Min. | Typ. | Max. | Unit          |
|---------------------|---|--|------|------|------|---------------|
| $f_{\text{CLKOUT}}$ | CLKOUT frequency parallel mode with DPLL  | BYP = GND, $f_{\text{DIN0-DIN7,CLKIN}}=4$ to 27MHz PulseWidth $_{\text{DIN0,CLKIN}} = 50\%$<br>$t_{\text{rDIN0,CLKIN}}=3\text{ns}$ (10% to 90%);<br>$t_{\text{fDIN0,CLKIN}}=3\text{ns}$ (90% to 10%) | 32   |      | 216  | MHz           |
| $t_{\text{SKEW1}}$  | Differential skew between signals on each differential pair ( $t_{\text{PLHD}} - t_{\text{PHLD}}$ ) | $t_{\text{rDIN}} = 4.9\text{ns}$ (10% to 90%);<br>$t_{\text{fDIN}} = 4.2\text{ns}$ (90% to 10%);<br>$f_{\text{DIN}} = 10\text{MHz}$ , PulseWidth $_{\text{DIN}} = 50\text{ns}$                       |      |      | 150  | ps            |
| $t_{\text{SKEW2}}$  | Channel to channel skew between any two signals on each different differential pair (Figure 6.)     | $t_{\text{rDIN}} = 4.9\text{ns}$ (10% to 90%);<br>$t_{\text{fDIN}} = 4.2\text{ns}$ (90% to 10%);<br>$f_{\text{DIN}} = 10\text{MHz}$ , PulseWidth $_{\text{DIN}} = 50\text{ns}$                       |      |      | 200  | ps            |
| $t_{\text{DV}}$     | Data valid before CLKOUT time (Figure 12.)  | BYP = GND, $f_{\text{DIN0-DIN7,CLKIN}}=4$ to 27MHz PulseWidth $_{\text{DIN0,CLKIN}} = 50\%$<br>$t_{\text{rDIN0,CLKIN}}=3\text{ns}$ (10% to 90%);<br>$t_{\text{fDIN0,CLKIN}}=3\text{ns}$ (90% to 10%) | 1    |      |      | ns            |
| $t_{\text{DH}}$     | Data valid hold after CLKOUT time (Figure 12.)  | BYP = GND, $f_{\text{DIN0-DIN7,CLKIN}}=4$ to 27MHz PulseWidth $_{\text{DIN0,CLKIN}} = 50\%$<br>$t_{\text{rDIN0,CLKIN}}=3\text{ns}$ (10% to 90%);<br>$t_{\text{fDIN0,CLKIN}}=3\text{ns}$ (90% to 10%) | 2    |      |      | ns            |
| $t_{\text{PLLS}}$   | DPLL settling time (EN to CLKOUT) 50% LH EN to 50% CLKOUT (first negative edge) (Figure 9.)         | $t_{\text{rEN}} = 2.0\text{ns}$ (10% to 90%)<br>$t_{\text{fEN}} = 2.0\text{ns}$ (90% to 10%)<br>DV0=DV1= $V_{DD}$ ; BYP= Gnd; DIN1-DIN7= $V_{DD}$ or Gnd;<br>$f_{\text{CLKIN}} = 4$ to 27MHz         |      | 70   |      | $\mu\text{s}$ |
| $J_{\text{CY-CY}}$  | RMS cycle-to-cycle jitter between CLKIN and CLKOUT signals  | $t_{\text{rCLKIN}} = 4.9\text{ns}$ (10% to 90%);<br>$t_{\text{fCLKIN}} = 4.2\text{ns}$ (90% to 10%);<br>$f_{\text{CLKIN}} = 4$ to 27MHz,<br>PulseWidth $_{\text{CLKIN}} = 50\%$                      |      | 100  |      | ps            |
|                     | Peak cycle-to-cycle jitter between CLKIN and CLKOUT signals   | $t_{\text{rCLKIN}} = 4.9\text{ns}$ (10% to 90%);<br>$t_{\text{fCLKIN}} = 4.2\text{ns}$ (90% to 10%);<br>$f_{\text{CLKIN}} = 4$ to 27MHz,<br>PulseWidth $_{\text{CLKIN}} = 50\%$                      |      | 600  |      |               |

Note: 1 50%  $V_{\text{DIN}}$  to 50%  $V_{\text{DOUT}}$

2 50% CLKIN (positive edge) to 50%  $V_{\text{DOUT}}$  (DIN0 will be referred to CLKOUT first positive edge; DIN7 will be referred to CLKOUT eighth positive edge)

3 Power down can be guaranteed when  $V_{\text{IO}}=1.8\text{V}$ , EN = GND, if low impedance < 1M $\Omega$  vs GND is guaranteed on  $V_{\text{DD}}$  pin

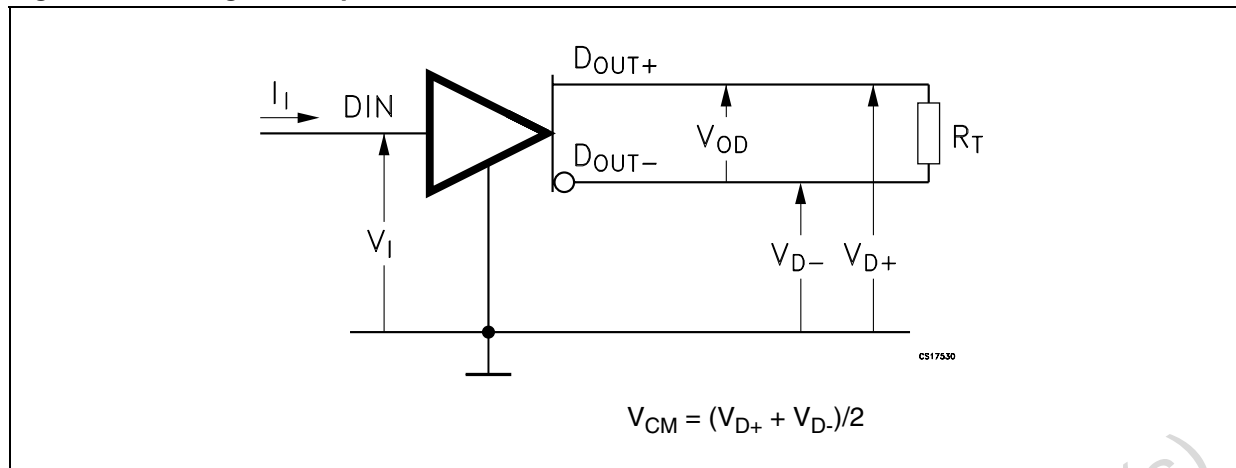
Table 9. Capacitive characteristics

| Symbol          | Parameter   | Test condition         |  | Value                 |      |      | Unit |
|-----------------|---|------------------------|--|-----------------------|------|------|------|
|                 |   | V <sub>DD</sub><br>(V) |  | T <sub>A</sub> = 25°C |      |      |      |
|                 |   |                        |  | Min.                  | Typ. | Max. |      |
| C <sub>IN</sub> | Input capacitance (DIN0-DIN7, CLKIN, EN, BYP, DV0, DV1) | 2.7 to 3.6             | V <sub>IO</sub> = 1.65V to 1.95V,<br>V <sub>I</sub> = GND or V <sub>DD</sub> |                       | 4    |      | pF   |

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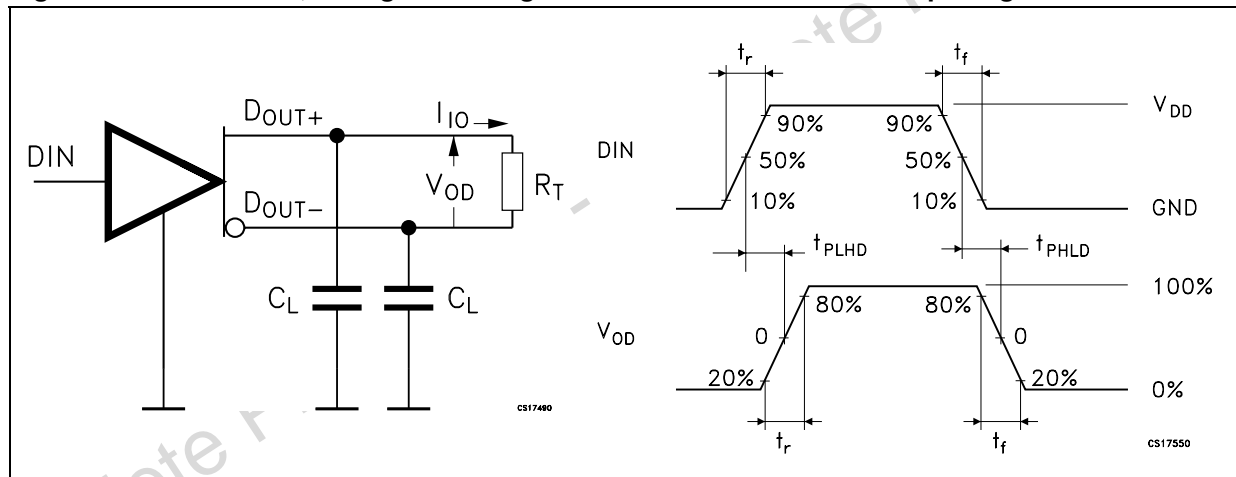
## 5 Test circuits and timing diagram

Figure 3. Voltage and input current definition



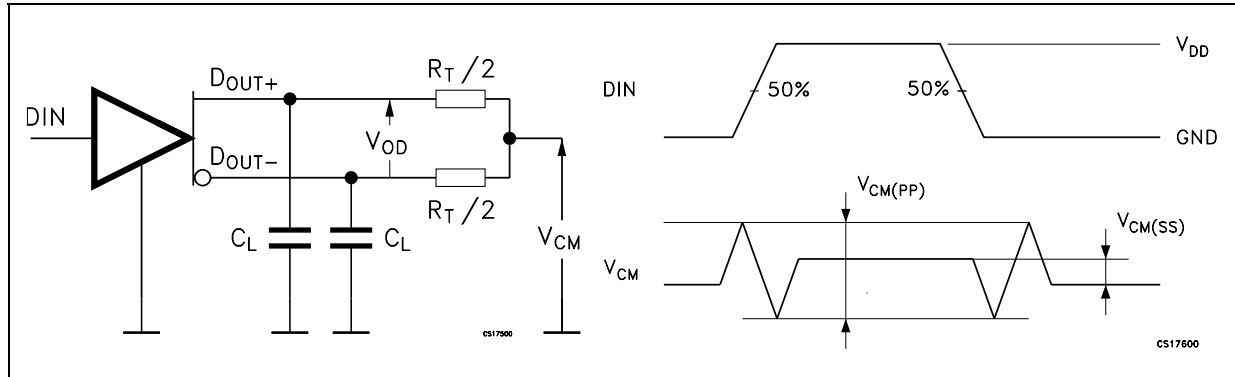
Note:  $R_T = 100 \Omega \pm 1\%$

Figure 4. Test circuit, timing and voltage definitions for differential output signal



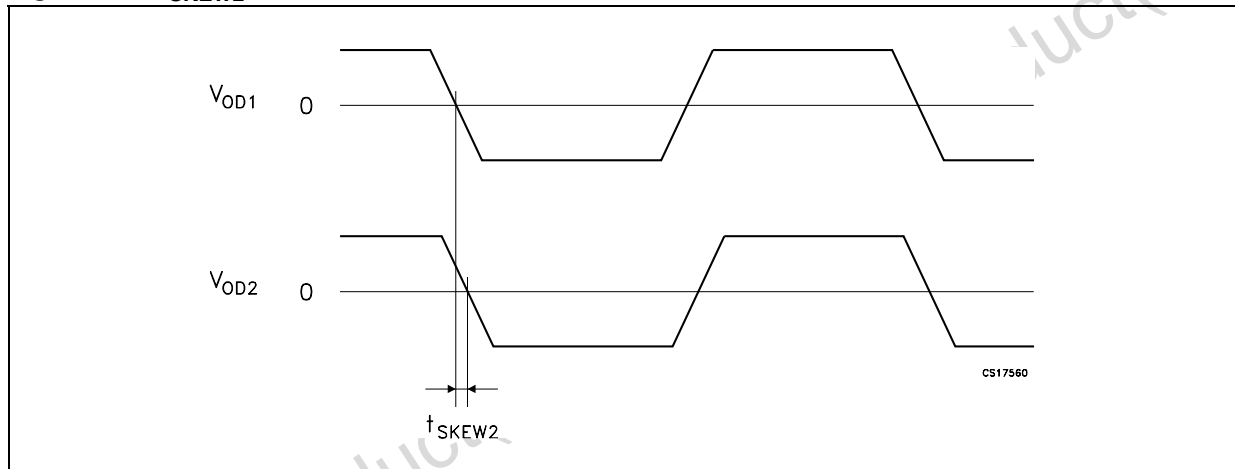
Note:  $R_T = 100 \Omega \pm 1\%$ ;  $C_L = 10pF$ ;  $t_{rDIN} = 4.9ns$ ;  $t_{fDIN} = 4.2ns$ ;  $f_{DIN} = 10MHz$ ;  $PulseWidth_{DIN} = 50ns$ .

Figure 5. Test circuit and definitions for the driver common mode output voltage



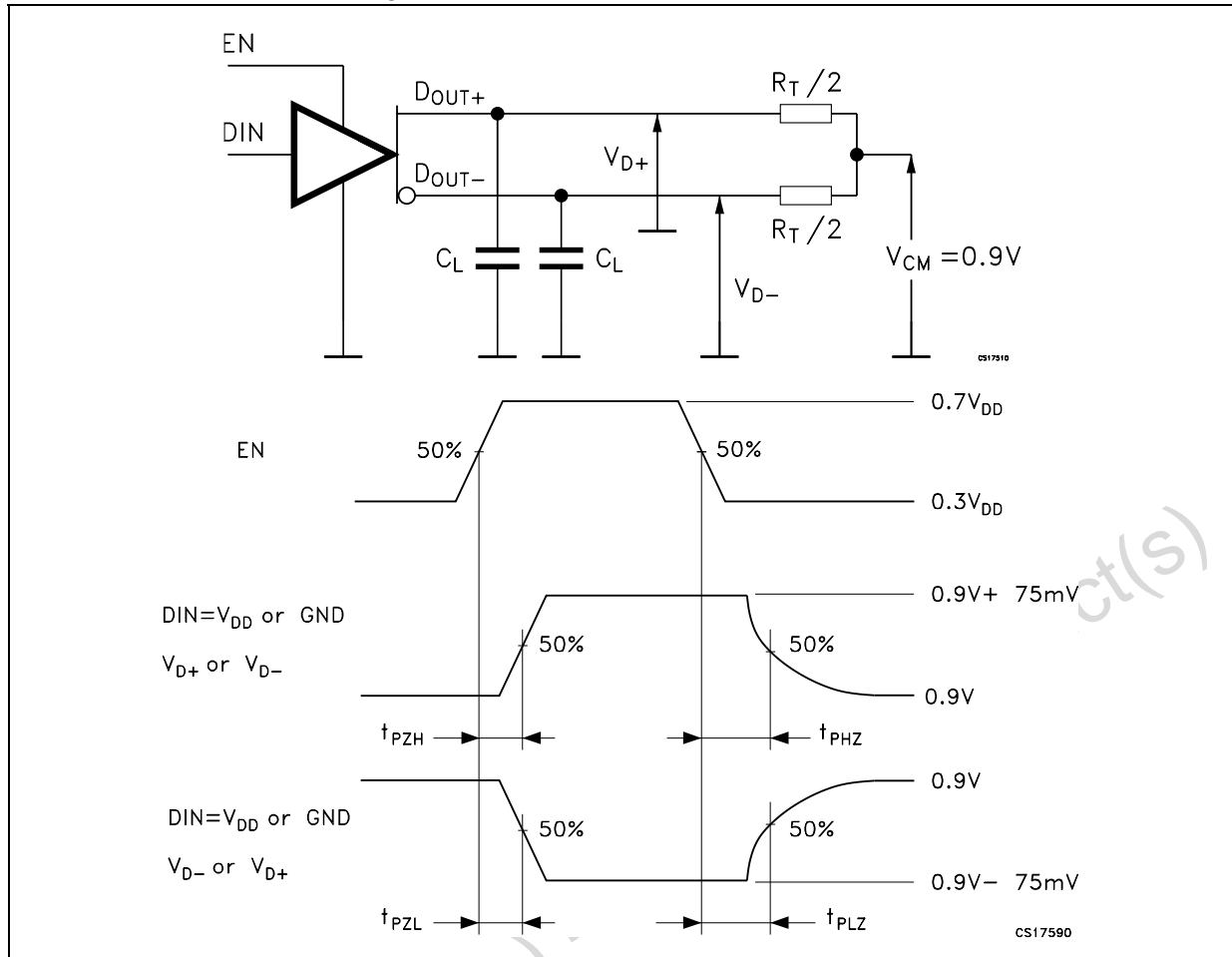
Note:  $R_T = 100 \Omega \pm 1\%$ ;  $C_L = 10\text{pF}$ ;  $t_{rDIN} = 4.9\text{ns}$ ;  $t_{fDIN} = 4.2\text{ns}$ ;  $f_{DIN} = 10\text{MHz}$ ;  $\text{PulseWidth}_{DIN} = 50\text{ns}$ .

Figure 6.  $t_{\text{SKEW2}}$



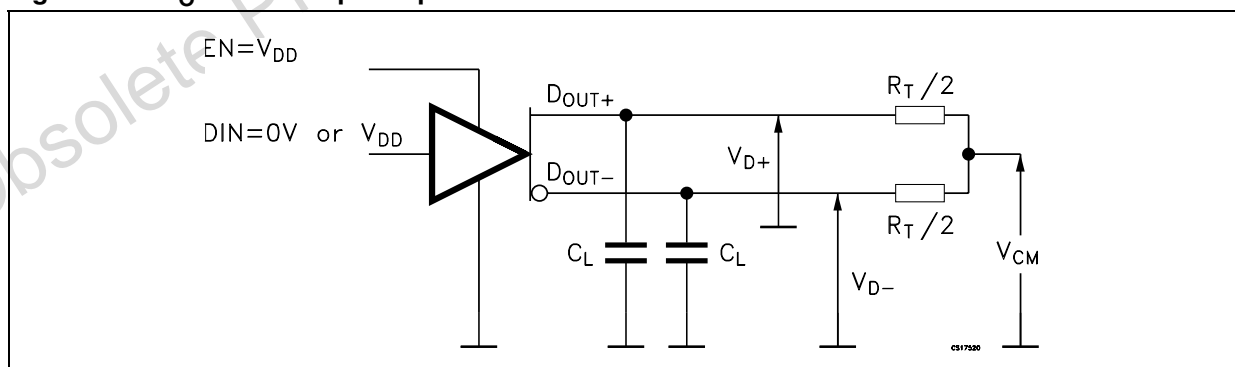
Note:  $R_T = 100 \Omega \pm 1\%$ ;  $C_L = 10\text{pF}$ ;  $t_{rDIN} = 4.9\text{ns}$ ;  $t_{fDIN} = 4.2\text{ns}$ ;  $f_{DIN} = 10\text{MHz}$ ;  $\text{PulseWidth}_{DIN} = 50\text{ns}$

Figure 7.  $t_{EN}$  ( $t_{PZL}$ ,  $t_{PZH}$ );  $t_{DIS}$  ( $t_{PHZ}$ ,  $t_{PLZ}$ )



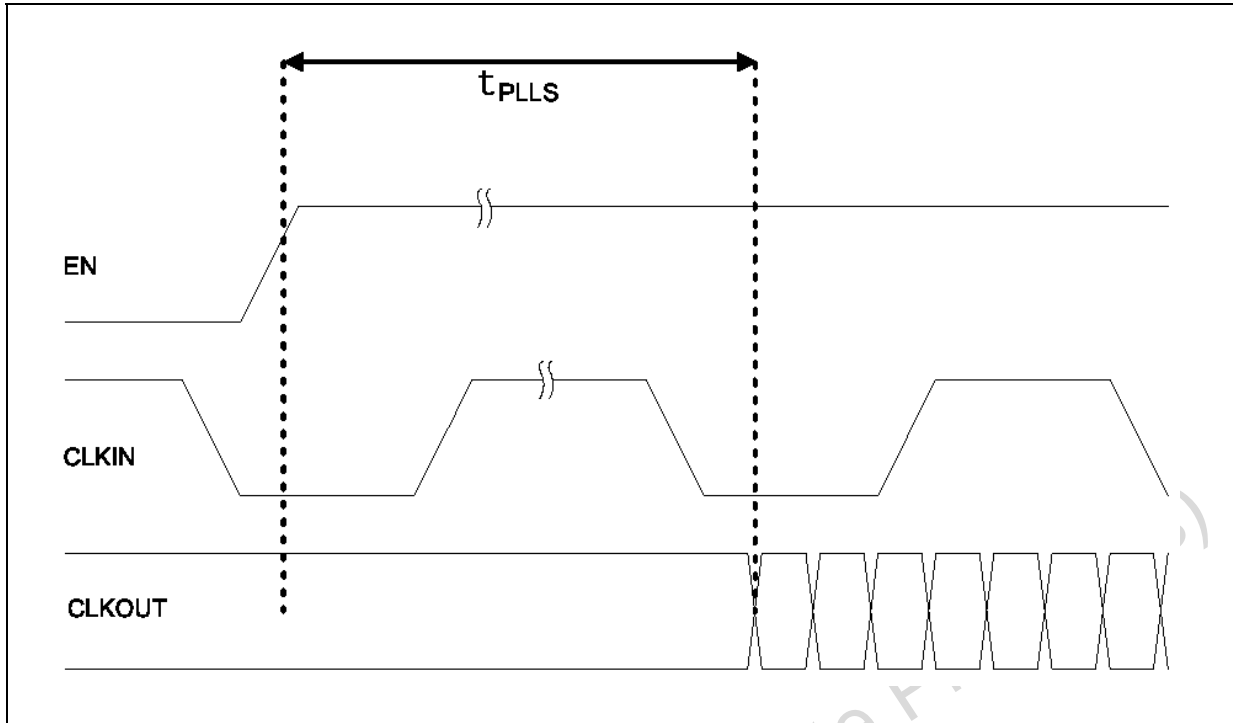
Note:  $R_T = 100 \Omega \pm 1\%$ ;  $C_L = 10pF$ ;  $t_{rDIN} = 2.0ns$ ;  $t_{fDIN} = 2.0ns$ ;  $f_{EN} = 1MHz$ ;  $PulseWidth_{DIN} = 500ns$

Figure 8.  $R_O$ : Driver output impedance



Note:  $R_T = 100 \Omega \pm 1\%$ ;  $C_L = 10pF$   
 $\Delta V_{X+} = V_{D+(VCM=1.0V)} - V_{D+(VCM=0.8V)}$ ;  $\Delta V_{X-} = V_{D-(VCM=1.0V)} - V_{D-(VCM=0.8V)}$ ;  
 $R_{O+} = (R_T/2 \times \Delta V_{X+}) / (200mV - \Delta V_{X+})$ ;  $R_{O-} = (R_T/2 \times \Delta V_{X-}) / (200mV - \Delta V_{X-})$

Figure 9.  $t_{PLL}$



Note: During  $t_{PLL}$  test  $DV0=DV1=V_{DD}$

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Figure 10. General timing diagram (parallel mode)

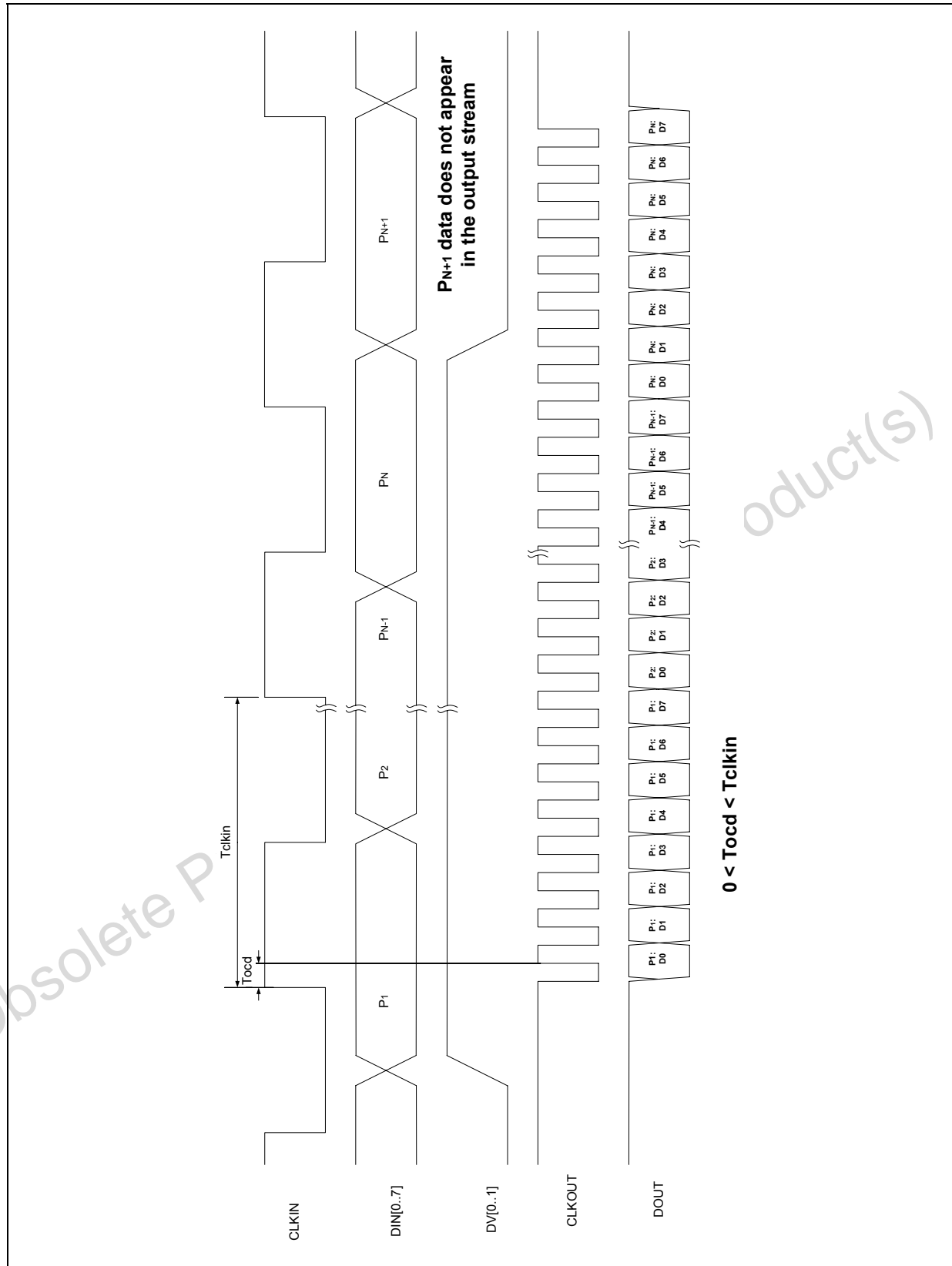
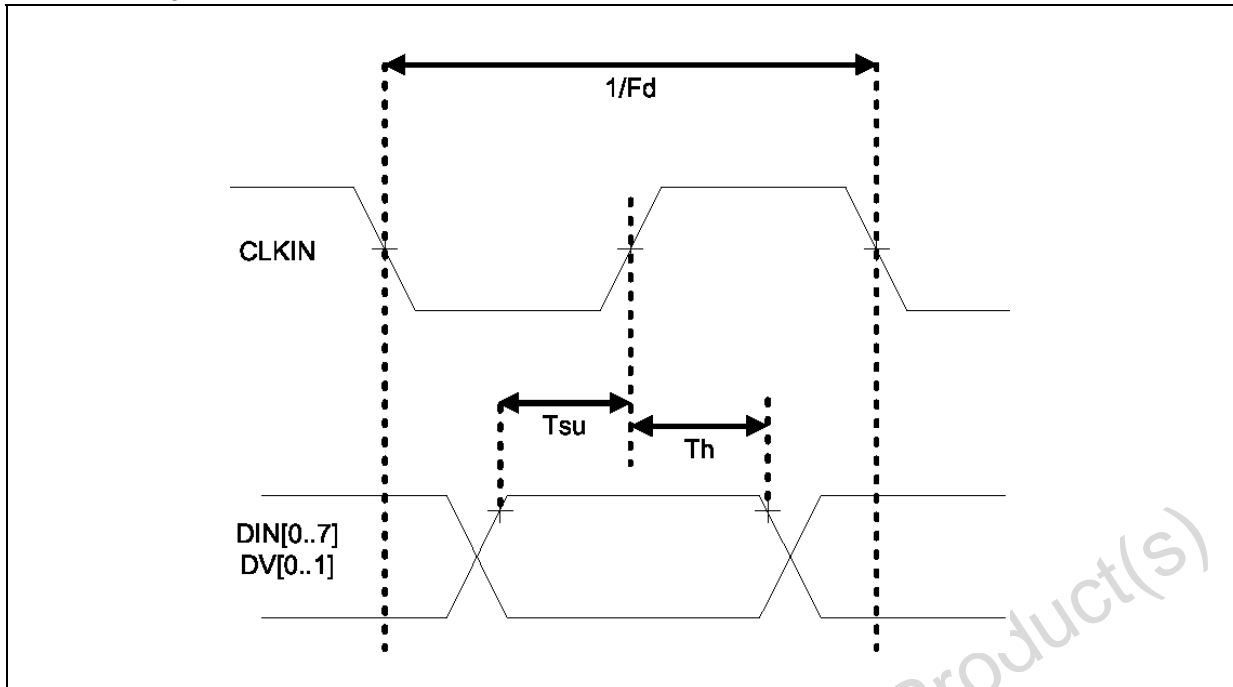
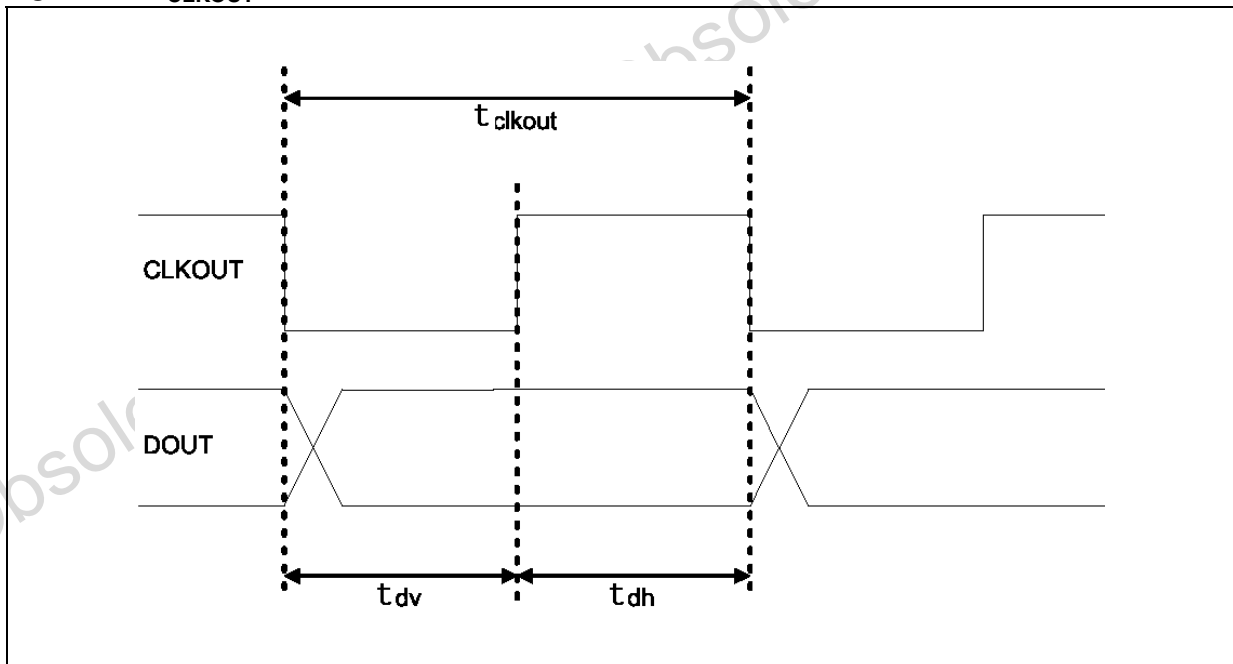


Figure 11.  $t_{CLKIN}$



Note:  $t_{CLKIN}$

Figure 12.  $t_{CLKOUT}$



Note:  $t_{CLKOUT}$

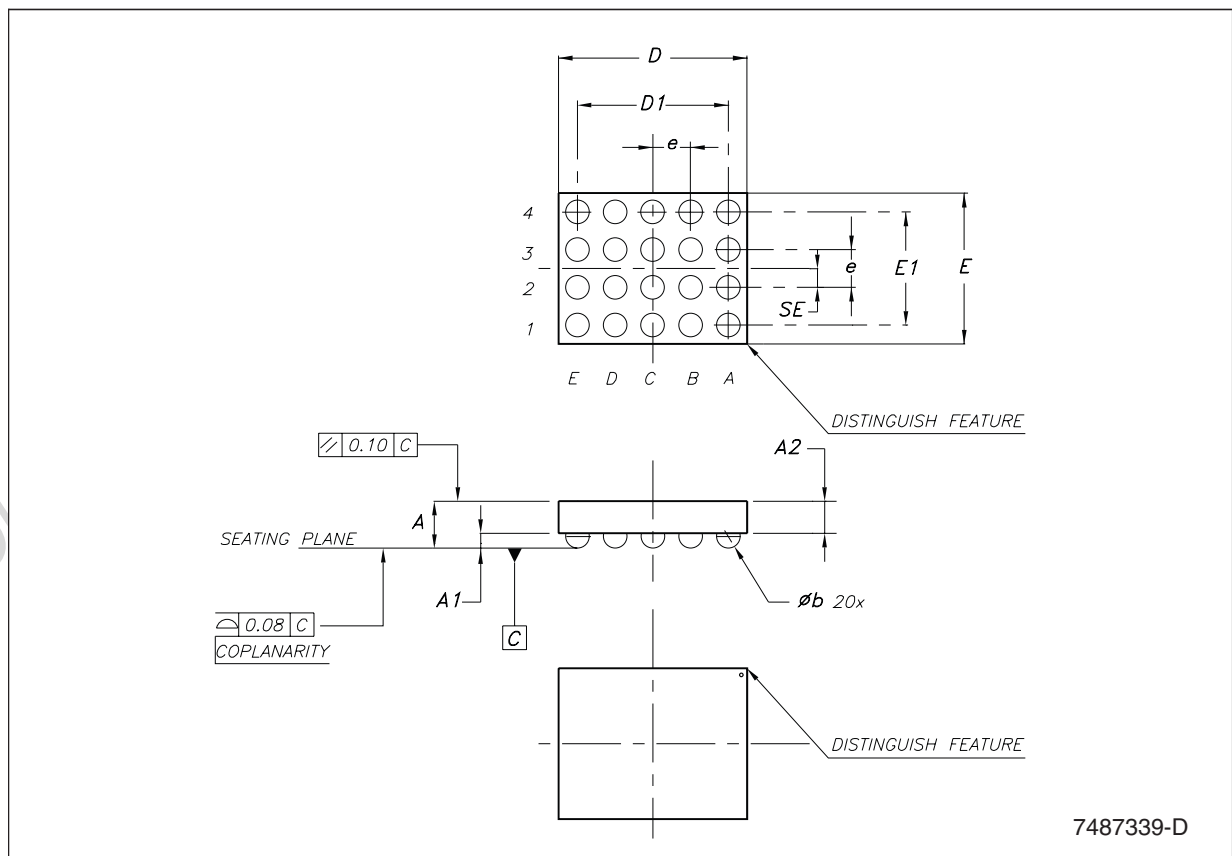
## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

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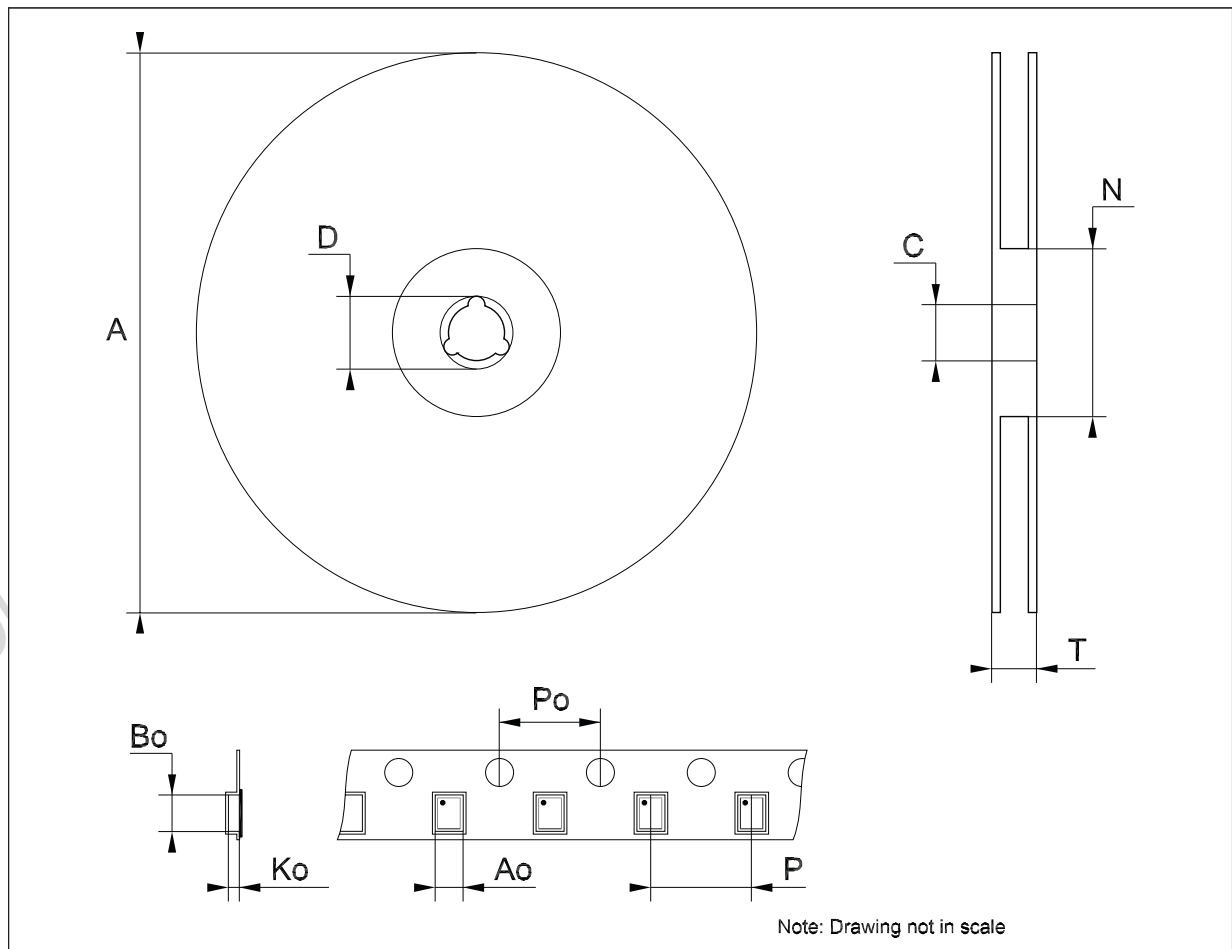
### Flip-Chip20 Mechanical Data

| Dim. | mm.  |      |      | mils. |      |      |
|------|------|------|------|-------|------|------|
|      | Min. | Typ. | Max. | Min.  | Typ. | Max. |
| A    | 0.81 | 0.89 | 1.00 | 31.9  | 35.0 | 39.4 |
| A1   | 0.15 | 0.24 | 0.35 | 5.9   | 9.4  | 13.8 |
| A2   |      | 0.65 |      |       | 25.6 |      |
| b    | 0.25 | 0.30 | 0.35 | 9.8   | 11.8 | 13.8 |
| D    | 2.41 | 2.46 | 2.51 | 94.9  | 96.9 | 98.8 |
| D1   |      | 2.00 |      |       | 78.7 |      |
| E    | 1.93 | 1.98 | 2.03 | 76.0  | 78.0 | 79.9 |
| E1   |      | 1.5  |      |       | 59.1 |      |
| e    |      | 0.50 |      |       | 19.7 |      |
| SE   |      | 0.25 |      |       | 9.8  |      |



**Tape & Reel Flip-Chip20 Mechanical Data**

| Dim. | mm.  |      |      | inch. |       |       |
|------|------|------|------|-------|-------|-------|
|      | Min. | Typ. | Max. | Min.  | Typ.  | Max.  |
| A    |      |      | 180  |       |       | 7.086 |
| C    | 12.8 |      | 13.2 | 0.504 |       | 0.519 |
| D    | 20.2 |      |      | 0.795 |       |       |
| N    | 60   |      |      | 2.362 |       |       |
| T    |      |      | 14.4 |       |       | 0.567 |
| Ao   | 2.13 | 2.23 | 2.33 | 0.084 | 0.088 | 0.092 |
| Bo   | 2.62 | 2.72 | 2.82 | 0.103 | 0.107 | 0.111 |
| Ko   | 1.05 | 1.15 | 1.25 | 0.041 | 0.045 | 0.049 |
| Po   | 3.9  |      | 4.1  | 0.153 |       | 0.161 |
| P    | 3.9  |      | 4.1  | 0.153 |       | 0.161 |



## 7 Revision history

Table 10. Revision history

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 01-Jun-2007 | 1        | Initial release. |

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