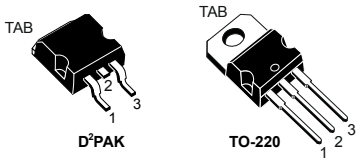
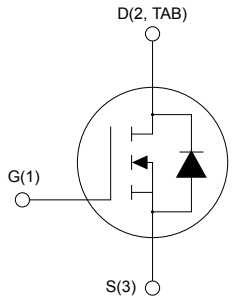
STB76NF75, STP76NF75

Datasheet

Automotive N-channel 75 V, 9.5 mΩ typ., 80 A STripFET II Power MOSFET in a D²PAK and TO-220 packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB76NF75	75 V	11 mΩ	80 A
STP76NF75			

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status links
STB76NF75
STP76NF75

Product summary	
Order code	**STB76NF75**
Marking	B76NF75
Package	D²PAK
Packing	Tape and reel
Order code	**STP76NF75**
Marking	P76NF75
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-source voltage (V_{GS} = 0 V)	75	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	75	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	80	A
	Drain current (continuous) at T_C = 100 °C	70	
I_{DM}(1)	Drain current (pulsed)	320	A
P_{TOT}	Total power dissipation at T_C = 25 °C	300	W
dv/dt(2)	Peak diode recovery voltage slope	12	V/ns
E_{AS}(3)	Single-pulse avalanche energy	700	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 80 A, di/dt ≤ 300 A/µs, V_{DD} ≤ $V_{(BR)DSS}$.*
3. *Starting T_J = 25 °C, I_D = 40 A, V_{DD} = 37.5 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	75	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 75 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 75 V, T_C = 125 °C(1)	-	-	10	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A	-	9.5	11	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 40 A	-	20	-	S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	3700	-	pF
C_{oss}	Output capacitance		-	730	-	pF
C_{rss}	Reverse transfer capacitance		-	240	-	pF
Q_g	Total gate charge	V_{DD} = 60 V, I_D = 80 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	117	160(1)	nC
Q_{gs}	Gate-source charge		-	27	-	nC
Q_{gd}	Gate-drain charge		-	47	-	nC

1. *Specified by design, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 37.5 V, I_D = 45 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	25	-	ns
t_r	Rise time		-	100	-	ns
$t_{d(off)}$	Turn-off delay time		-	66	-	ns
t_f	Fall time		-	30	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	80	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	320	A
V_{SD}(2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A, di/dt = 100 A/µs,	-	132	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 25 V, T_J = 150 °C	-	660	-	nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

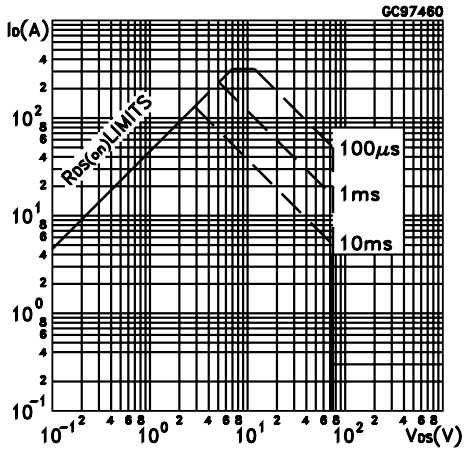


Figure 2. Thermal impedance

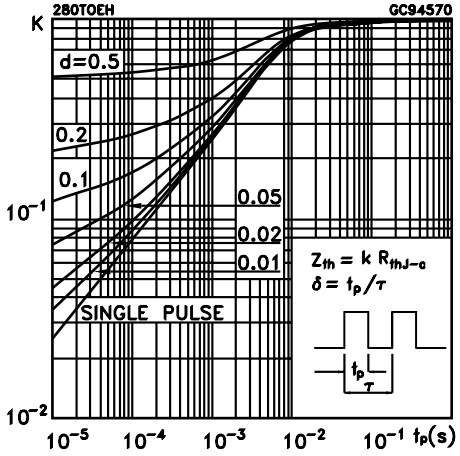


Figure 3. Output characteristics

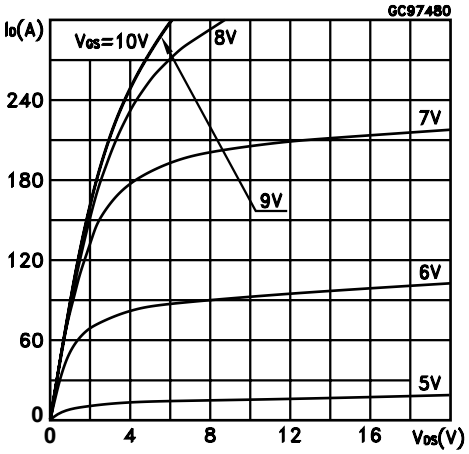


Figure 4. Transfer characteristics

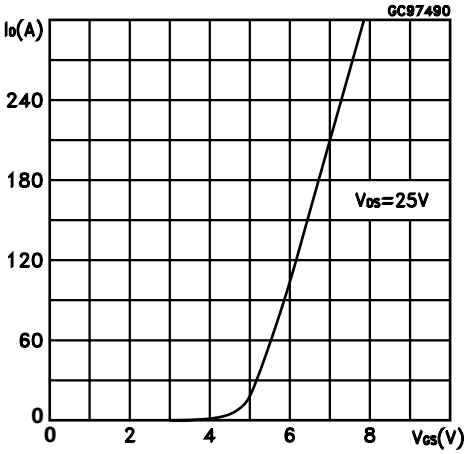


Figure 5. Trasconductance

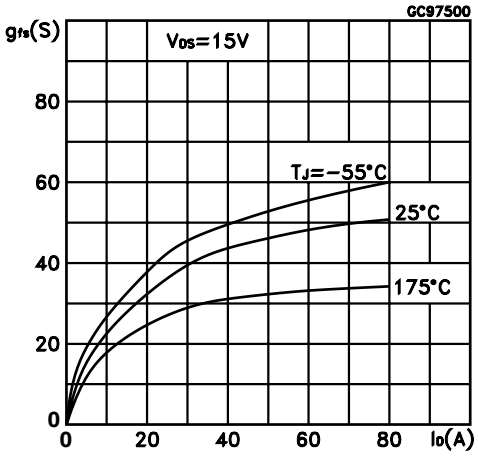


Figure 6. Static drain-source on-resistance

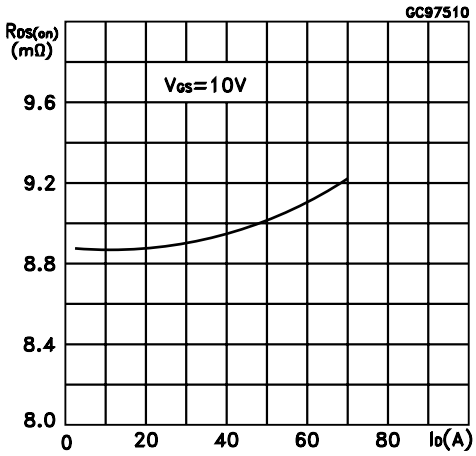


Figure 7. Gate charge vs gate-source voltage

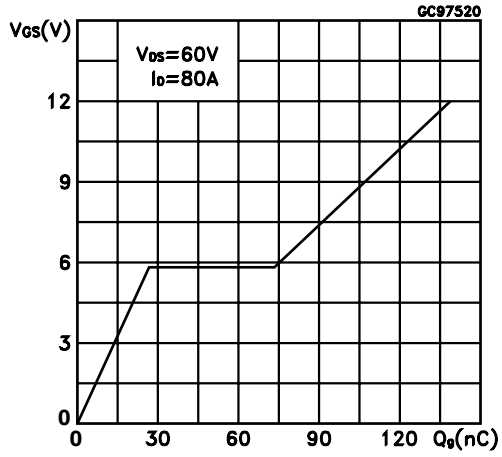


Figure 8. Capacitance variations

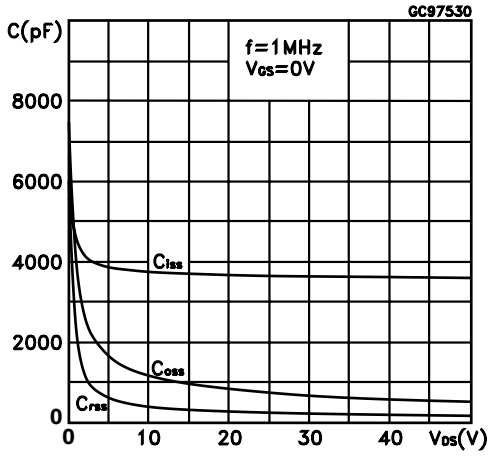


Figure 9. Normalized gate threshold voltage vs temperature

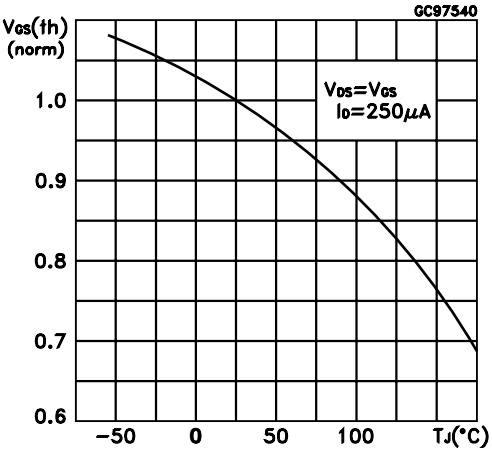


Figure 10. Normalized on-resistance vs temperature

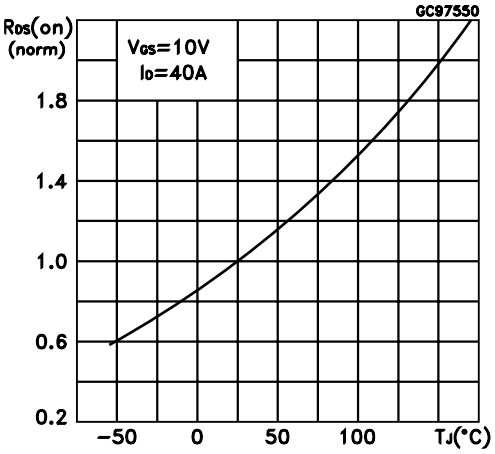


Figure 11. Typical reverse diode forward characteristics

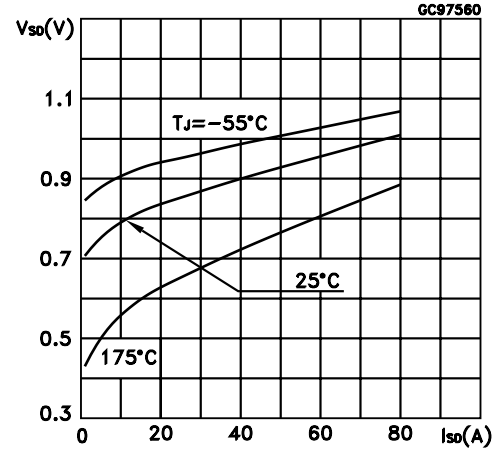
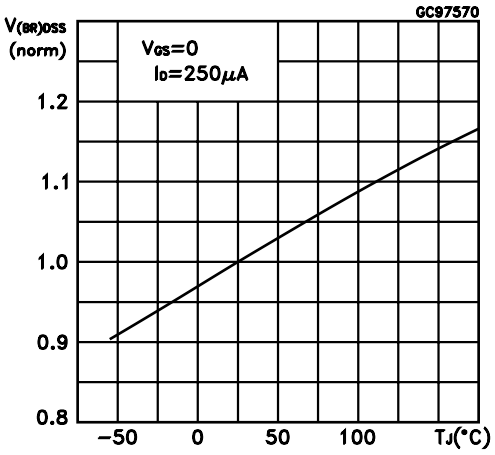


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

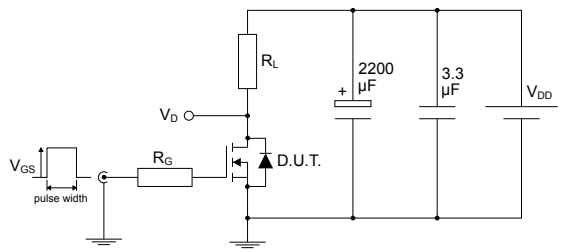


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Figure 14. Test circuit for gate charge behavior

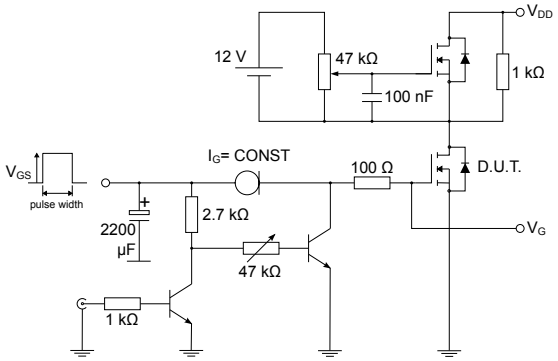

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Figure 15. Test circuit for inductive load switching and diode recovery times

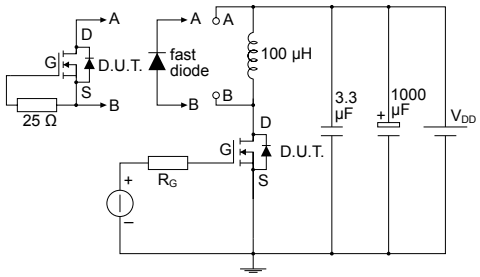

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Figure 16. Unclamped inductive load test circuit

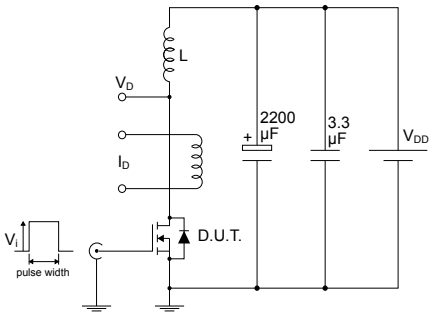

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Figure 17. Unclamped inductive waveform

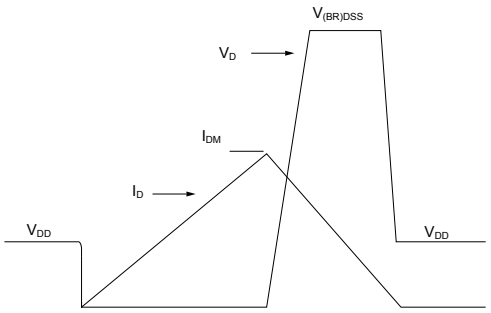

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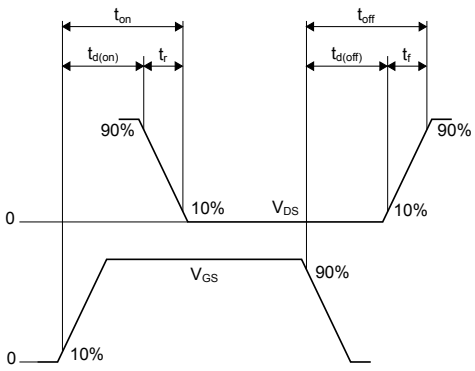
Figure 18. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 19. D²PAK (TO-263) type A package outline

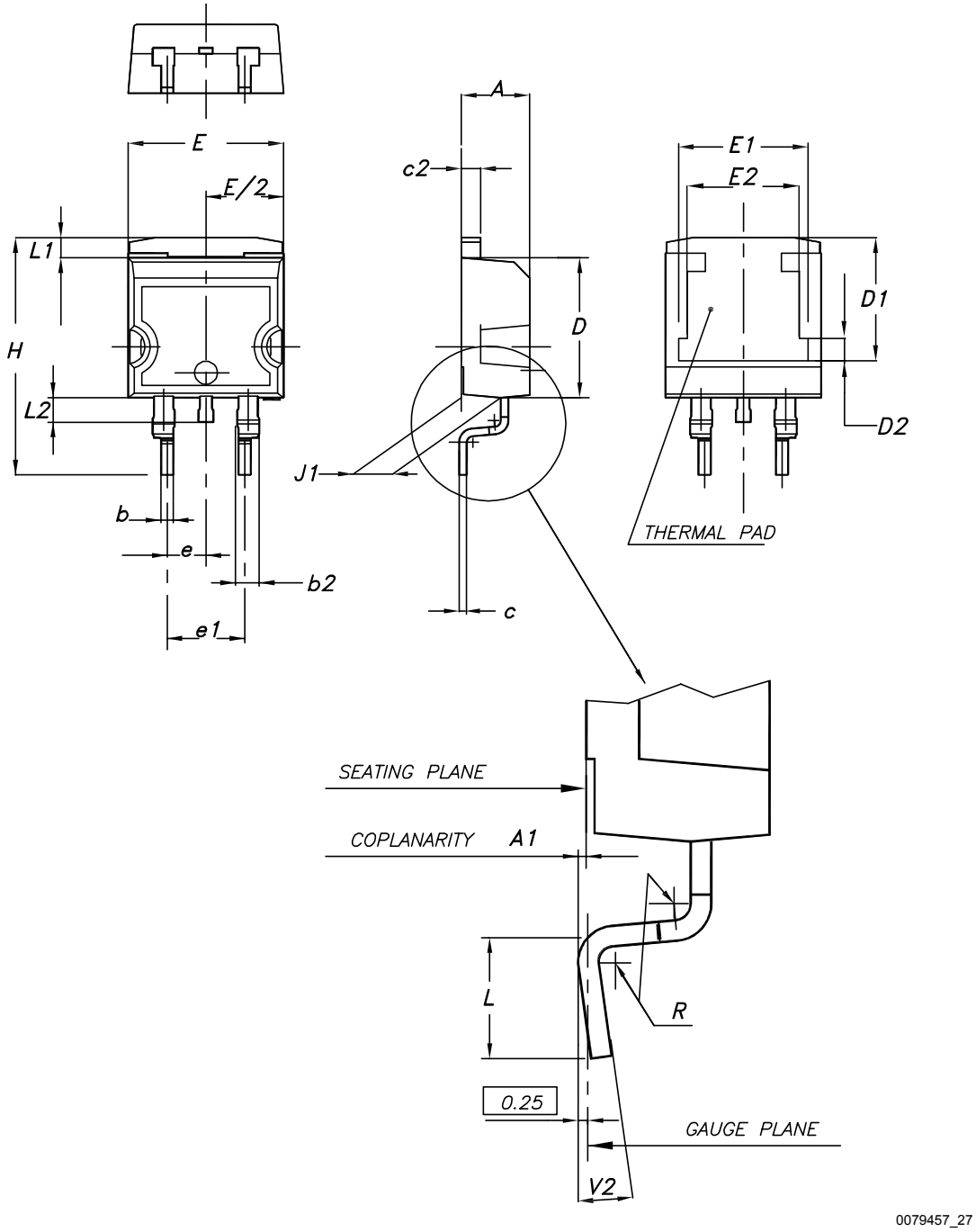
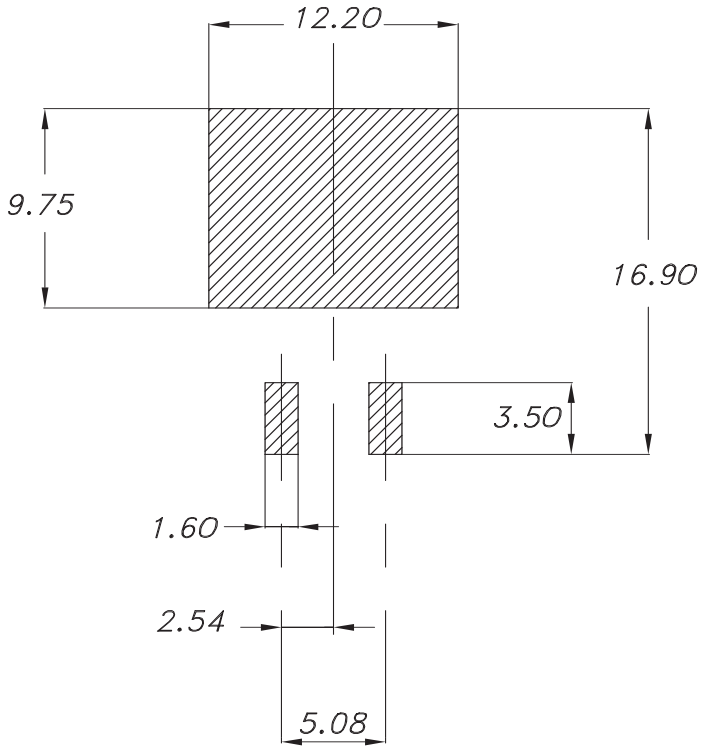


Table 7. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220 type A package information

Figure 21. **TO-220 type A package outline**

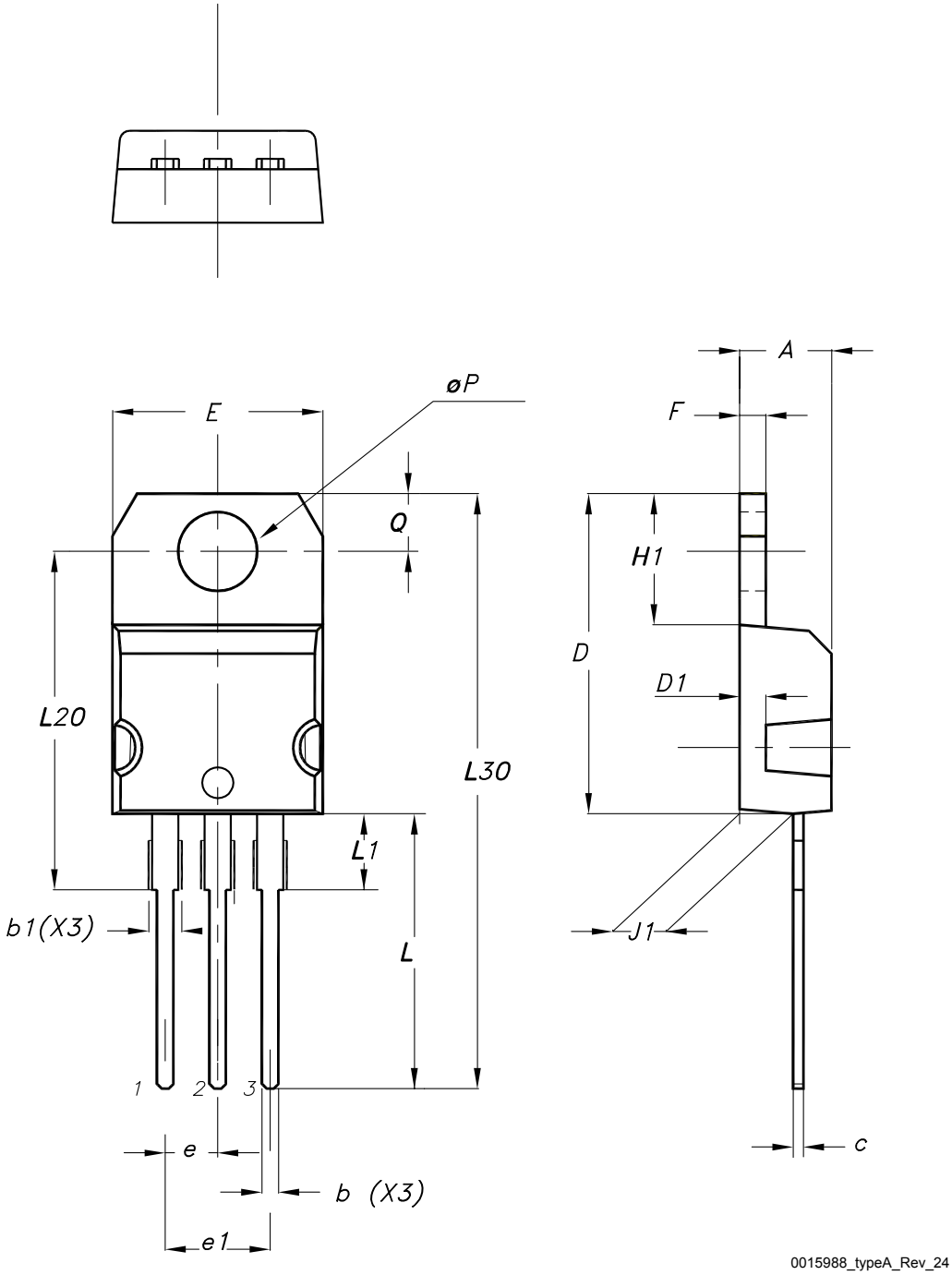
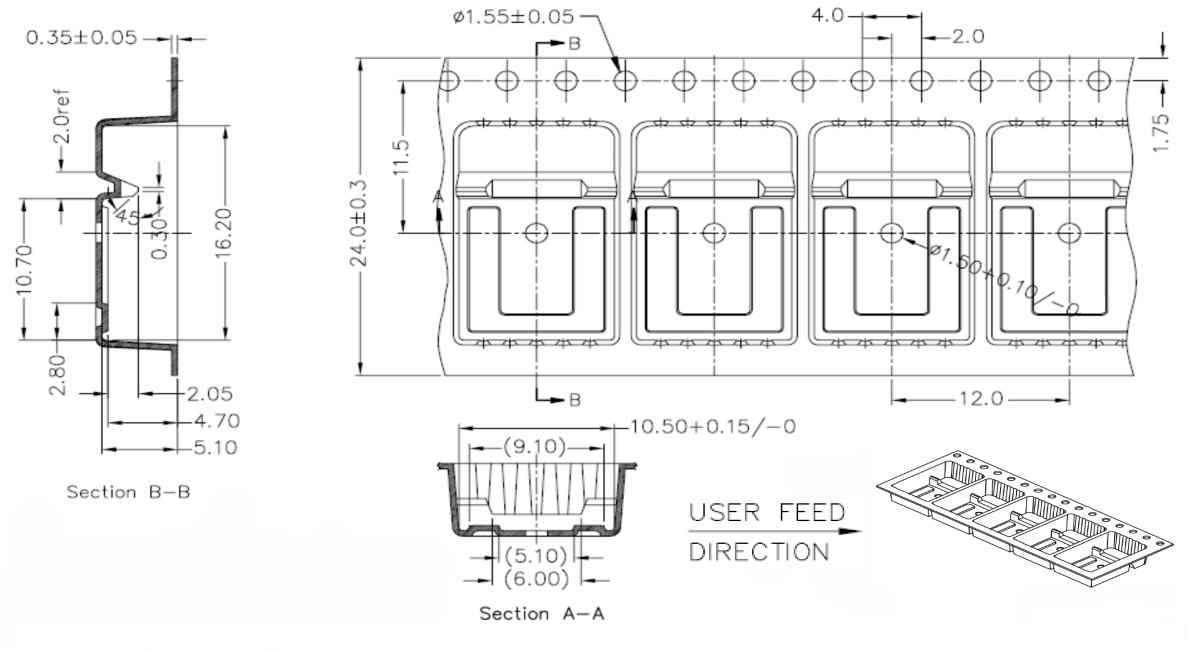


Table 8. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 D²PAK packing information

Figure 22. **D²PAK tape drawing (dimensions are in mm)**



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Revision history

Table 9. **Document revision history**

Date	Version	Changes
25-Jul-2007	1	First release.
14-Dec-2009	2	Added new package, mechanical data: I²PAK.
28-Jan-2026	3	Removed order code STI76NF75. Updated Section 4: Package information. Minor text changes.

Contents