DCP10001Y

Datasheet

Automotive 100 V, 1 A synchronous step-down converter



Maturity status link
DCP10001Y

Features

- AEC-Q100 Grade 1 qualified
- 6 V to 100 V input voltage range
- Supports 36 V, 48 V, 60 V, 72 V electric battery packs
- 1.5 V to 30 V output voltage range
- Compliant with IPC-2221B requirements for clearance and creepage
- Programmable switching frequency from 100 kHz to 1 MHz
- 1.5 % output voltage accuracy (whole temperature range)
- 750 [mΩ] / 300 [mΩ] Integrated Power MOSFETs
- V_2COT control mode architecture
- 14 µA no-load input quiescent current
- Dithering for EMI reduction
- Three different versions: 1A, 0.7A and 0.5A current capability
- Efficiency at 1 A load
  - 92 % for 48 V to 12 V @ 400 kHz conversion;
- Fixed 3.8 ms internal soft-start timer
- Overcurrent protection (OCP), overvoltage protection (OVP), and overtemperature protection (OTP).
- Operating temperature range: -40 °C to 150 °C

Applications

- Battery electric vehicle control supply
- EV GPS tracker

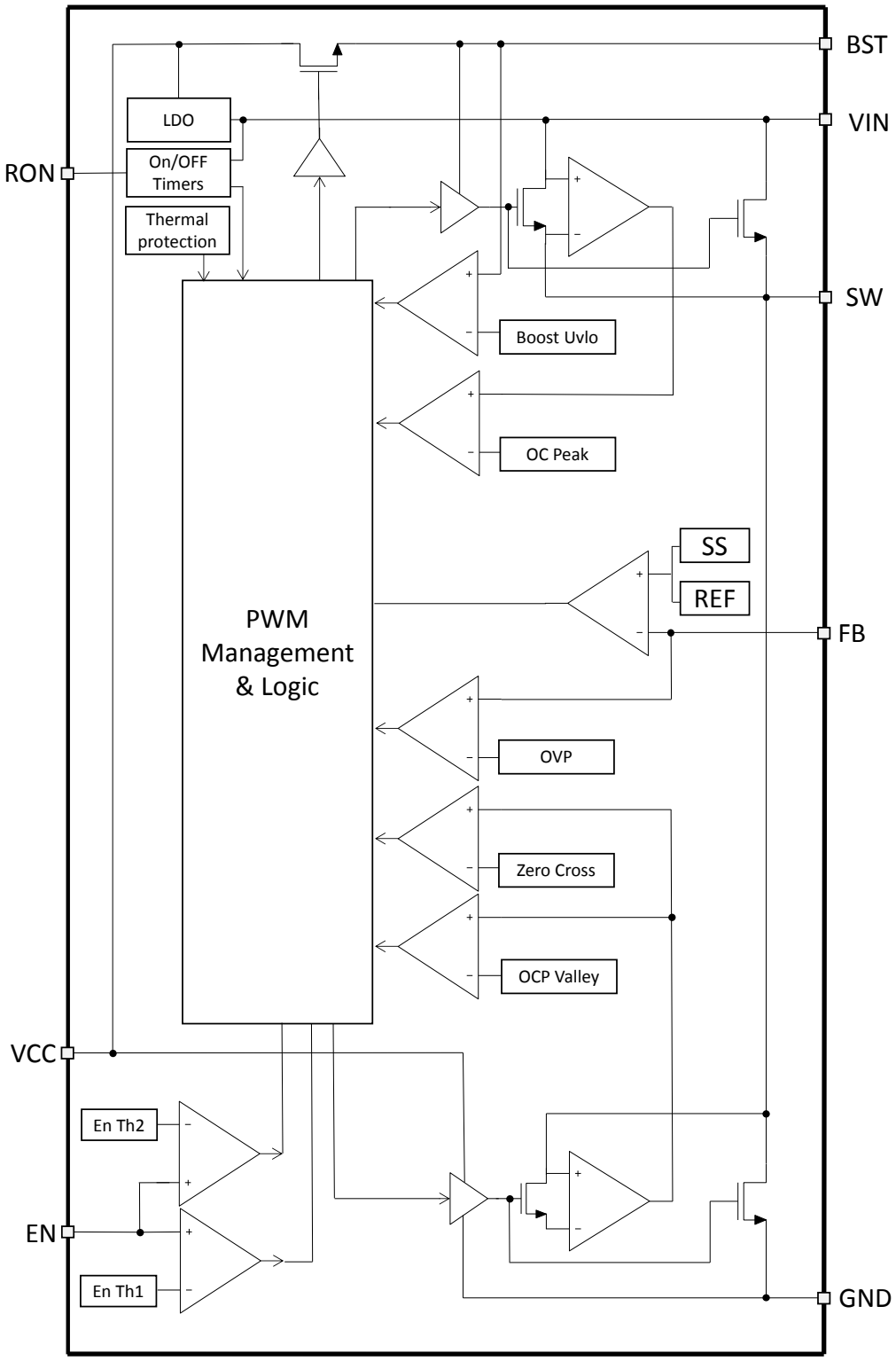
Description

The DCP10001Y is a synchronous, monolithic step-down converter that delivers up to 1 A of load current. It supports a wide input-voltage range and uses a V2COT (Voltage-Mode Constant On-Time) architecture to achieve fast load-transient response with fixed-frequency operation

The device is AEC-Q100 Grade 1 qualified and is available in an HSOP-8L 4.9 mm x 6 mm package. In shutdown mode, it draws less than 1 µA. When EN is asserted high, the device starts a 3.8 ms soft-start sequence. It also supports spread-spectrum operation for EMI reduction and includes OCP, OVP, and OTP protection features.

1 Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin connection (top view)**

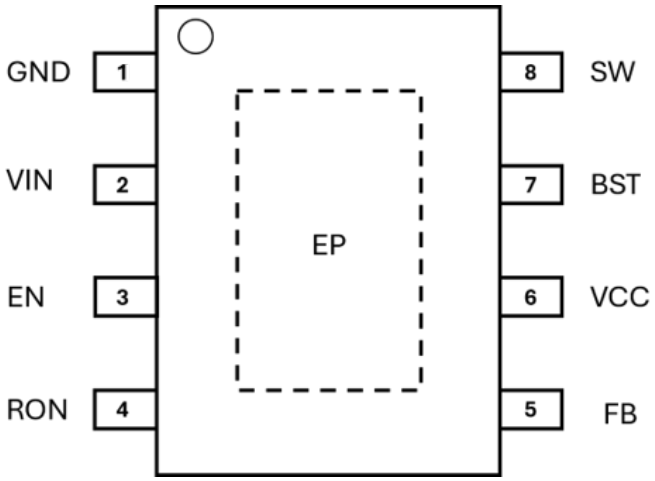


Table 1. **Pin description**

Pin #	Symbol	Function
1	GND	**System ground.** GND is the reference ground of the regulated output voltage. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
2	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
3	EN	**Enable.** Precision enable and undervoltage lockout (UVLO) programming pin. If the EN voltage is below 0.8 V, the converter is in shutdown mode with all functions disabled. If the EN voltage is above 0.8 V and below 1.2 V, the converter is in standby mode with the internal VCC regulator working but without switching. If the EN voltage is above 1.2 V, the start-up sequence begins.
4	RON	**On-Time programming.** Connect an external resistor to program the switch-on time.
5	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the primary output voltage. It is recommended to place the resistor divider as close as possible to FB. Vias should be avoided on the FB traces.
6	VCC	**Voltage bias.** This pin supplies the embedded analog circuitry. Connect a ceramic capacitor (≥ 1 µF) to filter internal voltage reference.
7	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
8	SW	**Switch output.** Connect SW to the output inductor and to the bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.
-	EP	**Exposed Pad.** No internal electrical connection. Connect the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

3 Typical application circuit

Figure 3. **Typical application circuit**

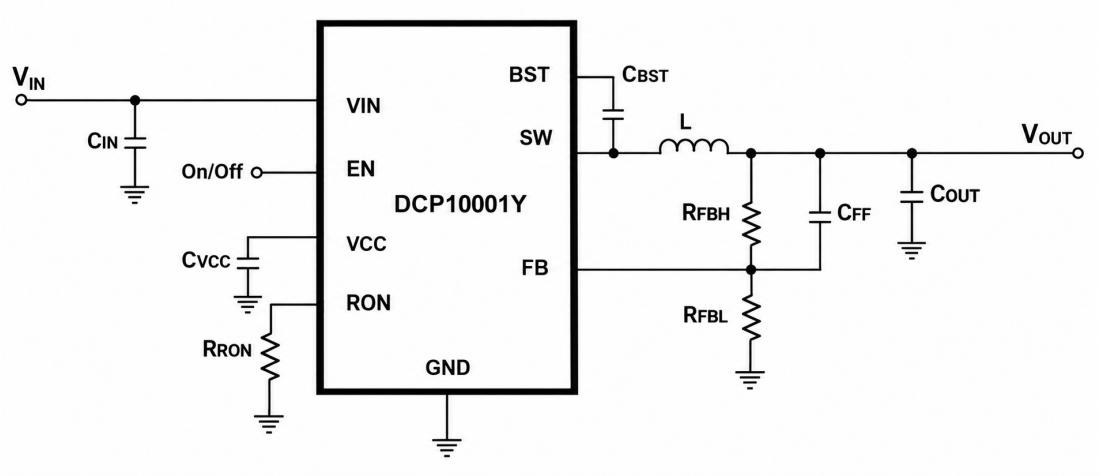


Table 2. **Typical application components 48 V_12 V_400 kHz**

Symbol	Value	Description	Note
C_{IN}	10 µF	Input capacitor	100 V
C_{VCC}	1 µF	VCC bypass capacitor	X7S
C_{BST}	330 pF	Bootstrap capacitor	X7S
C_{FF}	100 pF	Feed Forward capacitor	
C_{OUT}	22µF	Output capacitor	
R_{FBH}	65.9 KΩ	VOUT divider upper resistor	
R_{fbh}	4.7 KΩ	VOUT divider lower resistor	
R_{ron}	62 KΩ	T_{ON} resistor	
L	68 µH	Output inductor	100 V

4 Maximum ratings

Stressing the device above the ratings listed in Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	-0.3 to 100	V
V_{EN}	Enable pin voltage	-0.3 to 100	V
V_{FB}	Feedback pin voltage	-0.3 + 5.5	V
V_{RON}	R_{ON} pin maximum voltage	-0.3 + 5.5	V
V_{CC}	Voltage bias pin	-0.3 + 5.5	V
V_{SW}	DC voltage	-0.3 to 100	V
	AC voltage 20 ns	-3V	V
V_{BST_GND}	BST to GND voltage	-0.3 to 105.5	V
V_{BST_SW}	BST to SW voltage	-0.3 to 5.5	V
T_J	Operating junction temperature	-40 to 150	°C
T_{STG}	Storage temperature	-65 to 150	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{\theta}JA$	HSOP-8L Thermal resistance junction-ambient on demoboard 2Layer 2Oz 70mmx70mm	28	°C/W
$R_{\theta}JA$	HSOP-8L Thermal resistance junction-ambient on JEDEC Board 2s2P	32	°C/W
$R_{\theta}JC_bot$	HSOP-8L Thermal resistance junction-case bottom on JEDEC Board 2s2P	3	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM non-corner pins	500	V
		CDM corner pins	750	V

Table 6. Recommended operating conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
V_{IN}	Input voltage range	6		100	V
V_{SW}	Switch node voltage range			100	V
$V_{EN/UVLO}$	Enable voltage range			100	V
I_{LOAD}	Load current (for 1 A version)			1	A
C_{BST}	External BST to SW capacitance		100		nF
T_{OP}	Operating junction temperature range	-40		150	°C

5 Electrical characteristics

V_{IN} = 6 V to 100 V, T_J = -40 °C to +150 °C, typical values are at T_J = 25 °C, V_{IN} = 24 V and V_{EN} = 2 V; unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		6		100	V
$V_{IN-UVLO}$	V_{IN} undervoltage lockout	Rising input voltage	5	5.35	5.7	V
		Falling input voltage	4.85		5.55	V
$V_{EN-UVLO}$	V_{EN} undervoltage lockout	Rising input voltage	1.1	1.2	1.3	V
		Falling input voltage	1.0	1.1	0.9	
$V_{SD-UVLO}$	V_{SD} undervoltage lockout	Rising input voltage			1.1	V
		Falling input voltage (1)	0.15			
I_Q	Quiescent current	V_{EN} = 2.5 V; V_{FB} = 1.3 V		14		µA
I_{OFF}	Shutdown current	V_{EN} = GND		0.7	3	µA
$R_{DS(ON)-H}$	High-side MOSFET ON resistance	T_J=25 °C		750		mΩ
$R_{DS(ON)-L}$	Low-side MOSFET ON resistance	T_J=25 °C		300		mΩ
I_{LIM}	Peak current limit	DCP10001Y	1.3	1.5	1.75	A
		DCP100D7Y	0.95	1.125	1.3	A
		DCP100D5Y	0.65	0.75	0.9	A
I_{VLY}	Valley current limit	DCP10001Y	1.05	1.3	1.5	A
		DCP100D7Y	0.75	0.9	1.1	A
		DCP100D5Y	0.45	0.6	0.8	A
T_{ON_MIN}	Minimum on-time			60		ns
T_{OFF_MIN}	Minimum off-time			120		ns
T_{ON_1}	On-time	V_{IN} = 24V, R_{ron} = 20 kΩ	360	420	490	ns
T_{ON_2}	On-time	V_{IN} = 24V, R_{Ron} = 80 kΩ		1300		ns
T_{ON_3}	On-time	V_{IN} = 48V, R_{ron} = 20 kΩ		200		ns
T_{ON_4}	On-time	V_{IN} = 48V, R_{ron} = 80 kΩ		820		ns
V_{BST}	Bootstrap voltage			2.8	3.5	V
V_{FB}	Feedback voltage	V_{IN} =48V; T_J=25°C	0.792	0.8	0.808	V
			-1		+1	%
		V_{IN} =48V; T_J = -40 °C to 150 °C	0.788	0.8	0.812	V
			-1.5		+1.5	%
Soft-start						
t_{SS}	Internal Soft Start Timer		2.5	3.8	5.3	ms
Overvoltage protections						
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})			120		%
V_{OVP_HYST}	Overvoltage Hysteresis			6		%
Thermal shutdown						

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SHDWN}	Thermal shutdown temperature			175		°C
T_{Hys}	Thermal shutdown hysteresis			20		°C

1. *Specified by design.*

6 Typical characteristics

Figure 4. Efficiency V_{OUT} = 12 V @ 450KHz linear

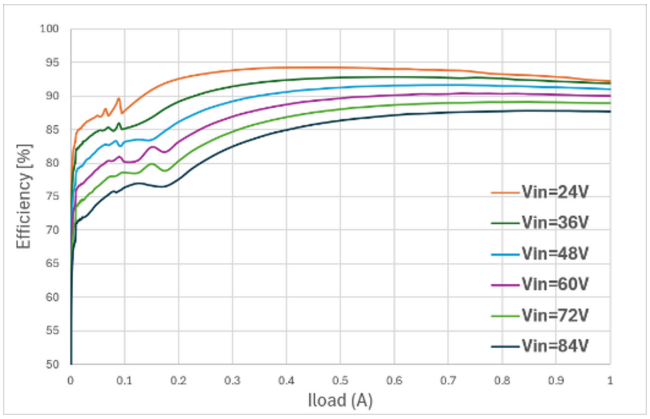


Figure 5. Efficiency V_{OUT} = 12 V @ 450 kHz logarithmic

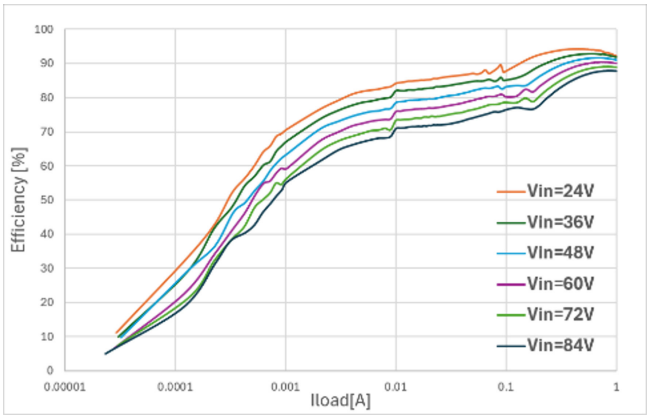


Figure 6. Shutdown current @ V_{IN} = 24V

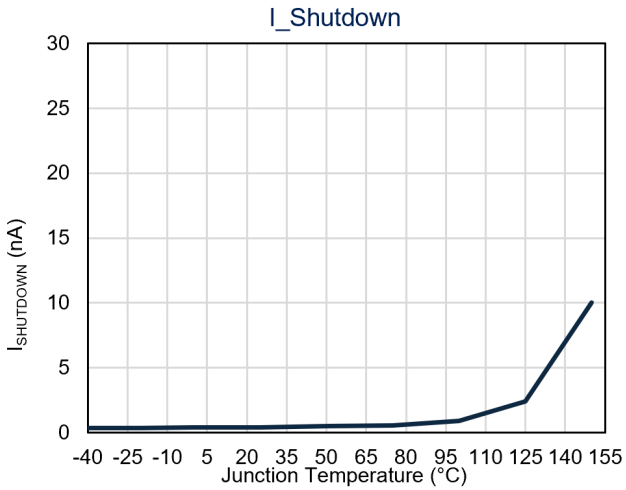


Figure 7. Shutdown current @ T_{amb}

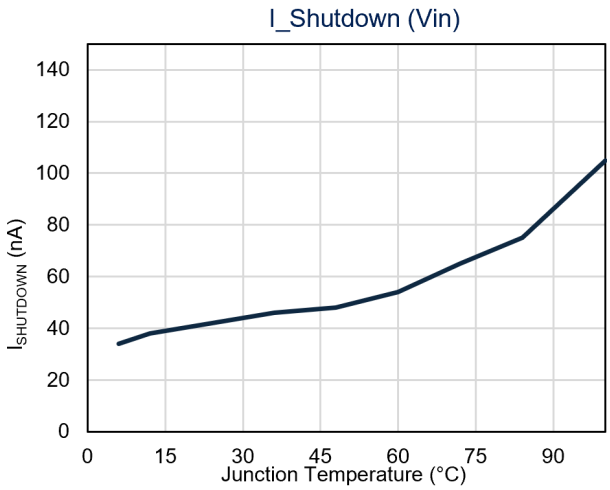


Figure 8. I_QUIESCENT @ V_{in} = 48V

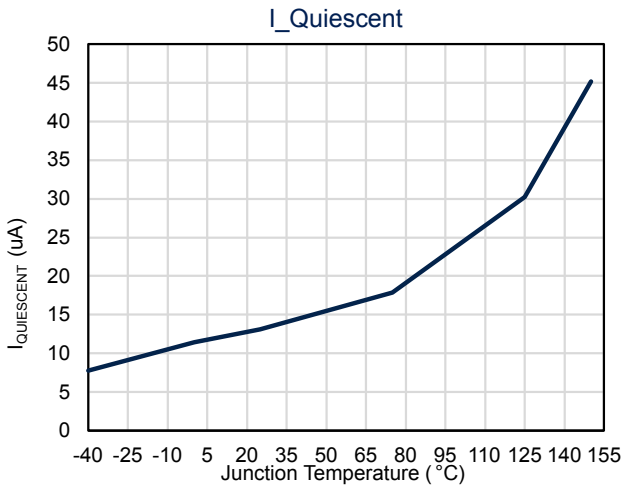


Figure 9. Feedback voltage regulation threshold

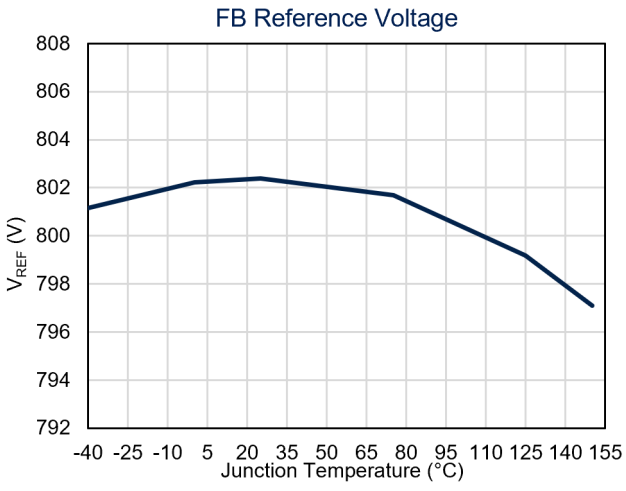


Figure 10. Internal VCC regulation

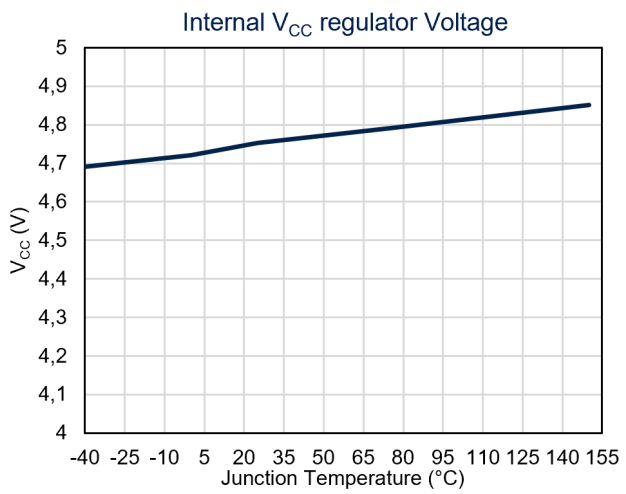


Figure 11. Peak and valley current @ 1 A

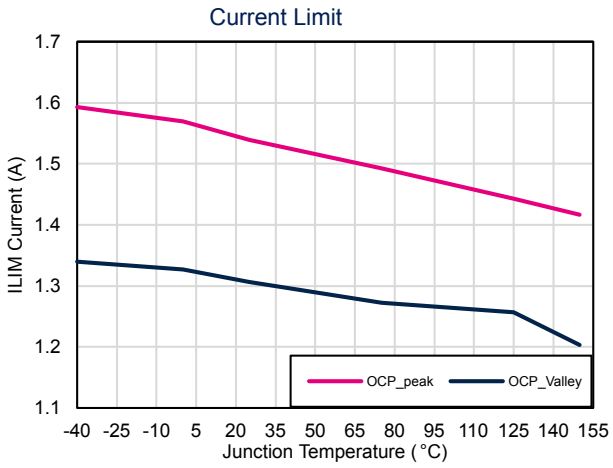


Figure 12. Minimum T_{ON} and T_{OFF}

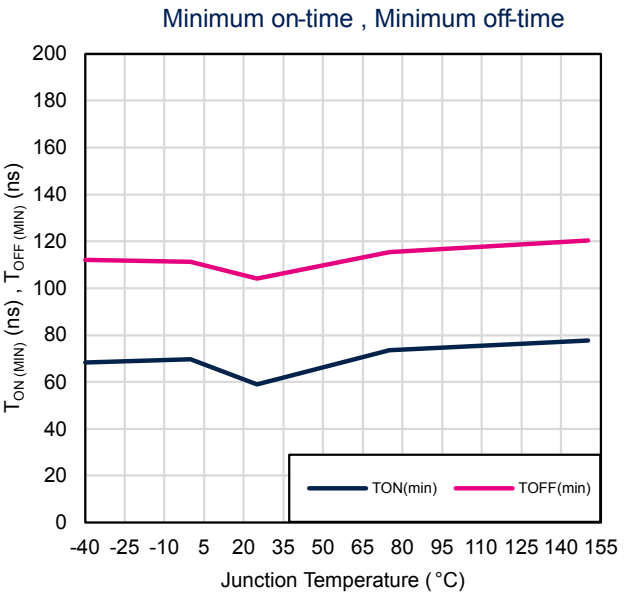


Figure 13. T_{ON} setting

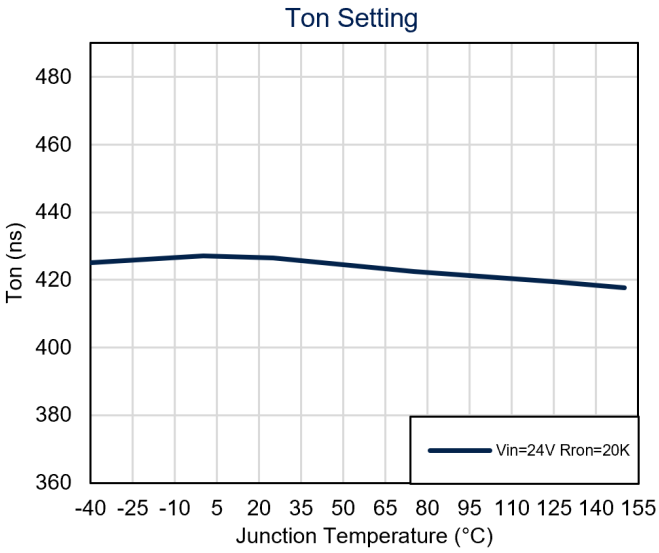


Figure 14. Input voltage thresholds

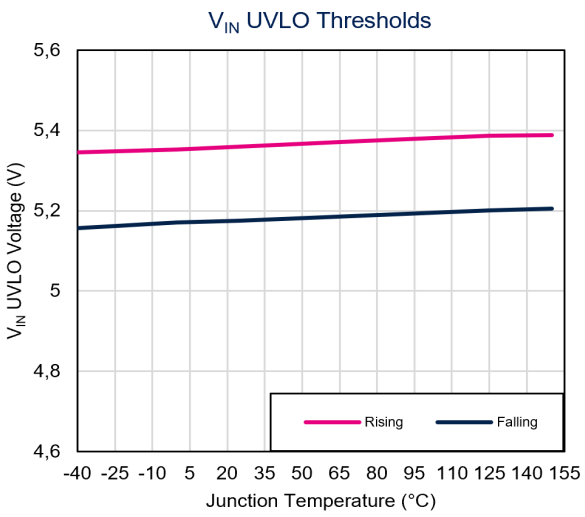


Figure 15. Bootstrap thresholds

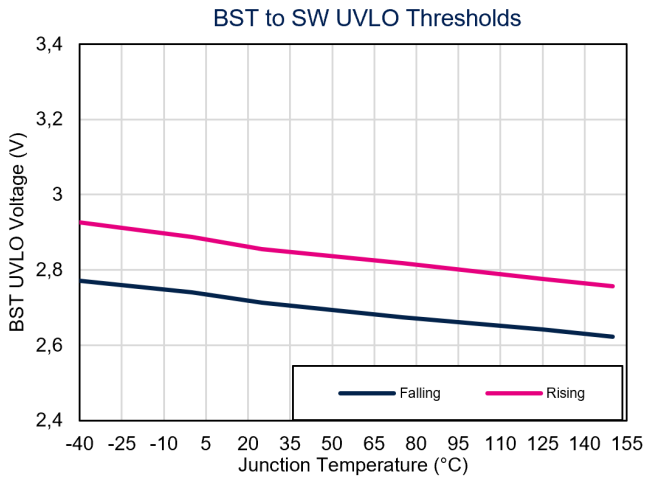


Figure 16. Enable thresholds

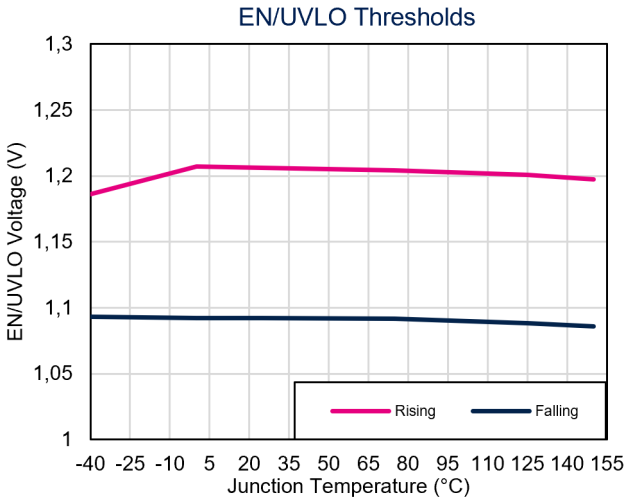
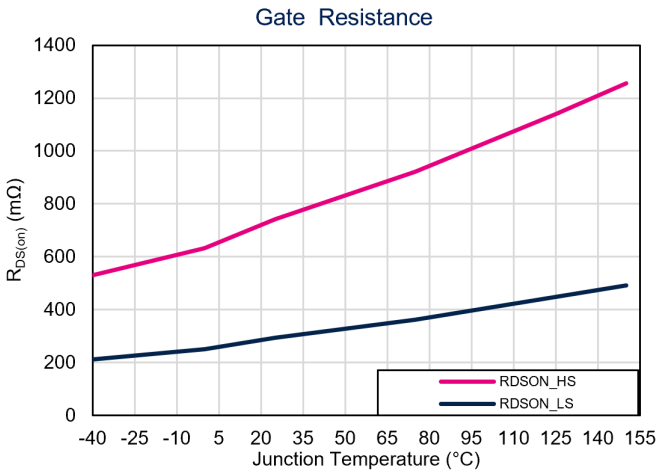


Figure 17. Gate resistance



7 Functional description

7.1 Overview

The DCP10001Y is an automotive-grade, monolithic step-down regulator qualified according to AEC-Q100 Grade 1, capable of delivering up to 1 A of load current. Its wide input-voltage range makes it suitable for a broad range of applications.

To support an input-voltage range of 6 V to 100 V, the DCP10001Y uses V^2COT compensation. This architecture combines the fast transient response of Constant-On-Time (COT) control with the ripple behavior of fixed-frequency PWM control.

With a 0.8 V internal reference, the device regulates output voltages from 1.5 V to 30 V with an output-voltage accuracy of ±1.5% over line, load, and temperature variations.

The DCP10001Y integrates low-$R_{DS(on)}$ N-channel MOSFETs, typically 300 mΩ on the low side and 750 mΩ on the high side, to improve full-load efficiency. Frequency dithering is enabled to reduce EMI.

A single resistor connected to RON and GND sets the on-time and switching frequency, ranging from 100 kHz to 1 MHz. In light-load conditions, SLEEP mode reduces quiescent current to 14 µA. Transitions between SLEEP, DCM, and CCM are designed to maintain stable output regulation.

The EN pin provides simple power sequencing. When EN is low, the device enters shutdown and reduces VIN bias current to less than 1 µA typical.

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1. Internal block overview

The main internal components, as illustrated in the block diagram in Figure 1, include:

- Power section: Comprising high-side and low-side power MOSFETs, gate driver, and current sensing.
- Control loop blocks: Featuring an error amplifier.
- T_{ON} block generator: Programs the switching frequency from 100 kHz to 1 MHz.
- Enable circuit: Includes soft-start management and a reset output signal for sequencing programming.
- Low drop-out linear regulator (LDO): Converts input voltage into V_{CC} for internal operation.
- Fault management: Provides protection against overcurrent (OCP), overvoltage (OVP), and overtemperature (OTP).

7.2 Power section

The DCP10001Y integrates N-channel power MOSFETs for synchronous switching operation. The high-side (HS) MOSFET is optimized for fast switching, while the low-side (LS) MOSFET uses a low $R_{DS(on)}$ to improve conversion efficiency. Together, the power stage supports up to 1 A of continuous output current over an input-voltage range up to 100 V.

The HS MOSFET drain is internally connected to VIN, and the LS MOSFET source is connected to GND. The HS MOSFET source and LS MOSFET drain are connected to the SW pin.

To reduce losses, the device implements anti-shoot-through and adaptive dead-time control to limit LS body-diode conduction. It also includes cross-conduction protection to reduce gate stress.

The HS MOSFET is driven through an internal bootstrap circuit, requiring only an external 100 nF capacitor between BST and SW. The bootstrap capacitor is recharged during LS on-time.

A minimum off-time (TOFF,MIN) ensures proper bootstrap recharge. In deep-sleep mode, the LS MOSFET is turned on only to recharge the bootstrap capacitor.

An internal linear regulator from VIN provides a nominal 4.7 V at VCC to supply the gate drivers, control logic, and internal circuitry. A 1 µF capacitor is recommended at VCC for stability. The VCC voltage may drop during sleep mode.

7.3 Enable pin (EN) functionality

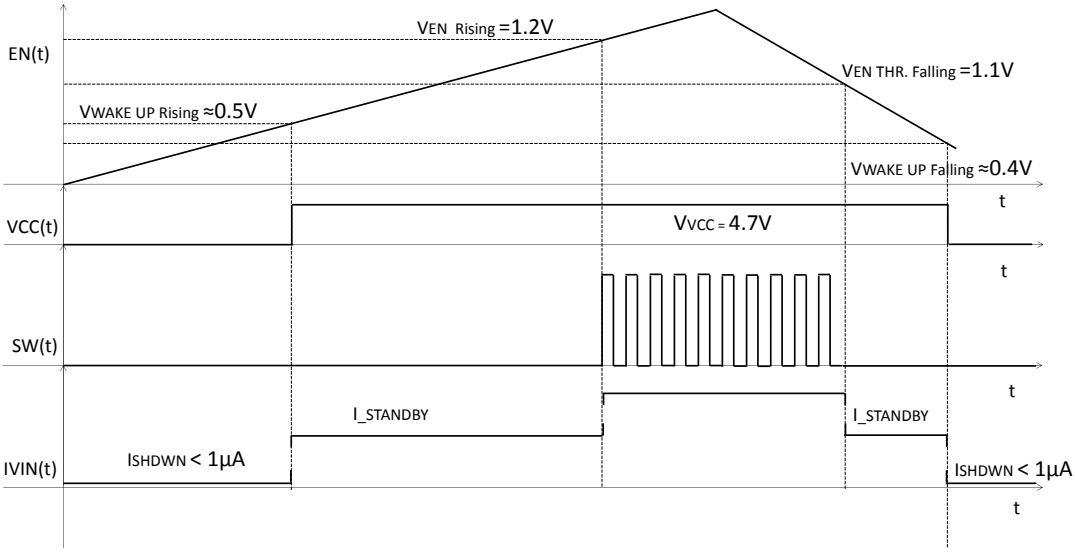
The EN pin is a digital input used to turn the device on or off. When the EN pin is held low, the input current is limited to approximately 1 µA.

To optimize EN threshold accuracy and current consumption, the device employs two distinct thresholds:

- Wake up threshold ($V_{sd-uvlo}$) Typ = 0.5 V
- START_UP threshold ($V_{en-uvlo}$) Typ = 1.2 V

The following diagram illustrates the described behavior:

Figure 18. Enable power up/down



• If the voltage on the EN pin is below the Vsd-uvlo threshold, the internal circuitry is disabled to ensure very low power consumption in the off state (ioff<1 µA).

• Once the EN pin voltage exceeds the Vsd-uvlo rising threshold, the device powers up the internal circuits, increasing current consumption.

• When the voltage surpasses the Ven-uvlo rising threshold, the device initiates switching activity as detailed in the Soft-start Section 7.4).

If the EN pin voltage falls below the Ven-uvlo rising threshold but stays above the Vsd-uvlo falling threshold, the device stops switching but keeps its internal blocks powered. Only when the voltage falls below the Vsd-uvlo falling threshold, does the device shut-down internal circuits, reducing current consumption to the off state level (ioff<1 µA).

The enable pin is VIN-compatible, allowing direct connection to the VIN pin if unused. A voltage divider can be designed on VIN to select the turn-on/off threshold for the startup sequence. See Section 8.2 for more details.

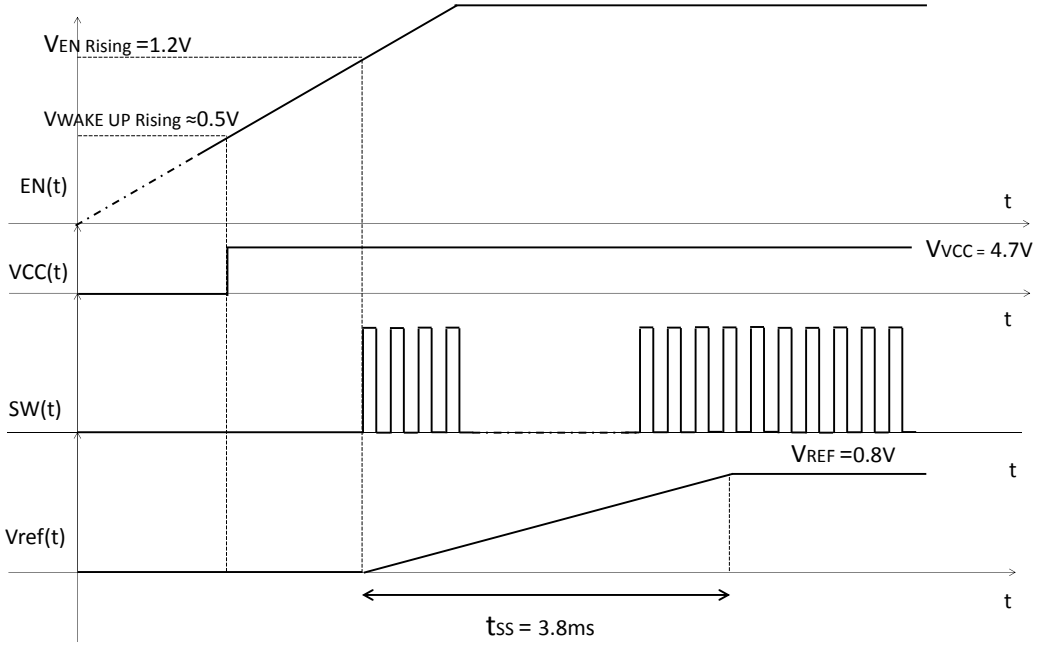
7.4 Soft-start

The device implements a soft-start sequence with a 3.8 ms start-up delay. During this phase, the FB pin voltage ramps toward the 0.8 V internal reference in small increments, minimizing inrush current and stress on external components.

Soft-start ends when FB reaches the reference voltage. During the ramp, T_{ON} is gradually limited to reduce output-voltage overshoot, which is common in COT architectures. All protection features remain active, and OCP is limited during the initial portion of the ramp (<100 mV) to prevent excessive inrush current.

Figure 19 illustrates the soft-start sequence. Once V_{EN} reaches its rising threshold, switching begins and the error amplifier voltage increases linearly to the reference level.

Figure 19. **Soft-start procedure**



If an unexpected event disables the device during normal operation, the DCP10001Y initiates a new soft-start cycle to restore normal operation. This occurs in the following cases:

- Thermal shutdown event
- UVLO (Undervoltage lockout)
- EN pin voltage rising above the V_{EN} threshold

7.5 Undervoltage lockout

When V_{IN} exceeds the V_{IN_UVLO} threshold, the internal blocks are enabled and current begins charging the VCC capacitor. Once V_{CC} rises above the V_{CC_UVLO} threshold, the device is ready to turn on and waits for the Power-On Reset (POR) signal from the EN pin.

The device continuously monitors V_{CC} for an undervoltage lockout (UVLO) condition. If the UVLO condition persists for more than 10 µs, the internal logic resets the device by turning off both the LS and HS MOSFETs.

After reset, if EN remains high, the device reinitiates the soft-start sequence.

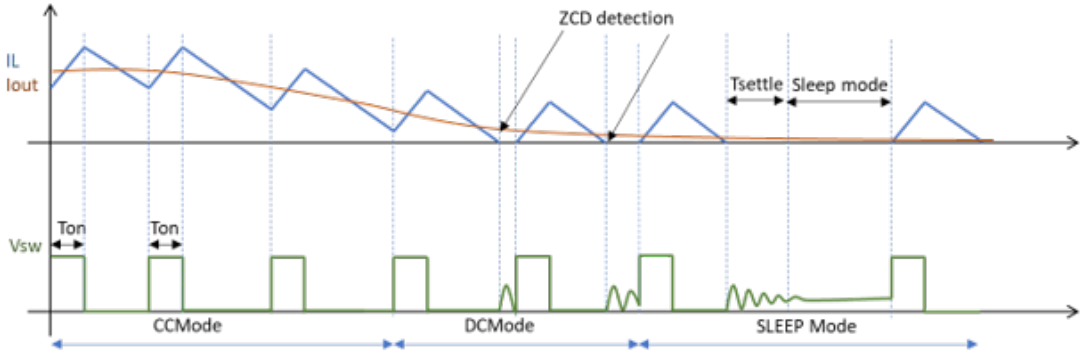
7.6 Device operating modes

When V_{IN} exceeds the UVLO threshold and EN is above the enable threshold, the device enters operating mode and initiates the soft-start sequence, as described in Section 7.4.

After soft-start, V_{OUT} is regulated in three operating modes:

- **CCM**: Fixed-frequency operation when the load current exceeds one-half of the inductor peak-to-peak ripple current.
- **DCM**: When the ZCD comparator is triggered, the LS switch turns off to prevent inductor current reversal and reduce power loss. In this mode, also referred to as diode emulation, the switching frequency may drop below the CCM frequency set by R_RON.
- **SLEEP**: If high impedance persists for longer than T_{SETTLE} (12 µs typ.), the device enters sleep mode. In this state, I_Q decreases to 14 µA typ., improving light-load efficiency. Internal control blocks are disabled to minimize current consumption. The device exits sleep mode rapidly when the control loop requests a new T_{ON}, limiting output-voltage drop.
- **OCP**: When I_{OUT} exceeds the maximum limit and I_{MIN} surpasses I_{VLY} (see the OCP section), V_{OUT} regulation may be compromised.

Figure 20. **ZCD detection**



Another operating zone is reached when I_{OUT} exceeds the maximum limit and I_{MIN} surpasses I_{VLY} (see Section 7.9.2: Overcurrent protection (OCP)). In this situation, V_{OUT} regulation may be compromised.

7.7 On-time generator (F_{SW})

Selecting the switching frequency requires a tradeoff between efficiency and component size. Lower frequencies reduce MOSFET switching losses, but require larger inductors and capacitors to maintain low output-voltage ripple.

In the DCP10001Y, the switching frequency is determined by T_{ON} in the COT architecture. T_ON is set by a resistor from R_{RON} to GND. The RON circuit generates a V_{IN}-feed forward on-time (Equation 1), keeping T_{ON} constant across the input-voltage range. The CCM switching frequency can then be estimated using Eq. (2)

$$T_{ON}\left(\mu s\right) = \frac{R_{RON}(k\Omega)}{2 \cdot V_{IN}(V)} \quad (1)$$

$$R_{RON}\left(k\Omega\right) = V_{OUT}\left(V\right) \cdot \frac{2000}{F_{SW}(kHz)} \quad (2)$$

The DCP10001Y operates with a minimum T_{ON} (high-side MOSFET on-time). If the programmed T_{ON} is below T_{ON_MIN}, the device maintains T_{ON_MIN}, which extends the switching period to achieve the required duty cycle (V_{OUT}/V_{IN}). As a result, F_{SW} may be lower than the value calculated using Eq. (2), and output-voltage ripple may increase.

This condition typically occurs during V_{IN} line transients. Equation 3 can be used to estimate the maximum V_{IN} before the switching frequency begins to decrease.

$$V_{IN_MAX}\left(V\right) = \frac{V_{OUT}(V)}{T_{ON_MIN}(ms) \cdot F_{SW}(kHz)} \quad (3)$$

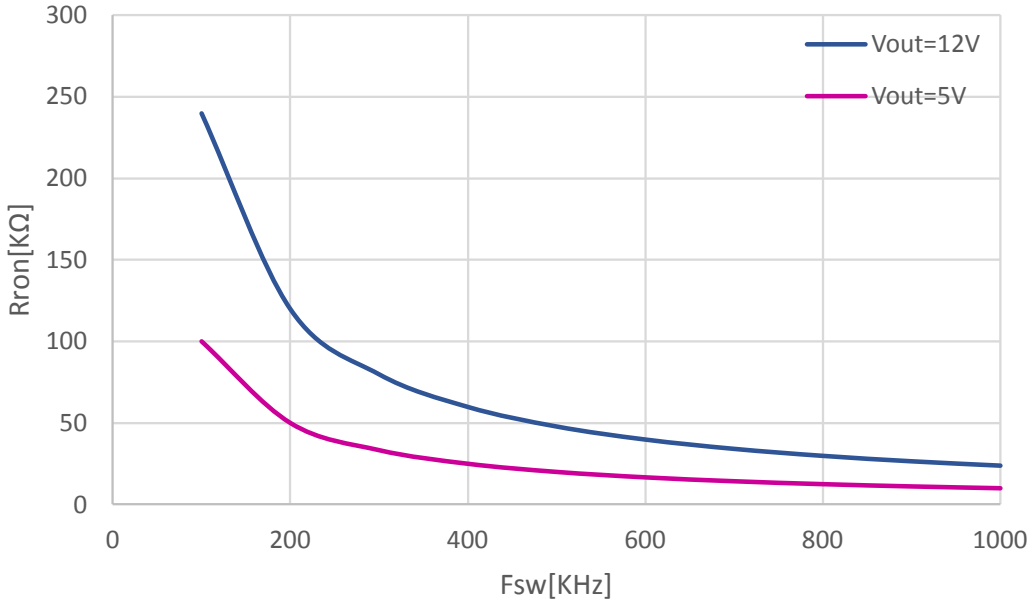
The DCP10001Y is typically set between 100 kHz and 1 MHz.

As described above, the switching frequency depends on V_{OUT} and R_{RON}, but this is true only to a first approximation. Since the loop is a Constant-On-Time (COT) architecture, losses are also considered in the recovery of the switching period (T_{SW}). Consequently, an increase in frequency with the output current is observed. The function that describes this dependency is detailed in Eq. (4).

$$F_{SW} = \frac{1}{T_{ON} \cdot \left(1 + \frac{V_{IN} - I_{OUT} \cdot R_{HS} - I_{OUT} \cdot DCR - V_{OUT}}{V_{OUT} + I_{OUT} \cdot R_{LS} + I_{OUT} \cdot DCR}\right)} \quad (4)$$

It is recommended to select an inductor with low **DCR** to minimize the impact of switching-frequency variation versus output current, especially in low-**V_{OUT}** applications, where the current dependence is more pronounced.

Figure 21. **Frequency setting**



7.8 Dithering

To reduce the cost of the input EMI filter, the DCP10001Y uses spread-spectrum dithering by default. This function is implemented by modulating T_{ON}. The ramp current of the on-time generator is varied within a defined percentage of its nominal value according to a fixed modulation pattern. As a result, F_{SW} may vary by ±6 % with a 11 kHz modulation frequency.

The variation of F_{SW} affects the compensation ramp (see Eq. (5)), and so the V_{OUT} ripple (see Eq. (6)).

For this reason, the output exhibits an extra ripple caused by the dithering.

$$\Delta Vramp = Vramp \cdot \left(e^{-\frac{1}{\tau \cdot 1.06 \cdot Fsw}} - e^{-\frac{1}{\tau \cdot 0.94 \cdot Fsw}} \right) \quad (5)$$

Where V_{RAMP} = 9 0 mV, t = 3.6 ns and F_{SW} is the F_{SW} set with R_{RON}.

$$\Delta Vout_{Dith} = V_{outProg}/Vref \cdot \Delta Vramp \quad (6)$$

The overall V_{OUT} ripple is composed by contribution of $\Delta V_{OUT_dithering}$ and ΔV_{OUT_COUT} (see Section 8.4)

For EMI compliance, it is recommended to set the switching frequency in the middle of the 300 kHz to 530 kHz range, where the CISPR 25 limits are less restrictive.

7.9 Protections

The DCP10001Y includes multiple protection features to prevent damage and ensure reliable operation. It responds to excessive output voltage or current by activating overvoltage protection (OVP) or overcurrent protection (OCP). Negative current protection (NCP) is enabled only when negative current is allowed, such as during OVP. If an excessive temperature is detected during operation, overtemperature protection (OTP) is triggered to protect the device.

7.9.1 Overvoltage protection (OVP)

The device implements overvoltage protection (OVP) to safeguard the load from excessive voltage levels. If V_{OUT} exceeds 120% of the selected V_{OUT}, the device detects an overvoltage fault and activates the low-side MOSFET to protect the load circuitry. The device is capable of sinking current only after an OVP event.

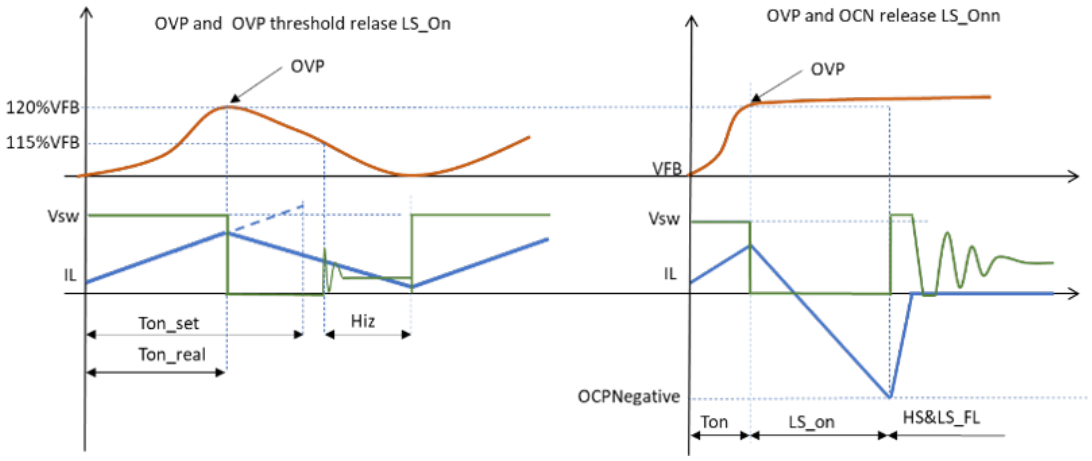
The low-side MOSFET is turned off when one of the following events is triggered:

- The negative current limit is reached (see negative current limit; Figure 22)
- V_{OUT}out reaches the lower OVP limit (115%) (Figure 22)
- An OTP event occurs

This protection is active from the soft-start phase until the device is turned off.

Overvoltage protection is a secondary-level protection and should not be triggered under normal operating conditions if the system is properly designed. In other words, the selection of external power components and the dynamic performance defined by the compensation network should ensure output voltage regulation below the overvoltage threshold, even in worst-case load transition scenarios. The protection is reliable and can operate during normal load transitions for systems whose dynamic performance does not align with the dynamic load requirements. Consequently, output voltage regulation may be affected.

Figure 22. Overvoltage protection



7.9.2 Overcurrent protection (OCP)

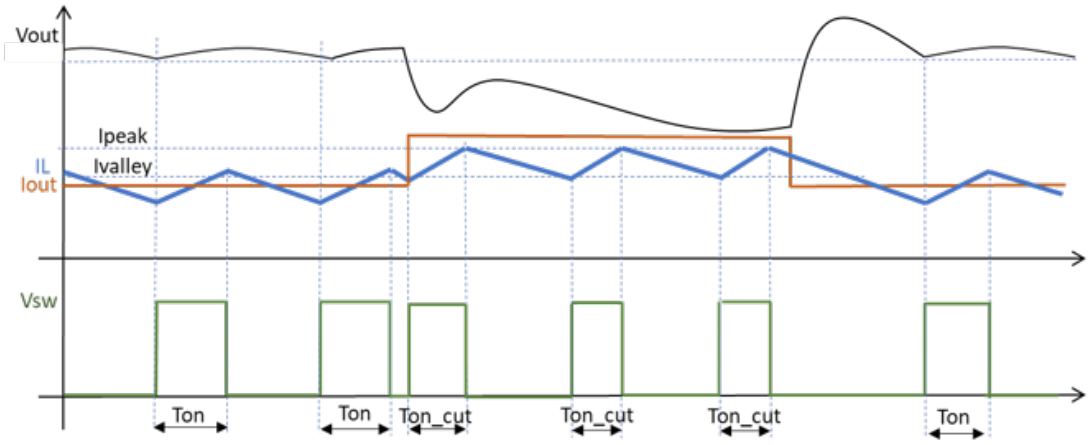
The DCP10001Y features pulse-by-pulse current sensing on both power stages (high-side and low-side MOSFETs) to provide effective current protection across the duty-cycle range. High-side current sensing is referred to as the peak current limit (I_{LIM}), while low-side current sensing is referred to as the valley current limit (I_{VLY}).

During T_{ON}, if the high-side current exceeds I_{LIM}, the HS MOSFET turns off before T_{ON} expires, and the LS MOSFET turns on to allow the inductor current to decrease.

During T_{OFF}, the current is monitored through the LS MOSFET. If the current remains above I_{VLY}, the device ignores any new T_{ON} requests and keeps the LS MOSFET on until the current falls below the valley current limit. Only then can the HS MOSFET turn on again.

This overcurrent protection scheme keeps the current between $\mathbf{I_{VLY}}$ and $\mathbf{I_{LIM}}$ during persistent overcurrent conditions, such as an output short-circuit, reducing device dissipation and preventing overheating. If the fault persists and dissipation remains excessive, **OTP** provides the next level of protection.

Figure 23. **Overcurrent protection**



7.9.3 Negative current protection (NCP)

The device includes negative current protection. In a typical buck configuration, it is not intended to sink current, and when the current becomes negative, Zero Current Detection (ZCD) prevents reverse current flow. However, the device allows current sinking during overvoltage protection (OVP). In this condition, if the current exceeds the negative current threshold, the device disables LS conduction, leaving the switching node floating (see Figure 23).

7.9.4 Thermal shutdown

The shutdown circuitry disables switching when the junction temperature exceeds 175 °C (see T_{SHDWN} in Section 5) to prevent further power dissipation and temperature rise. The thermal-sensing element is located near the power components to ensure rapid and accurate temperature detection. After a thermal protection event, the DCP10001Y restarts with the soft-start sequence. OTP is non-latching, allowing the device to cycle in and out of thermal shutdown if the fault persists. A hysteresis of approximately 20 °C prevents rapid on/off cycling.

8 Application Details

8.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity, a pulsed current flows into the input capacitor and therefore, its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depend on the electrical series resistance (ESR) value of the capacitors. Thus, low ESR capacitors (like multilayer ceramic capacitors) are usually selected thanks to their higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and thus contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS}=\left(\frac{I_{OUT_sec}}{N}\right)\cdot\sqrt{\left(1-\frac{D}{\eta}\right)\cdot\frac{D}{\eta}} \quad (7)$$

Where I_{OUT} is the maximum DC output current, D is the duty cycle, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_{OUT}/2$. In a specific application, the range of possible duty cycles has to be considered in order to find the maximum RMS input current. The maximum and minimum duty cycles can be calculated as

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INmin} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (8)$$

$$D_{min} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (9)$$

Where $\Delta V_{HIGHSIDE}$ and $\Delta V_{LOWSIDE}$ are the voltage drops across the embedded switches. The peak-to-peak voltage across the input filter can be calculated as

$$V_{PP} = \frac{I_{OUT}}{C_{IN}\cdot F_{SW}}\cdot\left(1-\frac{D}{\eta}\right)\cdot\frac{D}{\eta} + ESR\cdot(I_{OUT} + \Delta I_L) \quad (10)$$

In case of negligible ESR (MLCC capacitor), the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

$$C_{IN} = \frac{I_{OUT}}{V_{PP}\cdot F_{SW}}\cdot\left(1-\frac{D}{\eta}\right)\cdot\frac{D}{\eta} \quad (11)$$

Considering η = 1, this function has its maximum in D = 0.5:

$$C_{INmin} = \frac{I_{OUT}}{4\cdot V_{PPMAX}\cdot F_{SW}} \quad (12)$$

Typically, C_{IN} is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 5% V_{INMAX}.

Using a C_{IN} > 2.2 µF is suggested for a high-frequency range. The C_{IN} used must be of at least X7R quality. Consider the real C_{IN} voltage at V_{INMAX} using the manufacturing derating.

Check the layout guidelines section for the best C_{IN} placement on the board.

8.2 Enable power-up/down thresholds

The DCP10001Y EN pin is designed with two enable threshold levels. See Section 7.3.

The enable threshold for the system start-up and switch-off has been designed with a 100 mV hysteresis to guarantee good noise immunity and a programmable start-up.

The VIN start-up can be easily programmed connecting a voltage divider to the EN pin between VIN pin and GND.

The enable rising threshold is equal to 1.2 V. (refer to table Section 5).

The power-up threshold is adjusted according to the formula reported in Eq. (13).

$$V_{POWER_UP} = 1.2 \cdot \left(1 + \frac{R_{EN_H}}{R_{EN_L}}\right) \quad (13)$$

The enable falling threshold is equal to 1.1 V (refer to Section 5).

The turn-off threshold is obtained according to the formula reported in Eq. (14) :

$$V_{POWER_DOWN} = 1.1 \cdot \left(1 + \frac{R_{EN_H}}{R_{EN_L}}\right) \quad (14)$$

If the EN pin is not used, it can be connected directly to the VIN pin. In this case the device will start up/switch off once V_{IN} reaches/falls below $V_{IN\text{-}UVLO}$.

To maximize the overall system efficiency, it is suggested to use R_{EN_H} and R_{EN_L} between 10 kΩ and 1 MΩ.

8.3 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple. Usually, the inductor value is selected to keep the current ripple below 20% - 40% of the average output current over the input voltage range. The inductance value can be calculated be reverting Eq. (15).

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF} \quad (15)$$

Where T_{ON} and T_{OFF} are the on and off-time of the internal power switch. The maximum current ripple, at fixed V_{OUT}, is obtained at maximum T_{OFF} which is at the minimum duty cycle. So, fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated, as reported in Eq. (16) .

$$L_{min} = \frac{V_{OUT}}{\Delta IL_{MAX}} \cdot \frac{1 - D_{min}}{F_{SW}} \quad (16)$$

The peak current through the inductor is given by Eq. (17).

$$I_{L,PK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (17)$$

If the inductor value decreases, the peak current (which has to be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

It is recommended to select an inductor with a saturation current above the peak current limit.

8.4 Output capacitor selection

In the DCP10001Y, the V_{OUT} ripple is composed of two components:

- ΔV_{OUT}_Dith: the ripple generated by dithering (Section 7.8)
- ΔV_{OUT}_Cout: the ripple generated by dIL on C_{OUT}.

The value of C_{OUT} affects both components.

The ΔV_{OUT}_Cout depends mainly on the value of C_{OUT} and its ESR, as expressed by Eq. (18)
Eq. (18):

$$\Delta V_{OUT} = ESR \cdot \Delta I_{L,MAX} + \frac{\Delta I_{L,MAX}}{8 \cdot C_{OUT} \cdot F_{SW}} \quad (18)$$

For a multi-layer ceramic capacitor (MLCC), the capacitive component of the ripple dominates the resistive one, while the opposite is true for an electrolytic capacitor. Neglecting the ESR contribution, the minimum value of the output capacitor is given by Eq. (19):

$$C_{OUT,min,RIPPLE} = \frac{\Delta I_{L,MAX}}{8 \cdot \Delta V_{OUT} \cdot F_{SW}} \quad (19)$$

In V^{2}COT systems, ΔVOUT_COUT is critical for system stability. If the ripple is too low, the system may become unstable during V^{2}COT operation. Typically, when ΔVOUT_COUT is below 4 mV, increased jitter and multiple pulses in DCM may be observed. To avoid this issue, an external circuit can be added to increase the ripple on the FB pin using two capacitors and one resistor.

On the other hand, using too small a capacitance increases the ripple, but it also raises the risk of undershoot during transients and may trigger OVP during load release. A good compromise is to select C_{OUT} so that ΔVOUT_COUT is approximately 10 mV. The voltage ripple can be calculated using Eq. (18).

When selecting C_{OUT}, also consider the voltage derating of the capacitor.

8.5 Output voltage setting

The error amplifier reference voltage (V_{REF}) is 0.8 V typical (refer to Section 5). The output voltage is decreased though an external divider and compared with the internal reference. With the external divider, it is possible to adjust the radio of V_{OUT} as shown in Eq. (20):

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R_{UP}}{R_{DW}}\right) \quad (20)$$

High R_{UP} increases the efficiency at light loads, but the feedback can be more susceptible to noise. Therefore, R_{UP} should be selected within a range of 40 kΩ and 100 kΩ, R_{DW} is selected as consequence of V_{OUT} selected following Eq. (21):

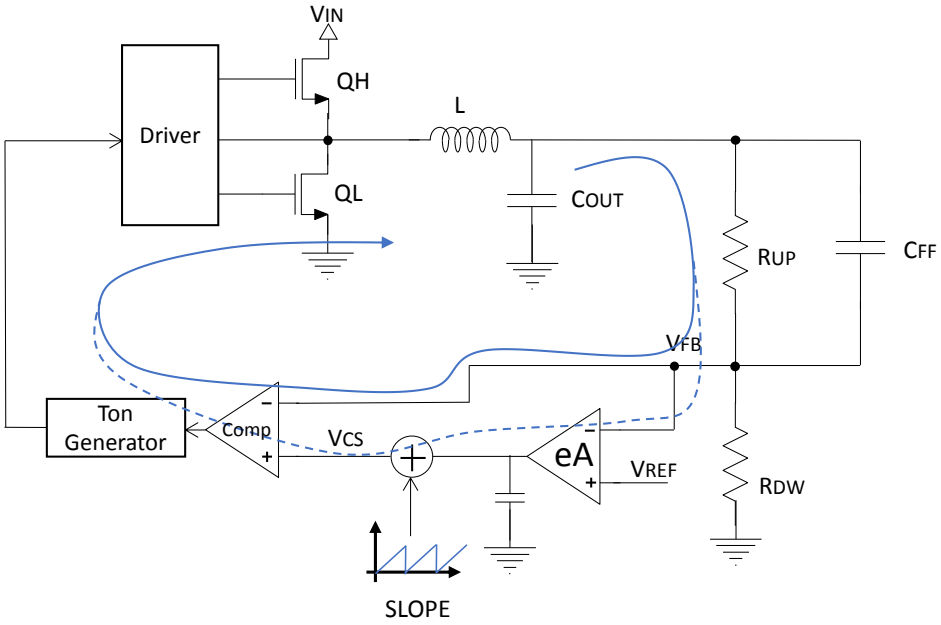
$$R_{DW} = R_{UP} \cdot \frac{0.8\,V}{V_{OUT} - 0.8\,V} \quad (21)$$

8.6 Compensation network

The DCP10001Y is based on a V^{2}COT control loop which combines the advantage of a COT loop (fast response with load transient) with the advantage of frequency clock loops.

The main structure of the loop is shown in Figure 24.

Figure 24. V²COT loop



The V²COT is composed of double feedback paths:

• Dotted line loop: A compensator with high DC gain and low bandwidth is put on the slow feedback path to improve accuracy performances. A slope during the time period is added to the compensator output node to ensure stability also in low ESR conditions (using the MLCC case).

• Linear line loop: fast loop. The V_{OUT} variation is sensed directly on the comparator with a fast response. As a result, the load transient the system behaves like a COT system loop.

The PWM comparator matches the error amplifier output node with the feedback voltage to generate the main PWM request. Once the V_{FB} goes below the error amplifier voltage (V_{CS}), a T_{ON} pulse is turned on.

Figure 25. V²COT waveforms

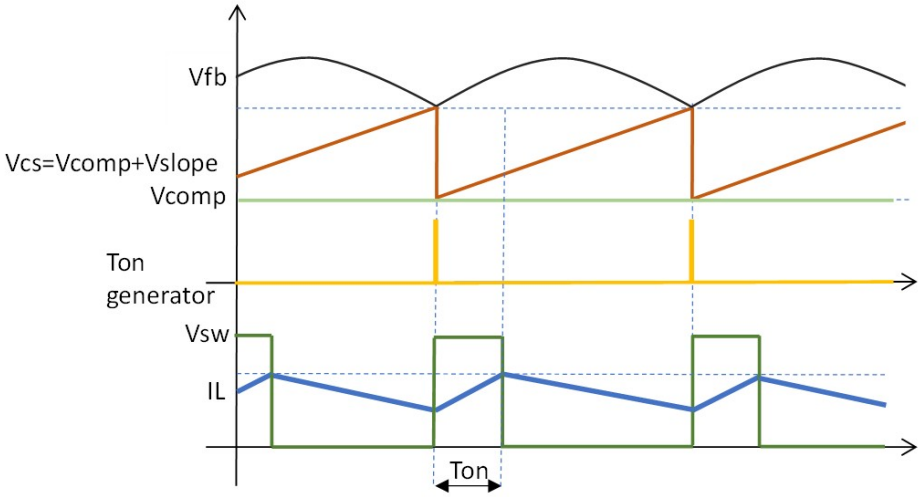
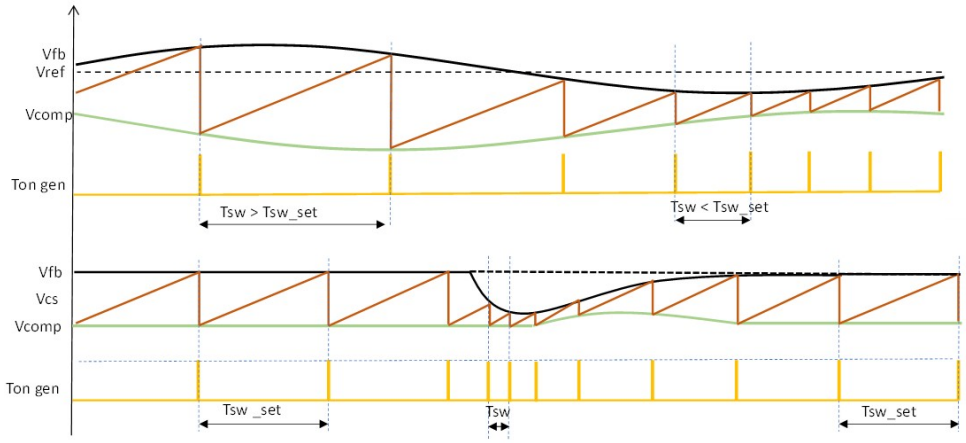


Figure 26 shows an example of system response of the two loops:

Example 1: V_{OUT} changes slowly (< bandwidth of dotted line loop) and therefore V_{FB}, partition of V_{OUT}, follows the same behavior. Embedded V_{COMP} follows with the integral signal of the error amplifier inverting input. Once V_{FB} is above the reference V_{REF}, the V_{COMP} pulse sawtooth signal (V_{CS}) needs more time to reach the V_{FB} value and F_{SW} decreases. Vice versa, when V_{FB} is below the reference the V_{CS} signal needs less time to reach V_{FB} value and F_{SW} is higher than F_{SW} set.

Example 2: Once V_{OUT} drops immediately, like in load transient event, the V_{COMP} is not able to follow the abrupt V_{OUT} transition in a short time. However, V_{CS} reaches the V_{FB} faster and F_{SW} increases quickly to avoid an extra V_{OUT} drop. In this case, the system behaves like a normal COT.

Figure 26. V_{OUT} variation example



C_{FF} capacitance is used to improve the stability condition and to inject an extra ripple on the feedback node, bypassing the effect of the resistor divider.

The C_{FF} suggested to best match the bandwidth (of the slow loop) and phase margin is calculated by Eq. (22):

$$C_{FF}=\frac{5\cdot\sqrt{V_{OUT}/V_{REF}}}{2\cdot\pi\cdot R_{UP}\cdot F_{SW}} \quad (22)$$

It is recommended to use a C_{FF} > 10 pF.

ST provides (on the ST web eDesignSuite) a proprietary tool to design and tailor any applications, and eDSim, an online simulation tool based on SIMetrix SIMPLIS to evaluate start-up, stability and load/line transient of the system.

8.7 Thermal considerations

The thermal design is important in order to prevent thermal shutdown of the device if the junction temperature goes above 175 °C. The three different sources of losses within the device are:

A. Conduction losses due to the on resistance of the high-side switch (R_{DSON_HS}) and low side switch (R_{DSON_LS}); these are equal to:

$$P_{COND} = R_{DSON_HS}\cdot I_{OUT}^2\cdot D + R_{DSON_LS}\cdot I_{OUT}^2\cdot\left(1-D\right) \quad (23)$$

Where D is the duty cycle of the selected application and is given by:

$$D = \frac{V_{OUT}+\left(R_{DSON_LS}+DCRl\right)\cdot I_{OUT}}{V_{IN}-\left(R_{DSON_{HS}}-R_{DSON_LS}\right)\cdot I_{OUT}} \quad (24)$$

In order to obtain a more accurate estimation, it is necessary to take into account that the amount of resistance of the internal power MOSFET increases with the temperature. For this reason, the value of R_{DSONHS} and R_{DSONLS}, should be increased, typically, by a factor equal to 15%.

B. Switching losses due to high-side Power MOSFET turn ON and OFF; these can be calculated as

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} \quad (25)$$

Where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high-side power switch (VDS) and the current flowing into it during the turn ON and turn OFF phases.

T_{SW} is the equivalent switching time. For this device, the typical value for the equivalent switching time is 20 ns.

C. Quiescent current losses, calculated as:

$$P_Q = V_{IN} \cdot I_{SB,MAX} \quad (26)$$

Where I_{SB} is the quiescent current out of sleep and it is given by:

$$I_{Q,MAX} = 0.4[mA] \quad (27)$$

The power losses are given by:

$$P_{LOSS} = P_{COND} + P_{SW} + P_Q \quad (28)$$

The junction temperature T_J can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS} \quad (29)$$

Where T_A is the ambient temperature. R_{thJA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from junction to ambient. For this device, the exposed pad provides the primary thermal path for dissipating heat.

The measured R_{thJA} under JEDEC conditions is typically approximately 32 °C/W. However, on the application board, this value may vary depending on copper thickness, layout, and available board area. For example, the STEVAL-10001Y12V board, which uses a 2-layer PCB with 2 oz copper on both top and bottom layers, reports a R_{thJA} of 28 °C/W. In applications with limited space, R_{thJA} may increase further; therefore, the layout should be optimized to achieve the best thermal performance.

8.8 Layout considerations

The PCB layout of the switching DCDC regulators minimizes the noise injected in high-impedance nodes and interference generated by the high-current switching loops.

In a step-down converter, the input loop (including the input capacitor, the DC-DC regulator and ground connection) is the most critical one due to high-value pulsed current flowing through it. In order to minimize the EMI, this loop must be as short as possible with an adequate input capacitor placed very close to the DCP10001Y's VIN and GND pins (pin 2 and pin 1).

The feedback pin (FB) connection to the external resistor divider is a high-impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high-current paths. To reduce the pick-up noise, the resistor divider must be placed very close to the device.

Thanks to the exposed pad of the device, the ground plane helps to reduce the injection of ambient thermal resistance. Six vias on the exposed pad are suggested for an adequate connection to the bottom layer, which helps to reduce the ambient thermal resistance. A wide ground plane enhances the thermal performance of the converter, allowing high-power conversion.

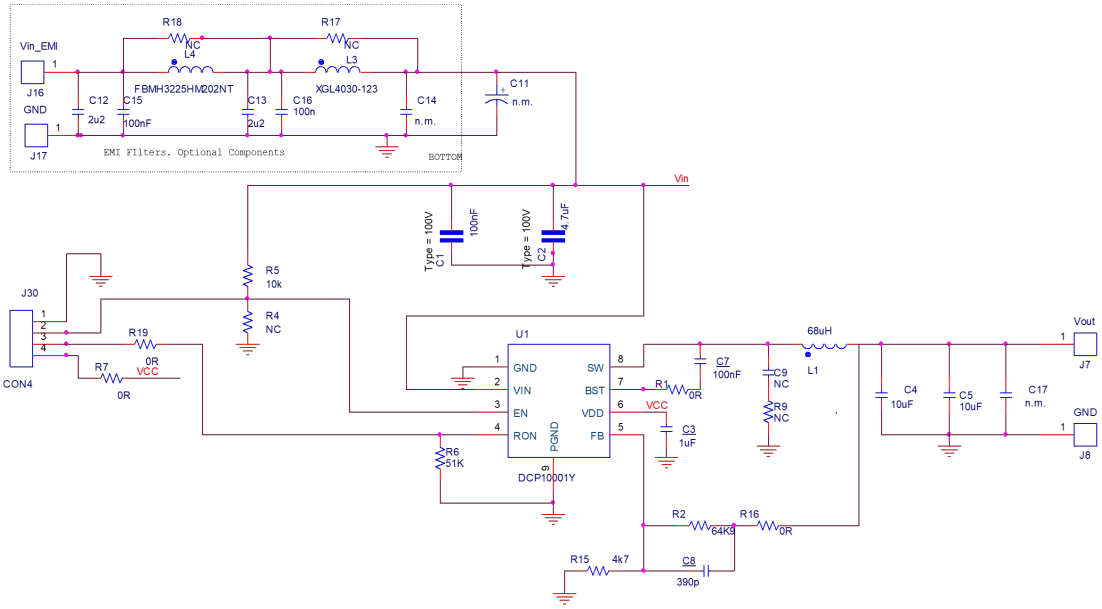
Refer to the Section 9.2: Layout evaluation board for an example of a PCB layout.

9 Application demoboard

For further information, consult the STEVAL10001Y12V user manual.

9.1 Schematic

Figure 27. **Schematic**



9.2 Layout

Figure 28. **Top view**

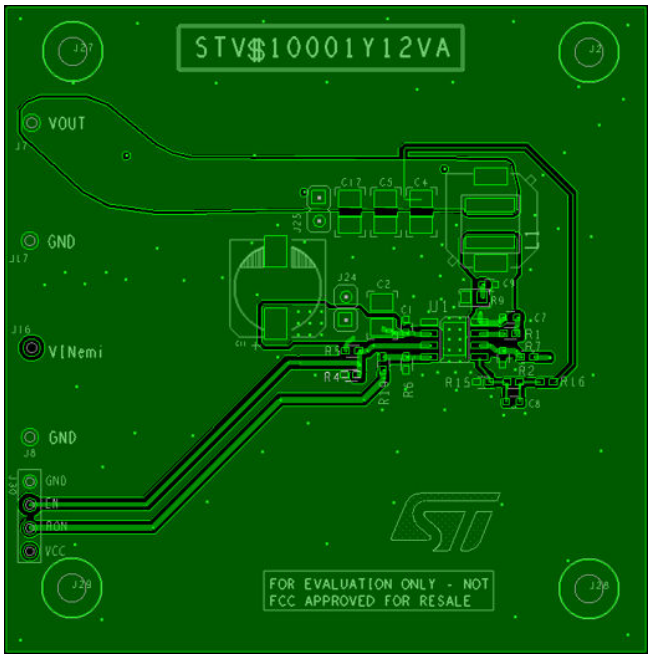
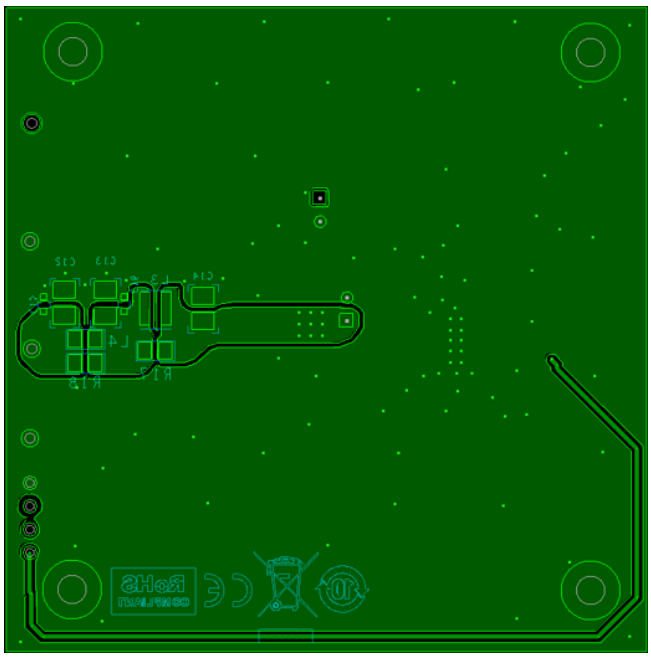


Figure 29. **Bottom view**



9.3 Application board curves

Figure 30. No_load

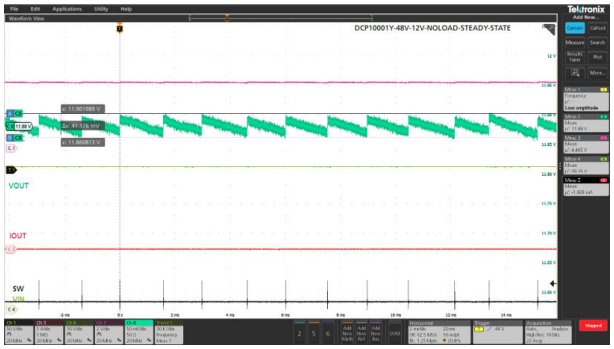


Figure 31. No_load_zoom

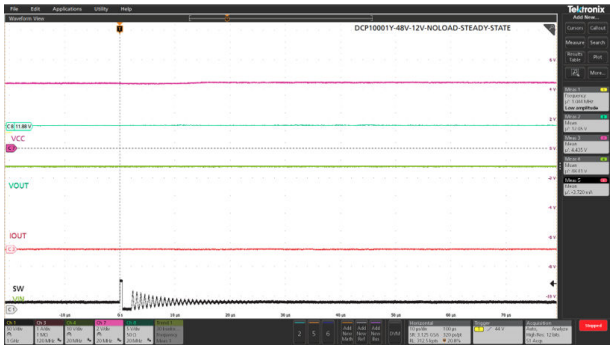


Figure 32. Full_load (1A)

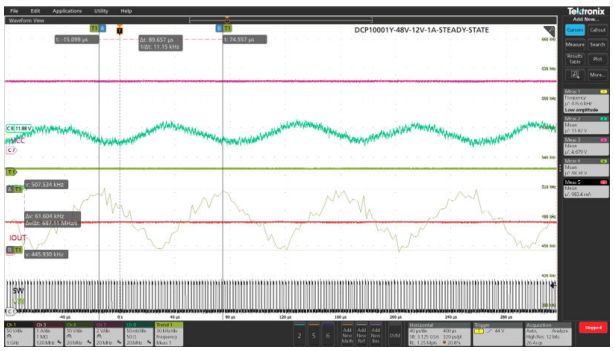


Figure 33. Load transient 0.2A to 1A_2A/us

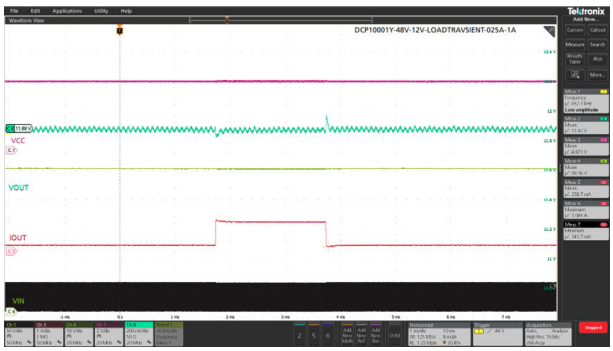


Figure 34. Vin start up no load

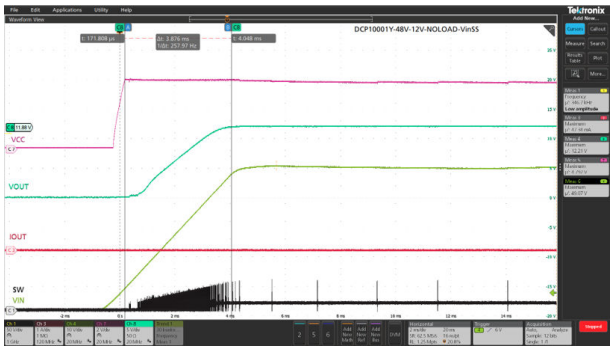


Figure 35. Vin start up full load (12 Ohm)

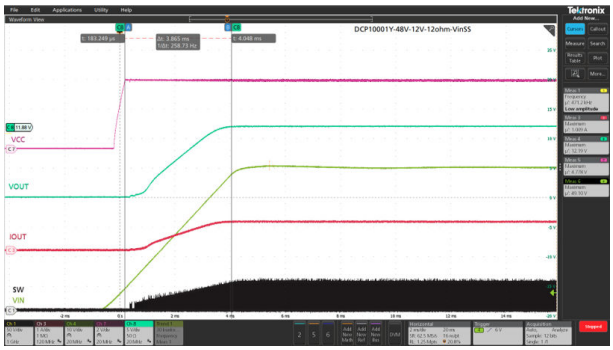


Figure 36. EN On/Off/ no load

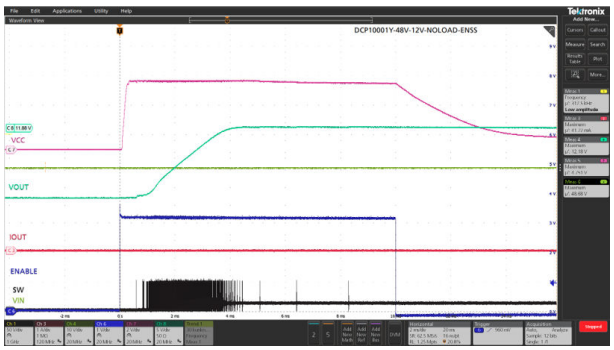


Figure 37. EN On/Off Full Load (12 Ohm)

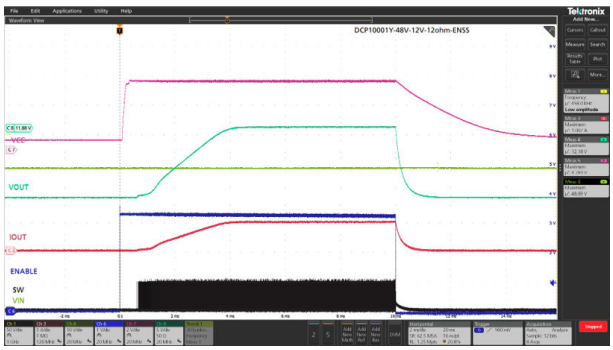


Figure 38. En on prebias start up

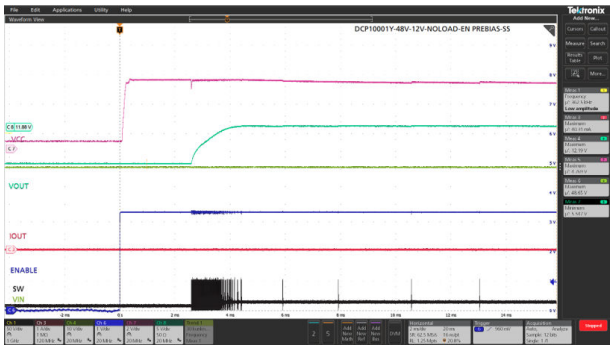


Figure 39. Vout short @start up

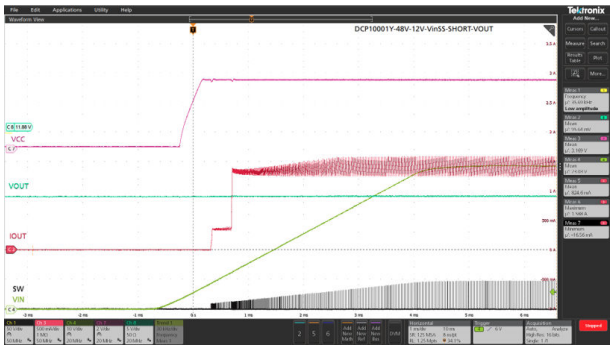


Figure 40. Vout short enter

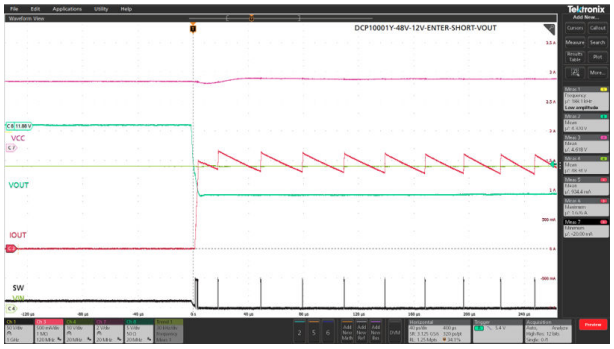
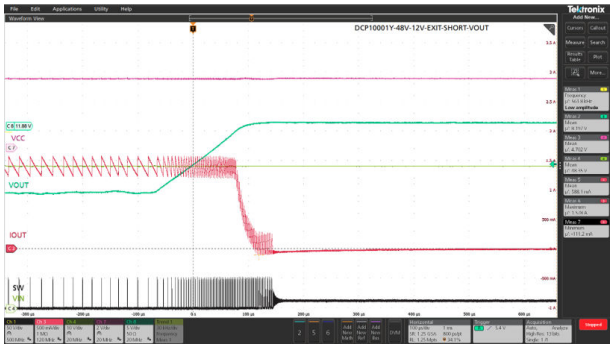


Figure 41. Vout short exit



9.4 Application curves application

Figure 42. Efficiency V_{OUT} = 12 V @ 450 KHz linear

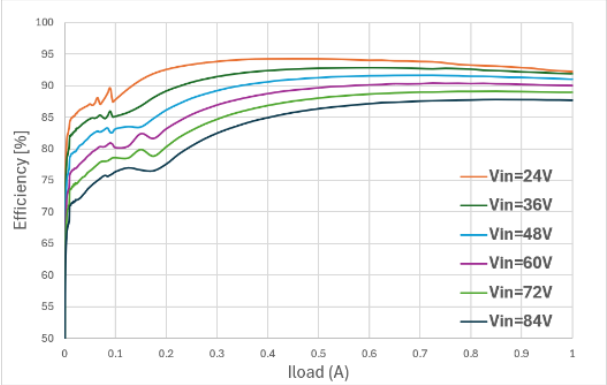
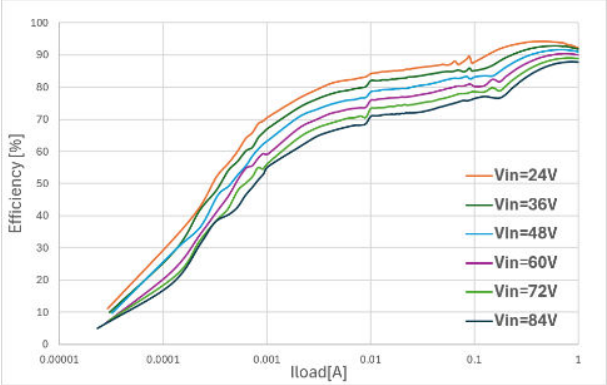


Figure 43. Efficiency V_{OUT}=12V @ 450 KHz logarithmic



9.5 Typical application example

In this session, the main application parameter for the typical application for 3 different switching frequencies is suggested:

- 100 kHz: high-efficiency applications
- 400 kHz: EMI optimized applications
- 1000 kHz: High-frequency applications

Figure 44. Typical schematic

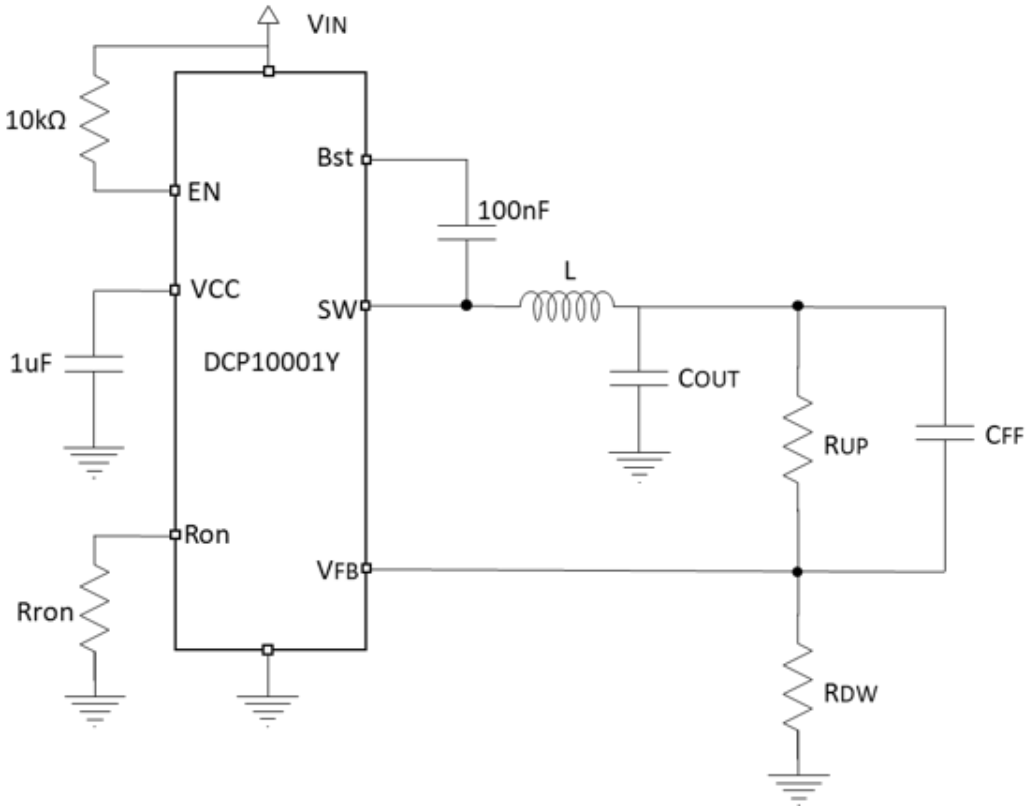


Table 8. **Typical application values for 1 A version**

FSW (kHz)	VIN (V)	VOUT (V)	Rron (k)	L (uH)	Cout (uF)	Rup (Kohm)	Rdwc (Kohm)	Cff (uF)
100	72	24	470	390	47	46.4	1.6	2500
100	72	12	240	330	47	51.1	3.65	1000
100	72	5	100	150	47	105	20	270
100	48	12	240	330	47	51.1	3.65	1000
100	48	5	100	150	47	105	20	220
100	48	3.3	68	100	47	27	8.66	560
100	24	12	240	330	47	51.1	3.65	1000
100	24	5	100	120	47	105	20	220
100	24	3.3	68	100	47	27	8.66	680
400	72	24	120	100	22	46.4	1.6	820
400	72	12	62	82	22	51.1	3.65	620
400	72	5	24.9	33	22	105	20	120
400	48	12	62	68	22	51.1	3.65	560
400	48	5	24.5	33	22	105	20	120
400	48	3.3	17	22	22	27	8.66	270
400	24	12	62	47	22	51.1	3.65	470
400	24	5	24.9	33	22	105	20	120
400	24	3.3	17	22	22	27	8.66	270
1000	72	24	51	68	10	46.4	1.6	470
1000	72	12	26.1	33	10	51.1	3.65	220
1000	72	5	11	15	10	105	20	47
1000	48	12	26.1	33	10	51.1	3.65	220
1000	48	5	11	15	10	105	20	47
1000	48	3.3	7.5	10	10	27	8.66	120
1000	24	12	26.1	22	10	51.1	3.65	180
1000	24	5	11	15	10	105	20	47
1000	24	3.3	7.5	10	10	27	8.66	120

Table 9. **Typical application values for 0.7 A version**

FSW (kHz)	VIN (V)	VOUT (V)	Rron (k)	L (uH)	Cout (uF)	Rup (Kohm)	Rdw (Kohm)	Cup (uF)
100	72	24	470	470	47	46.4	1.6	2200
100	72	12	240	330	47	51.1	3.65	2200
100	72	5	100	150	47	105	20	270
100	48	12	240	330	47	51.1	3.65	1000
100	48	5	100	150	47	105	20	220
100	48	3.3	68	100	47	27	8.66	560
100	24	12	240	330	47	51.1	3.65	1000
100	24	5	100	220	47	105	20	220
100	24	3.3	68	100	47	27	8.66	680

FSW (kHz)	VIN (V)	VOUT (V)	Rron (k)	L (uH)	Cout (uF)	Rup (Kohm)	Rdw (Kohm)	Cup (uF)
400	72	24	120	150	10	46.4	1.6	820
400	72	12	62	100	10	51.1	3.65	390
400	72	5	24.9	47	10	105	20	100
400	48	12	62	100	10	51.1	3.65	390
400	48	5	24.9	47	10	105	20	100
400	48	3.3	17	33	10	27	8.66	220
400	24	12	62	68	10	51.1	3.65	330
400	24	5	24.9	47	10	105	20	100
400	24	3.3	17	33	10	27	8.66	220
1000	72	24	51	68	10	46.4	1.6	470
1000	72	12	26.1	47	10	51.1	3.65	220
1000	72	5	11	22	10	105	20	56
1000	48	12	26.1	33	10	51.1	3.65	220
1000	48	5	11	22	10	105	20	56
1000	48	3.3	7.5	15	10	27	8.66	120
1000	24	12	26.1	22	10	51.1	3.65	180
1000	24	5	11	22	10	105	20	56
1000	24	3.3	7.5	15	10	27	8.66	150

Table 10. Typical application values for 0.5 A version

FSW (kHz)	VIN (V)	VOUT (V)	Rron (k)	L (uH)	Cout (uF)	Rup (Kohm)	Rdw (Kohm)	Cup (uF)
100	72	24	470	750	47	46.4	1.6	2200
100	72	12	240	470	47	51.1	3.65	1200
100	72	5	100	270	47	105	20	330
100	48	12	240	470	47	51.1	3.65	1000
100	48	5	100	220	47	105	20	330
100	48	3.3	68	180	47	27	8.66	820
100	24	12	240	330	47	51.1	3.65	1000
100	24	5	100	120	47	105	20	270
100	24	3.3	68	150	47	27	8.66	820
400	72	24	120	220	10	46.4	1.6	820
400	72	12	62	150	10	51.1	3.65	560
400	72	5	24.9	68	10	105	20	100
400	48	12	62	120	10	51.1	3.65	470
400	48	5	24.9	56	10	105	20	100
400	48	3.3	17	47	10	27	8.66	270
400	24	12	62	120	10	51.1	3.65	470
400	24	5	24.9	47	10	105	20	100
400	24	3.3	17	47	10	27	8.66	270
1000	72	24	120	220	10	46.4	1.6	470
1000	72	12	26.1	68	10	51.1	3.65	270

FSW (kHz)	VIN (V)	VOUT (V)	Rron (k)	L (uH)	Cout (uF)	Rup (Kohm)	Rdw (Kohm)	Cup (uF)
1000	72	5	11	22	10	105	20	56
1000	48	12	26.1	56	10	51.1	3.65	220
1000	48	5	11	33	10	105	20	68
1000	48	3.3	7.5	22	10	27	8.66	180
1000	24	12	26.1	33	10	51.1	3.65	220
1000	24	5	11	22	10	105	20	56
1000	24	3.3	7.5	47	10	27	8.66	180

Note:

- The Rron values are selected to get a typical Fsw at full load.
- The L values are chosen considering Iripple as 30%-40% of Imax.
- Using the EDesign tool gives a broader view of the application's characteristics

10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 HSOP8 package information

Figure 45. HSOP8 package outline BOTTOM View

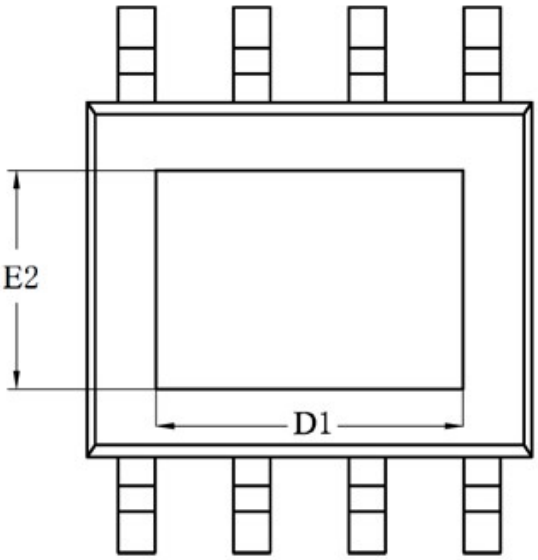


Figure 46. HSOP8 Package outline SIDE View

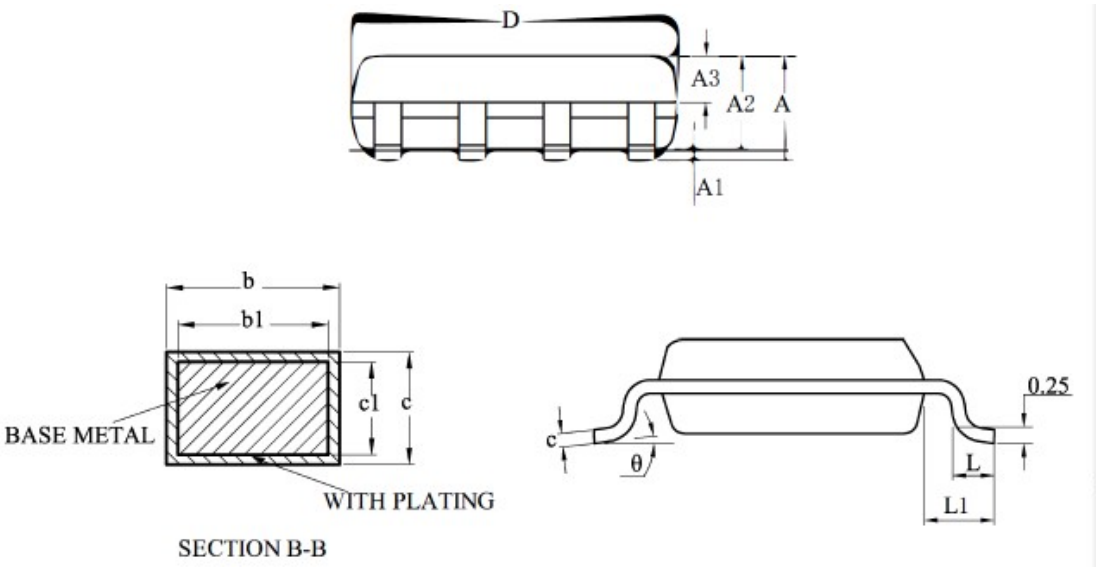


Figure 47. **HSOP8 Package outline TOP View**

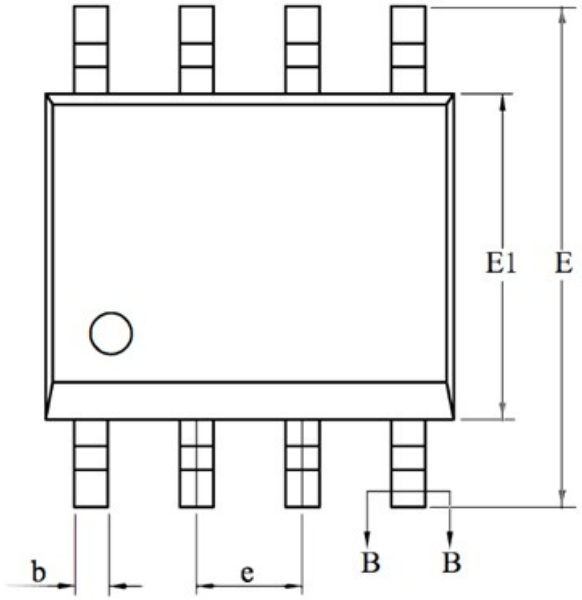
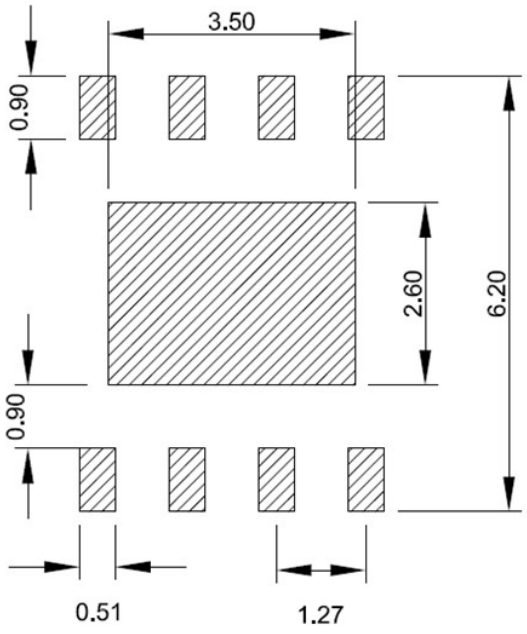


Table 11. **HSOP8 package mechanical data**

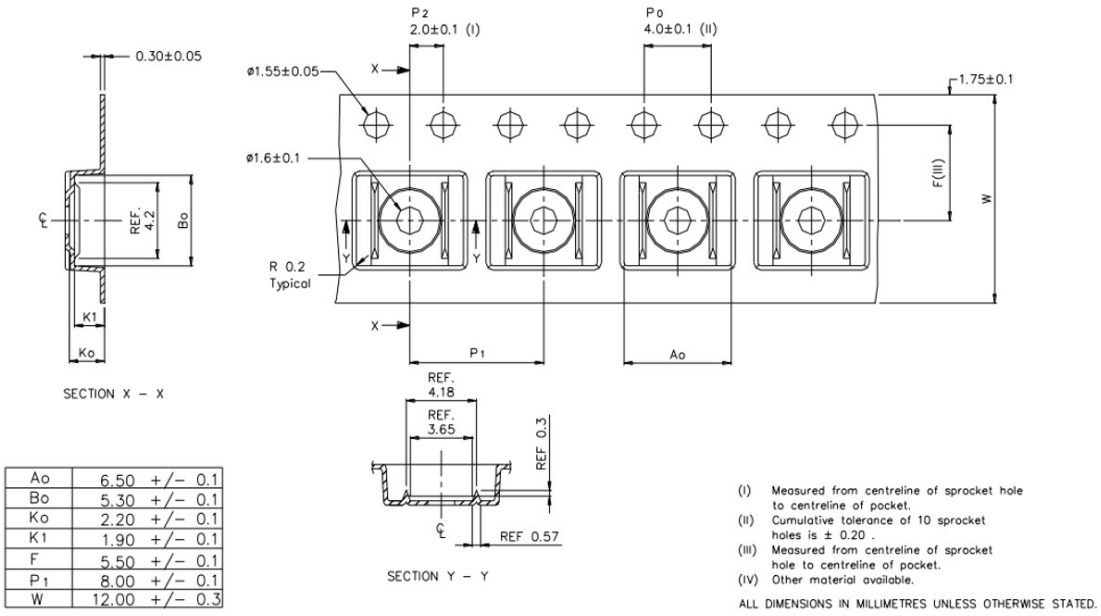
Dim.	mm		
	Min.	Typ.	Max.
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
B1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
D1		3.1 REF	
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
h	0.25	-	0.50
L	0.50	0.60	0.80
L1		1.05REF	
O	0	-	8°

Figure 48. **HSOP8 Recommended Footprint (Dimensions in mm)**



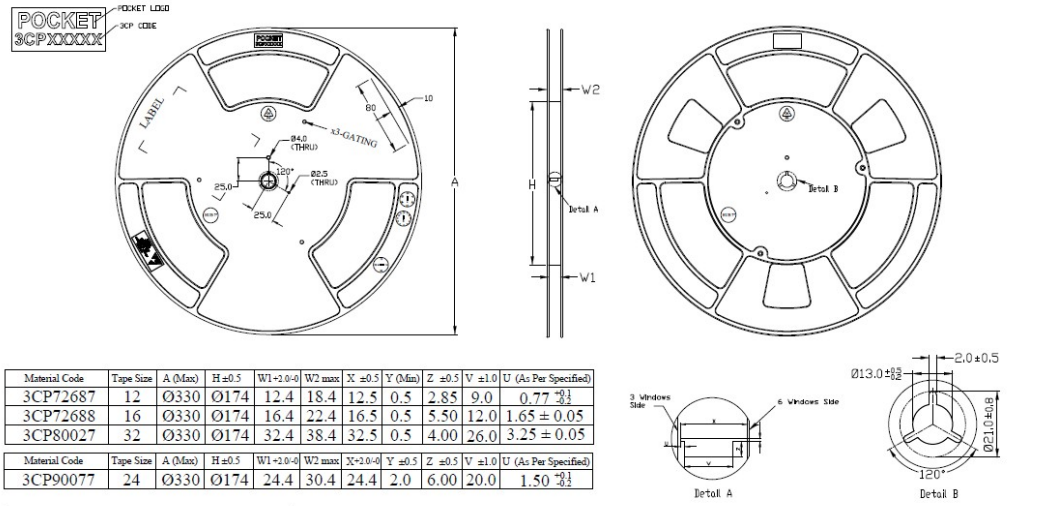
10.2 Package information

Figure 49. **Carrier type**



Ao	6.50 +/– 0.1
Bo	5.30 +/– 0.1
Ko	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 50. **Plastic reel**



Material Code	Tape Size	A (Max)	H ±0.5	W1 +2.0/-0	W2 max	X ±0.5	Y (Min)	Z ±0.5	V ±1.0	U (As Per Specified)
3CP72687	12	Ø330	Ø174	12.4	18.4	12.5	0.5	2.85	9.0	$0.77^{+0.1}_{-0.2}$
3CP72688	16	Ø330	Ø174	16.4	22.4	16.5	0.5	5.50	12.0	1.65 ± 0.05
3CP80027	32	Ø330	Ø174	32.4	38.4	32.5	0.5	4.00	26.0	3.25 ± 0.05

Material Code	Tape Size	A (Max)	H ±0.5	W1 +2.0/-0	W2 max	X +2.0/-0	Y ±0.5	Z ±0.5	V ±1.0	U (As Per Specified)
3CP90077	24	Ø330	Ø174	24.4	30.4	24.4	2.0	6.00	20.0	$1.50^{+0.1}_{-0.2}$

SURFACE RESISTIVITY		
LEGEND	TYPE	SR RANGE (ohms/sq)
C	CONDUCTIVE	$< 10^{5}$
A	ANTISTATIC	10^{5-11}
S	STANDARD	$=> 10^{12}$

Notes :

1. General Draft To Be : 0.5°
2. Corner and Edge Radius to be : 0.50 mm
3. All Edged To Be Free From Flash.

REV	DESCRIPTION	BY	DATE
A	Initial release	SURIA	09/07/2024

TITLE: WELDED REEL (13X7)
ST MUAR

POCKET PACKAGING SDN.BHD.

DRAWN: SURIA
APPROVED: KELVIN
DATE: 09/07/2024
DATE: 09/07/2024
PLR PART NO.: PLR-B-AS-13x7x12-FR
CUST PART NO.: 3CP72687
MATERIAL: PS
SCALE: 2 : 1

GEN. TOL.	METRIC
X.X	±0.25mm
X.XX	±0.13mm

11 Ordering Information

Table 12. **Order codes**

P/N	Package	Vout	Grade	Marking	Max current
DCP10001PHRY	HSOP 8L	ADJ	Automotive	BC01Y	1 A
DCP100D7PHRY	HSOP 8L	ADJ	Automotive	BCD7Y	0.7 A
DCP100D5PHRY	HSOP 8L	ADJ	Automotive	BCD5Y	0.5 A

Revision history

Table 13. **Revision history**

Date	Revision	Changes
16-Oct-2026	1	Initial release.

Contents

1 **Diagram** 2
2 **Pin configuration** 3
3 **Typical application circuit** 4
4 **Maximum ratings** 5
5 **Electrical characteristics** 6
6 **Typical characteristics** 8
7 **Functional description** 11
7.1 Overview 11
7.2 Power section 11
7.3 Enable pin (EN) functionality 11
7.4 Soft-start 12
7.5 Undervoltage lockout 13
7.6 Device operating modes 13
7.7 On-time generator (F_{SW}) 14
7.8 Dithering 15
7.9 Protections 15
7.9.1 Overvoltage protection (OVP) 16
7.9.2 Overcurrent protection (OCP) 16
7.9.3 Negative current protection (NCP) 17
7.9.4 Thermal shutdown 17
8 **Application Details** 18
8.1 Input capacitor selection 18
8.2 Enable power-up/down thresholds 19
8.3 Inductor selection 19
8.4 Output capacitor selection 20
8.5 Output voltage setting 20
8.6 Compensation network 20
8.7 Thermal considerations 22
8.8 Layout considerations 23
9 **Application demoboard** 24
9.1 Schematic 24
9.2 Layout 24
9.3 Application board curves 25
9.4 Application curves application 27

9.5 Typical application example 27
10 Package information 31
10.1 HSOP8 package information 31
10.2 Package information 33
11 Ordering Information 35
Revision history 36

List of tables

Table 1. Pin description . . . 3
Table 2. Typical application components 48 V_12 V_400 kHz . . . 4
Table 3. Absolute maximum ratings . . . 5
Table 4. Thermal data . . . 5
Table 5. ESD performance . . . 5
Table 6. Recommended operating conditions . . . 5
Table 7. Electrical characteristics . . . 6
Table 8. Typical application values for 1 A version . . . 28
Table 9. Typical application values for 0.7 A version . . . 28
Table 10. Typical application values for 0.5 A version . . . 29
Table 11. HSOP8 package mechanical data . . . 32
Table 12. Order codes . . . 35
Table 13. Revision history . . . 36

List of figures

Figure 1. Block diagram . . . 2
Figure 2. Pin connection (top view) . . . 3
Figure 3. Typical application circuit . . . 4
Figure 4. Efficiency V_{OUT} = 12 V @ 450KHz linear . . . 8
Figure 5. Efficiency V_{OUT} = 12 V @ 450 kHz logarithmic . . . 8
Figure 6. Shutdown current @ V_{IN} = 24V . . . 8
Figure 7. Shutdown current @ T_{amb} . . . 8
Figure 8. I_QUIESCENT @ V_{in} = 48V . . . 8
Figure 9. Feedback voltage regulation threshold . . . 8
Figure 10. Internal VCC regulation . . . 9
Figure 11. Peak and valley current @ 1 A . . . 9
Figure 12. Minimum T_{ON} and T_{OFF} . . . 9
Figure 13. T_{ON} setting . . . 9
Figure 14. Input voltage thresholds . . . 10
Figure 15. Bootstrap thresholds . . . 10
Figure 16. Enable thresholds . . . 10
Figure 17. Gate resistance . . . 10
Figure 18. Enable power up/down . . . 12
Figure 19. Soft-start procedure . . . 13
Figure 20. ZCD detection . . . 14
Figure 21. Frequency setting . . . 15
Figure 22. Overvoltage protection . . . 16
Figure 23. Overcurrent protection . . . 17
Figure 24. V^2COT loop . . . 21
Figure 25. V^2COT waveforms . . . 21
Figure 26. V_{OUT} variation example . . . 22
Figure 27. Schematic . . . 24
Figure 28. Top view . . . 24
Figure 29. Bottom view . . . 24
Figure 30. No_load . . . 25
Figure 31. No_load_zoom . . . 25
Figure 32. Full_load (1A) . . . 25
Figure 33. Load transient 0.2A to 1A_2A/us . . . 25
Figure 34. Vin start up no load . . . 25
Figure 35. Vin start up full load (12 Ohm) . . . 25
Figure 36. EN On/Off/ no load . . . 26
Figure 37. EN On/Off Full Load (12 Ohm) . . . 26
Figure 38. En on prebias start up . . . 26
Figure 39. Vout short @start up . . . 26
Figure 40. Vout short enter . . . 26
Figure 41. Vout short exit . . . 26
Figure 42. Efficiency V_{OUT} = 12 V @ 450 KHz linear . . . 27
Figure 43. Efficiency V_{OUT}=12V @ 450 KHz logarithmic . . . 27
Figure 44. Typical schematic . . . 27
Figure 45. HSOP8 package outline BOTTOM View . . . 31
Figure 46. HSOP8 Package outline SIDE View . . . 31
Figure 47. HSOP8 Package outline TOP View . . . 32
Figure 48. HSOP8 Recommended Footprint (Dimensions in mm) . . . 33
Figure 49. Carrier type . . . 33
Figure 50. Plastic reel . . . 34

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