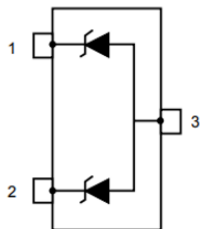


Automotive dual-line unidirectional ESD protection in SOT323



SOT 323-3L (Jedec SC-70)




Pin layout

Product status link

[ESDA5WY](#)

Features

- AEC-Q101 qualified 
- Dual-line unidirectional ESD and EOS protection
- Very low leakage current at V_{RM} ($I_R < 50$ nA)
- 175 W peak pulse power (8/20 μ s)
- High ESD protection level: up to 25 kV
- Fast turn-on and low clamping voltage
- Operating T_j max: 175 °C
- SOT 323-3L package
- ECOPACK2 RoHS compliant component
- Complies with the following standards:
 - J-STD-020 MSL level 1 and UL94, V0
 - IPC7531 footprint and JEDEC registered package
 - ISO 10605 - C = 150 pF, R = 330 Ω :
 - ± 30 kV (air discharge)
 - ± 25 kV (contact discharge)
 - ISO 10605 - C = 330 pF, R = 330 Ω :
 - ± 30 kV (air discharge)
 - ± 20 kV (contact discharge)
 - ISO 7637-3:
 - Pulse 3a : -150 V; pulse 3b : +150 V
 - Pulse 2a: +/- 85 V

Application

Low speed and DC automotive applications where electrostatic discharges and other transients must be suppressed such as:

- Microcontrollers and integrated circuit (SBC, DSP) low speed and power lines
- MOSFET gate protection
- Switches and buttons
- Audio lines
- I2C, SPI communication bus

Description

ESDA5WY, an automotive unidirectional transient voltage suppressor (TVS) has been designed for use in harsh environments to protect sensitive electronics from damage or latch-up due to electrical overstress (EOS), lightning surge and ESD without ageing effect and performance drifts.

It can therefore advantageously replace MOV (metal oxide varistor) or MLV (multi-layer varistor) as well as zener diodes, which are optimized for voltage regulation. It is the right choice for high reliability and quality systems.

In addition, this product is available in a small popular SOT323-3L (Jedec SC-70) with 2.1 mm x 2.0 mm footprint, ideal for space constrained applications.

1 Characteristics

1.1 Pin configuration and function

Table 1. ESDA5WY series pin description

Pin #	Type	Description
1	I/O1	ESD protection cathode 1
2	I/O2	ESD protection cathode 2
3	GND	Common anode

Figure 1. ESDA5WY series pinout (top view)


1.2 Absolute maximum ratings

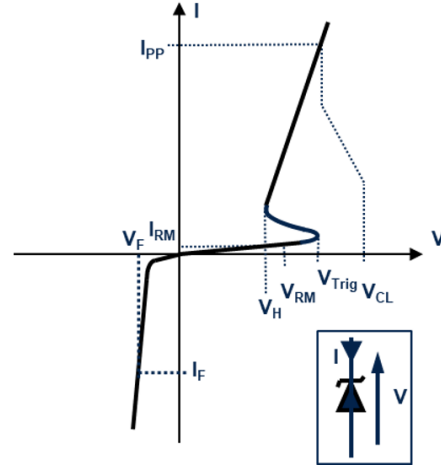
Table 2. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Value	Unit	
V_{ESD}	Electrostatic discharge	ISO 10605 - C = 150 pF, R = 330 Ω : Contact discharge	± 25	kV
		Air discharge	± 30	
	Electrostatic discharge	ISO 10605 - C = 330 pF, R = 330 Ω : Contact discharge	± 20	
		Air discharge	± 30	
P_{PP}	Peak pulse power	IEC 61000-4-5 (2 Ω) – $t_p = 8/20\ \mu\text{s}$	175	W
I_{PP}	Peak pulse current	IEC 61000-4-5 (2 Ω) – $t_p = 8/20\ \mu\text{s}$	12	A
T_j	Operating junction temperature range		-55 to +175	°C
T_{stg}	Storage temperature range		-65 to +175	
T_L	Maximum lead temperature for soldering during 10 s		260	

1.3 Electrical characteristics

Figure 2. Electrical characteristics (definitions)

V_{RM}	Stand-off voltage
I_{RM}	Leakage current @ V_{RM}
V_{TRIG}	Triggering voltage
V_H	Holding voltage
V_{CL}	Clamping voltage
I_{PP}	Peak pulse current
V_F	Forward voltage
I_F	Current at V_F
R_D	Dynamic resistance
C_L	Line capacitance


Table 3. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{RM}	Reverse stand-off voltage	Any I/O pin to GND			5.5	V
I_{RM}	Reverse leakage current at V_{RM}	$V_{RM} = 5.5\text{ V}$ Any I/O pin to GND		3	50	nA
V_{TRIG}	Triggering voltage	Higher voltage than V_{TRIG} guarantees the protection turn-on Any I/O pin to GND	6.0		10	V
V_H	Holding voltage	Lower voltage than V_H guarantees the protection turn-off Any I/O pin to GND	5.5			V
V_F	Forward voltage	$I_F = 200\text{ mA}$ GND to any I/O pin		1.05	1.2	V
$V_{CL}^{(1)}$	ESD clamping voltage	TLP measurement, $t_p = 100\text{ ns}$, $I_{PP} = 16\text{ A}$ Any I/O pin to GND		14.0		V
	EOS clamping voltage	IEC 61000-4-5 surge, $t_p = 8/20\text{ }\mu\text{s}$, $I_{PP} = 12\text{ A}$ Any I/O pin to GND			14.5	V
$R_d^{(1)}$	Dynamic resistance	8/20 μs waveform Any I/O pin to GND		0.59		Ω
$C_{I/O-GND}^{(1)}$	Line capacitance	$V_R = 0\text{ V}$, $F = 1\text{ MHz}$, $V_{OSC} = 30\text{ mV}$ Any I/O pin to GND		4.0	4.8	pF
$\alpha T^{(1)(2)}$	Temperature coefficient	Any I/O pin to GND			3.5	$10^{-4}/^{\circ}\text{C}$

1. Specified by design – Not tested in production.

2. $\Delta V_{BR} = \alpha T \times (T_{amb} - 25\text{ }^{\circ}\text{C}) \times V_{BR} (25\text{ }^{\circ}\text{C})$

1.4 Characteristics (curves)

Figure 3. Peak pulse current versus clamping voltage (8/20 μ s waveform)

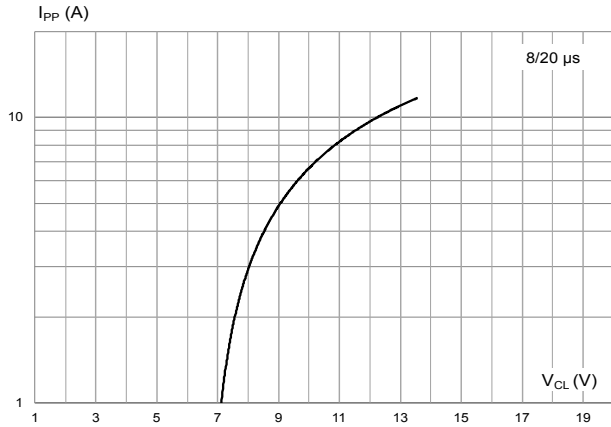


Figure 4. Peak forward current versus forward voltage drop (8/20 μ s waveform)

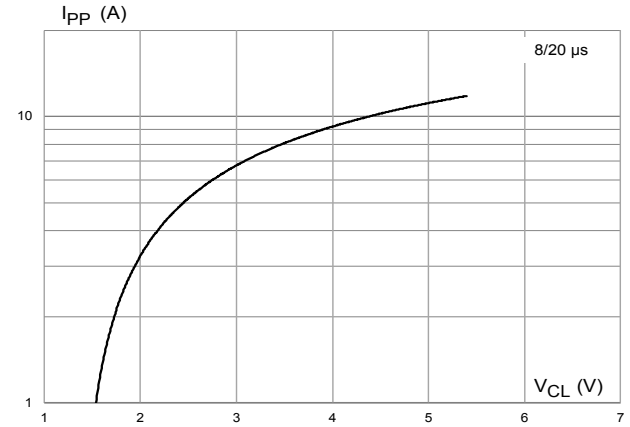


Figure 5. Junction capacitance versus reverse applied voltage

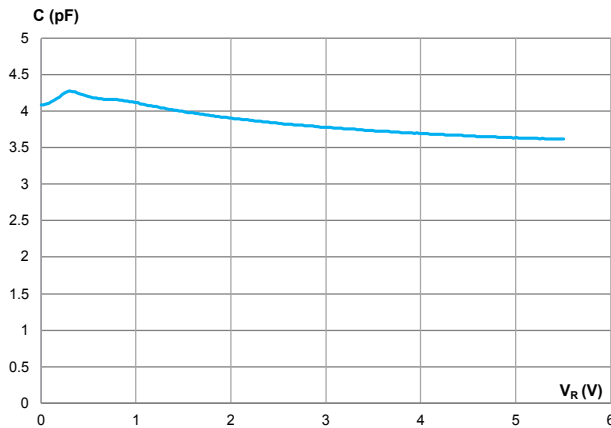


Figure 6. Leakage current versus junction temperature

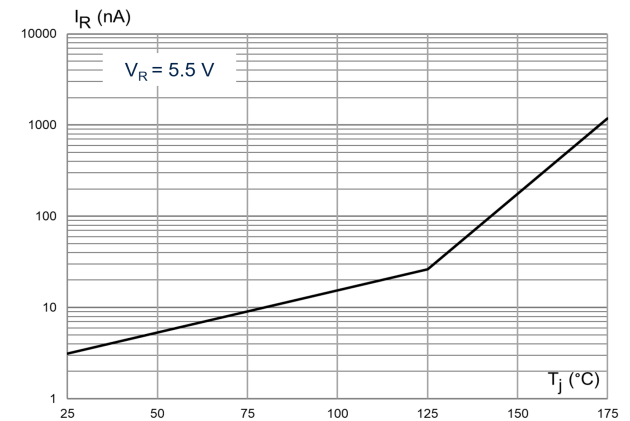


Figure 7. TLP characteristic

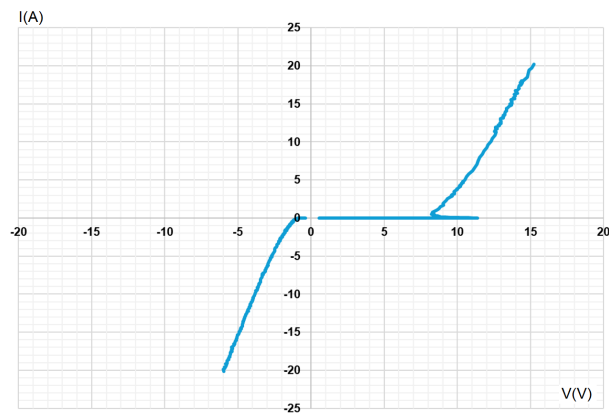


Figure 8. Reponse to ISO 10605 - C = 150 pF, R = 330 Ω (+8 kV contact)

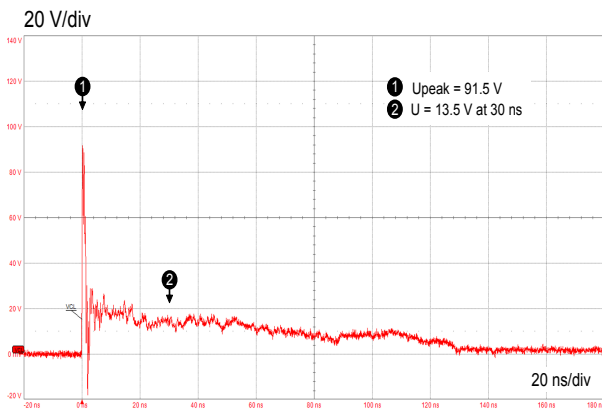


Figure 9. Reponse to ISO 10605 - C = 150 pF, R = 330 Ω (-8 kV contact)

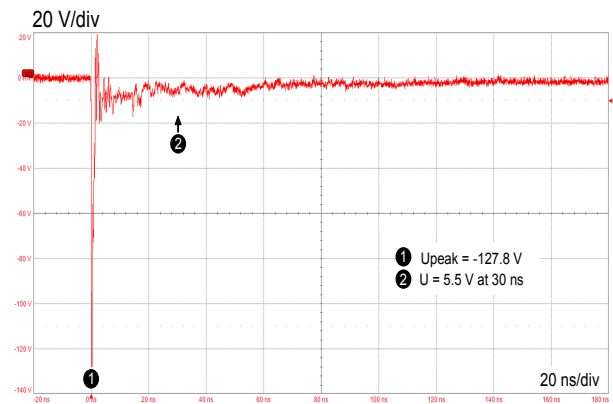


Figure 10. Response to ISO 7637-3 Pulse 3a: -150 V

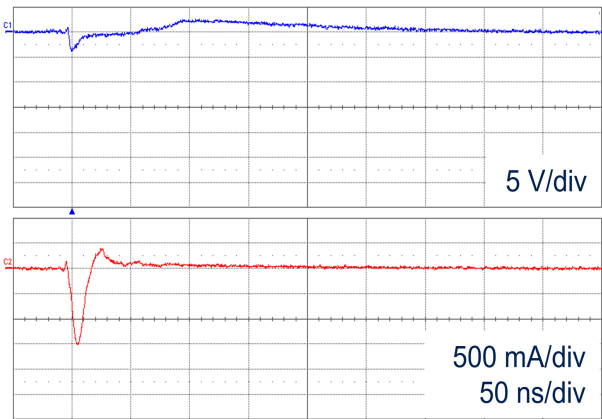


Figure 11. Response to ISO 7637-3 Pulse 3b: +150 V

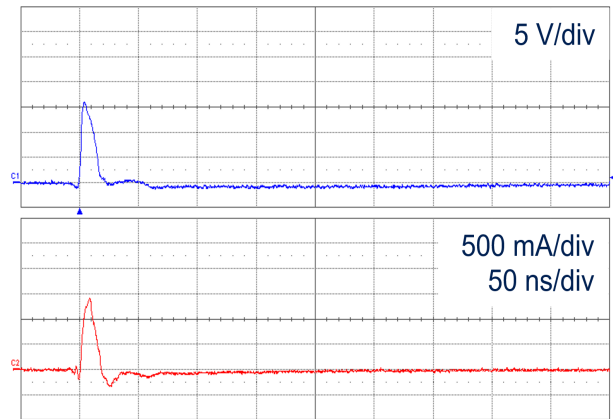


Figure 12. Response to ISO 7637-3 Pulse 2a: -85 V

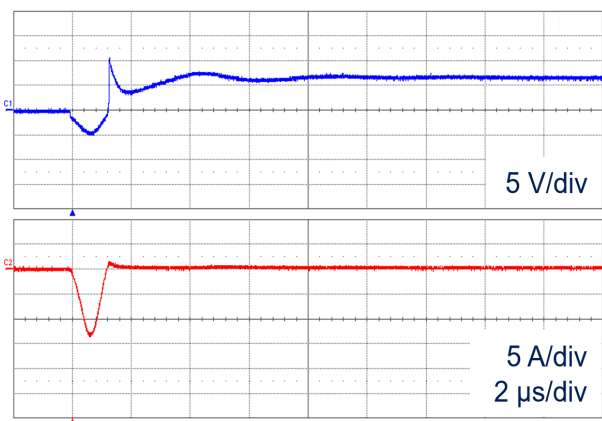
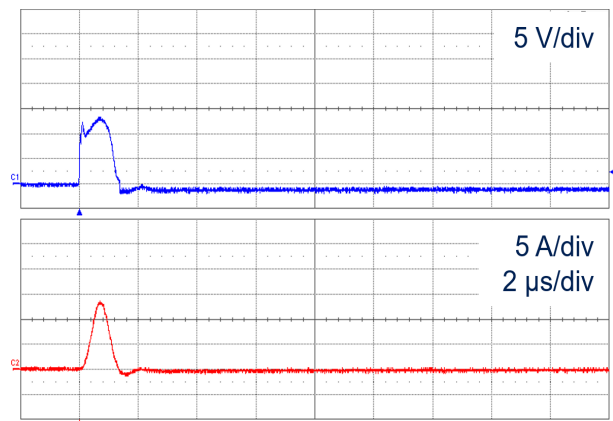


Figure 13. Response to ISO 7637-3 Pulse 2a: +85 V



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 SOT323-3L package information

- Epoxy meets UL 94, V0
- Lead-free package

Figure 14. SOT323-3L package outline

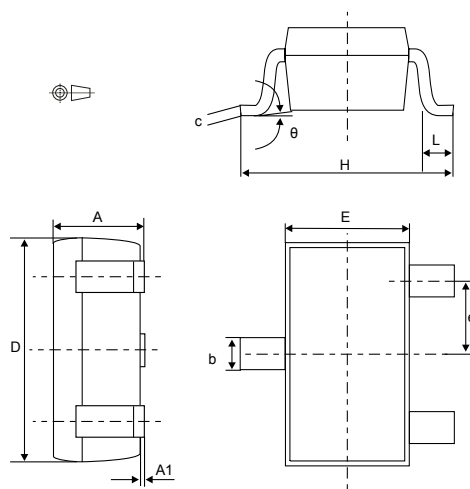


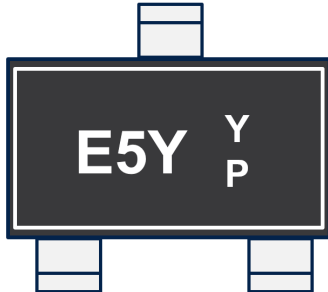
Table 4. SOT323-3L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.031		0.043
A1	0.00		0.10	0.000		0.003
b	0.25		0.40	0.0098		0.0157
c	0.10		0.26	0.003		0.0102
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.0452	0.0492	0.0531
e	0.60	0.65	0.70	0.024	0.026	0.028
H	1.80	2.10	2.40	0.070	0.082	0.094
L	0.10	0.20	0.30	0.004	0.008	0.012
Θ		0	30°	0		30°

1. Values in inches are converted from mm and rounded to 3 or 4 decimal digits.

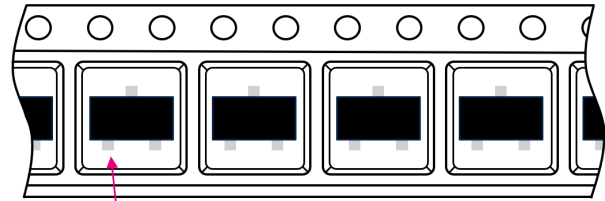
2.2 Packing and marking information

Figure 15. Marking layout



Y : Year
P : Assembly location

Figure 16. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Only pin 1 must be used to orient the component for its placement on a PCB.

Figure 17. Reel dimensions (mm)

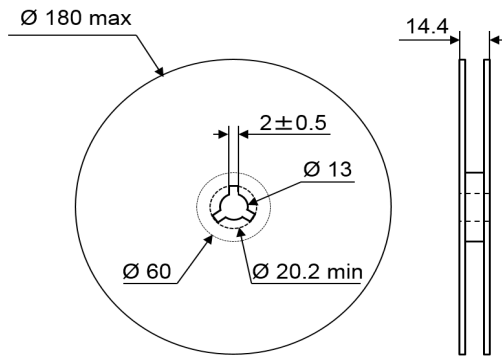


Figure 18. Tape and reel orientation

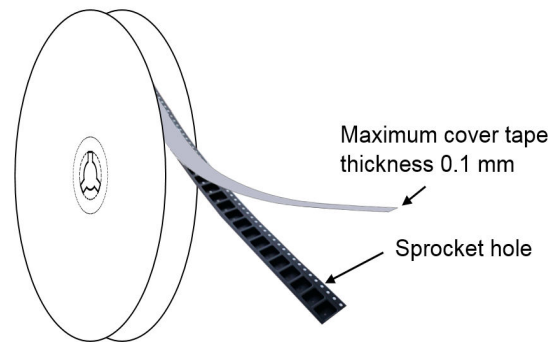


Figure 19. Inner box dimensions (mm)

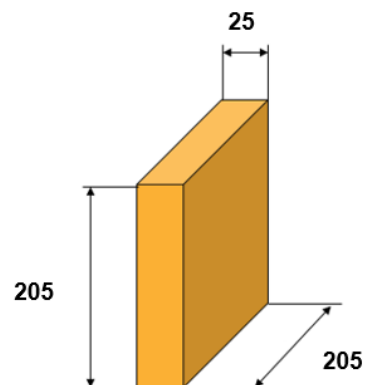
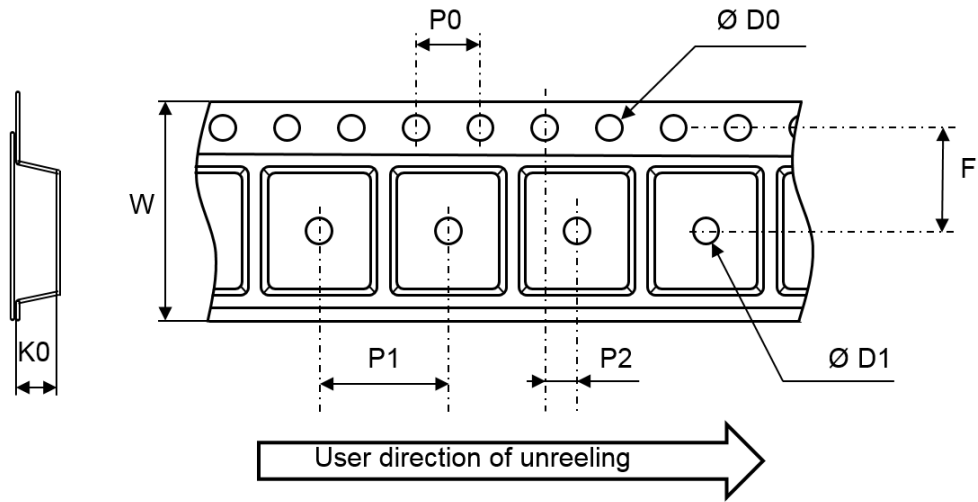
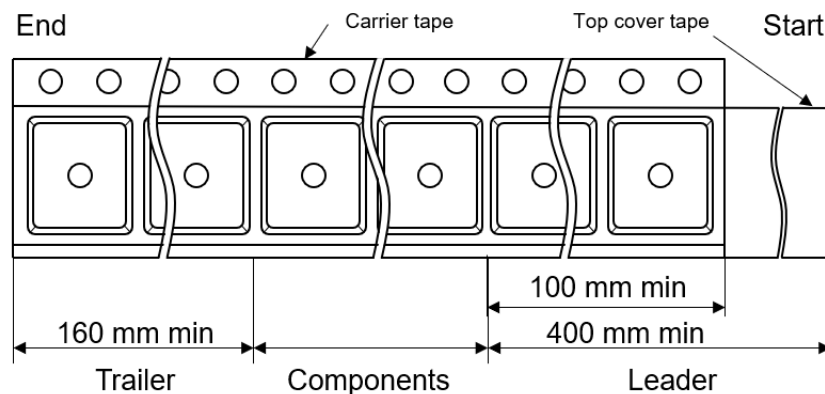


Figure 20. Tape outline


Note: Pocket dimensions are not on scale
 Pocket shape may vary depending on package

Table 5. Tape and reel mechanical data

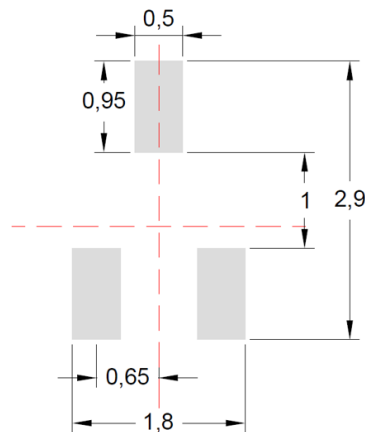
Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	1.00		
F	3.45	3.50	3.55
K0	1.12	1.22	1.32
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

Figure 21. Tape leader and trailer dimensions


3 Recommendations on PCB assembly

3.1 Recommended footprint

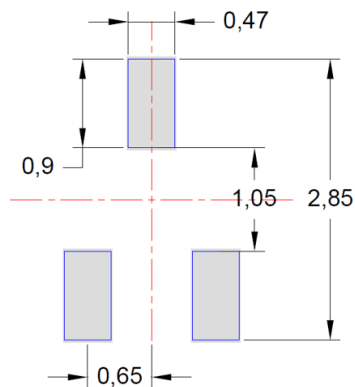
Figure 22. Recommended footprint in mm



3.2 Stencil opening design

- Stencil opening thickness: 75 μm to 125 μm / 3 mils to 5 mils
- Stencil opening ratio : 90%

Figure 23. Stencil opening recommendations



3.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 μm per IPCJ STD-005.

3.4 Placement

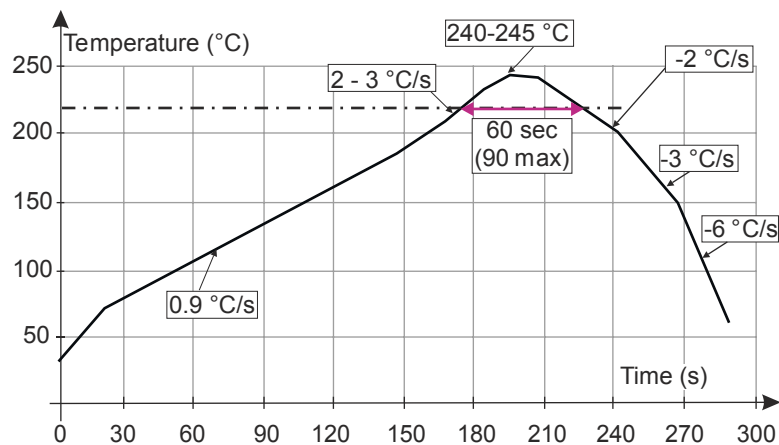
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of $\pm 50 \mu\text{m}$ is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

3.6 Reflow profile

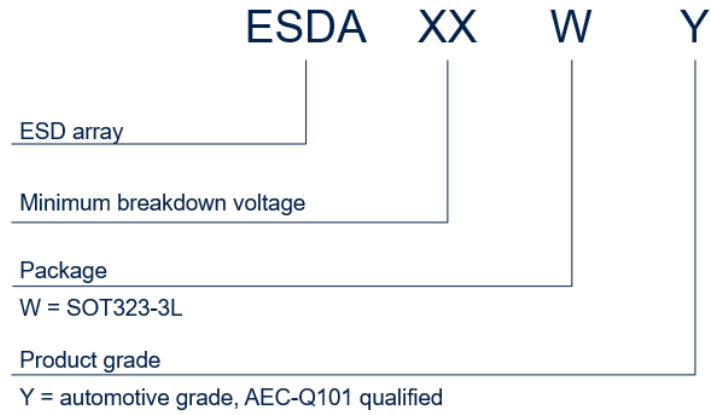
Figure 24. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 25. Ordering information scheme



Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDA5WY	E5Y ⁽¹⁾	SOT323-3L	6 mg	3000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly locations.

Revision history

Table 6. Document revision history

Date	Revision	Changes
20-Jun-2024	1	Initial release.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2024 STMicroelectronics – All rights reserved