ESDALC5-1BF4

Low clamping and low capacitance bidirectional single line ESD protection

Features

- Low clamping voltage
- Bidirectional device
- Low leakage current
- 0201 package
- Ultra low PCB area: 0.18 mm²
- ECOPACK®2 compliant component
- Exceeds the following standard:
  - IEC 61000-4-2 level 4 = ±15 kV (air discharge) and ±8 kV (contact discharge)

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Description

The ESDALC5-1BF4 is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

Figure 1: Functional diagram
1 Characteristics

Table 1: Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PP}$</td>
<td>Peak pulse voltage</td>
<td>Contact discharge</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Air discharge</td>
<td>30</td>
</tr>
<tr>
<td>$P_{PP}$</td>
<td>Peak pulse power dissipation (8/20 μs)</td>
<td></td>
<td>28</td>
</tr>
<tr>
<td>$I_{PP}$</td>
<td>Peak pulse current (8/20 μs)</td>
<td></td>
<td>2.5</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature range</td>
<td></td>
<td>-40 to +150</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage temperature range</td>
<td></td>
<td>-65 to +150</td>
</tr>
<tr>
<td>$T_L$</td>
<td>Maximum lead temperature for soldering during 10 s</td>
<td></td>
<td>260</td>
</tr>
</tbody>
</table>

Figure 2: Electrical characteristics (definitions)

Table 2: Electrical characteristics (Tamb = 25 °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR}$</td>
<td>$I_R = 1$ mA</td>
<td></td>
<td>5.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{RM}$</td>
<td>$V_{RM} = 5$ V</td>
<td></td>
<td>100</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$C_{LINE}$</td>
<td>$F = 1$ MHz, $V_{LINE} = 0$ V, $V_{OSC} = 30$ mV</td>
<td></td>
<td>10</td>
<td>12</td>
<td>pF</td>
</tr>
</tbody>
</table>
**ESDALC5-1BF4**

**Characteristics**

**Figure 3:** Leakage current versus junction temperature (typical values)

**Figure 4:** Junction capacitance versus reverse voltage applied (typical values)

**Figure 5:** ESD response to IEC 61000-4-2 (+8 kV contact discharge)

**Figure 6:** ESD response to IEC 61000-4-2 (-8 kV contact discharge)

**Figure 7:** TLP characteristic

**Figure 8:** S21 attenuation measurement result
2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 0201 package information

The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.
Table 3: 0201 package mechanical data

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Dimensions</th>
<th>Millimeters</th>
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<tbody>
<tr>
<td></td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td>A</td>
<td>0.280</td>
<td>0.300</td>
</tr>
<tr>
<td>b</td>
<td>0.125</td>
<td>0.140</td>
</tr>
<tr>
<td>D</td>
<td>0.570</td>
<td>0.600</td>
</tr>
<tr>
<td>D1</td>
<td></td>
<td>0.350</td>
</tr>
<tr>
<td>E</td>
<td>0.270</td>
<td>0.300</td>
</tr>
<tr>
<td>E1</td>
<td>0.175</td>
<td>0.190</td>
</tr>
<tr>
<td>fD</td>
<td>0.110</td>
<td>0.125</td>
</tr>
<tr>
<td>fE</td>
<td>0.040</td>
<td>0.055</td>
</tr>
</tbody>
</table>

Figure 10: Marking

The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 11: Tape and reel specification (in mm)
3  Recommendation on PCB assembly

3.1  Footprint

![Footprint diagram]

Figure 12: Footprint (dimensions in mm)

1. SMD footprint design is recommended.

3.2  Stencil opening design

1. Recommended design reference
   a. Stencil opening thickness: 75 μm / 3 mils

![Stencil window position diagram]

Figure 13: Recommended stencil window position in mm (inches)

3.3  Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with particle size 20-38 μm
3.4 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 14: ST ECOPACK® recommended soldering reflow profile for PCB mounting

Minimize air convection currents in the reflow oven to avoid component movement.
4 Ordering information

Figure 15: Ordering information scheme

Table 4: Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty.</th>
<th>Delivery mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESDALC5-1BF4</td>
<td>C&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>0201</td>
<td>0.116 mg</td>
<td>15000</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

Notes:

<sup>(1)</sup>The marking can be rotated by multiples of 90° to differentiate assembly location.

5 Revision history

Table 5: Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tr>
<td>06-Feb-2014</td>
<td>1</td>
<td>First issue.</td>
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<tr>
<td>01-Jun-2017</td>
<td>2</td>
<td>Updated Table 3: &quot;0201 package mechanical data&quot;. Updated Section 3.2: &quot;Stencil opening design&quot;.</td>
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<td>08-Feb-2018</td>
<td>3</td>
<td>Updated Table 2: &quot;Electrical characteristics (Tamb = 25 °C)&quot;.</td>
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