10 V ultra-low clamping single line high speed bidirectional ESD protection

**Features**

- Ultra-low clamping voltage: 10 V TLP at 16 A Ipp
- Bidirectional protection diode
- Very high bandwidth: 24 GHz
- Very low dynamic resistance: 0.5 Ω
- Suitable for RF antenna application with very low harmonic:
  - H3 < -50 dBm at 20 dBm power:
    - 710 MHz, 824 MHz and 2.4 GHz
- ST0201 package
- ECOPACK2 compliant component
- Exceeds IEC 61000-4-2 level 4:
  - ±12 kV (contact discharge)
  - ±20 kV (air discharge)

**Application**

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- USB 3.2 Gen 1 and Gen 2
- RF antenna
- Ethernet 1000 BASE-T
- Ethernet 10G BASE-T
- Display port
- LVDS

**Description**

The **ESDZX051-1BF4** is a bidirectional single line TVS diode designed to protect the data lines or other I/O ESD transients. Thanks to extra low capacitance, **ESDZX051-1BF4** can protect high speed differential lines with no impact on signal integrity.

With an extremely low clamping voltage, **ESDZX051-1BF4** is able to protect the most sensitive, submicron technology circuits.
1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{pp}</td>
<td>Peak pulse voltage</td>
<td>±12</td>
<td>kV</td>
</tr>
<tr>
<td>P_{pp}</td>
<td>Peak pulse power (8/20 μs)</td>
<td>20</td>
<td>W</td>
</tr>
<tr>
<td>I_{pp}</td>
<td>Peak pulse current (8/20 μs)</td>
<td>4</td>
<td>A</td>
</tr>
<tr>
<td>T_j</td>
<td>Operating junction temperature range</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>Storage junction temperature range</td>
<td>-65 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>T_L</td>
<td>Maximum lead temperature for soldering during 10 s</td>
<td>260</td>
<td></td>
</tr>
</tbody>
</table>

Table 2. Electrical characteristics (values) (T_{amb} = 25 °C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{TRIG}</td>
<td>Maximum off-state voltage</td>
<td></td>
<td>9.6</td>
<td>10.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_H</td>
<td>Lower voltage than V_H guarantees the protection turn-off</td>
<td></td>
<td>1.4</td>
<td>1.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{HOLD}</td>
<td>Minimum on-state current</td>
<td></td>
<td>35</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>V_{RM}</td>
<td>Reverse working voltage</td>
<td></td>
<td>3.6</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{RM}</td>
<td>Leakage current</td>
<td>V_{RM} = 3.6 V</td>
<td></td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>V_{CL}</td>
<td>Clamping voltage</td>
<td>I_{pp} = 4 A - 8/20μs</td>
<td>4</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 kV contact discharge after 30 ns, IEC 61000-4-2</td>
<td>11</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TLP measurement (pulse duration 100 ns)</td>
<td>I_{pp} = 16 A</td>
<td>10</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I_{pp} = 4 A</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_D</td>
<td>Dynamic resistance, TLP pulse duration 100 ns (from 4 A to 16 A I_{pp})</td>
<td></td>
<td>0.5</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>f_C</td>
<td>Cut-off frequency</td>
<td></td>
<td>-3dB</td>
<td>24</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>C_{LINE}</td>
<td>Line capacitance</td>
<td>V_{LINE} = 0 V, F = 3 GHz</td>
<td>0.28</td>
<td>0.35</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_{LINE} = 0 V, F = 10 GHz</td>
<td>0.25</td>
<td>0.33</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 1. Electrical characteristics (definitions)
1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature (typical values)

![Leakage current versus junction temperature](image)

Figure 3. Junction capacitance versus frequency (typical values)

![Junction capacitance versus frequency](image)

Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

![ESD response to IEC 61000-4-2](image)

Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

![ESD response to IEC 61000-4-2](image)

Figure 6. S21 attenuation measurement results

![S21 attenuation measurement results](image)

Figure 7. TLP measurement

![TLP measurement](image)
Figure 8. Harmonic measurement at 710 MHz : H2

Figure 9. Harmonic measurement at 710 MHz : H3

Figure 10. Harmonic measurement at 824 MHz : H2

Figure 11. Harmonic measurement at 824 MHz : H3

Figure 12. Harmonic measurement at 2.4 GHz : H2

Figure 13. Harmonic measurement at 2.4 GHz : H3
2 Application information

2.1 Latch-up consideration

There is a potential risk of latch-up using SCR based ESD protection if the working voltage $V_{RM}$ is higher than $V_H$ voltage.

To ensure a latch-up free state, the current injected in the protection must be lower than the holding current $I_{HOLD}$ when the voltage across the protection device is equal to $V_{HOLD}$. The following equation gives the latch-up free condition.

$$I_{HOLD} > \frac{V_{SOURCE_{max}} - V_{HOLD}}{R_{SOURCE_{min}}}$$
3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 ST0201 package information

Figure 14. ST0201 package outline

Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Table 3. 0201 package mechanical data

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Millimeters</td>
</tr>
<tr>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>A</td>
<td>0.130</td>
</tr>
<tr>
<td>b</td>
<td>0.1675</td>
</tr>
<tr>
<td>D</td>
<td>0.560</td>
</tr>
<tr>
<td>D1</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>0.260</td>
</tr>
<tr>
<td>E1</td>
<td>0.205</td>
</tr>
<tr>
<td>fD</td>
<td></td>
</tr>
<tr>
<td>fE</td>
<td></td>
</tr>
</tbody>
</table>
Figure 15. Tape and reel specification (in mm)

All dimensions are typical values in mm

User direction of unreeling

0.2 ±0.02
8.0 ±0.30 / -0.10
0.34 ±0.03
2.0 ±0.05
Ø 1.75 ±0.10
2.0 ±0.05
0.3 raised cross-bar

2.0 ±0.05
4.0 ±0.10
Ø 1.5 ±0.10
3.50 ±0.05
1.75 ±0.10
0.20 ±0.03
0.64 ±0.03
2.0 ±0.05
Ø 0.17 ±0.05
4 Recommendation on PCB assembly

4.1 Footprint

1. SMD footprint design is recommended

![Figure 16. Footprint in mm](#)

4.2 Stencil opening design

1. Recommended design reference
   a. Stencil opening dimensions: 75 µm / 3 mils
   b. Stencil aperture ratio: 100%

![Figure 17. Stencil opening recommendations](#)
4.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

4.4 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

4.6 Reflow profile

*Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting*

![Reflow profile graph](image)

Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.
5 Ordering information

Figure 19. Ordering information scheme

ESDZX 05 1 - 1 B F4

- ESD protection with snapback effect
- Low capacitance
- \[ V_{RM} \]
- 05 = 5.0 V max.
- Version
- Number of lines
- B = Bi-directional
- Package
- F4 = ST0201

Table 4. Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking(1)</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty.</th>
<th>Delivery mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESDZX051-1BF4</td>
<td>N</td>
<td>ST0201</td>
<td>0.116 mg</td>
<td>15000</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

1. The marking can be rotated by multiples of 90° to differentiate assemble location.
## Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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<tr>
<td>27-Jan-2020</td>
<td>1</td>
<td>First issue.</td>
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<tr>
<td>30-Mar-2020</td>
<td>2</td>
<td>Updated Table 2.</td>
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*Table 5. Document revision history*