GANSPIN611

Datasheet

High-voltage half-bridge GaN motor driver

QFN 9 x 9 x 1 mm

Product status link

GANSPIN611

Product label

Features

- Power system-in-package family integrating high-voltage GaN transistors in half-bridge configuration with high-voltage gate driver:
  - $R_{DS(ON)}$ = 138 mΩ
  - $I_{DS(MAX)}$ = 10 A
- Reverse conduction capability and zero reverse recovery loss
- 10 V/ns typ. output dV/dt in both hard-on and hard-off, tailored for motor control
- Externally adjustable turn-on dV/dt
- Linear regulators to regulate high-side and low-side driver supply voltage
- Internal bootstrap diode
- Comparator for overcurrent detection with Smart Shutdown function
- UVLO protection on VCC, V_{HS} and V_{LS}
- Interlocking function, shutdown, standby and fault pins
- 55 ns gate driver leading to overall 150 ns typ. output propagation delay
- 3.3 V to 20 V compatible inputs with hysteresis and pull-down

Applications

- Home appliances
- Compressors
- Pumps
- Fans
- Personal care appliances
- Factory automation
- Servo drives
- Power tools

Description

GaN-based motion control is the focus of the GaNSPIN platform. Unlike many general-purpose solutions or those tailored for power conversion, the GaNSPIN series is specifically engineered to meet the peculiar demands of motion control systems.

The GANSPIN611 is an advanced power system-in-package integrating two enhancement mode GaN transistors in half-bridge configuration driven by a state-of-the-art high-voltage, high-frequency gate driver.

The integrated power GaNs have $R_{DS(ON)}$ of 138 mΩ and 650 V drain source breakdown voltage, while the high-side of the embedded gate driver can be easily supplied by the integrated bootstrap diode.

The GANSPIN611, being designed for motion control, optimizes the output dV/dt to 10 V/ns typ. for both hard-on and hard-off. This is required in motor control for EMI, motor winding, and ball bearing reliability.

Robustness and reliability are also distinctive factors of the GaNSPIN series. Embedding advanced protections, GaNSPIN devices ensure the best possible system robustness. SmartShutdown overcurrent protection delivers the fastest response possible thanks to embedded logic and dedicated fast comparators.

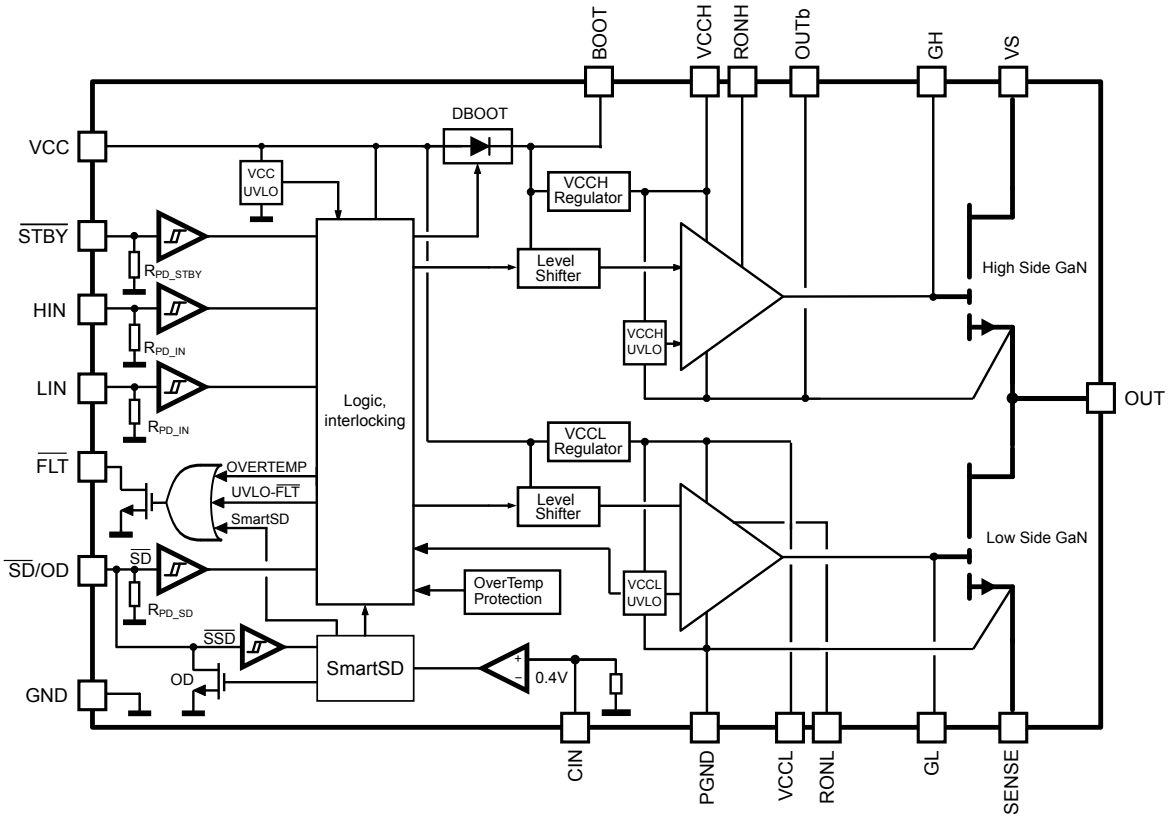
The GANSPIN series also features linear regulators on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions, and the interlocking function avoids cross-conduction conditions. The UVLO is fine-tuned for motion control for optimal performances.

The GANSPIN611 is available in a compact 9x9x1 mm QFN package and operates in the industrial temperature range, -40 °C to 125 °C.

The GaNSPIN611 is pin-to-pin with GaNSPIN612 ($R_{DS(ON)}$ of 270 mΩ) to maximize scalability in a platform approach.

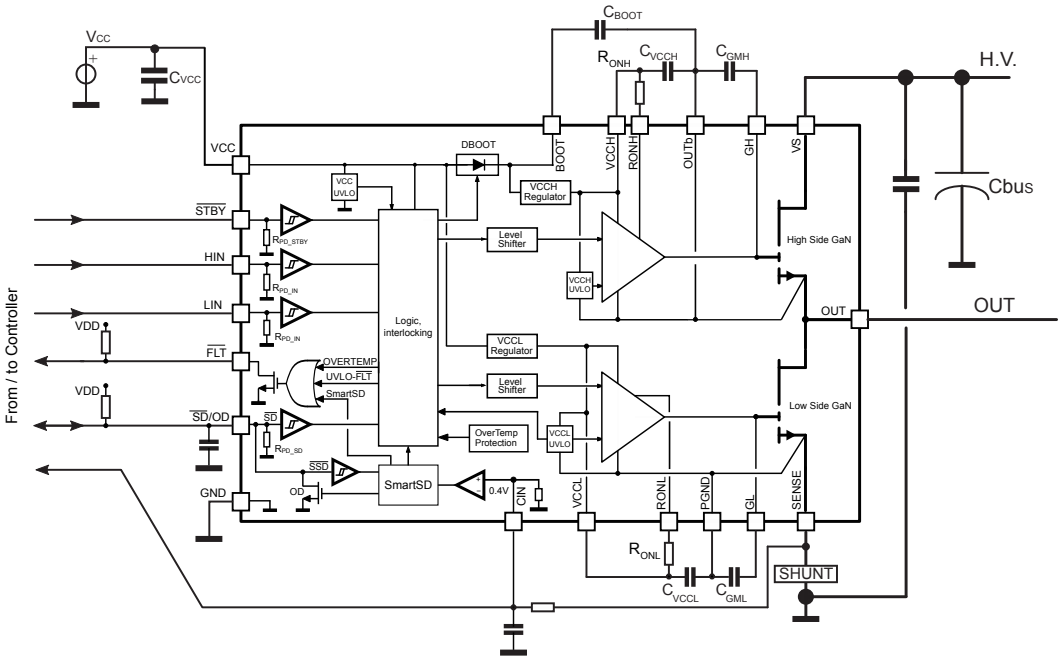
1 Block diagram

Figure 1. **GANSPIN611 block diagram**



2 Typical application schematic

Figure 2. Typical motor control application schematic



3 Pin descriptions

Figure 3. **GANSPIN611 pin connections**

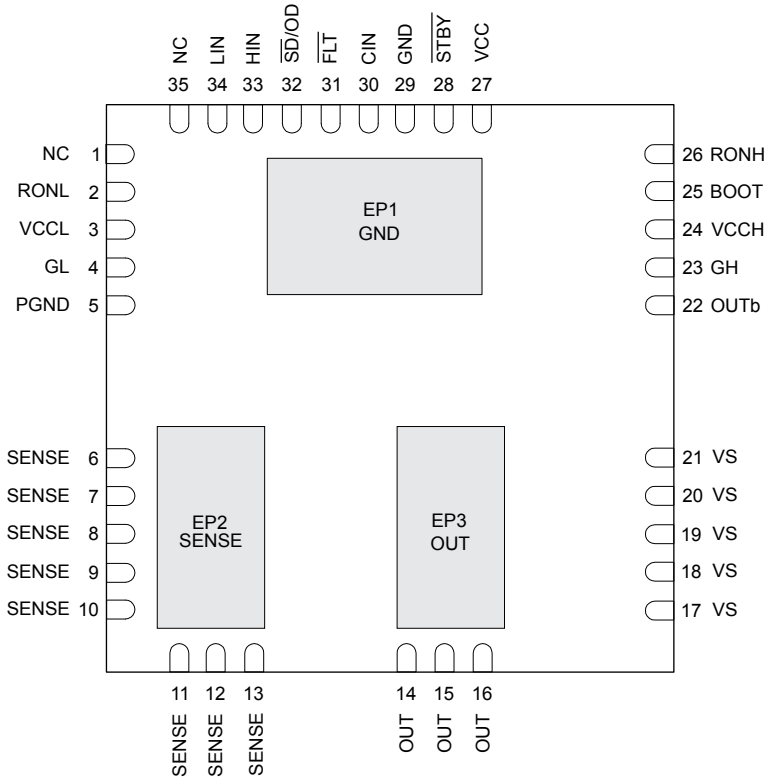


Table 1. **GANSPIN611 pin list**

Pin N.	Name	Type	Function
1, 35	NC	-	Not connected pin. The pins can be either connected to GND or left floating.
2	RONL	Output	A resistor connected between this pin and VCCL sets the turn-on resistor of the low-side driver. Mounting the resistor as close as possible to the RONL pin optimizes the operation of the driver. It is possible to drive the GaN with minimum internal resistance connecting the RONL pin to VCCL pin.
3	VCCL	Power	Output of the linear regulator that supplies the output stage of the low-side driver. A ceramic capacitor of 47 nF min. (X7R, 16 V) must be placed as close as possible between this pin and PGND.
4	GL	Output	Gate of low-side GaN transistor. Add 680 pF capacitor to PGND.
5	PGND	Power	Reference potential of low-side driver and relevant external components (VCCL capacitor and components connected to GL). This pin is internally connected to the low-side GaN transistor source.
6 to 13, EP2	SENSE	Power	Source of low-side GaN transistor. The exposed pad has both an electrical and thermal purpose: low-side transistor power losses are dissipated soldering EP2 to proper copper area.
14, 15, 16, EP3	OUT	Power	Middle point of half-bridge. The exposed pad has both an electrical and thermal purpose: high-side transistor power losses are dissipated soldering EP3 to proper copper area.
17 to 21	VS	Power	Drain of high-side GaN transistor.
22	OUTb	Power	Reference potential of high-side driver and relevant external components (BOOT capacitor, VCCH capacitor, and components connected to GH). This pin is internally connected to the high-side GaN transistor source.

Pin N.	Name	Type	Function
23	GH	Output	Gate of the high-side GaN transistor. Add 680 pF capacitor to OUTb.
24	VCCH	Power	Output of the linear regulator that supplies the output stage of the high-side driver. A ceramic capacitor of 47 nF min. (X7R, 16 V) must be placed as close as possible between this pin and OUTb.
25	BOOT	Power	Supply voltage of high-side floating driver. A ceramic capacitor equal or greater than C_{VCCH} (X7R, 50 V) must be placed as close as possible between this pin and OUTb. The input of the high-side driver regulator is internally connected to this pin.
26	RONH	Output	A resistor connected between this pin and VCCH sets the turn-on resistor of the high-side driver. Mounting the resistor as close as possible to the RONH pin optimizes the operation of the driver. It is possible to drive the GaN with minimum internal resistance connecting the RONH pin to VCCH pin.
27	VCC	Power	Supply voltage of logic section. A small bypass capacitor (100 nF typ.) very close to the pin is required to get a clean bias voltage for the signal part of the IC. The large bulk capacitor that is normally used to supply the controller is sufficient to also supply GANSPIN611: if not present, a value equal or larger than 2.2 µF is suggested. The input of the low-side driver regulator is internally connected to this pin.
28	$\overline{\text{STBY}}$	Input	Standby mode activation pin. Setting this pin to GND, the IC enters a low consumption mode to facilitate the design of low consumption topologies. The internal pull-down resistor is there to avoid uncertain voltage application when IC is not biased. Connect this pin to VCC if standby function is not used.
29, EP1	GND	Power	Ground pin. Common potential of the logic section of the device. The exposed pad has both an electrical and thermal purpose: power dissipation of linear regulators, drivers, and level shifter units can be dissipated soldering EP1 to proper copper area.
30	CIN	Input	Comparator input pin for smartSD. In case of triggering, both GaN are immediately turned off and $\overline{\text{SD}}$/OD is pulled low. The shunt voltage filtering capacitor shall be placed near CIN pin and on the PCB side of the IC to maximize noise immunity. Connect to GND if not used.
31	$\overline{\text{FLT}}$	Output	Fault signaling pin. An open-drain MOSFET is turned on to pull the pin down when UVLO, standby, comparator, or overtemperature protection are active. Connect to GND if not used.
32	$\overline{\text{SD}}$/OD	Input	Shutdown input (active low) / open-drain output for comparator with smartSD. When this pin is pulled to GND, the IC immediately interrupts the switching activity defined by LIN and HIN. When CIN exceeds the threshold, smartSD interrupts the switching activity and pulls low the $\overline{\text{SD}}$/OD pin. Once the overcurrent has ended, the open-drain is released. The internal pull-down resistor is there to avoid uncertain voltage application when IC is not biased.
33	HIN	Input	High-side logic input pin. Driving pulses to control the high-side switch can be applied to this pin. Schmitt trigger input, 20 V tolerant, buffers the input signal before driving level shifters.
34	LIN	Input	Low-side logic input pin. Driving pulses to control the low-side switch can be applied to this pin. Schmitt trigger input, 20 V tolerant, buffers the input signal before driving level shifters.

4 Electrical data

4.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 2 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages referred to ground pins unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_{VS-OUT}	High-side GaN Drain-to-Source blocking voltage	T_J = 25 °C, OUT = GND, DC voltage, I_{VS} < 20 µA	650	V
		t_{PULSE} < 100 ns (1)	750	V
I_D	Drain current (per GaN transistor)	DC @ T_{CB} = 25 °C (1) (2)	9.7	A
		DC @ T_{CB} = 100 °C (1) (2)	6.4	A
		Peak @ T_{CB} = 25 °C (1) (2) (3)	16	A
VCC	Logic supply voltage		-0.3 to 21	V
PGND	Low-side driver ground vs. logic ground (4)	VCC = 14 V	-7 to 7	V
$V_{VCC-PGND}$	Logic supply vs. low-side driver ground		-0.3 to 21	V
V_{VCCL}	Regulated low-side driver supply vs. logic ground		-0.3 to 14	V
V_{LS}	Regulated low-side driver supply voltage (4) (5) (6)		-0.3 to 7	V
I_{LS_OUT}	Low-side regulator maximum current (4) (5)	Internal and RONL average consumption (6)	Self-limited	mA
$V_{VCC-VCCL}$	Maximum low-side dropout voltage		-0.3 to self-regulated	V
V_{GL}	Low-side gate to PGND voltage	DC values	-0.3 to VCCL+0.3	V
V_{RONL}	Low-side turn-on resistor pin max. voltage		(GL-0.3V) to (VCCL+0.3V)	V
V_{BOOT}	BOOT pin voltage referred to GND		-0.3 to 621	V
V_{BO}	High-side regulator input voltage (5) (7)		-0.3 to 21	V
V_{HS}	Regulated high-side driver supply voltage (5) (7)		-0.3 to 7	V
I_{HS_OUT}	High-side regulator maximum current (5) (7)	Internal and RONH average consumption (6)	Self-limited	mA
$V_{BOOT-VCCH}$	Maximum high-side dropout voltage		-0.3 to self-regulated	V
V_{GH}	High-side gate to OUTb voltage (7)		-0.3 to VCCH+0.3	V
V_{RONH}	High-side turn-on resistor pin max. voltage		(GH-0.3V) to (VCCH+0.3V)	V
R_{BOOT}	Minimum external bootstrap diode series resistance (if present)		2.7	Ω
dV_{OUT}/dt	Maximum OUT voltage slew rate (1)		120	V/ns
CIN	Comparator input voltage		-0.3 to 21	V
V_{in}	Logic inputs voltage range (LIN, HIN, $\overline{SD}$/OD, $\overline{STBY}$, $\overline{FLT}$)		-0.3 to 21	V

Symbol	Parameter	Test condition	Value	Unit
I_{FLT}	Maximum $\overline{FLT}$ pin current (DC inward)	VCC = 7.0 V	10	mA
I_{OD}	Maximum $\overline{SD}$/OD pin current (DC inward)	VCC = 12.0 V	10	mA
T_J	Junction temperature		-40 to 150	°C
T_{stg}	Storage temperature		-55 to 150	°C
ESD	HBM (Human Body Model)	ANSI/ESDA/JEDEC JS-001-2017	2	kV
	CDM (Charged Device Model)	ANSI/ESDA/JEDEC JS-002-2018	1	kV

1. *Range estimated by characterization on a limited number of samples, not tested in production.*
2. *T_{CB} is the temperature of the case-exposed pad.*
3. *Value specified by design factor, pulse duration limited to 10 µs and junction temperature.*
4. *PGND internally connected to SENSE.*
5. *$V_{LS} = V_{VCCL-PGND}$, $V_{HS} = V_{VCCH-OUTb}$, $V_{BO} = V_{BOOT-OUTb}$.*
6. *The internal low-side and high-side voltage regulators are not intended to be connected to external load or voltage sources.*
7. *OUTb internally connected to OUT.*

4.2 Recommended operating conditions

All voltages referred to ground pins unless otherwise specified. The junction temperature must be maintained within recommended operating conditions with proper thermal design.

Table 3. Recommended operating conditions

Symbol	Parameter	Note	Min.	Max.	Unit
VCC	Logic supply voltage		10.7	18	V
$V_{VCC-PGND}$	Logic supply voltage vs, PGND		7.5	18	V
PGND	Low-side driver ground (1)		-3	3	V
V_{BO}	$V_{BOOT-OUTb}$ pin voltage		7.5	20	V
VS	Bus supply voltage		0	520	V
V_{OUT}	OUT pin voltage		-9.3 (2) (3)		V
VCCL	Low-side driver voltage vs. GND		3		V
V_{BOOT}	BOOT to GND voltage	(4)	0	540	V
CIN	Comparator input voltage		0	15	V
V_i	Logic inputs voltage range		0	20	V
R_{RONL}, R_{RONH}	External RON resistors		0	500	Ω
C_{VCCH}, C_{VCCL}	Driver supply voltage bypass capacitors (5)		47	220	nF
C_{BO}	High-side driver linear regulator input capacitors (6)		C_{VCCH}	3300	nF
C_{GMH}, C_{GML}	External gate capacitance		680	1800	pF
t_{DT}	Suggested minimum deadtime (7)		300		ns
t_{INmin}	Minimum duration of input pulse		600		ns
f_{sw}	Switching frequency	Duty cycle = 50%		200 (3)	kHz
T_{J-op}	Junction temperature		-40	125	°C

1. *PGND internally connected to SENSE.*
2. *V_{BO} = 20 V, VCC = 10.7 V*
3. *The actual limit depends on power dissipation constraints.*
4. *BOOT must be ≥ 5V to propagate high-side commands.*
5. *X7R, 16V, ceramic capacitor having ESR lower or equal to 50 mΩ.*
6. *X7R, 50V, ceramic capacitor having ESR lower or equal to 50 mΩ.*
7. *Minimum value with minimum C_{GMx}.*

4.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J-CB)}$	Thermal resistance junction to each GaN transistor exposed pad	1.9	°C/W
$R_{th(J-A)}$	Thermal resistance junction-to-ambient (1)	17.8	°C/W

1. *The junction to ambient thermal resistance is obtained simulating the device mounted on a 2s2p (4 layer) FR4 board as JESD51-5,7 with 6 thermal vias for each exposed pad. Power dissipation uniformly distributed over the two GaN transistors.*

5 Electrical characteristics

Testing conditions: T_J = 25 °C, VCC = V_{BO} = $\overline{SD}$/OD = $\overline{STBY}$ = 12 V; $\overline{FLT}$ = floating;
RONL = VCCL; RONH = VCCH, SENSE = CIN = PGND = 0 V; VS = 0 V;
C_{VCCH} = C_{VCCL} = 47 nF, C_{BO} = 220 nF.
All voltages referred to GND, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
GaN power transistor - electrical characteristics						
$V_{(BR)DS\_H}$	Drain to source blocking voltage	VS to OUT, DC voltage I_{DSS} < 20 µA, GH = OUTb (1)	650			V
		VS to OUT, t_{PULSE} = 100 ns (2)	750			
$V_{GS(th)}$	Gate to source threshold voltage	LIN = 3.3 V, SENSE = GND RONL = GL = 10 kΩ to OUT, $I_{OUT-SENSE}$ = 2.5 mA		1.7		V
		HIN = 3.3 V, OUT = GND, RONH = GH = 10 kΩ to VS, I_{VS-OUT} = 2.5 mA				
I_{DSS}	Zero gate voltage drain current	V_{VS-OUT} = 600 V, GH = OUTb		0.45	20	µA
		$V_{OUT-SENSE}$ = 600 V, GL = PGND				
I_{GS}	Gate to source current	V_{VS-OUT} = 0 V, RONH = GH OUT = GND, $V_{GH-OUTb}$ = 6 V		60		µA
		$V_{OUT-SENSE}$ = 0 V, RONL = GL $V_{GL-PGND}$ = 6 V				
$R_{DS(on)}$	Drain to source on-state resistance	$I_{OUT-SENSE}$ / I_{VS-OUT} = 3.2 A		138	190	mΩ
		$I_{OUT-SENSE}$ / I_{VS-OUT} = 3.2 A T_J = 125 °C (2)		270		
GaN power transistor – characterization values						
Q_G	Total gate charge	V_{GS} = 0 to 6 V V_{DS} = 400 V (2)		2.8		nC
Q_{OSS}	Output charge	V_{GS} = 0 V		24		nC
E_{OSS}	Output capacitance stored energy	V_{DS} = 400 V		3.5		µJ
C_{OSS}	Output capacitance	f = 100 kHz (2)		30		pF
$C_{O(ER)}$	Effective output capacitance energy related	V_{GS} = 0 V		43		pF
$C_{O(TR)}$	Effective output capacitance time related	V_{DS} = 0 to 400 V (2)		60		pF
Q_{RR}	Reverse Recovery Charge			0		nC
I_{RRM}	Reverse Recovery Current			0		A
V_{plat}	Gate plateau voltage	V_{DS} = 400 V, I_D = 1.6 A		2		V
V_{SD}	Source-drain reverse voltage	V_{GS} = 0 V, I_S = 1.6 A		2.2		V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
GaN power transistor – inductive load switching characteristics						
$t_{(on)}$	Hard turn-on time	V_{VS} = 400 V		100		ns
t_{fall}	V_{DS} hard turn-on fall time	I_D = 1.6 A		20		ns
SR_{fall}	V_{DS} hard turn-on slew rate	R_{ONH} = R_{ONL} = 33 Ω		12		V/ns
E_{on}	Hard turn-on switching losses	C_{GMH} = C_{GML} = 680 pF See Figure 4 for definitions (2)		42		µJ
$t_{(off)}$	Hard turn-off time	V_{VS} = 400 V		100		ns
t_{rise}	V_{DS} hard turn-off rise time	I_D = 1.6 A		30		ns
SR_{rise}	V_{DS} hard turn-off slew rate	C_{GMH} = C_{GML}= 680 pF		8		V/ns
E_{off}	Hard turn-off switching losses	See Figure 4 for definitions (2)		3		µJ
Logic section supply						
VCC_{thON}	VCC UVLO turn-ON threshold		9.5	10.0	10.6	V
VCC_{thOFF}	VCC UVLO turn-OFF threshold		9.0	9.5	10.1	V
VCC_{hys}	VCC UV hysteresis		0.3	0.5	0.7	V
I_{QVCC}	VCC quiescent supply current	$\overline{STBY}$ = $\overline{SD}$/OD = 5 V LIN = HIN = 0 V, V_{BO} = 15 V		900	1200	µA
		LIN = $\overline{STBY}$ = $\overline{SD}$/OD = 5 V HIN = 0 V, V_{BO} = 15 V		1080	1450	µA
I_{QVCCU}	VCC undervoltage quiescent supply current	VCC = 7.0 V		570	760	µA
I_{SBVCC}	VCC standby supply current	$\overline{STBY}$ = 0 V, BOOT = 10 V		500	650	µA
I_{SVCC}	VCC switching supply current (2)	$\overline{STBY}$ = $\overline{SD}$/OD = 5 V V_{BO} = 15 V, V_{OUT} = V_{VS} = 0 V LIN = ¬ HIN, f_{SW} = 50 kHz, D = 50% C_{GMH} = C_{GML} = 680 pF		1.55		mA
R_{BLEED}	Low-side gate bleeder	VCCL = VCC = 0 V PGND = GND, V_{GL} = 0.1 V	75	100	125	kΩ
$t_{startup}$	VCC startup time from VCC = 10.5 V to GL = on	LIN = $\overline{STBY}$ = $\overline{SD}$/OD = 5 V HIN = 0 V			12	µs
Gate driver voltage regulators VCCL (V_{LS}) and VCCH (V_{HS})						
V_{HS} V_{LS}	VCCx regulator output voltage	I_{VCCx} < 10 mA_{DC}	5.55	6.00	6.45	V
		T_J = -40 °C to +125 °C (2)	5.4		6.6	V
V_{HSthON} V_{LSthON}	VCCx UVLO turn-on voltage		4.45	4.80	5.15	V
		T_J = -40 to +125°C (2)			5.25	V
$V_{HSthOFF}$ $V_{LSthOFF}$	VCCx UVLO turn-off voltage		4.30	4.65	4.95	V
		T_J = -40 to +125°C (2)	4.2			V
$V_{HSthHYS}$ $V_{LSthHYS}$	VCCx UVLO hysteresis		0.15	0.20	0.23	V
V_{DROP_H}	VCCH regulator drop-out voltage	BOOT = 12 V, OUT = 6 V, I_{VCCH} = 10 mA			0.6	V

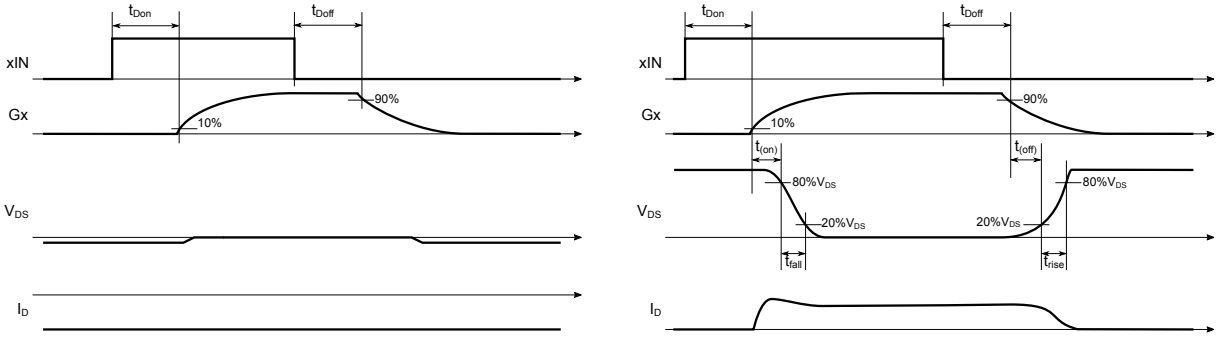
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
High-side driver section						
I_{QBO}	V_{BO} quiescent supply current	$\overline{STBY}$ = $\overline{SD}$/OD = 3.3 V LIN = HIN = 0 V, V_{BO} = 12 V		240	340	µA
		HIN = $\overline{STBY}$ = $\overline{SD}$/OD = 3.3 V LIN = 0 V, V_{BO} = 12 V		330	460	µA
I_{SBO}	V_{BO} switching supply current (2)	$\overline{SD}$/OD = $\overline{STBY}$ = 3.3 V VS = 0, V_{BOOT} = 12 V HIN f_{SW} = 50 kHz C_{GMH} = C_{GML} = 680 pF		0.8		mA
$t_{HSstart}$	High-side startup time	D_{BOOT} = STTH1R06, R_{BOOT} = 2.7 Ω from LIN = 3.3 V to V_{HS} > 5.1 V			5	µs
I_{LK}	Driver high-voltage leakage current	BOOT = OUT = 600 V			11	µA
R_{DBOOT}	Bootstrap diode on resistance	LIN = $\overline{STBY}$ = $\overline{SD}$/OD = 3.3 V HIN = 0 V, $V_{VCC-BOOT}$ = 0.5 V		120	140	Ω
Logic inputs and timings						
V_{ih}	High level logic threshold voltage	T_J = 25 °C	2.0	2.27	2.5	V
		T_J = -40 to +125°C (2)			2.7	V
V_{il}	Low level logic threshold voltage	T_J = 25 °C	1.1	1.31	1.45	V
		T_J = -40 to +125°C (2)	0.8			V
V_{ihys}	Logic input threshold hysteresis		0.7	0.96	1.2	V
V_{SSD}	SmartSD unlatch threshold	T_J = 25 °C	0.5	0.65	0.8	V
		T_J = -40 to +125°C (2)			0.9	V
I_{INh}	LIN, HIN logic ‘1’ input bias current	LIN, HIN = 3.3 V	15	22	36	µA
I_{INl}	LIN, HIN logic ‘0’ input bias current	LIN, HIN = 0 V			1	µA
R_{PD_IN}	LIN, HIN pull-down resistor	LIN, HIN = 3.3 V	90	150	220	kΩ
I_{SDh}	$\overline{SD}$/OD logic ‘1’ input bias current	$\overline{SD}$/OD = 3.3 V	7	10	15	µA
I_{SDl}	$\overline{SD}$/OD logic ‘0’ input bias current	$\overline{SD}$/OD = 0 V			1	µA
R_{PD_SD}	$\overline{SD}$/OD pull-down resistor	$\overline{SD}$/OD = 3.3 V	220	330	450	kΩ
R_{ON_OD}	$\overline{SD}$/OD on-resistance	$\overline{SD}$/OD = 400 mV, CIN = 2 V	25	40	58	Ω
I_{OL_SD}	$\overline{SD}$/OD low level sink current		7	10	16	mA
t_{OD_fall}	$\overline{SD}$/OD loaded fall time	C_L = 10 nF, R_{PU} = 10 kΩ to 5 V 90% to 10% $\overline{SD}$/OD		0.75		µs
I_{STBYh}	$\overline{STBY}$ logic ‘1’ input bias current	$\overline{STBY}$ = 3.3 V	7	10	15	µA
I_{STBYl}	$\overline{STBY}$ logic ‘0’ input bias current	$\overline{STBY}$ = 0 V			1	µA
R_{PD_STBY}	$\overline{STBY}$ pull-down resistor	$\overline{STBY}$ = 3.3 V	220	330	450	kΩ
R_{ON_FLT}	$\overline{FLT}$ on-resistance	V_{FLT} = 400 mV, VCC = 12 V	60	80	135	Ω
		V_{FLT} = 400 mV, VCC = 3.3 V	90	145	200	Ω
I_{OL_FLT}	$\overline{FLT}$ low level sink current	V_{FLT} = 400 mV	3	5	7	mA
I_{FLTh}	$\overline{FLT}$ high level bias current (when off)	V_{FLT} = 3.3 V			1	µA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{FLTI}	$\overline{FLT}$ low level bias current (when off)	V_{FLT} = 0 V			1	µA
$V_{VCC-FLT}$	Min VCC voltage forcing $\overline{FLT}$ low				3.3	V
t_{Don}	LIN/HIN to GL/GH gate driver turn-on propagation delay	LIN or HIN = 0 V to 3.3 V, C_{GMx} = 0 pF	40	55	70	ns
t_{Doff}	LIN/HIN to GL/GH gate driver turn-off propagation delay	LIN or HIN = 3.3 V to 0 V, C_{GMx} = 0 pF	40	55	70	ns
t_{SDon}	$\overline{SD}$/OD to Gx turn-on propagation delay	$\overline{SD}$/OD = 0 V to 3.3 V, C_{GMx} = 0 pF	45	65	100	ns
t_{SDoff}	$\overline{SD}$/OD to Gx turn-off propagation delay	$\overline{SD}$/OD = 3.3 V to 0 V, C_{GMx} = 0 pF	40	65	100	ns
$t_{STBYoff}$	Standby to output turn-off propagation delay	$\overline{STBY}$ = 3.3 V to 0 V, C_{GMx} = 0 pF	40	70	100	ns
t_{STBY}	Minimum time to enter low consumption	$\overline{STBY}$ = 3.3 V to 0 V (2)	0.7		2	µs
$t_{STBY-FLT}$	Standby enters signaling to $\overline{FLT}$	$\overline{STBY}$ = 3.3 V to 0 V $\overline{FLT}$ = 10 kΩ pull up to 5 V		1		µs
t_{WU}	Wake-up time from standby	$\overline{STBY}$ = 0 V to 3.3 V, LIN = 3.3 V *(Time from $\overline{STBY}$ rising to GL rising)*			5	µs
t_{WU-FLT}	Standby end signaling to $\overline{FLT}$	$\overline{STBY}$ = 0 V to 3.3 V, $\overline{FLT}$ = 10 kΩ pull up to 5 V *(Time from $\overline{STBY}$ rise to V_{FLT} 1.8 V)*		3	5	µs
Comparator protection						
CIN_{th}	Comparator threshold		350	400	450	mV
R_{PD_CIN}	CIN pull-down resistor	CIN = 1 V	75	100	125	kΩ
$t_{CIN-OUT}$	Comparator delay to half bridge output	CIN 0 V to 0.8 V: GH, GL 90%, C_{GMx} = 0 pF		180	230	ns
t_{CIN-OD}	Comparator delay to $\overline{SD}$/OD	CIN 0 V to 0.8 V $\overline{SD}$/OD 90% (10 kΩ to 5 V, C_{OD} = 0 pF)		140	190	ns
$t_{CIN-FLT}$	Comparator delay to $\overline{FLT}$	CIN 0 V to 0.8 V: $\overline{FLT}$ 90% (10 kΩ to 5 V)		140	190	ns
$t_{CINfilter}$	Comparator input filter	CIN pulse 0 - 0.8 V	55	90	125	ns
Overtemperature Protection						
T_{TSD}	Shutdown temperature	(2)		175		°C
T_{HYS}	Temperature hysteresis	(2)		20		°C
t_{TSD}	Overtemperature protection enabling time	(2) After $\overline{STBY}$ = high			20	µs

1. *Tested on wafer.*
2. *Not tested in production: value by characterization on a limited number of samples.*

5.1 Characterization figures

Figure 4. Timing definitions



(a) Soft Switching Transitions

(b) Hard Switching Transitions

Figure 5. Typ I_D vs. V_{DS} at T_J = 25 °C

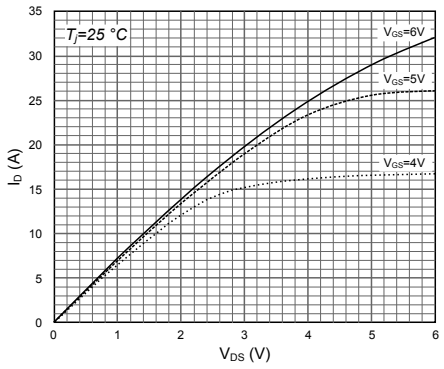


Figure 6. Typ I_D vs. V_{DS} at T_J = 125 °C

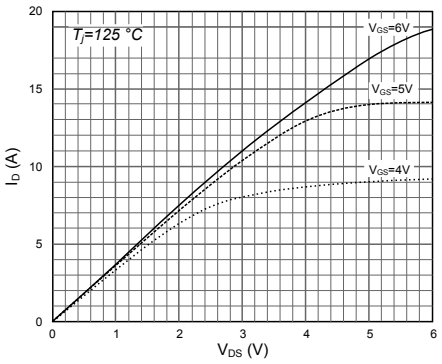


Figure 7. Typ I_S vs. V_{SD} at T_J = 25 °C

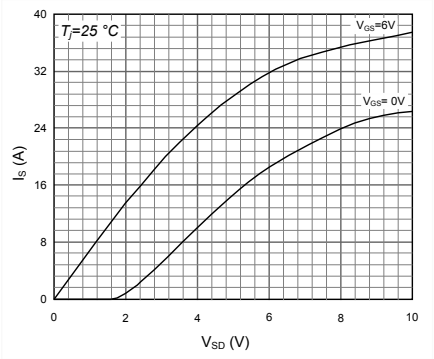


Figure 8. Typ $I_S$vs. V_{SD} at T_J = 125 °C

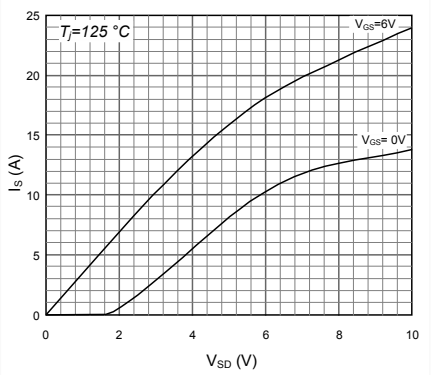


Figure 9. Typ I_D vs. V_{GS} at T_J = 25 °C

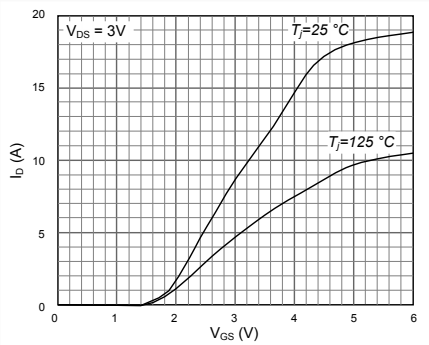


Figure 10. Typ $R_{DS(on)}$ vs. T_J normalized at 25 °C

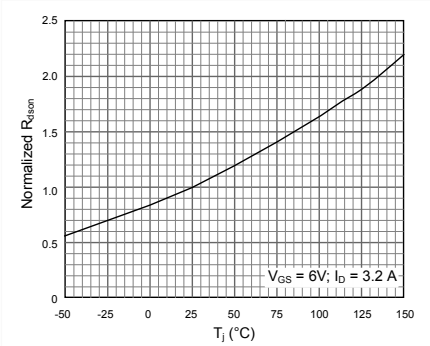


Figure 11. Typ Gate charge at T_J = 25 °C

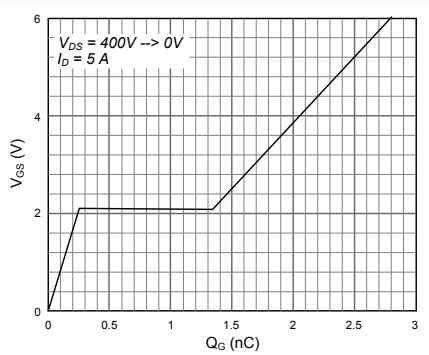


Figure 12. Typ R_{Dboot} vs. T_J

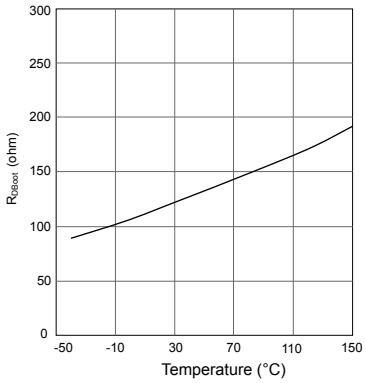


Figure 13. Typ hard-on dV/dt at 400 V (*)

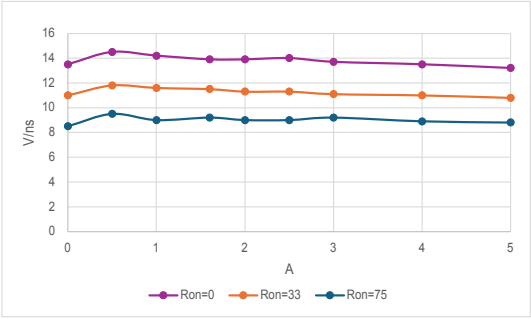


Figure 14. Typ hard-on dV/dt at 300 V (*)

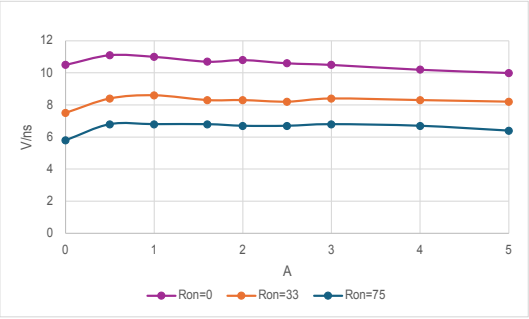
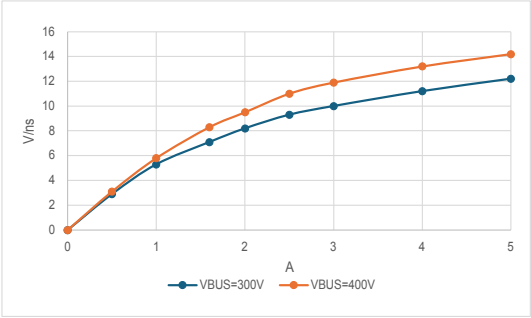


Figure 15. Typ hard-off dV/dt (*)



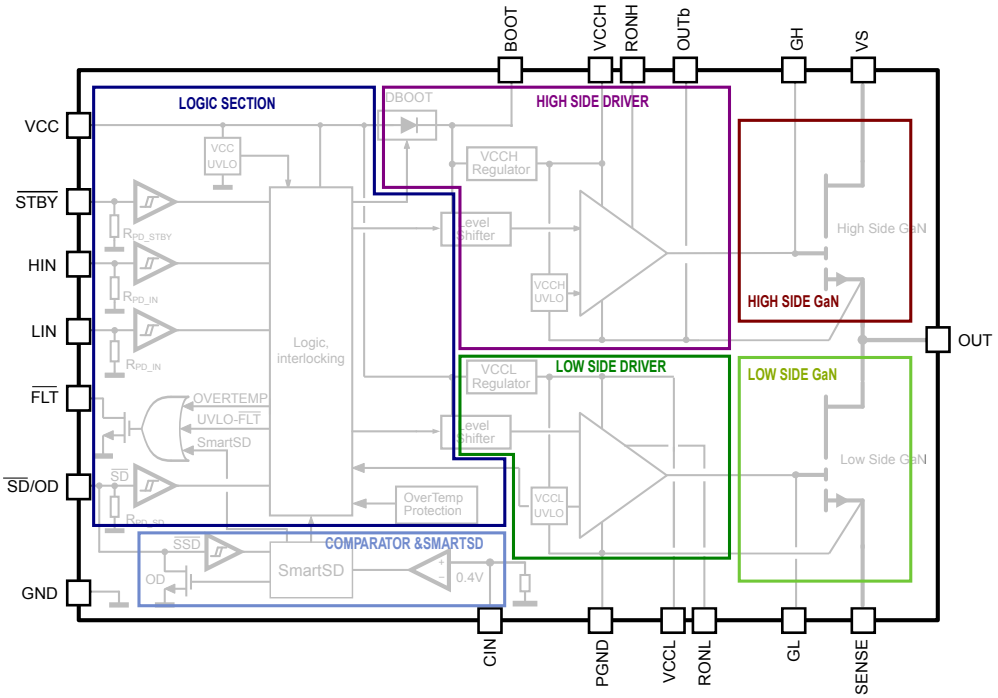
Note: *(*) Refer to Section 6.3.*

6 Device description

6.1 Device structure

Figure 16 is a simplified version of the block diagram of GANSPIN611. It consists of basic structures described in the following sections. Furthermore, GaN's gate terminal is externally accessible.

Figure 16. GANSPIN611 simplified block diagram



6.1.1 GaN power stage

The GaN transistors are the power switches that implement the switching stage of the power topology.

6.1.2 Logic section

This section receives the input signals, manages the system protection (UVLO, comparator and, gate driver overtemperature), and transfers the input pulses to relevant drivers through level shifters.

It is electrically referred to GND pin and supplied by VCC pin.

6.1.3 Comparator and smart shutdown

The embedded comparator, typically used for overcurrent detection, immediately turns off both GaN transistors, leaving the half-bridge in high impedance, once CIN input exceeds the threshold. The event is signaled to the $\overline{SD}$/OD and $\overline{FLT}$ pins.

The smart shutdown (SmartSD) feature allows to automatically keep the switches off for the desired time to cool down the device.

6.1.4 Low-side driver

This block receives input pulses from the level shifter and provides driving action to the low-side GaN transistor.

It is electrically referred to PGND, which is connected to the Kelvin source connection of the low-side GaN transistor. Its input circuitry is supplied by VCC, while an integrated voltage regulator stabilizes the supply voltage of the output stage of the driver (V_{LS}). A UVLO comparator interrupts the half-bridge activity if the regulator's output voltage is insufficient for a proper GaN driving. A dedicated description of UVLO protection is described in the dedicated Section 6.5.2.

A dedicated pin can be used to optionally increase turn-on resistance to lower hard-on dV/dt, while turn-off driving resistance is internally fixed.

The low-side driver has been designed to allow the use of current sense resistors without impacting the applied V_{GS} voltage.

6.1.5 High-side driver

This block receives input pulses from the logic section through the level shifter and provides driving action to the high-side GaN transistor.

It is electrically referred to OUTb, that is connected to the Kelvin source connection of the high-side GaN transistor. Its input circuitry is supplied by the voltage present at BOOT pin, while an integrated voltage regulator stabilizes the supply voltage of the output stage of the driver (V_{HS}). A UVLO comparator interrupts the high-side GaN activity if the regulator's output voltage is insufficient for a proper GaN driving. A dedicated description of UVLO protection is described in the dedicated Section 6.5.4.

A dedicated pin can be used to optionally increase turn-on resistance to lower hard-on dV/dt, while turn-off driving resistance is internally fixed.

This section includes an equivalent bootstrap diode, synchronous with low-side on-time, that generates floating supply voltage (V_{BO}), starting form VCC voltage.

6.2 GaN transistors

The GANSPIN611 embeds two 650 V enhanced mode GaN transistors, connected in a half-bridge configuration. The technology of the embedded GaN transistors does not need bipolar driving: for this reason, negative voltage to turn off the transistor is not necessary.

The low-side GaN transistor is electrically connected between the OUT pin set (drain) and SENSE pin set (source): the SENSE exposed pad also represents a thermal buffer for this transistor. A suitable copper area is required to dissipate the power losses generated during normal operation.

The high-side GaN transistor is electrically connected between VS pins (drain) and OUT pins (source): the OUT exposed pad also represents a thermal buffer for this transistor. As suggested for low-side connection, a suitable copper area is required to dissipate the power losses generated during normal operation.

The embedded GaN transistors do not have intrinsic body diode and, consequently, exhibit zero reverse recovery losses. Nevertheless, the reverse conduction is permitted both during on-state and during off-state. Anti-parallel diodes are not required for proper functionality of the GANSPIN611 in both resonant and hard switching operation.

6.3 Output dV/dt control

The GANSPIN611 internal gate driver is designed to achieve a limited output dV/dt, which is essential for most motor control applications. The maximum dV/dt is set around 10 V/ns for both turn-on and turn-off. The turn-on dV/dt, typically the most critical, can be further reduced by increasing the R_{ONH} and R_{ONL} resistors.

The main reasons to limit dV/dt in motor control applications are:

- **EMI control**: to comply with regulatory emission masks.
- **Motor winding reliability**: in high-voltage applications with long cables, voltage overshoots on motor poles or windings can cause partial discharge, reducing winding lifetime.
- **Ball bearing reliability**: parasitic capacitance between windings and the rotor generates current peaks during dV/dt transitions to chassis earth. If these currents flow through steel ball bearings, they can damage rollers and races, shortening bearing life.

GaN transistors have no recovery losses, so EMI emissions are lower than MOS or IGBT devices at the same dV/dt. Therefore, GaN devices often push dV/dt higher to minimize switching losses. However, EMI remains the primary reason for dV/dt limitation. Motor winding and bearing degradation are less common and usually occur only at very high dV/dt levels in specialized motors.

The actual dV/dt in the system is determined by several factors and, under given driving and load conditions, strongly depends on the motor construction, mainly on the interwinding capacitance. Typically, motors with higher power rating or inductance values tend to exhibit slower dV/dt during transients at a given load current. To adapt the switching behavior to the user's system, the GASPIN611 allows tuning the dV/dt via the R_{ONx} gate resistors, which can be connected between VCCx and RONx pins.

The GANSPIN611 is designed to limit both hard-on and hard-off dV/dt in the range of 10 V/ns when the bus voltage is VS = 320 V_{DC}.

Hard turn-on dV/dt transients show low dependence on the load current value and are influenced by parasitic load capacitance. The maximum turn-on dV/dt (around 15-20 V/ns) is achieved with RONx directly tied to VCCx (R_{ONx} = 0 Ω) on a low parasitic capacitance load.

As shown in Figure 13 and Figure 14, the turn-on speed can be reduced by connecting an SMD resistor (R_{ONx}) between VCCx and RONx pins. This allows fine-tuning of the dV/dt at the cost of a slight increase in E_{on} losses.

Hard turn-on dV/dt approximately follows this formula (which fits the characterization shown in Figure 13 and Figure 14, and is valid for loads with low parasitic capacitance):

$$dV/dt \approx 4.5 \; x \; V_{DC} \; /(120 + R_{ONx}) \quad (1)$$

Hard turn-off dV/dt transients are proportional to the load current and inversely proportional to the total output node capacitance (including motor winding parasitic capacitance, cable and PCB capacitance, and GaN C_{OSS}) at low load current (Figure 15). At higher currents, GANSPIN611 limits hard-off dV/dt to about 10 V/ns to prevent excessive slew rates. The value of the R_{ONx} resistors does not affect hard turn-off dV/dt.

Thanks to the relatively low dV/dt at low currents and the 10 V/ns limit at high currents, reducing hard-off dV/dt is usually unnecessary. If hard-off dV/dt is low in an application, the most likely cause is the high parasitic total capacitance on the OUT node combined with the low load current.

Some customers add a high-voltage capacitor on the output node to reduce both hard-on and hard-off dV/dt, similar to loads with high parasitic capacitance. However, this increases switching losses and reduces efficiency. Therefore, it is recommended to tune dV/dt with R_{ONx} resistors to minimize efficiency losses.

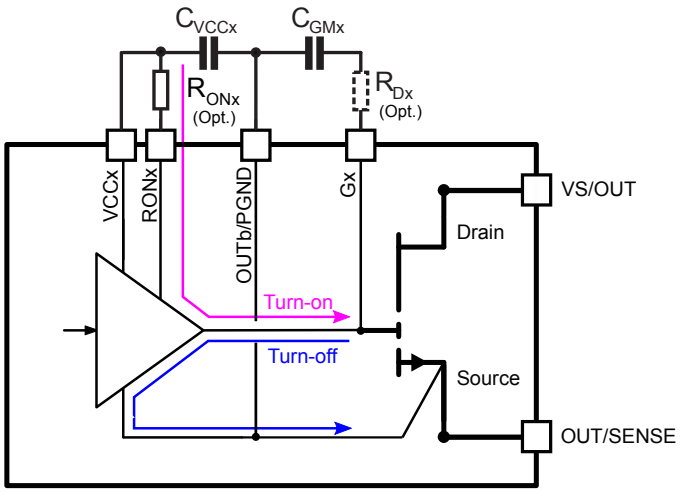
Figure 13, Figure 14 and Figure 15 show dV/dt characterization with different R_{ONx} values versus load current on a load with minimal parasitic capacitance.

These values are similar to those for small motors with short cables (e.g., small hairdryers), but larger motors may exhibit significantly lower dV/dt, sometimes up to half, as observed in some refrigerator compressors or with long cables. Therefore, it is recommended to tune dV/dt on the target motor using R_{ONH} and R_{ONL} resistors.

To avoid induced turn-on phenomena, a capacitor C_{GMx} must be connected to GH and GL as shown in Figure 17.

Increasing C_{GMx} beyond the minimum recommended value has limited effect on hard turn-off dV/dt but increases propagation delay and dead time. A higher C_{GMx} may provide extra margin against induced turn-on at high currents but is usually unnecessary. A small damping resistor R_{Dx} (typically 2.2 Ω) in series with C_{GMx} may be needed for maximum switching current operation, especially with more inductive 2-layer PCBs.

Figure 17. GANSPIN611 gate driving network for dV/dt control



6.4 Truth table and control inputs

The GANSPIN611 has four logic inputs to control the embedded high-side and low-side power transistors.

- LIN: low-side driver input, active high;
- HIN: high-side driver input, active high.
- $\overline{\text{STBY}}$: standby input, active low;
- $\overline{\text{SD}}$/OD: shutdown input, active low.

An open-drain output is there ($\overline{\text{FLT}}$) to communicate externally the operating status of the device. For a proper level of this function, the VCC must be higher than $V_{VCC-FLT}$.

The $\overline{\text{SD}}$/OD pin is also used as an output for the comparator with SmartSD disable time function (see Section 6.7).

Table 6 summarizes the different IC operating modes depending on the input pin configurations.

Output pin configuration and IC consumption are also reported.

Table 6. Truth table

Mode	INPUTS				OUTPUTS			
	$\overline{\text{STBY}}$	$\overline{\text{SD}}$/OD	LIN	HIN	OUT	GL	GH	$\overline{\text{FLT}}$
Standby	L	X	X	X	High-Z	L	L	L
Shutdown	H	L	X	X	High-Z	L	L	H
High-Z	H	H	L	L	High-Z	L	L	H
Low-side on	H	H	H	L	L	H	L	H
High-side on	H	H	L	H	H	L	H	H
Interlocking	H	H	H	H	High-Z	L	L	H
Overcurrent	H	L (1)	X	X	High-Z	L	L	L

1. *Forced low from the internal open-drain when CIN > CIN_{th}.*

The logic inputs have internal pull-down resistors to set a defined logic level even in case of high impedance on signal lines. As a result, the transistors are set to off in the case of unconnected input pins.

The front-end of logic inputs consists of a comparator having a fixed threshold and defined hysteresis to ensure precise and robust level detection. The input pins can accept an input voltage up to 20 V independently from the VCC voltage level.

Propagation delays between LIN and HIN input pins to the transistor's gate are matched to obtain the best symmetry and minimum pulse width distortion.

The minimum duration of the pulse that can be transferred from LIN and HIN to the transistor gate is longer than t_{INmin}; shorter pulses may be blanked.

If a remote controller or monitoring unit can exploit the $\overline{\text{FLT}}$ function, a pull-up current or an external resistor (R_{PU_FLText}) is required to properly detect the activation of the internal open-drain unit. In this case, the high-level voltage can be set to a maximum level of 20 V independently from VCC. When unused, this pin must be connected to GND.

The $\overline{\text{STBY}}$ pin is intended to activate standby mode to reduce the IC consumption during long-lasting inactive times or between burst modes. The description of this mode is reported in Section 6.6.

6.5 Supply rails, LDOs, UVLO protections, and bootstrap diode

The GANSPIN611 is supplied by two rails: VCC, referred to GND, and BOOT referred to OUTb.

Integrated LDOs generate supply voltages for low-side and high-side output stages (V_{LS} and V_{HS}). Undervoltage circuitries monitor VCC, V_{LS} and V_{HS}.

An integrated bootstrap diode is there to generate floating supply voltage for the high-side structure.

6.5.1 VCC supply structure and relevant UVLO protection

The VCC pin supplies the logic circuit, the input structure of the low-side driver, and the integrated bootstrap structure (D_{BOOT}). Low-ESR ceramic capacitors must be connected as close as possible between VCC and GND (100 nF typ., X7R, 50 V).

Undervoltage protection is available on the VCC supply pin. A hysteresis sets the turn-off threshold.

When VCC voltage reaches the V_{CCthON} threshold, the device enters normal operation: if V_{LS} is above UVLO level and the $\overline{STBY}$ pin is high, the $\overline{FLT}$ pin is released and the device sets drivers output according to actual input pins.

When VCC voltage goes below the $V_{CCthOFF}$ threshold, both high-side and low-side gate driver outputs are forced low and the $\overline{FLT}$ pin is forced low to signal the state to remote controllers.

6.5.2 V_{LS} supply structure and relevant UVLO protection

The integrated VCCL regulator is fed by VCC voltage to stabilize the low-side driver output terminal (VCCL, referred to PGND or, shortly V_{LS} = 6 V typ.).

Low-ESR ceramic capacitors must be connected as close as possible between VCCL and PGND (C_{VCCL} recommended value is 100 nF, X7R, 16 V) to obtain a clean supply voltage.

An undervoltage protection is available on the V_{LS} supply voltage that bias the low-side driver output stage.

When V_{LS} voltage reaches the V_{LSthON} threshold, the device enables the low-side driver normal operation.

When V_{LS} voltage goes below the $V_{LSthOFF}$ threshold, both high-side and low-side gate driver outputs are forced low and the $\overline{FLT}$ pin is forced low to signal this condition to the remote controllers.

6.5.3 Bootstrap diode

The GANSPIN611 integrates a bootstrap diode structure connected between the VCC and BOOT pins, to supply the high-side floating supply voltage $V_{BOOT\text{-}OUTb}$ (or shortly V_{BO}). A very low ESR ceramic capacitor (C_{BOOT} to be selected between 100 nF and 3.3 µF, X7R, 50 V) must be placed as close as possible between the BOOT and OUT pins.

The bootstrap DC characteristics are detailed in Figure 12.

The final voltage drop between VCC and V_{BO} depends on multiple factors like duty cycle, operating frequency, GaN gate charge, GaN leakage, temperature, etc. In case the voltage on V_{BO} is not sufficient for a proper VCCH regulator operation, either increasing the VCC value or using an external bootstrap diode can obtain a correct V_{BO} voltage.

A resistor $R_{BOOT} \geq 2.7\ \Omega$ must be placed in series with the above mentioned external bootstrap diode to limit the amount of peak charging current flowing into the internal connection between OUTb and OUT.

6.5.4 V_{HS} supply structure and relevant UVLO protection

The integrated VCCH regulator is connected to the V_{BO} voltage to stabilize the high-side driver output terminal (VCCH, referred to OUTb or, shortly, V_{HS} = 6 V typ.).

The high-side LDO is equipped with fast startup turn-on circuitry to minimize the wake-up time especially during intermittent operation (burst mode).

Low-ESR ceramic capacitors must be connected as close as possible between VCCH and OUTb (C_{VCCH} recommended value is 100 nF, X7R, 16 V) to obtain a clean supply voltage.

An undervoltage protection is available on the V_{HS} supply voltage that bias the high-side driver output stage (VCCH – OUTb).

When V_{HS} voltage reaches the V_{HSthON} threshold, the high-side driver is enabled to accept turn-on/off commands from the input logic block.

When V_{HS} voltage goes below the $V_{HSthOFF}$ threshold, the high-side gate driver output is forced low.

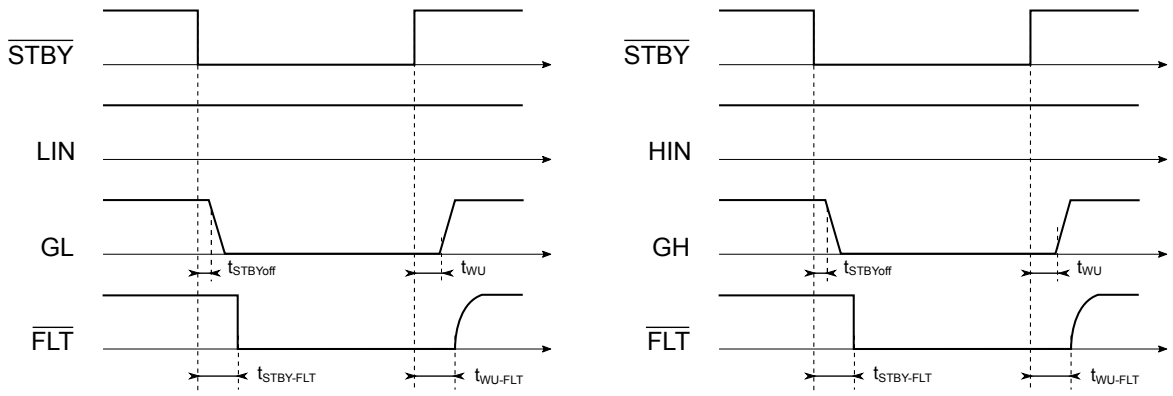
V_{HS} UVLO status is not signaled on the $\overline{FLT}$ pin and the low-side driver continues to operate according to inputs and other protections.

6.6 Standby

The GANSPIN611 is designed to reduce the current consumption of both the logic portion and low-side driver when the $\overline{STBY}$ pin is pulled to GND. Low-side and high-side output are immediately set low to leave the half-bridge in a 3-state, while the $\overline{FLT}$ pin is forced low, and consumption is reduced if the $\overline{STBY}$ pin is pulled to GND for at least t_{STBY}. The overtemperature and the comparator protections are disabled in this operating condition.

Setting the $\overline{STBY}$ pin high, the device wakes up and operation is restored: the $\overline{FLT}$ pin is released within t_{WU-FLT} while the driver's outputs are set according to inputs, providing that relevant UVLOs are not active, within t_{WU}.

Figure 18. Standby timings



6.7 Comparator with SmartSD

The GANSPIN611 integrates a comparator committed to the fault sensing function.

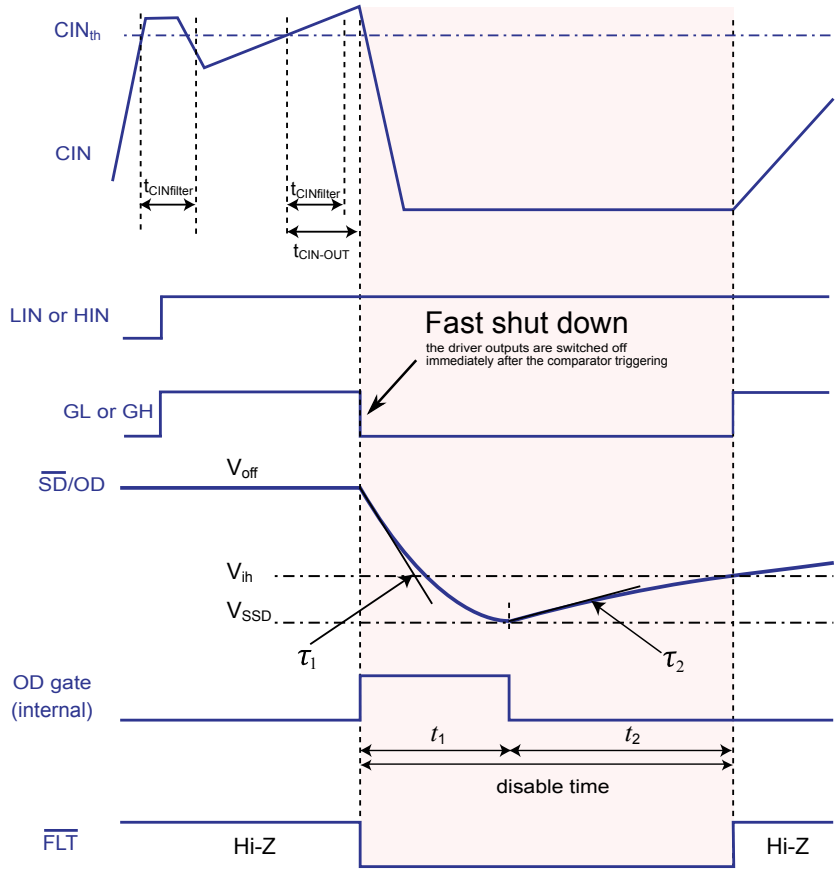
The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function with an automatic OFF-time mechanism (Smart Shutdown) providing the possibility to increase the disable time after the fault event up to an arbitrary value without increasing the delay time of the protection.

The comparator has an internal voltage reference CIN_{th} connected to the inverting input, while the non-inverting input is available on the CIN pin. The output signal of the comparator is filtered from glitches shorter than $t_{CINfilter}$ and then fed to the Smart Shutdown logic.

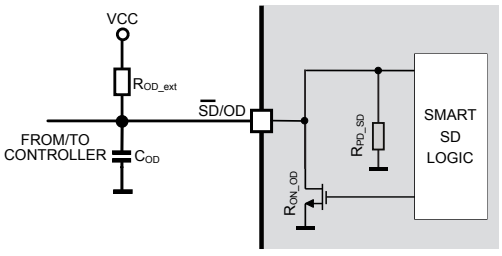
The $\overline{SD}$/OD is connected to a timing capacitor C_{OD} and a pull-up to determine the output disable time of the fault event.

When an overcurrent is detected, gates are immediately turned off, the $\overline{FLT}$ pin is forced low to signal the state to the controller, the $\overline{SD}$/OD pin discharges C_{OD} down to V_{SSD} and then the external pull-up charges it again. Once C_{OD} reaches V_{ih}, the gate driving restarts and $\overline{FLT}$ is released.

Figure 19. Smart Shutdown timing waveforms



SMART SHUTDOWN CIRCUIT
automatic off time



An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{SSD} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{SSD} - V_{off}}{V_{ih} - V_{off}}\right)$$

Where:

$$\tau_1 = \left(R_{ON\_OD} // R_{OD\_ext}\right) \cdot C_{OD}$$

$$\tau_2 = \left(R_{PD\_SD} // R_{OD\_ext}\right) \cdot C_{OD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{OD\_ext}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{OD\_ext}} \cdot V_{BIAS}$$

6.8 Thermal shutdown

The GANSPIN611 provides a thermal shutdown protection feature to protect the gate driver from operating at abnormal temperature.

When, during active mode, the junction temperature reaches the T_{TSD} temperature threshold, the device turns the driver outputs off to leave the half-bridge in 3-state and signals this condition forcing the $\overline{FLT}$ pin low. The status of all the input pins is ignored.

When the junction temperature is lower than T_{TSD}-T_{HYS}, the device operation is restored and the $\overline{FLT}$ pin is released.

Since the temperature sensor is located on the driver-exposed pad EP1, temperature sensing of GaN transistors is typically not accurate: the temperature difference of the GaN exposed pad EP2 and EP3 depends on PCB layout and system cooling.

The overtemperature detection is inactive when the device is operating in standby mode to minimize consumption.

The overtemperature detection is inactive when the device is operating in standby mode or in VCC UVLO to minimize consumption. On standby mode exit or VCC UVLO exit, overtemperature requires t_{TSD} to protect against overtemperature.

7 PCB, BOM, and layout recommendations

7.1 PCB suggestions

This section lists some tips to facilitate the PCB routing of the GANSPIN611.

7.1.1 External BOM values selection and placement

A list of recommended value ranges for some key components are reported.

The bulk capacitors required for VCC, VCCL, VCCH, and BOOT must be placed as close as possible to relevant pins and relevant references. Such capacitors must be low ESR/ESL ceramic components having rated voltages that are almost twice the maximum operating voltages to overcome the well-known value modulation versus bias voltage.

The eventual external bootstrap diode, useful to reduce the high-side startup time, requires a series resistance larger than 2.7 Ω. In case an external bootstrap diode is used, the C_{BOOT} capacitor must be placed on the PCB in a way that the negative terminal is put as close as possible to the OUTb pin: this arrangement ensures that the charging current flows in the shortest track as possible. The lower the R_{BOOT} resistor, the lower high-side startup time but the higher diode recovery losses and EMI. To minimize high-side startup time is recommended to minimize C_{BOOT} and C_{VCCH}. A good trade-off to limit also VCCx ripple is to use C_{VCCH} = C_{VCCL} = 100 nF.

The gate capacitor C_{GMx}, must be adjacent to the GH to OUTb and GL to PGND pins.

The turn-on programming resistors, R_{ONL} and R_{ONH}, used to tune the hard-on dV/dt, must be placed very close to the relevant IC to minimize the length of the track connected to the RONx pin. If not used, a direct connection between the RONx pin and VCCx pin is required

Table 7. External BOM summary

Symbol	Function	Value (range)	Technology	Min. rating
C_{VCC}	VCC large bulk capacitor (it is normally used as bulk capacitor of controller too)	2.2 to 10 µF	EL-Cap (or X7R)	25 V (50 V)
	VCC bypass capacitor	100 nF	X7R	50 V
C_{BOOT}	BOOT to OUTb bypass capacitor	C_{VCCH} to 3300 nF	X7R	50 V
C_{VCCL}	VCCL to PGND bypass capacitor	47 nF to 220 nF	X7R	16 V
C_{VCCH}	VCCH to OUT bypass capacitor	47 nF to 220 nF	X7R	16 V
R_{BOOT}	Current limiting resistor of external D_{BOOT}	≥ 2.7 Ω		
D_{BOOT}	External bootstrap diode (if needed)	STTH1R06 or equivalent	Turbofast	600 V / 1 A
C_{GML}	GL to PGND gate capacitor	680 pF	X7R	16 V
C_{GMH}	GH to OUTb gate capacitor	680 pF	X7R	16 V
R_{ONx}	Turn-on resistors of LS and HS GaNs	0 Ω to 2 kΩ		

To speed-up start-up time, the user shall minimize C_{BOOT} and C_{VCCH}.

Most motor control applications (depending on gate load) are optimized when using C_{VCCx} = 100 nF and C_{BOOT} = 220 to 470 nF. A larger C_{BOOT} capacitor could be rarely required in specific applications if a very long high side on-time is required. On all other applications is recommended to keep C_{BOOT} small to avoid increasing start-up time, the potential need of the additional external bootstrap diode, the diode dissipation. In extreme cases, as in all gate driver applications, excessive C_{BOOT} and small C_{VCC} can lead to VCC drops due to charge sharing when low-side turns on, detected by the VCC UVLO.

PGND is internally connected to the SENSE pin: do not connect externally to any other GND or SENSE route.

OUTb is internally connected to the OUT pin: do not connect externally to the OUT route.

VCCL and VCCH are the output access to the internal voltage regulator: forcing these pins to external voltage regulators may result in unrecoverable damage of the IC.

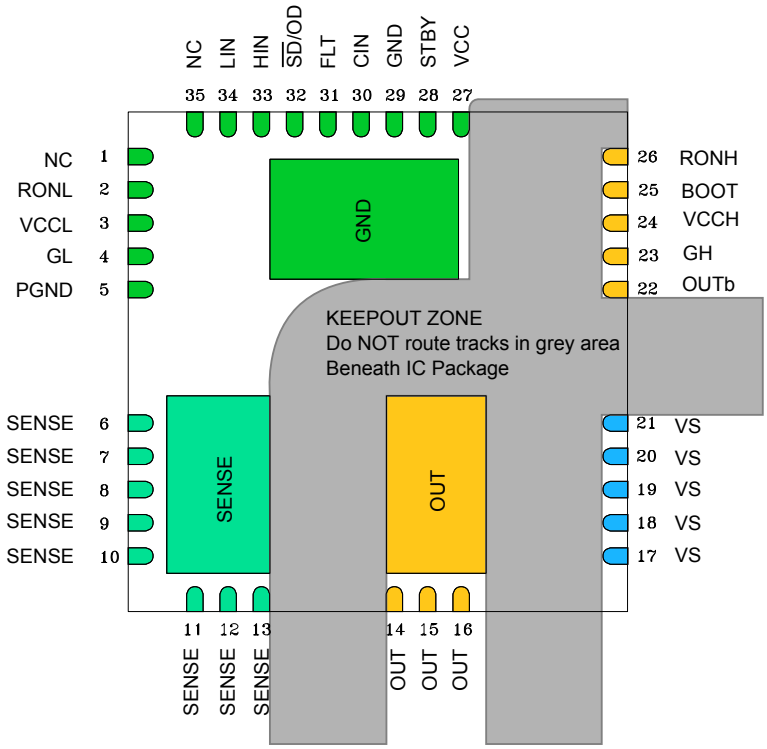
The GANSPIN611 has a comparator that, once connected CIN to the shunt resistor, can provide an effective programmable overcurrent protection.

A GND to PGND ground bounce noise could be present on an applicative board summing to the shunt voltage, determining spurious overcurrent intervention. We recommend using an RC filter on CIN pin to filter out this noise. The filtering capacitor shall be placed adjacent to CIN pin and on the same PCB side of the GANSPIN611 for maximum filtering effect.

7.1.2 Distances

The QNF9x9x1 package is designed to simplify the respect of the safety norms regarding creepage distances. The gray area depicted in Figure 20 represents the distances to maintain the creepages at PCB level. The pin sets are colored differently to represent the pins that are referred to the same voltage reference.

Figure 20. Keepout regions for safety



7.1.3 Noise reduction

To minimize the noise generation during normal operation of typical applications, a few simple steps can be followed:

1. Connect signal GND and power GND to a single star point. Signal ground consists of controller GND and signal GND of the GANSPIN611.
2. If a shunt resistor is necessary, this component should have very small ELS and be placed as close as possible to the GANSPIN611. A standard SMD shunt is typically suitable, but in the case of high current transients resulting in high dI/dt, lower ESL could be required. A cheaper alternative to a low ESL resistor consists of the parallel of multiple smaller resistors (for example, 3x 0603 SMD resistors have similar ESL of a 1020 package shunt resistor and is much lower than a 2010 standard package).
3. To minimize parasitic capacitance and noise generation, it is preferable to route the OUT node very closely to the load minimizing the overlap with any other nets.
4. Components connected to BOOT, VCCH, RONH, and OUTb floats together with the OUT node. They must be placed as close as possible to the listed pins minimizing the overlap with other nets.
5. Keep current loops as small as possible. A high-voltage ceramic capacitor connected between high-voltage bus and power ground and placed as close as possible to the GANSPIN611 facilitates the reduction of such loops.
6. To increase thermal performance and maximum power, thermal vias could be used under SENSE and OUT exposed pads. However, keep the high-voltage power loop made with the VS ceramic capacitor as close and as small as possible to minimize stray inductance. Due to the intrinsic small capacitance of GaN and a VS high stray inductance, some oscillations could be observed after a dI/dt transition. In such cases, adding a 1-2.2 Ω resistor in series to the GH/GL capacitance helps to dump those oscillations faster.

Heat generated by the IC can be dissipated using exposed pads:

1. SENSE and OUT exposed pads are intended to spread out the heat generated by the GaN during switching activity. The use of standard vias beneath the EPs helps to both transfer heat between different layers and minimize the risk of voids (air bubbles) between IC’s exposed pads and PCB footprint. Keep the ground return track of the VS ceramic capacitor as close as possible to the device. Consider that the copper layer on the same side of the device is the most thermally efficient since vias add a resistive contribution on the thermal transfer.
2. The GND exposed pad dissipates only the gate driver power, which is typically low in the relatively low frequency hard switching applications (compared to the high frequency resonant applications). It is recommended to exploit PCB space to dissipate the OUT and SENSE exposed pads.
3. The VS pin set is not responsible for thermal dissipation: the net connected to this potential has to be sized for RMS current only.
4. High copper thickness (2 oz) improves the heat spreading and helps to transfer far from the IC. Smaller support thickness (for example, FR4 – 1 mm instead of 1.6 mm) helps to transfer the heat between copper layers, but care should be taken on parasitic capacitance generation and board robustness.

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN 9 x 9 x 1 mm, 35 leads, 0.6 mm pitch, package information

Table 8. QFN 9 x 9 x 1 mm, 35 leads, 0.6 mm pitch, package dimensions

Symbol	Dimensions [mm]		
	Min.	Typ.	Max
A	0.90	0.98	1.05
A3	-	0.127	-
b	0.25	0.30	0.35
D	8.96	9.00	9.04
E	8.96	9.00	9.04
D1	3.30	3.40	3.50
E1	2.06	2.16	2.26
D2	1.76	1.86	1.96
E2	3.10	3.20	3.30
D3	1.70	1.80	1.90
E3	3.10	3.20	3.30
e	-	0.6 Ref	-
K	0.2	-	-
L	0.35	0.45	0.55
n (1)	35		
	TOLERANCE		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

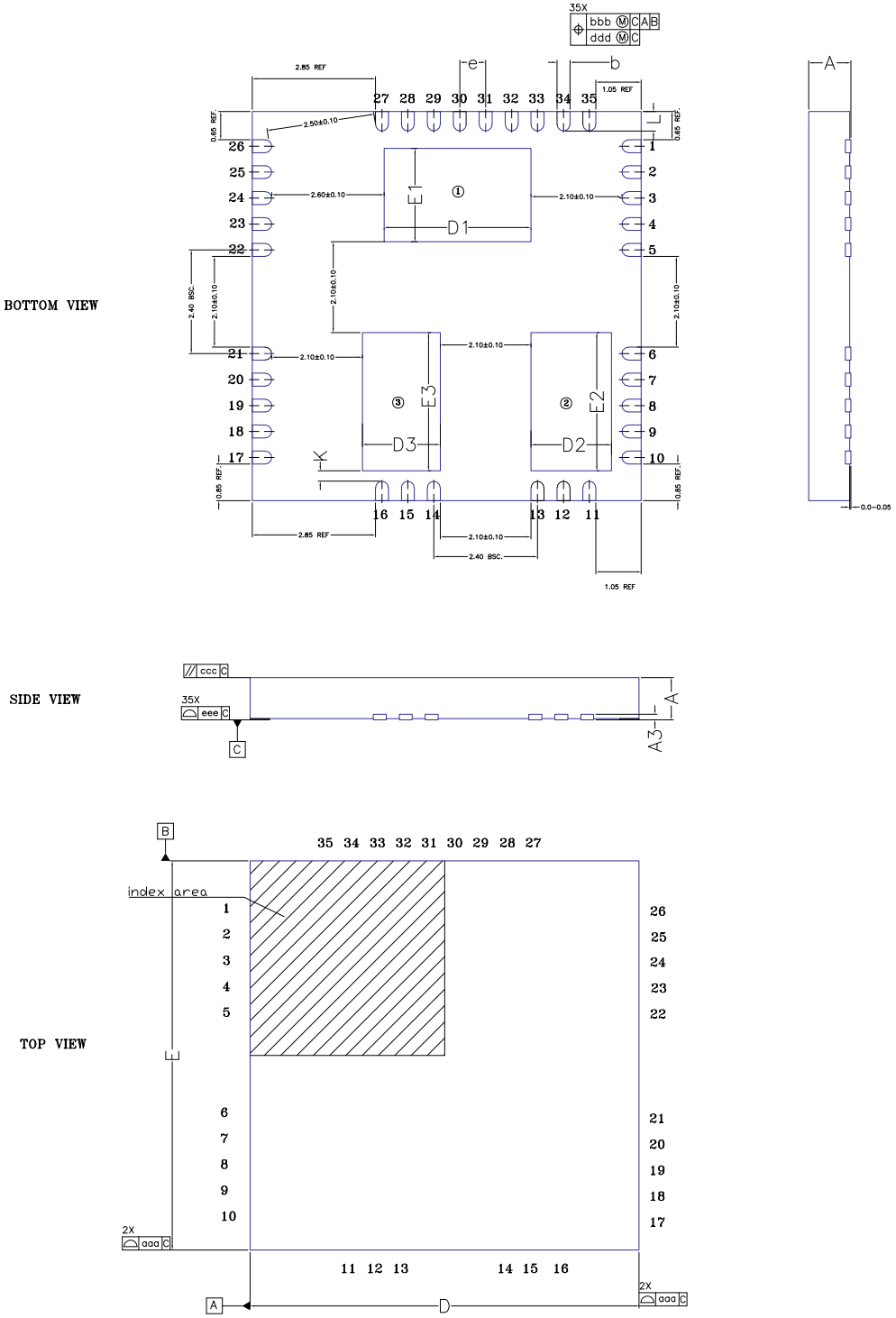
1. *n is the total number of terminals*

Note: Dimensioning and tolerances conform to ASME Y14.5-2009.

Note: Dimensions do not include mold protrusion, not to exceed 0.15 mm.

Note: Package outline exclusive of metal burr dimensions.

Figure 21. **QFN 9 x 9 x 1 mm, 35 leads, 0.6 mm pitch, package outline**



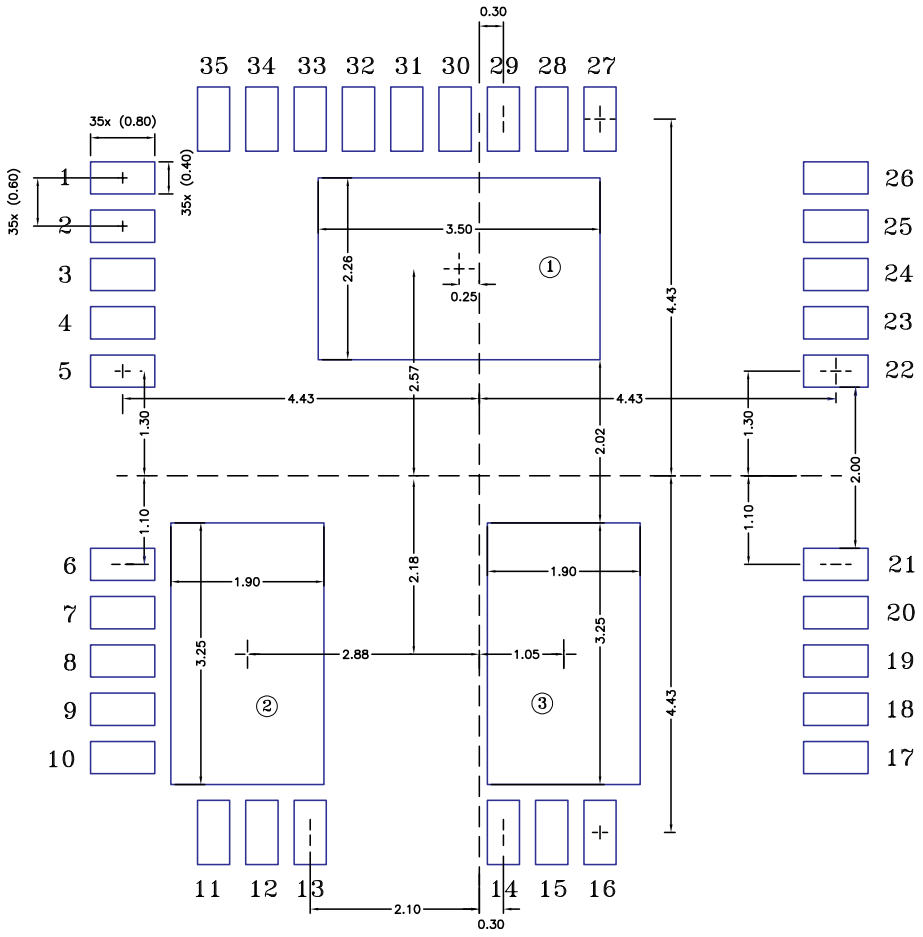
8.2 Suggested footprint

The GANSPIN611 footprint for the PCB layout is usually defined based on several design factors such as assembly plant technology capabilities and board component density. For easy device usage and evaluation, STMicroelectronics provides the following footprint design, which is suitable for the largest variety of PCBs.

The following footprint indicates the copper area that should be free from the solder mask, while the copper area could extend beyond the indicated areas especially for EP2 and EP3. To aid thermal dissipation, it is recommended to add, if possible, thermal vias under these EPADs to transfer and dissipate device heat to the other PCB copper layers.

A PCB layout example is available with the GANSPIN611 evaluation board.

Figure 22. QFN 9 x 9 x 1 mm, 35 leads, 0.6 mm pitch, suggested footprint



9 Ordering information

Table 9. **Order code**

Order code	Package	Package marking	Packing
GANSPIN611	QFN 9x9x1 mm	GANSPIN611	Tray
GANSPIN611TR	QFN 9x9x1 mm	GANSPIN611	Tape and Reel

Revision history

Table 10. **Document revision history**

Date	Version	Changes
26-Sep-2025	1	Initial release.
10-Feb-2026	2	Updated document title. Updated Figure 2 and label of Figure 10; added Figure 13, Figure 14, and Figure 15. Updated Table 2 (added note (4) to PGND), Table 3 (added note (1)), Table 5 (general testing conditions), Table 9 (package marking). Added Section 6.3.

Contents

List of tables

List of figures

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