HVLED815PF

Offline LED driver with primary-sensing and high power factor up to 15 W

Datasheet - production data

Features

- High power factor capability (> 0.9)
- 800 V, avalanche rugged internal 6 Ω Power MOSFET
- Internal high voltage startup
- Primary sensing regulation (PSR)
- ± 3% accuracy on constant LED output current
- Quasi-resonant (QR) operation
- Optocoupler not needed
- Open or short LED string management
- Automatic self supply

Applications

- AC-DC LED driver bulb replacement lamps up to 15 W, with high power factor
- AC-DC LED drivers up to 15 W

Description

The HVLED815PF device is a high voltage primary switcher intended for operating directly from the rectified mains with minimum external parts and enabling high power factor (> 0.90) to provide an efficient, compact and cost effective solution for LED driving. It combines a high-performance low voltage PWM controller chip and an 800 V, avalanche rugged Power MOSFET, in the same package. There is no need for the optocoupler thanks to the patented primary sensing regulation (PSR) technique. The device assures protection against LED string fault (open or short).

Table 1. Device summary

<table>
<thead>
<tr>
<th>Order code</th>
<th>Package</th>
<th>Packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td>HVLED815PF</td>
<td>SO16N</td>
<td>Tube</td>
</tr>
<tr>
<td>HVLED815PFTR</td>
<td>SO16N</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>
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1 Principle application circuit and block diagram

1.1 Principle application circuit

Figure 1. Application circuit for high power factor LED driver - single range input
Figure 2. Application circuit for standard LED driver
1.2 Block diagram

Figure 3. Block diagram
## 2 Pin description and connection diagrams

### Figure 4. Pin connection (top view)

![Pin connection diagram](image)

### 2.1 Pin description

<table>
<thead>
<tr>
<th>No.</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SOURCE</td>
<td>Source connection of the internal power section.</td>
</tr>
<tr>
<td>2</td>
<td>CS</td>
<td>Current sense input. Connect this pin to the SOURCE pin (through an R₁ resistor) to sense the current flowing in the MOSFET through an RSENSE resistor connected to GND. The CS pin is also connected through dedicated R₀OS, R₀FF resistors to the input and auxiliary voltage, in order to modulate the input current flowing in the MOSFET according to the input voltage and therefore achieving a high power factor. See Section 4.11: High power factor implementation on page 26 for more details. The resulting voltage is compared with the voltage on the ILED pin to determine MOSFET turn-off. The pin is equipped with 250 ns blanking time after the gate drive output goes high for improved noise immunity. If a second comparison level located at 1 V is exceeded, the IC is stopped and restarted after VCC has dropped below 5 V.</td>
</tr>
<tr>
<td>3</td>
<td>VCC</td>
<td>Supply voltage of the device. A capacitor, connected between this pin and ground, is initially charged by the internal high voltage startup generator; when the device is running, the same generator keeps it charged in case the voltage supplied by the auxiliary winding is not sufficient. This feature is disabled in case a protection is tripped. A small bypass capacitor (100 nF typ.) to GND may be useful to get a clean bias voltage for the signal part of the IC.</td>
</tr>
</tbody>
</table>
2.2 Thermal data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max. value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RthJP</td>
<td>Thermal resistance, junction to pin</td>
<td>10</td>
<td>°C/W</td>
</tr>
<tr>
<td>RthJA</td>
<td>Thermal resistance, junction to ambient</td>
<td>110</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ptot</td>
<td>Maximum power dissipation at TA = 50 °C</td>
<td>0.9</td>
<td>W</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature range</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction temperature range</td>
<td>-40 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Table 3. Thermal data
3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>1, 13 - 16</td>
<td>Drain-to-source (ground) voltage</td>
<td>-1 to 800</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>1, 13 - 16</td>
<td>Drain current$^{(1)}$</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>$E_{av}$</td>
<td>1, 13 - 16</td>
<td>Single pulse avalanche energy ($T_J = 25 , ^\circ C, I_D = 0.7 , A$)</td>
<td>50</td>
<td>mJ</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>3</td>
<td>Supply voltage ($I_{CC} &lt; 25 , mA$)</td>
<td>Self limiting</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DMG}$</td>
<td>6</td>
<td>Zero current detector current</td>
<td>±2</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{CS}$</td>
<td>2</td>
<td>Current sense analog input</td>
<td>-0.3 to 3.6</td>
<td>V</td>
</tr>
<tr>
<td>$V_{COMP}$</td>
<td>7</td>
<td>Analog input</td>
<td>-0.3 to 3.6</td>
<td>V</td>
</tr>
</tbody>
</table>

$^{(1)}$ Limited by maximum temperature allowed.

3.2 Electrical characteristics

Table 5. Electrical characteristics$^{(1)}$ (2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(BR)}DSS$</td>
<td>Drain-source breakdown</td>
<td>$I_D &lt; 100 , \mu A; T_J = 25 , ^\circ C$</td>
<td>800</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>OFF-state drain current</td>
<td>$V_{DS} = 750 , V; T_J = 125 , ^\circ C$$^{(3)}$ See Figure 5</td>
<td>80</td>
<td></td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>Drain-source ON-state resistance</td>
<td>$I_D = 250 , mA; T_J = 25 , ^\circ C$</td>
<td>6</td>
<td>7.4</td>
<td></td>
<td>\Omega</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 , mA; T_J = 125 , ^\circ C$$^{(3)}$ See Figure 6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{OSS}$</td>
<td>Effective (energy related) output capacitance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High voltage startup generator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{START}$</td>
<td>Min. drain start voltage</td>
<td>$I_{CHARGE} &lt; 100 , \mu A$</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>$I_{CHARGE}$</td>
<td>$V_{CC}$ startup charge current</td>
<td>$V_{DRAIN} &gt; V_{Start}; V_{CC} &lt; V_{CCOn}$ $T_J = 25 , ^\circ C$</td>
<td>4</td>
<td>5.5</td>
<td>7</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DRAIN} &gt; V_{Start}; V_{CC} &lt; V_{CCOn}$</td>
<td></td>
<td></td>
<td></td>
<td>+/- 10%</td>
</tr>
<tr>
<td>$V_{CC_RESTART}$</td>
<td>$V_{CC}$ restart voltage (VCC falling)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>After protection tripping</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Operating range</td>
<td>After turn-on</td>
<td>11.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC_ON}$</td>
<td>Turn-on threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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### Table 5. Electrical characteristics (1) (2) (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC_OFF</td>
<td>Turn-off threshold</td>
<td>(4)</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>V</td>
</tr>
<tr>
<td>VZ</td>
<td>Internal Zener voltage</td>
<td>I CC = 20 mA</td>
<td>23</td>
<td>25</td>
<td>27</td>
<td>V</td>
</tr>
</tbody>
</table>

### Supply current

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC_START-UP</td>
<td>Startup current</td>
<td>See Figure 7</td>
<td>200</td>
<td>300</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Iq</td>
<td>Quiescent current</td>
<td>See Figure 8</td>
<td>1</td>
<td>1.4</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Operating supply current at 50 kHz</td>
<td>See Figure 9</td>
<td>1.4</td>
<td>1.7</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Iq(fault)</td>
<td>Fault quiescent current</td>
<td>See Figure 10</td>
<td>250</td>
<td>350</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

### Startup timer

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSTART</td>
<td>Start timer period</td>
<td></td>
<td>105</td>
<td>140</td>
<td>175</td>
<td>µs</td>
</tr>
<tr>
<td>TRESTART</td>
<td>Restart timer period during burst mode</td>
<td></td>
<td>420</td>
<td>500</td>
<td>700</td>
<td>µs</td>
</tr>
</tbody>
</table>

### Demagnetization detector

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDmgdb</td>
<td>Input bias current</td>
<td>V DMG = 0.1 to 3 V</td>
<td>0.1</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>VDMGH</td>
<td>Upper clamp voltage</td>
<td>I DMG = 1 mA</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VDMGL</td>
<td>Lower clamp voltage</td>
<td>I DMG = - 1 mA</td>
<td>-90</td>
<td>-60</td>
<td>-30</td>
<td>mV</td>
</tr>
<tr>
<td>VDMGA</td>
<td>Arming voltage</td>
<td>Positive-going edge</td>
<td>100</td>
<td>110</td>
<td>120</td>
<td>mV</td>
</tr>
<tr>
<td>VDMGT</td>
<td>Triggering voltage</td>
<td>Negative-going edge</td>
<td>50</td>
<td>60</td>
<td>70</td>
<td>mV</td>
</tr>
<tr>
<td>TBLANK</td>
<td>Trigger blanking time after MOSFET turn-off</td>
<td>V COMP ≥ 1.3 V</td>
<td>6</td>
<td>30</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>VCOMP</td>
<td>Upper COMP voltage</td>
<td>V DMG = 2.3 V, V COMP = 1.65 V</td>
<td>70</td>
<td>100</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>VCOMPL</td>
<td>Lower COMP voltage</td>
<td>V DMG = 2.7 V, V COMP = 1.65 V</td>
<td>400</td>
<td>750</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

### Line feedforward

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFF</td>
<td>Equivalent feedforward resistor</td>
<td>I DMG = 1 mA</td>
<td>45</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

### Transconductance error amplifier

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF</td>
<td>Voltage reference</td>
<td>T J = 25 °C</td>
<td>2.45</td>
<td>2.51</td>
<td>2.57</td>
<td>V</td>
</tr>
<tr>
<td>gm</td>
<td>Transconductance</td>
<td>∆I COMP = ± 10 µA</td>
<td>1.3</td>
<td>2.2</td>
<td>3.2</td>
<td>ms</td>
</tr>
<tr>
<td>Gv</td>
<td>Voltage gain</td>
<td>(5) Open loop</td>
<td>73</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>GB</td>
<td>Gain-bandwidth product</td>
<td>(6) Open loop</td>
<td>500</td>
<td></td>
<td></td>
<td>KHz</td>
</tr>
</tbody>
</table>

### Hysteresis

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCOMPBM</td>
<td>Burst mode threshold</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

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### Table 5. Electrical characteristics (1) (2) (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VILEDx</td>
<td>Maximum value</td>
<td>V_COMP = V_COMPL</td>
<td>1.5</td>
<td>1.6</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>V_CLED</td>
<td>Current reference voltage</td>
<td>(6) V_LD = 0.4 V, V_DM = 0 V, T_J = 25 °C</td>
<td>207.76</td>
<td>212</td>
<td>216.24</td>
<td>mV</td>
</tr>
</tbody>
</table>

### Current sense

<table>
<thead>
<tr>
<th>tLEB</th>
<th>Leading-edge blanking</th>
<th>(5)</th>
<th>330</th>
<th></th>
<th></th>
<th>ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_D</td>
<td>Delay-to-output (H-L)</td>
<td></td>
<td>90</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>V_Csx</td>
<td>Max. clamp value</td>
<td>(4) dVcs/dt = 200 mV/µs</td>
<td>0.7</td>
<td>0.75</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>V_Csds</td>
<td>Hiccup mode OCP level</td>
<td>(4)</td>
<td>0.92</td>
<td>1</td>
<td>1.08</td>
<td>V</td>
</tr>
</tbody>
</table>

1. V_CC = 14 V (unless otherwise specified).
2. Limits are production tested at T_J = T_A = 25 °C, and are guaranteed by statistical characterization in the range T_J -25 to +125 °C.
3. Not production tested, guaranteed statistical characterization only.
4. Parameters tracking each other (in the same section).
5. Guaranteed by design.
6. Production tested only.

### Figure 5. OFF-state drain and source current test circuit

![Figure 5. OFF-state drain and source current test circuit](image)

**Note:** The measured I_DS is the sum between the current across the startup resistor and the effective MOSFET's OFF-state drain current.
Figure 6. C\text{OSS} output capacitance variation

![Graph showing C\text{OSS} variation with V\text{ds}]

Figure 7. Startup current test circuit

![Circuit diagram for startup current test]

Figure 8. Quiescent current test circuit

![Circuit diagram for quiescent current test]

\[
l_q = l_{q_{\text{meas}}} - \frac{0.11 \times 3V}{3.3k\Omega} - 100\mu A
\]
Figure 9. Operating supply current test circuit

Note: The circuit across the DMG pin is used for switch on synchronization.

Figure 10. Quiescent current during fault test circuit
4 Device description

The HVLED815PF device is a high voltage primary switcher intended for operating directly from the rectified mains with minimum external parts to provide high power factor (> 0.90) and an efficient, compact and cost effective solution for LED driving. It combines a high-performance low voltage PWM controller chip and an 800 V, avalanche rugged Power MOSFET, in the same package.

The PWM is a current mode controller IC specifically designed for ZVS (“Zero Voltage Switching”) flyback LED drivers, with constant output current (CC) regulation using primary sensing feedback (PSR). This eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sense on the secondary side, while still maintaining a good LED current accuracy. Moreover, it guarantees a safe operation when short-circuit of one or more LEDs occurs.

The device can also provide a constant output voltage regulation (CV): it allows the application to be able to work safely when the LED string opens due to a failure.

In addition, the device offers the shorted secondary rectifier (i.e. LED string shorted due to a failure) or transformer saturation detection.

Quasi-resonant operation is achieved by means of a transformer demagnetization sensing input that triggers MOSFET turn-on. This input serves also as both output voltage monitor, to perform CV regulation, and input voltage monitor, to achieve mains-independent CC regulation (line voltage feedforward).

The maximum switching frequency is top limited below 166 kHz, so that at medium-light load a special function automatically lowers the operating frequency while still maintaining the operation as close to ZVS as possible. At very light load, the device enters a controlled burst mode operation that, along with the built-in high voltage startup circuit and the low operating current of the device, helps minimize the residual input consumption.

Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip is able to power itself directly from the rectified mains. This is useful especially during CC regulation, where the flyback voltage generated by the winding drops.

4.1 Application information

The device is an off-line LED driver with all-primary sensing, based on quasi-resonant flyback topology, with high power factor capability. In particular, using different application schematic the device is able to provide a compact, efficient and cost-effective LED driver solution with high power factor (PF > 0.9 - see application schematic in Figure 1 on page 4) or with standard power factor (PF > 0.5/0.6 - see application schematic in Figure 2 on page 5), based on the specific application requirements.

Referring to the application schematic in Figure 1, the IC modulates the input current according to the input voltage providing the high power factor capability (PF > 0.9) keeping a good line regulation. This application schematic is intended for a single range input voltage.

For wide range application a different reference schematic can be used; refer to AN4346 application note for further details.
Moreover, the device is able to work in different modes depending on the LED's driver load condition (see Figure 11):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions (see the hyperbolic-like portion of the curves in Figure 11). Minimum turn-on losses, low EMI emission and safe behavior in short-circuit are the main benefits of this kind of operation.

2. Valley-skipping mode at medium/ light load. Depending on voltage on COMP pin, the device defines the maximum operating frequency of the converter. As the load is reduced, MOSFET's turn-on does not occur any more on the first valley but on the second one, the third one and so on. In this way the switching frequency is no longer increased (piecewise linear portion in Figure 11).

3. Burst mode with no or very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with constant peak current. Decreasing the load result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

**Figure 11. Multi-mode operation of HVLED815PF (constant voltage operation)**

4.2 Power section and gate driver

The power section guarantees safe avalanche operation within the specified energy rating as well as high dv/dt capability. The Power MOSFET has a $V_{\text{DSS}}$ of 800 V min. and a typical $R_{\text{DS(on)}}$ of 6 $\Omega$.

The internal gate driver of the Power MOSFET is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the Power MOSFET cannot be turned on accidentally.
4.3 High voltage startup generator

*Figure 12* shows the internal schematic of the high voltage start-up generator (HV generator). It includes an 800 V-rated N-channel MOSFET, whose gate is biased through the series of a 12 MΩ resistor and a 14 V Zener diode, with a controlled, temperature compensated current generator connected to its source.

The HV generator input is in common with the DRAIN pins, while its output is the supply pin of the device (VCC pin). A mains “UVLO” circuit (separated from the UVLO of the device that sense VCC) keeps the HV generator off if the drain voltage is below VSTART (50 V typical value).

*Figure 12. High voltage start-up generator: internal schematic*

With reference to the timing diagram of *Figure 13*, when power is applied to the circuit and the voltage on the input bulk capacitor is high enough, the HV generator is sufficiently biased to start operating, thus it will draw about 5.5 mA (typical) to the VCC capacitor.

Most of this current will charge the bypass capacitor connected between the VCC pin and ground and make its voltage rise linearly. As soon as the VCC pin voltage reaches the VCC_ON turn on threshold (13 V typ.) the chip starts operating, the internal Power MOSFET is enabled to switch and the HV generator is cut off by the Vcc_OK signal asserted high.

The IC is powered by the energy stored in the VCC capacitor.

The chip is able to power itself directly from the rectified mains: when the voltage on the VCC pin falls below VCC_RESTART (10.5 V typ.), during each MOSFET’s off-time the HV current generator is turned on and charges the supply capacitor until it reaches the VCC_ON threshold.

In this way, the self-supply circuit develops a voltage high enough to sustain the operation of the device. This feature is useful especially during constant current (CC) regulation, when the flyback voltage generated by the auxiliary winding alone may not be able to keep VCC pin above VCC_RESTART.
### 4.4 Secondary side demagnetization detection and triggering block

The demagnetization detection (DMG) and triggering blocks switch on the Power MOSFET if a negative-going edge falling below 50 mV is applied to the DMG pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is used to detect transformer demagnetization for QR operation, where the signal for the DMG input is obtained from the transformer's auxiliary winding used also to supply the IC.

---

**Figure 13. Timing diagram: normal power-up and power-down sequences**

**Figure 14. DMG block, triggering block**

The triggering block is blanked after MOSFET’s turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the DMG circuit.
erroneously. This $T_{\text{BLANK}}$ blanking time is dependent on the voltage on COMP pin: it is
$T_{\text{BLANK}} = 30 \mu s$ for $V_{\text{COMP}} = 0.9$ V, and decreases almost linearly down to $T_{\text{BLANK}} = 6 \mu s$ for
$V_{\text{COMP}} = 1.3$ V.

The voltage on the pin is both top and bottom limited by a double clamp, as illustrated in the
internal diagram of the DMG block of Figure 14. The upper clamp is typically located
at 3.3 V, while the lower clamp is located at -60 mV. The interface between the pin and the
auxiliary winding will be a resistor divider. Its resistance ratio as well as the individual
resistance values will be properly chosen (see Section 4.6, Section 4.7 on page 22 and
Section 4.11 on page 26).

Please note that the maximum $I_{\text{DMG}}$ sunk/sourced current has to not exceed ±2 mA (AMR)
in all the $V_{\text{IN}}$ range conditions. No capacitor is allowed between DMG pin and the auxiliary
transformer.

The switching frequency is top limited below 166 kHz, as the converter's operating
frequency tends to increase excessively at light load and high input voltage.

A starter block is also used to start up the system, that is, to turn on the MOSFET during
converter power-up, when no or a too small signal is available on the DMG pin. The starter
frequency is 2 kHz if COMP pin is below burst mode threshold, i.e. 1 V, while it becomes
8 kHz if this voltage exceeds this value.

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary
winding becomes large enough to arm the DMG circuit, MOSFET's turn-on will start to be
locked to transformer demagnetization, hence setting up QR operation. The starter is
activated also when the IC is in "Constant Current" regulation and the output voltage is not
high enough to allow the DMG triggering.

If the demagnetization completes - hence a negative-going edge appears on the DMG pin -
after a time exceeding time $T_{\text{BLANK}}$ from the previous turn-on, the MOSFET will be turned
on again, with some delay to ensure minimum voltage at turn-on. If, instead, the negative-
going edge appears before $T_{\text{BLANK}}$ has elapsed, it will be ignored and only the first
negative-going edge after $T_{\text{BLANK}}$ will turn-on the MOSFET. In this way one or more drain
ringing cycles will be skipped ("valley-skipping mode", Figure 15) and the switching
frequency will be prevented from exceeding $1/T_{\text{BLANK}}$.

Figure 15. Drain ringing cycle skipping as the load is progressively reduced

Note: That when the system operates in valley skipping-mode, uneven switching cycles may be
observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET
is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for
cycle-by-cycle energy balance may fall in between. Thus one or more longer switching
cycles will be compensated by one or more shorter cycles and vice versa. However, this
mechanism is absolutely normal and there is no appreciable effect on the performance of
the converter or on its output voltage.
4.5 Constant current operation

*Figure 16* presents the principle used for controlling the average output current of the flyback converter.

The voltage of the auxiliary winding is used by the demagnetization block to generate the control signal for the internal MOSFET switch Q. A resistor R in series with it absorbs a current equal to \( \frac{V_{ILED}}{R} \), where \( V_{ILED} \) is the voltage developed across the capacitor \( C_{LED} \) capacitor.

The flip-flop's output is high as long as the transformer delivers current on secondary side. This is shown in *Figure 17*.

*Figure 16. Current control principle*

*Figure 17. Constant current operation: switching cycle waveforms*
The capacitor $C_{LED}$ has to be chosen so that its voltage $V_{ILED}$ can be considered as a constant. Since it is charged and discharged by currents in the range of some ten µA ($I_{REF} = 20$ µA typ.) at the switching frequency rate, a capacitance value in the range 4.7 - 10 nF is suited for switching frequencies in the ten kHz. When high power factor schematic is implemented, a higher capacitor value should be used (i.e. 1 µF - 10 µF).

The average output current $I_{OUT}$ can be expressed as:

**Equation 1**

$$I_{OUT} = \frac{I_{SEC}}{2} \times \left( \frac{T_{ONSEC}}{T} \right)$$

Where $I_{SEC}$ is the secondary peak current, $T_{ONSEC}$ is the conduction time of the secondary side and $T$ is the switching period.

Taking into account the transformer ratio $N$ between primary and secondary side, $I_{SEC}$ can also be expressed as a function of the primary peak current $I_{PRIM}$:

**Equation 2**

$$I_{SEC} = N \times I_{PRIM}$$

As in steady state the average current $I_{CLED}$:

**Equation 3**

$$[I_{REF} \times (T - T_{ONSEC})] + \left( I_{REF} - \frac{V_{ILED}}{R} \right) \times T_{ONSEC} = 0$$

Which can be solved for $V_{ILED}$:

**Equation 4**

$$V_{ILED} = (R \times I_{REF}) \times \frac{T}{T_{ONSEC}} = V_{CLED} \times \frac{T}{T_{ONSEC}}$$

where $V_{CLED} = R \times I_{REF}$ and it is internally defined (0.2 V typical - see Table 5: Electrical characteristics on page 9).

The $V_{ILED}$ pin voltage is internally compared with the CS pin voltage (constant current comparator):

**Equation 5**

$$V_{CS} = R_{SENSE} \times I_{PRIM} = R_{SENSE} \times \frac{I_{SEC}}{N}$$

Combining (1), (2), (4), and (5) the average output current results:

**Equation 6**

$$I_{OUT} = \frac{N}{2} \times \frac{V_{ILED}}{R_{SENSE}}$$
Equation 6 shows that the average output current $I_{OUT}$ does not depend anymore on the input voltage $V_{IN}$ or the output voltage $V_{OUT}$, neither on transformer inductance values. The external parameters defining the output current are the transformer ratio $n$ and the sense resistor $R_{SENSE}$.

Equation 6 is valid for both standard and high power factor implementation.

4.6 Constant voltage operation

The IC is specifically designed to work in primary regulation and the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode.

Figure 18 shows the internal schematic of the constant voltage mode and the external connections.

Due to the parasitic wires resistance, the auxiliary voltage is representative of the output just when the secondary current becomes zero. For this purpose, the signal on DMG pin is sampled-and-held at the end of transformer's demagnetization to get an accurate image of the output voltage and it is compared with the error amplifier internal reference voltage $V_{REF}$ (2.51 V typ. - see Table 5: Electrical characteristics on page 9).

During the MOSFET's OFF-time the leakage inductance resonates with the drain capacitance and a damped oscillation is superimposed on the reflected voltage. The S/H logic is able to discriminate such oscillations from the real transformer's demagnetization.

When the DMG logic detects the transformer's demagnetization, the sampling process stops, the information is frozen and compared with the error amplifier internal reference. The internal error amplifier is a transconductance type and delivers an output current proportional to the voltage unbalance of the two outputs: the output generates the control voltage that is compared with the voltage across the sense resistor, thus modulating the cycle-by-cycle peak drain current.

The COMP pin is used for the frequency compensation: usually, an RC network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

As a result, the output voltage $V_{OUT}$ at zero-load (i.e. no LED on the LED driver output) can be selected through the $R_{FB}$ resistor in according to Equation 7:

Equation 7

$$R_{FB} = R_{DMG} \cdot \left[ \frac{V_{REF}}{\left( \frac{N_{AUX}}{N_{SEC}} + V_{OUT} \right) - V_{REF}} \right]$$

Where $N_{AUX}$ and $N_{SEC}$ are the auxiliary and secondary turn's number respectively.

The $R_{DMG}$ resistor value can be defined depending on the application parameters (see Section 4.7: Voltage feedforward block).
4.7 Voltage feedforward block

The current control structure uses the $V_{\text{CLED}}$ voltage to define the output current, according to Equation 6 in Section 4.5. Actually, the constant current comparator will be affected by an internal propagation delay $T_D$, which will switch off the MOSFET with a peak current than higher the foreseen value.

This current overshoot will be equal to:

Equation 8

$$\Delta I_{PRIM} = \frac{V_{IN} \cdot T_D}{\xi_p}$$

The previous terms introduce a small error on the calculated average output current set-point, depending on the input voltage.

The HVLED815PF device implements a line feedforward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The internal schematic is shown in Figure 19.
During MOSFET's ON-time the current sourced from DMG pin is mirrored inside the “Feedforward Logic” block in order to provide a feedforward current, $I_{FF}$.

Such “feedforward current” is proportional to the input voltage according to Equation 9:

\[
I_{FF} = \frac{V_{IN} \cdot \frac{N_{AUX}}{N_{PRIM}}}{R_{dmg}} = \frac{V_{IN}}{m \cdot R_{dmg}}
\]

Where $m$ is the primary-to-auxiliary turns ratio.

According to the schematic in Figure 19, the voltage on the non-inverting comparator will be:

\[
V(-) = (R_{SENSE} \cdot I_D) + [I_{FF} \cdot (R_{FF} + R_{SENSE})]
\]

The offset introduced by feedforward compensation will be:

Equation 11

\[
V_{OFFSET} = \frac{V_{IN}}{m \cdot R_{dmg}} \cdot (R_{FF} + R_{SENSE})
\]

As $R_{FF} \gg R_{SENSE}$, the previous one can be simplified as:

Equation 12

\[
V_{OFFSET} = \frac{V_{IN}}{m \cdot R_{dmg}} \cdot R_{FF}
\]

This offset is proportional to $V_{IN}$ and it is used to compensate the current overshoot, according to Equation 13:
Finally, the $R_{DMG}$ resistor can be calculated as follows:

**Equation 14**

$$R_{dmg} = \frac{N_{AUX}}{N_{PRIM}} \cdot \frac{L_p \cdot R_{FF}}{T_D \cdot R_{SENSE}}$$

In this case the peak drain current does not depend on input voltage anymore, and as a consequence the average output current $I_{OUT}$ does not depend from the $V_{IN}$ input voltage.

When high power factor is implemented (see Section 4.11), the feedforward current has to be minimized because the line regulation is assured by the external offset circuitry (see Figure 1: Application circuit for high power factor LED driver - single range input on page 4).

The maximum value is limited by the minimum $I_{DMG}$ internal current needed to guarantee the correct functionality of the internal circuitry:

**Equation 15**

$$R_{dmg}^{MAX} = \frac{N_{AUX}}{N_{PRIM}} \cdot \frac{V_{in\_min\,(ac)} \cdot \sqrt{2}}{100\mu A}$$

### 4.8 Burst mode operation at no load or very light load

When the voltage at the COMP pin falls 65 mV is below the internally fixed threshold $V_{COMPBM}$, the IC is disabled with the MOSFET kept in OFF state and its consumption reduced at a lower value to minimize $V_{CC}$ capacitor discharge.

In this condition the converter operates in burst mode (one pulse train every $T_{START} = 500 \mu s$), with minimum energy transfer.

As a result of the energy delivery stop, the output voltage decreases: after 500 $\mu$s the controller switches on the MOSFET again and the sampled voltage on the DMG pin is compared with the internal reference $V_{REF}$. If the voltage on the EA output, as a result of the comparison, exceeds the $V_{COMPL}$ threshold, the device restarts switching, otherwise it stays OFF for another 500 $\mu$s period.

In this way the converter will work in burst mode with a nearly constant peak current defined by the internal disable level. A load decrease will then cause a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This kind of operation, shown in the timing diagrams of Figure 20 along with the others previously described, is noise-free since the peak current is low.
4.9 Soft-start and starter block

The soft-start feature is automatically implemented by the constant current block, as the primary peak current will be limited from the voltage on the $C_{\text{LED}}$ capacitor.

During the startup, as the output voltage is zero, the IC will start in constant current (CC) mode with no high peak current operations. In this way the voltage on the output capacitor will increase slowly and the soft-start feature will be ensured.

Actually the $C_{\text{LED}}$ value is not important to define the soft-start time, as its duration depends on others circuit parameters, like transformer ratio, sense resistor, output capacitors and load. The user will define the best appropriate value by experiments.

4.10 Hiccup mode OCP

The device is also protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturated flyback transformer. An internal comparator monitors continuously the voltage on CS pin and activates a protection circuitry if this voltage exceeds an internally fixed threshold $V_{\text{CSdis}}$ (1 V typ. - see Table 5: Electrical characteristics on page 9).

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped, the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator will be tripped again a real malfunction is assumed and the device will be stopped.

This condition is latched as long as the device is supplied. While it is disabled, however, no energy is coming from the self-supply circuit; hence the voltage on the $V_{\text{CC}}$ capacitor will decay and cross the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the VCC voltage still needs to go below its restart voltage before the $V_{\text{CC}}$ capacitor is charged again and the device restarted.
Ultimately, this will result in a low-frequency intermittent operation (hiccup mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of Figure 21.

**Figure 21. Hiccup mode OCP: timing diagram**

4.11 **High power factor implementation**

Referring to the principle application schematic in *Figure 1 on page 4*, two contributions are added on the CS pin in order to implement the high power factor capability (through \( R_{PF} \) resistor) and keeping a good line regulation (through \( R_{OS} \) resistor). The application schematic on *Figure 1* is intended for a single range input voltage. For wide range application a different reference schematic can be used; refer to AN4346 application note for further details.

Through the \( R_{PF} \) resistor a contribution proportional to the input voltage is added on the CS pin: as a consequence the input current is proportional to the input voltage during the line period, implementing a high power factor correction. The contribution proportional to the input voltage is generated using the auxiliary winding, as a consequence a diode in series to the \( R_{PF} \) resistor is needed.

Through the \( R_{OS} \) resistor a positive contribution proportional to the average value of the input voltage is added on the CS pin in order to keep a good line regulation.

The voltage contribution proportional to the average value of the input voltage is generated through the low pass filter \( R_A/R_B \) resistor and \( C_{OS} \) capacitor. A diode in series to the \( R_A/R_B \) resistor is suggested to avoid the discharge of \( C_{OS} \) capacitor in any condition.

The \( R_1 \) resistor between CS and SOURCE pin is needed to add on the CS pin also the contribution proportional the output current through the \( R_{SENSE} \) resistor.
The components selection flow starts from the $R_{DMG}$ resistor: this resistor has to be selected in order to minimize the internal feedforward effect.

The maximum selectable value is limited by the minimum internal current circuitry $I_{DMG}$ needed to guarantee the correct functionality of the internal circuitry:

**Equation 16**

$$R_{dmg_{\text{MAX}}} = \frac{N_{AUX}}{N_{PRIM}} \cdot \frac{V_{IN_{\text{MIN}}} \times \sqrt{2}}{100\mu A}$$

where $N_{AUX}$ and $N_{PRIM}$ are the auxiliary and primary turn's number respectively and $V_{IN_{\text{MIN}}}$ is the minimum rms input voltage of the application (i.e. 88 V for 110 Vac or 175 V for 230 Vac range).

The $R_{FB}$ resistor defines the $V_{OUT}$ output voltage value in the open circuit condition (no-load condition, i.e. no LED on the output of LED driver) and it can be selected using the following relationship:

**Equation 17**

$$R_{FB} = R_{DMG} \cdot \left[ \frac{V_{REF}}{\left( \frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT} \right) - V_{REF}} \right]$$

where $N_{AUX}$ and $N_{SEC}$ are the auxiliary and secondary turn's number respectively and $V_{REF}$ is the internal reference voltage ($V_{REF} = 2.51$ V typ - see *Table 5: Electrical characteristics on page 9*).

The $R_{1}$ resistor is typically selected in the range of 500 $\Omega$ - 1.5 k$\Omega$ in order to minimize the internal feedforward effect and to minimize the power dissipation on the $R_{A}/R_{B}$ resistor offset circuitry.
The $R_A$, $R_B$, $R_{OS}$ resistors are selected to add a positive offset on CS pin in order to keep a good line regulation over the input voltage range and can be selected using Equation 18:

$$R_{OS} = R_1 \cdot \left\{ \frac{V_{OS,TYP}}{V_{CLED}} \cdot \frac{N_{SEC}}{V_{OUT} \cdot N_{PRIM}} \cdot \sqrt{2 \cdot P_{OUT} \cdot L_P \cdot F_{SW}} \right\} - 1$$

Where $V_{OS,TYP}$ is the desired voltage across $C_{OS}$ capacitor applying the $V_{IN,TYP}$ typical input voltage (i.e. $V_{IN,TYP} = 220$ V for 176/264 Vac input range); $F_{SW}$ is the switching frequency and can be estimated using Equation 19, where $f_T$ and $f_R$ are the transition and resonant frequency respectively:

$$F_{SW} = \frac{2 \cdot f_T}{1 + \frac{f_T}{f_R} + \sqrt{1 + 2 \cdot \frac{f_T}{f_R}}}$$

**Equation 19**

$$f_T = \frac{1}{2 \cdot P_{OUT} \cdot L_P \cdot \left\{ \frac{1}{V_{IN,TYP} \cdot \sqrt{2}} + \frac{N_{SEC}}{V_{OUT} \cdot N_{PRIM}} \right\}^2}$$

**Equation 20**

$$f_R = \frac{1}{2 \cdot \pi \cdot L_P \cdot C_D}$$

where $C_D$ is the total equivalent capacitor afferent at the drain node.

Based on the desired voltage across the $C_{OS}$ capacitor and calculated $R_{OS}$ resistor, then the sum of $R_A$ and $R_B$ can then calculated as a results of partitioning divider:

$$R_A + R_B = R_{OS} \cdot \frac{\left( V_{IN,TYP} \cdot \sqrt{2} \cdot \frac{2}{\pi} - V_{OS,TYP} \right)}{V_{OS,TYP}}$$

**Equation 22**

Using the previous $R_{OS}$ resistor value the $R_{PF}$ resistor can be estimated using Equation 23:

$$R_{PF} = \frac{\left( V_{IN,TYP} \cdot \sqrt{2} \cdot \frac{N_{AUX}}{N_{PRIM}} \right)}{\left[ \left( V_{IN,TYP} \cdot \sqrt{2} \cdot \frac{N_{AUX}}{N_{PRIM}} + R_{OS} \right) + (V_{OS,TYP} \cdot R_{DMG}) \right]} \cdot (R_{OS} \cdot R_{DMG})$$

**Equation 23**
Finally the current sense resistor $R_{\text{SENSE}}$ can be estimated in order to select the desiderated average output current value:

**Equation 24**

\[
R_{\text{SENSE}} = \frac{N_{\text{PRIM}}}{N_{\text{SEC}}} \cdot \frac{1}{2} \cdot \frac{V_{\text{CLED}}}{I_{\text{OUT}}}
\]

where $V_{\text{CLED}}$ is internally defined (0.2 V typical - see Table 5: Electrical characteristics on page 9).

**System design tips**

Starting from the previous estimated components value, further fine-tuning on the real LED driver board could be necessary and it can be easily done considering that:

- Decreasing/increasing the $R_{\text{PF}}$ resistor value, the power factor effect increases/decreases.
- Decreasing/increasing the $R_{\text{OS}}$ resistor value, the line regulation effect increases/decreases.
- Decreasing/increasing the $R_{\text{OS}}$ resistor value, the $R_A + R_B$ resistors value should be increased/decreased to keep the desiderated voltage across the $C_{\text{OS}}$ capacitor (**Equation 22**).
- Decreasing/increasing the $R_{\text{SENSE}}$ resistor value the average output current increases/decreases (**Equation 24**).

**4.12 Layout recommendations**

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the HVLED815PF device as well. Careful component placing, correct traces routing, appropriate traces widths and compliance with isolation distances are the major issues.

In particular:

- Current sense resistor ($R_{\text{SENSE}}$) should be connected as close as possible to the SOURCE pin, maintaining the trace for the GND as short as possible.
- Resistor connected on CS pin ($R_{\text{OS}}, R_{\text{PF}}, R_1$) should be connected as close as possible to the pin.
- Compensation network ($R_{\text{COMP}}, C_{\text{COMP}}$) should be connected as close as possible to the COMP pin, maintaining the trace for the GND as short as possible.
- Signal ground should be routed separately from power ground, as well from the sense resistor trace.
- DMG partition resistors ($R_{\text{DMG}}, R_{\text{FB}}$) should be connected as close as possible to the DMG pin, minimizing the equivalent parasitic capacitor on DMG pin.
Figure 23. Suggested routing for the LED driver
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 24. SO16N package outline
### Table 6. SO16N package mechanical data

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### Figure 25. SO16N recommended footprint (dimensions are in mm)

![SO16N Recommended Footprint Diagram](image-url)
# Revision history

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**Table 7. Document revision history**

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>26-Jul-2012</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>29-Aug-2012</td>
<td>2</td>
<td>Added Table 2: Pin description on page 7.</td>
</tr>
<tr>
<td>23-Oct-2012</td>
<td>3</td>
<td>Modified T(_J) value on Table 3: Thermal data. Updated T(_J) value in note 2 (below Table 5: Electrical characteristics). Minor text changes.</td>
</tr>
<tr>
<td>31-Jan-2013</td>
<td>4</td>
<td>Added sections from 4.1 to 4.12. Modified Figure 1: Application circuit for high power factor LED driver - single range input and Figure 2: Application circuit for standard LED driver.</td>
</tr>
<tr>
<td>18-Feb-2014</td>
<td>5</td>
<td>Updated Section : Features on page 1 (replaced ± 5% by ± 3% in accuracy on constant LED output current). Updated Table 5: Electrical characteristics (updated Test condition, Values and Units of V(_{\text{LED}}) symbol, added note 6. below Table 5). Updated Section 5: Package information (reversed order of Figure 24: SO16N package outline and Table 6: SO16N package mechanical data, updated titles of Figure 24 and Table 6). Minor modifications throughout document.</td>
</tr>
</tbody>
</table>
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