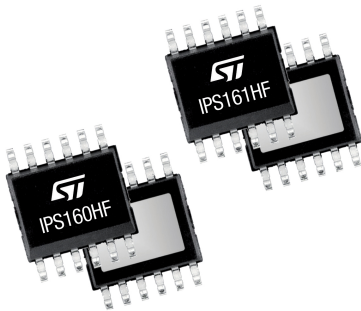


## Single channel high-side switches



## Features

- 8 V to 60 V operating voltage range
- Minimum output current limitation: 0.7 A (IPS161HF) or 2.5 A (IPS160HF)
- Short propagation delay at start-up
- Fast demagnetization of inductive load
- Non-dissipative short-circuit protection (cut-off)
- Programmable cut-off delay time using external capacitor
- Ground disconnection protection
- V<sub>CC</sub> disconnection protection
- Thermal shutdown protection
- Undervoltage lock-out
- Diagnostic signalization for: open load in off-state, cut-off and junction thermal shutdown
- Designed to meet IEC 61131-2
- PowerSSO12 package

## Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Dometics
- General power supply switch


## Description

The [IPS160HF](#) (I<sub>out</sub> = 2.4 A) and [IPS161HF](#) (I<sub>out</sub> = 0.6 A) are monolithic devices which can drive capacitive, resistive or inductive loads with one side connected to ground.

The 60 V operating range and Ron = 60 mΩ, combined with the extended diagnostic (Open Load, Over Load, Overtemperature) and the < 60 us propagation delay time at startup (enabling Class 3 for interface types C and D), make the IC suitable for applications implementing the proper architectures to address higher SIL levels.

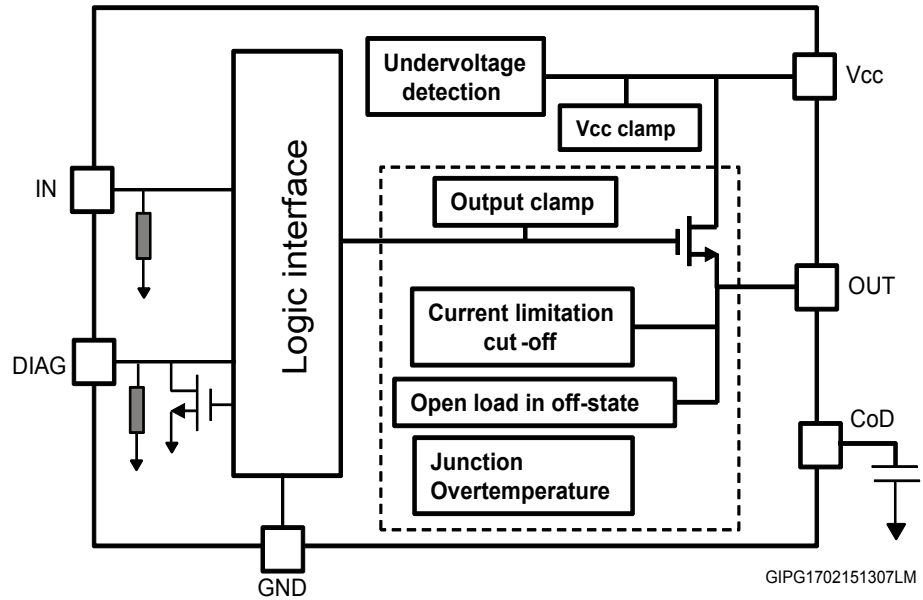
The built-in overload and thermal shutdown protections guarantee the ICs, the application and the load against electrical and thermal overstress. Furthermore, in order to minimize the power dissipation when the output is shorted, a low-dissipative short-circuit protection (cut-off) is implemented to limit the output average current value and consequent device overheating. Cut-off delay time can be set by soldering an external capacitor or disabled by a resistor on pin 4 (CoD).

The DIAG common diagnostic open drain pin reports the open load in off-state, cut-off (overload) and thermal shutdown.

Product status		
IPS160HF		
IPS161HF		
Product label		
		
Product summary		
Order code	IPS160HF	IPS160HFTR
	IPS161HF	IPS161HFTR
Package	PowerSSO12	
Packing	Tube	Tape and reel

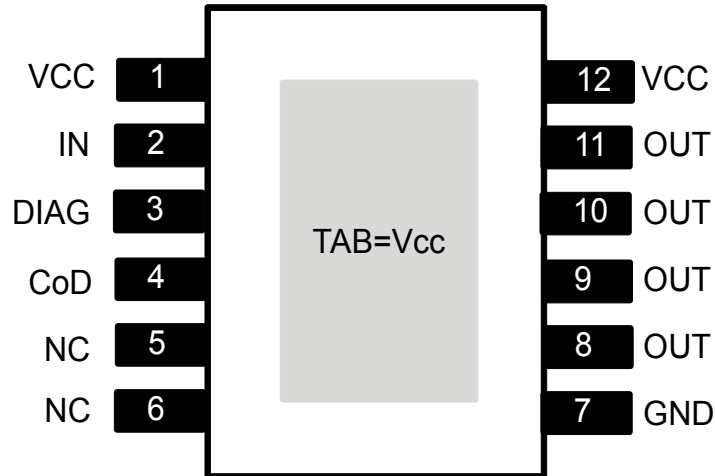
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description

Figure 2. Pin connection (top view)



GIPG1702151321LM

Table 1. Pin configuration

Number	Name	Function	Type
1, 12, TAB	VCC	Device supply voltage	Supply
2	IN	Channel input	Input
3	DIAG	Common diagnostic pin for thermal shutdown, cut-off and open load	Output open drain
4	CoD	Cut-off delay pin, cannot be left floating. Connected to GND by 1 kΩ resistor to disable the cut-off function. Connect to a C <sub>CoD</sub> capacitor to set the cut-off delay see <a href="#">Table 8. Protection and diagnostic</a>	Input
5, 6	NC	Not connected	
7	GND	Device ground	Ground
8, 9, 10, 11	OUT	Channel power stage output	Output

### IN

This pin drives the output stage to pin OUT. IN pin has internal weak pull-down resistors, see [Table 7. Logic inputs](#).

### OUT

Output power transistor is in high-side configuration, with active clamp for fast demagnetization.

### DIAG

This pin is used for diagnostic purposes and is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown, cut-off, or open load in off-state.

### CoD

This pin cannot be left floating and can be used to program the cut-off delay time  $t_{\text{coff}}$ , see [Table 8. Protection and diagnostic](#) through an external capacitor ( $C_{\text{CoD}}$ ). The cut-off function can be completely disabled by connecting the CoD pin to GND through 1 kΩ resistor: in this condition, the output channel remains in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered.

### GND

IC ground.

### VCC

IC supply voltage.

### Reverse polarity

The IC can be protected against reverse polarity using two different solutions:

1. Placing a resistor  $R_{\text{GND}}$  between IC GND pin and load connection point to GND ( $R_{\text{GND}} > V_{\text{CC}}/I_{\text{CC}}$ , see [Table 2. Absolute maximum rating](#)). Note that power dissipated by  $R_{\text{GND}}$  during reverse polarity condition is  $V_{\text{CC}}^2/R_{\text{GND}}$ .
2. Placing a diode in parallel to  $R_{\text{GND}}$

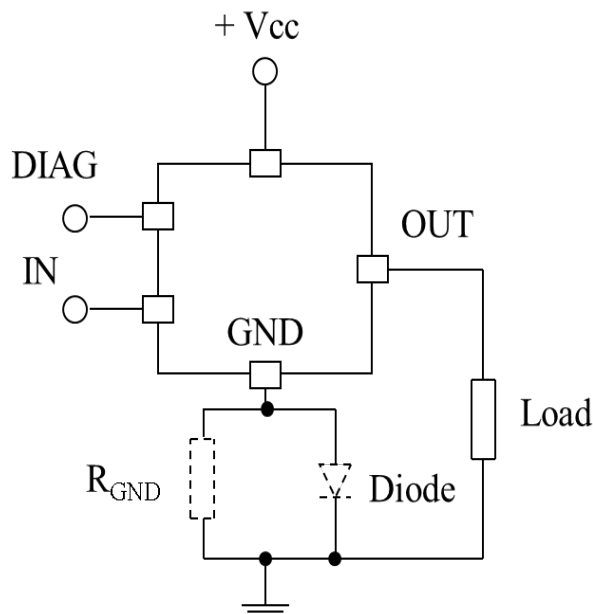
The diode must be selected such that its  $V_{\text{RRM}} > |V_{\text{CC}}|$  and power dissipation capability is higher than  $V_{\text{F}} \cdot I_{\text{S}}$  (see [Table 4](#)).

In normal operation (no reverse polarity), there is a voltage drop ( $\Delta V$ ) between GND of the device and GND of the module.

Using option 1,  $\Delta V = R_{\text{GND}} \cdot I_{\text{CC}}$ .

Using option 2,  $\Delta V = V_{\text{F}}@I_{\text{S}}$ .

**Figure 3. Reverse polarity protection schematic**



### 3 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	-0.3 to 65	V
V <sub>OUT</sub>	Output channel voltage	V <sub>CC</sub> -V <sub>clamp</sub> to V <sub>CC</sub> +0.3	V
I <sub>IN</sub>	Input current	-10 to +10	mA
V <sub>IN</sub>	IN voltage	V <sub>CC</sub>	V
V <sub>COD</sub>	Output cut-off voltage pin	5.5	V
I <sub>COD</sub>	Input current on cut-off pin	-1 to +10	mA
V <sub>DIAG</sub>	Fault voltage	V <sub>CC</sub>	V
I <sub>DIAG</sub>	Fault current	-5 to +10	mA
I <sub>CC</sub>	Maximum DC reverse current flowing through the IC from GND to V <sub>CC</sub>	-250	mA
I <sub>OUT</sub>	Output stage current	Internally limited	A
-I <sub>OUT</sub> <sup>(1)</sup>	Maximum DC reverse current flowing through the IC from OUT to V <sub>CC</sub>	5	
E <sub>AS</sub> <sup>(1)</sup>	Single pulse avalanche energy (T <sub>AMB</sub> = 125 °C, V <sub>CC</sub> = 24 V, I <sub>load</sub> = 0.5 A)	3000	mJ
	Single pulse avalanche energy (T <sub>AMB</sub> = 125 °C, V <sub>CC</sub> = 24 V, I <sub>load</sub> = 1 A)	1000	
P <sub>TOT</sub>	Power dissipation at T <sub>C</sub> = 25 °C <sup>(2)</sup>	Internally limited	W
T <sub>STG</sub>	Storage temperature range	-55 to 150	°C
T <sub>J</sub>	Junction temperature	-40 to 150	

1. Verified on STEVAL-IFP028V1 and STEVAL-IFP034V1 application board

2.  $(T_{JSD(MAX)} - T_C) / R_{th(JA)}$

**Note:** Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		1s	2s2p	2s2p (with 4 thermal vias)	
R <sub>th(JC)</sub>	Thermal resistance junction-case	0.4	0.9	0.5	°C/W
R <sub>th(JA)</sub>	Thermal resistance junction-ambient	117	57	29	

**Note:** R<sub>th(JC)</sub> is intended between the die and the bottom case surface measured by cold plate as per JESD51. R<sub>th(JA)</sub> according JESD51-3 (1s) JESD51-5 (2s2p) and JESD51-7 (2s2p and thermal vias).

## 4 Electrical characteristics

(8 V < V<sub>CC</sub> < 60 V; -40 °C < T<sub>J</sub> < 125 °C, unless otherwise specified)

**Table 4. Supply**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply voltage		V <sub>UVON</sub>		60	V
V <sub>UVON</sub>	Undervoltage on threshold		6.9		8	V
V <sub>UVOFF</sub>	Undervoltage off threshold		6.5		7.8	V
V <sub>UVH</sub>	Undervoltage hysteresis		0.15	0.5		V
I <sub>S</sub>	Supply current in off-state	V <sub>CC</sub> = 24 V		300	500	μA
		V <sub>CC</sub> = 60 V		350	600	
	Supply current in on-state	V <sub>CC</sub> = 24 V		1	1.4	mA
		V <sub>CC</sub> = 60 V		1.4	2.1	
I <sub>LGND</sub>	GND disconnection output current	V <sub>GND</sub> = V <sub>IN</sub> = V <sub>CC</sub> , V <sub>OUT</sub> = 0 V; T <sub>J</sub> = 25°C			0.5	mA
		V <sub>GND</sub> = V <sub>IN</sub> = V <sub>CC</sub> , V <sub>OUT</sub> = 0 V; T <sub>J</sub> = 125°C			0.55	

**Table 5. Output stage**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R <sub>DS(on)</sub>	On-state resistance	V <sub>CC</sub> = 24 V I <sub>OUT</sub> = 1 A @ T <sub>J</sub> = 25 °C		60	80	mΩ
		V <sub>CC</sub> = 24 V I <sub>OUT</sub> = 1 A @ T <sub>J</sub> = 125 °C			120	
V <sub>OUT(OFF)</sub>	Off-state output voltage	V <sub>IN</sub> = 0 V and I <sub>OUT</sub> = 0 A			2	V
I <sub>OUT(OFF)</sub>	Off-state output current	V <sub>CC</sub> = 24 V, V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 0 V			3	μA
		V <sub>CC</sub> = 60 V, V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 0 V			10	
I <sub>OUT(OFF-min)</sub>	Off-state output current	V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 4 V	-35		0	

**Table 6. Switching (V<sub>CC</sub> = 24 V; -40 °C < T<sub>J</sub> < 125 °C, R<sub>LOAD</sub> = 48 Ω)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>r</sub>	Rise time	I <sub>OUT</sub> = 0.5 A, (see Figure 4. Timing in normal operation )		10		μs
t <sub>f</sub>	Fall time			10		
t <sub>PD(H-L)</sub>	Propagation delay time off			20		
t <sub>PD(L-H)</sub>	Propagation delay time on			30		
t <sub>D(VCC-ON)</sub>	Power-on delay time from V <sub>CC</sub> rising edge	I <sub>OUT</sub> = 0.5 A, (see Figure 5. Propagation delay at start-up)		32	60	

Figure 4. Timing in normal operation

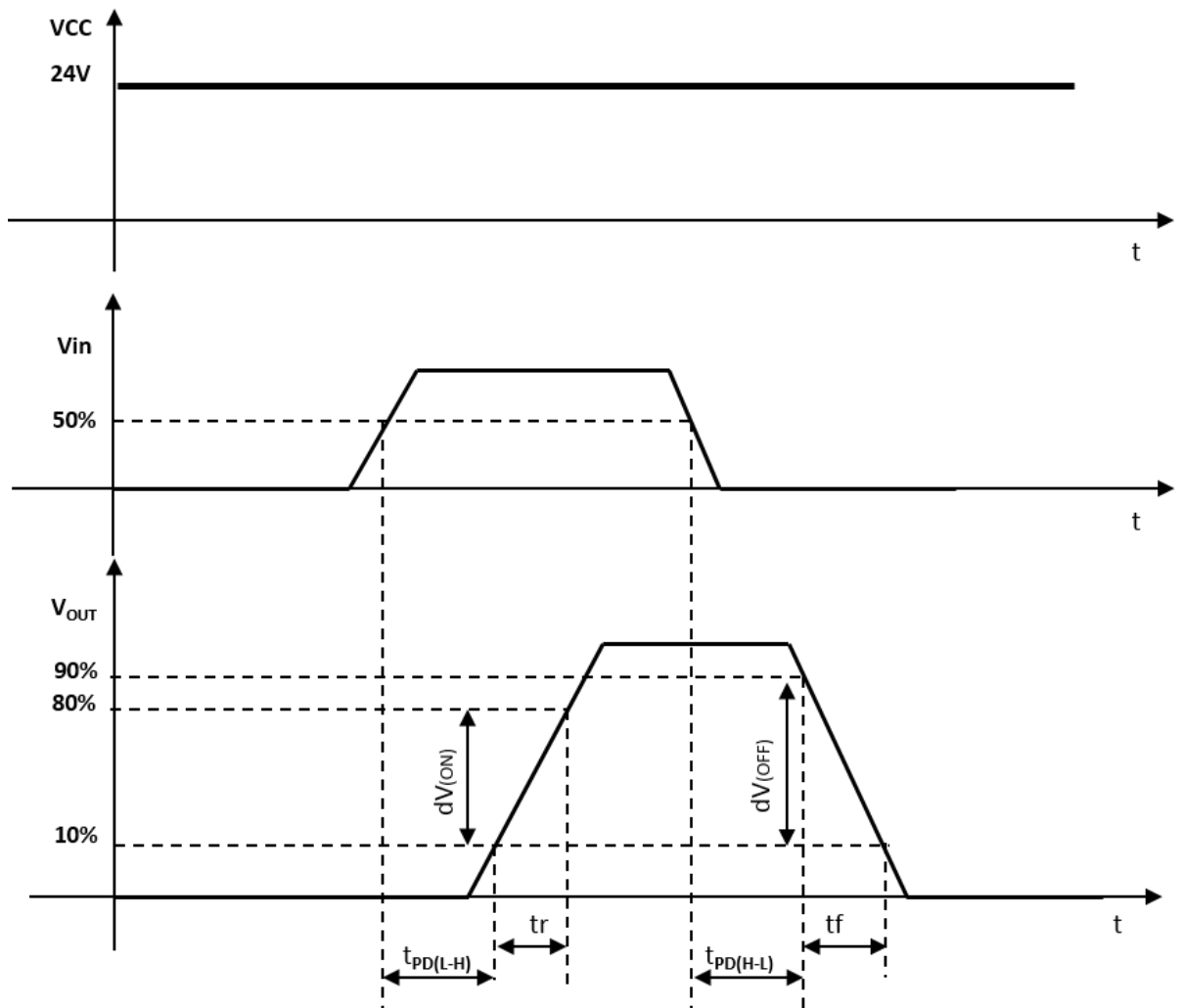


Figure 5. Propagation delay at start-up

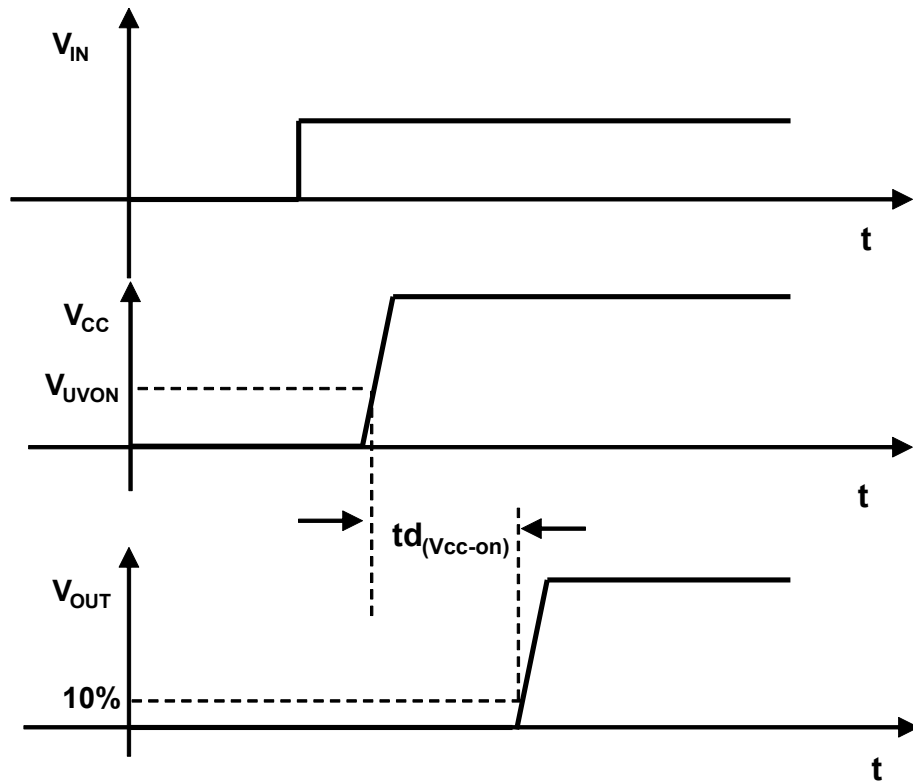


Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.8	V
$V_{IH}$	Input high level voltage		2.2			
$V_{I(HYST)}$	Input hysteresis voltage			0.4		
$I_{IN}$	Input current	$V_{CC} = V_{IN} = 36\text{ V}$			200	$\mu\text{A}$
		$V_{CC} = V_{IN} = 60\text{ V}$			550	



**Table 8. Protection and diagnostic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
V <sub>clamp</sub>	V <sub>CC</sub> active clamp	I <sub>CC</sub> = 10 mA	65.5	68.5	71.5	V	
V <sub>demag</sub>	Demagnetization voltage	I <sub>OUT</sub> = 0.5 A; load = 1 mH	V <sub>CC</sub> -71.5	V <sub>CC</sub> -68.5	V <sub>CC</sub> -65.5		
V <sub>OLoff</sub>	Open load (off-state) or short to V <sub>CC</sub> detection threshold		2		4		
t <sub>BKT</sub>	Open load blanking time				200	μs	
V <sub>DIAG</sub>	Voltage drop on DIAG	I <sub>DIAG</sub> = 4 mA			1	V	
I <sub>DIAG</sub>	DIAG pin leakage current	V <sub>CC</sub> ≤ 36 V			110	μA	
		36 V < V <sub>CC</sub> ≤ 60 V			180		
I <sub>PK</sub>	Output current limitation activation threshold	IPS161HF	V <sub>CC</sub> ≤ 24 V, RLOAD ≤ 10 mΩ	1.3		2.1	A
		IPS160HF		3.0		4.6	
I <sub>LIM</sub>	Output current limitation	IPS161HF		0.7		1.7	
		IPS160HF		2.5		4.2	
t <sub>coff</sub>	Cut-off current delay time	Programmable by the external capacitor on CoD pin. Cut-off is disabled when CoD pin is connected to GND through 1 kΩ resistor. T <sub>J</sub> < T <sub>JSD</sub>	50x <sub>CCOD</sub> [nf] ± 35% <sup>(1)</sup>			μs	
t <sub>res</sub>	Output stage restart delay time	T <sub>J</sub> < T <sub>JSD</sub>	32xt <sub>COFF</sub> [μs] ± 40%				
T <sub>JSD</sub>	Junction temperature shutdown		150	170	190	°C	
T <sub>JHYST</sub>	Junction temperature thermal hysteresis			15			

1. The formula is guaranteed in the range 10 nF ≤ C<sub>COOD</sub> ≤ 100 nF.

## 5 Output logic

Table 9. Output stage truth table

Operation	IN	OUT	DIAG
Normal	L	L	H
	H	H	H
Cut-off	L	L	L
	H	L	L
Overtemperature	L	L	L
	H	L	L
Open load	L	H <sup>(1)</sup>	L <sup>(1)</sup>
	H	H	H
UVLO	X	L	X
	X	L	X

1. External pull-up resistor is used

## 6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

### 6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ( $V_{UV(off)}$ ). Normal operation restarts after  $V_{CC}$  exceeds the turn-on threshold ( $V_{UV(on)}$ ). Turn-on and turn-off thresholds are defined in [Table 4. Supply](#).

### 6.2 Overtemperature

The output stage turns off when its internal junction temperature ( $T_J$ ) exceeds the shutdown threshold  $T_{JSD}$ . Normal operation restarts when  $T_J$  comes back below the reset threshold ( $T_{JSD} - T_{JHYST}$ ), see [Table 8. Protection and diagnostic](#). The internal fault signal is set when the channel is off due to thermal protection and it is reset when the junction triggers the reset threshold. This same behavior is signaled on the DIAG pin.

### 6.3 Cut-off

The IC can limit the output current at the power stage by its embedded output current limitation circuit.

This circuit continuously monitor the output current and, when load is increasing, at the triggering of its activation threshold ( $I_{pk}$ ) it starts limiting to  $I_{LIM}$  limitation level: while current limitation is active the IC enters an high dissipation status.

The IC implements the cut-off feature which limits the duration of the current limitation condition.

The duration of the current limitation condition ( $T_{COFF}$ ) can be set by a capacitor ( $C_{CoD}$ ) placed between CoD and GND pins. The design rule for  $C_{CoD}$  is:

$$t_{COFF[us]} \pm 35\% = 50 \times C_{CoD[nF]}$$

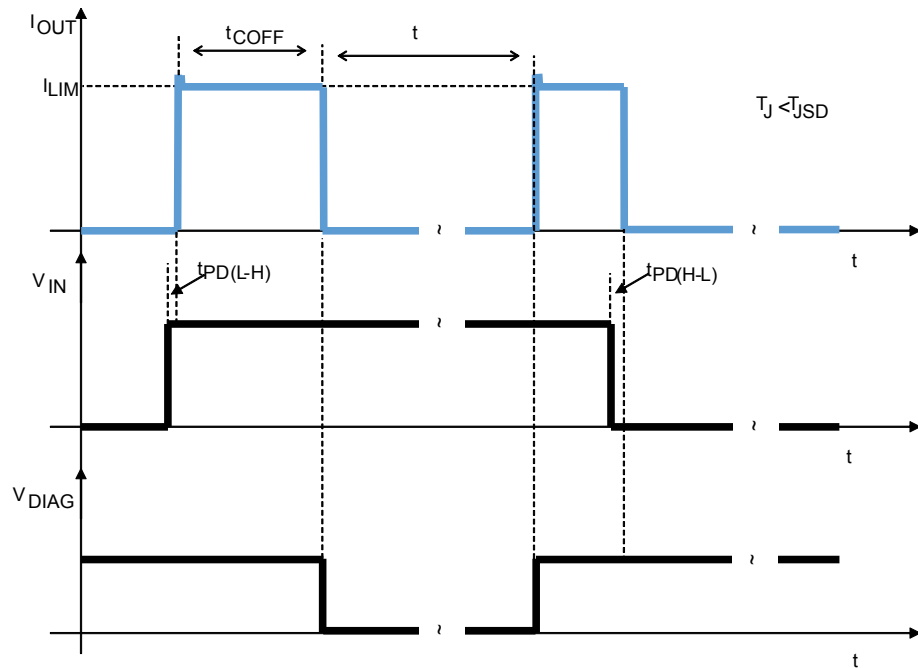
The  $\pm 35\%$  drift is guaranteed in the range of  $10 \text{ nF} < C_{CoD} < 100 \text{ nF}$ ; lower capacitance than 10 nF can be used.

If  $I_{LIM}$  threshold is triggered, the output stage remains in the current limitation condition ( $I_{OUT} = I_{LIM}$ ) no longer than  $t_{COFF}$ . If  $t_{COFF}$  elapses, the output stage turns off and restarts after the  $t_{RES}$  restart time.

Thermal shutdown protection has higher priority than cut-off:

- IC is forced off if  $T_{JSD}$  is triggered before  $t_{COFF}$  elapses
- if  $T_{JSD}$  is triggered, IC is maintained off even after the  $t_{RES}$  has elapsed and until the  $T_J$  falls below  $T_{JSD} - T_{JHYST}$

Figure 6. Current limitation and cut-off



The fault condition is reported on the DIAG pin. The internal cut-off flag signal is latched at output switch-off and released after the time  $t_{RES}$ , the same behavior is signaled on DIAG pin.

The status of the DIAG is independent on the IN pin status.

If CoD pin is connected to GND through 1 k $\Omega$  resistor (cut-off feature disabled), when the output channel triggers the limitation threshold, it remains on, in current limitation condition, until the input becomes LOW or the thermal protection threshold is triggered.

In case of low ambient temperature conditions ( $T_{AMB} < -20\text{ }^{\circ}\text{C}$ ) and high supply voltage ( $V_{CC} > 36\text{ V}$ ), the cut-off function requires activation in order to avoid damaging the IC.

The following table shows the suggested cut-off delay for different operating voltages.

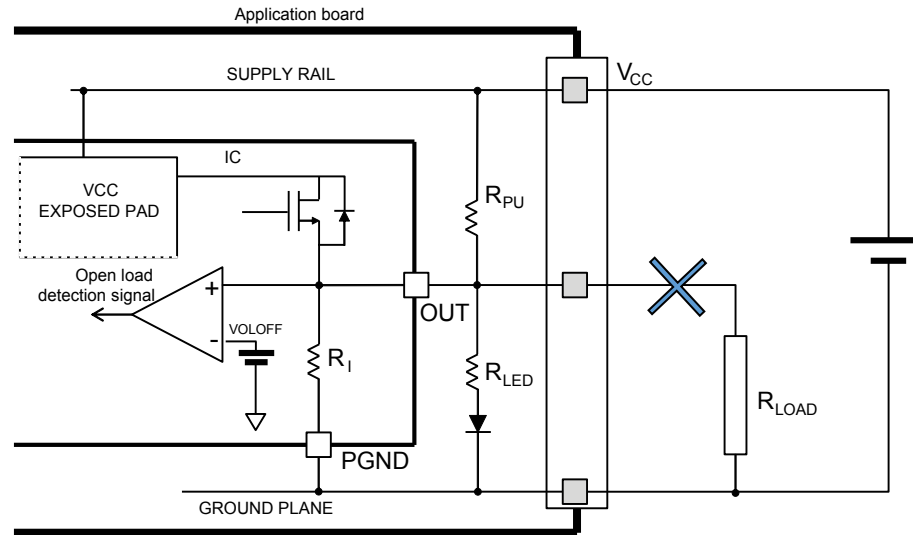
Table 10. Minimum cut-off delay for  $T_{AMB}$  less than  $-20\text{ }^{\circ}\text{C}$

$V_{CC}$ [V]	Cut-off delay [ $\mu\text{s}$ ]	Cut-off capacitance [nF]
36-48	100	2.2
48-60	50	1

## 6.4 Open load in off-state

The IC provides the open load detection feature which detects if the load is disconnected from the OUT pin. This feature can be activated by a resistor ( $R_{PU}$ ) between OUT and VCC pins.

Figure 7. Open load off-state



In case of wire break and during the OFF state ( $I_N = \text{low}$ ), the output voltage  $V_{OUT}$  rises according to the partitioning between the external pull-up resistor and the internal impedance of the IC ( $130 \text{ k}\Omega < R_I < 360 \text{ k}\Omega$ ).

The effect of the LED (if any) on the output pin has to be considered as well. In case of wire break and during the ON state ( $I_N = \text{high}$ ), the output voltage  $V_{OUT}$  is pulled up to  $V_{CC}$  by the low resistive integrated switch. If the load is not connected, in order to guarantee the correct open load signalization it must result:

$$V_{OUT} > V_{OLoff(max)}$$

Referring to the circuit in Figure 7. Open load off-state:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times (I_{RI} + I_{LED} + I_{RL}) \quad (1)$$

therefore:

$$R_{PU} < \frac{V_{CC(min)} - V_{OLoff(max)}}{\left(\frac{V_{OLoff(max)}}{R_I(min)} + \frac{V_{OLoff(max)} - V_{LED}}{R_{LED}}\right)} \quad (2)$$

If the load is connected, in order to avoid any false signalization of the open load, the following condition must hold:

$$V_{OUT} < V_{OLoff(min)}$$

By taking into account the circuit in figure 6:

$$V_{OUT} = V_{CC} - R_{PU} \times I_{PU} = V_{CC} - R_{PU} \times \left(\frac{V_{OUT}}{R_I} + \frac{V_{OUT} - V_{LED}}{R_{LED}} + \frac{V_{OUT}}{R_L}\right) \quad (3)$$

so:

$$R_{PU} > \frac{V_{CC(max)} - V_{OLoff(min)}}{\left(\frac{V_{OLoff(min)}}{R_I(max)} + \frac{V_{OLoff(min)} - V_{LED}}{R_{LED}} + \frac{V_{OLoff(min)}}{R_L}\right)} \quad (4)$$

The fault condition is signaled on the DIAG pin and the fault reset occurs when load is reconnected.

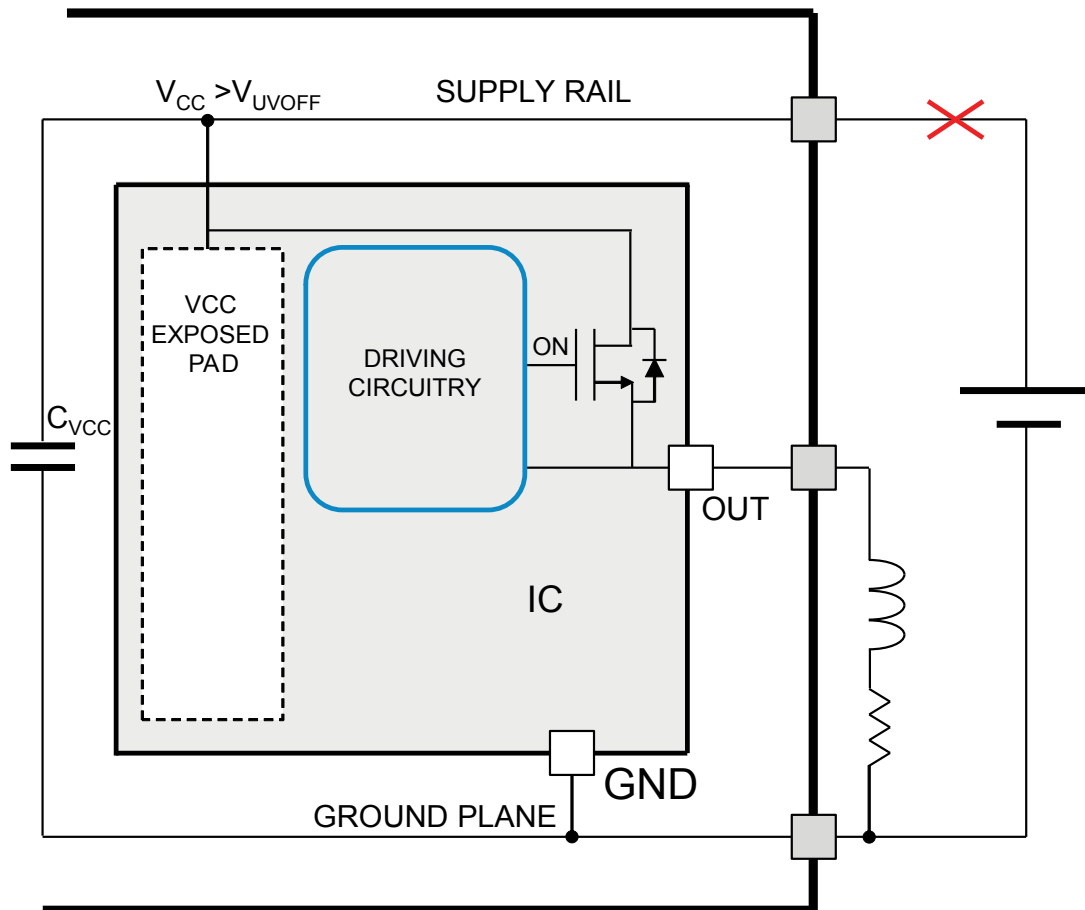
If the channel is switched on by the IN pin, the fault condition is no longer detected.

When an inductive load is driven, some ringing of the output voltage may be observed at the end of the demagnetization. In fact, the load is completely demagnetized when  $I_{LOAD} = 0$  A and the OUT pin remains floating until next turn-on. In order to avoid false detection of the open load event when driving inductive loads, the open load signal is masked for  $t_{BKT}$ . So, the open load is reported on the DIAG pin with a delay of  $t_{BKT}$  and if the open load event is triggered for more than  $t_{BKT}$ .

## 6.5 VCC disconnection protection

The IC is protected despite the  $V_{CC}$  disconnection event. This event is intended as the disconnection of the  $V_{CC}$  wire from the application board, see figure below. When this condition happens, the IC continues working normally until the voltage on the  $V_{CC}$  pin is  $\geq V_{UVOFF}$ . Once the  $V_{UVOFF}$  is triggered, the output channel is turned off independently on the input status. In case of inductive load, if the  $V_{CC}$  is disconnected while the output channel is still active, the IC allows the discharge of the energy still stored in the inductor through the integrated power switch.

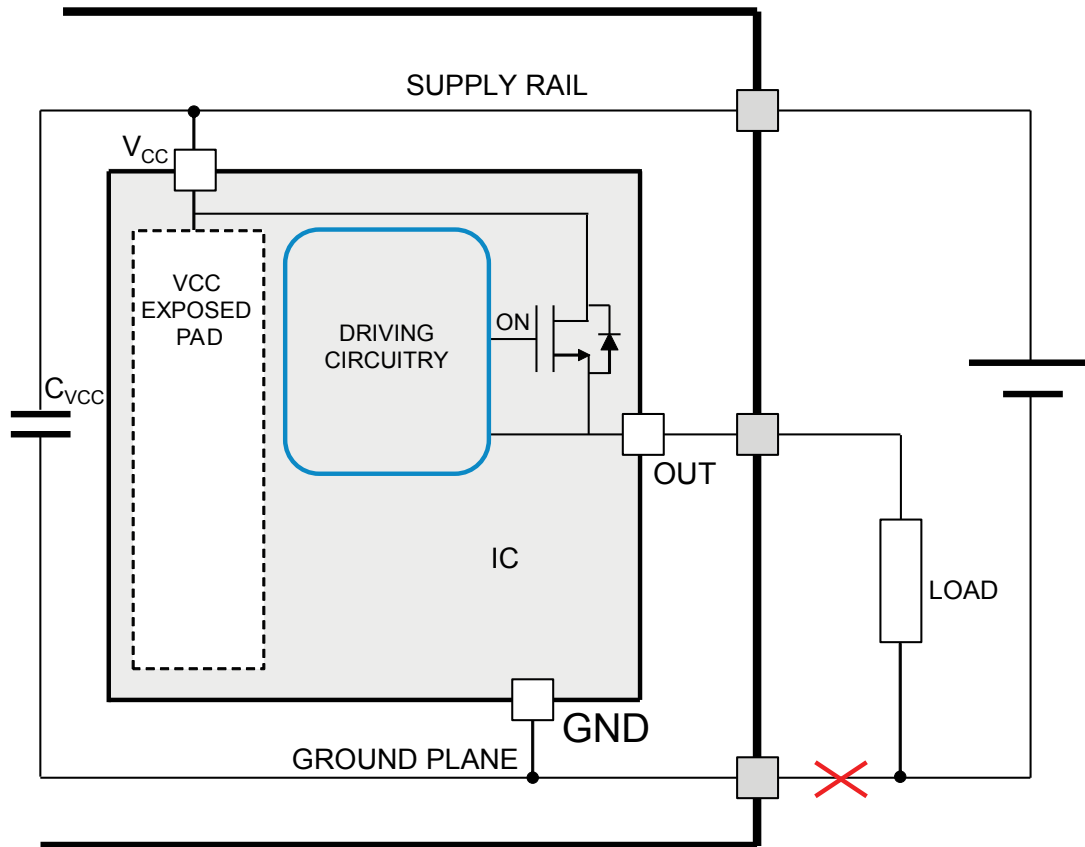
Figure 8. VCC disconnection  
APPLICATION BOARD



## 6.6 GND disconnection protection

GND disconnection is intended as the disconnection event of the application ground, see figure below. When this event happens, the IC continues working normally until the voltage between  $V_{CC}$  and GND pins of the IC is  $\geq V_{UVOFF}$ . The voltage on GND pin of the IC rises up to the supply rail voltage level. In case of GND disconnection event, a current ( $I_{LGND}$ ) flows through OUT pin. Table 4. Supply shows  $I_{OUT} = I_{LGND}$  for the worst case GND disconnection event where the output is shorted to ground.

Figure 9. GND disconnection  
APPLICATION BOARD



## 7 Active VDS clamp

Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on output.

The OUT pin is pulled down to  $V_{\text{demag}}$ . The conduction state is modulated by internal circuitry in order to keep the OUT pin voltage at about  $V_{\text{demag}}$  until the load energy has been dissipated. The energy is dissipated both in the IC internal switch and in the load resistance.

**Figure 10. Active clamp equivalent principle schematic**

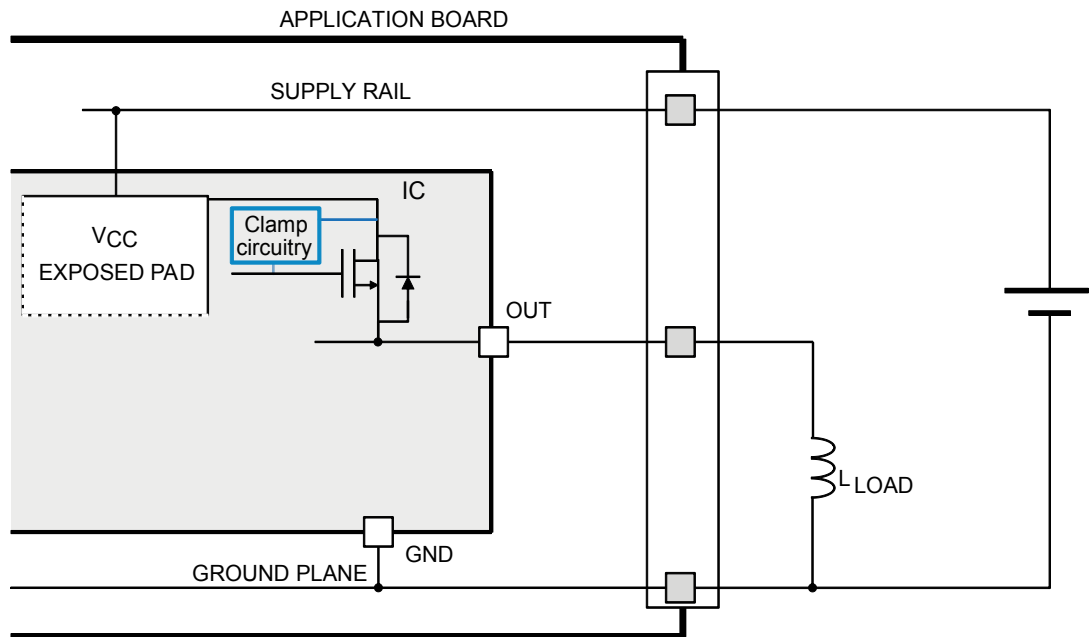
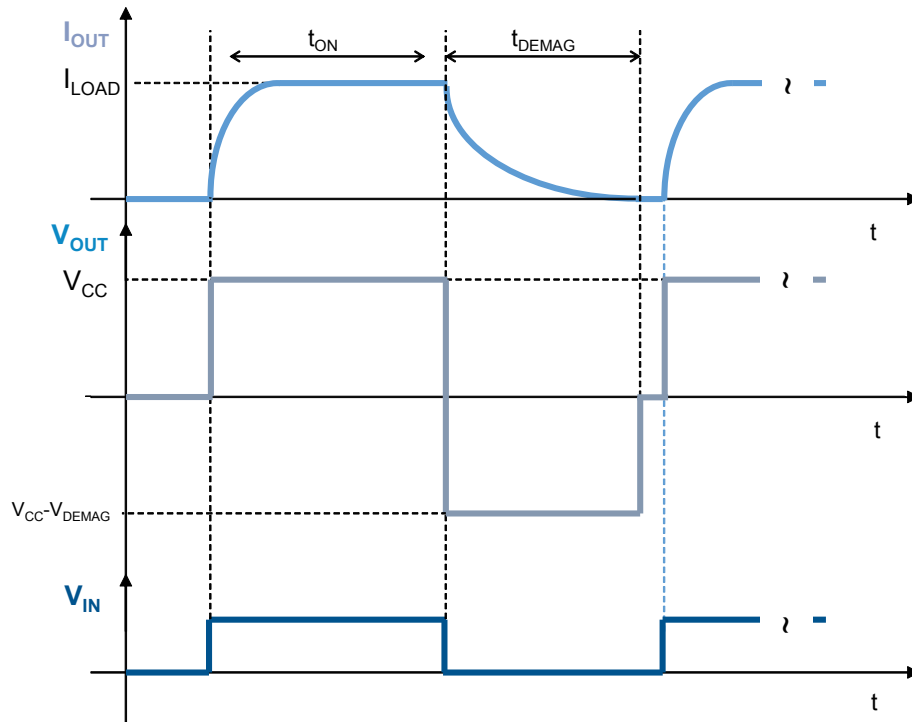


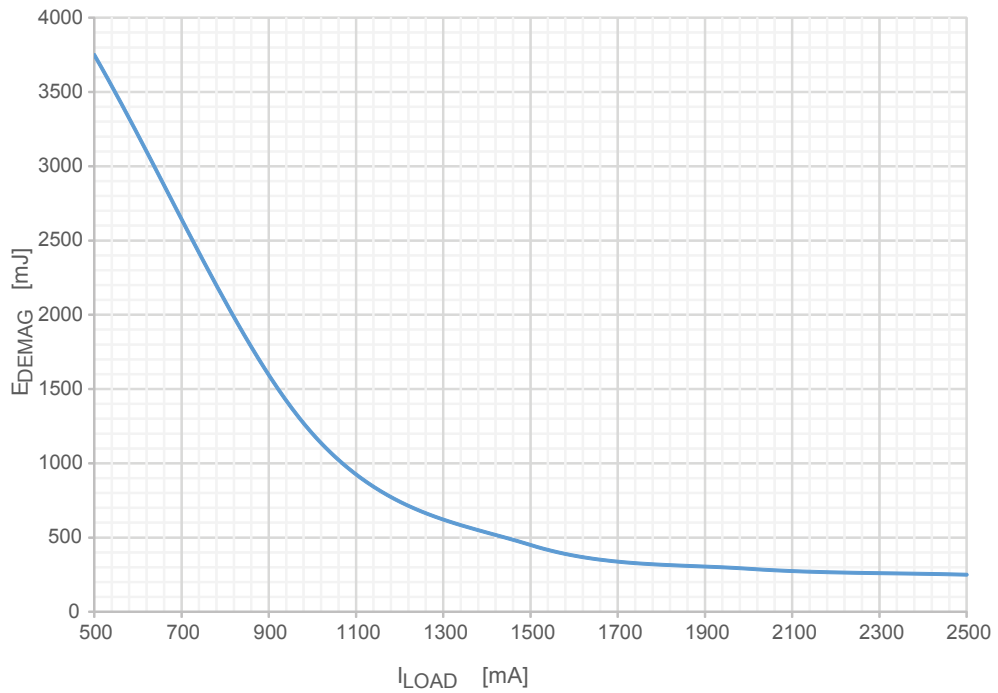


Figure 11. Fast demag waveforms



The demagnetization of inductive load causes large electrical and thermal stress on the IC. The plot below shows the maximum demagnetization energy that the IC can tolerate in a single demagnetization pulse with  $V_{CC} = 24\text{ V}$  and  $T_{AMB} = 125\text{ }^{\circ}\text{C}$ . If higher demagnetization energy is required, then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

**Figure 12. Typical demagnetization energy (single pulse) at  $V_{CC} = 24\text{ V}$  and  $T_{AMB} = 125\text{ }^{\circ}\text{C}$**



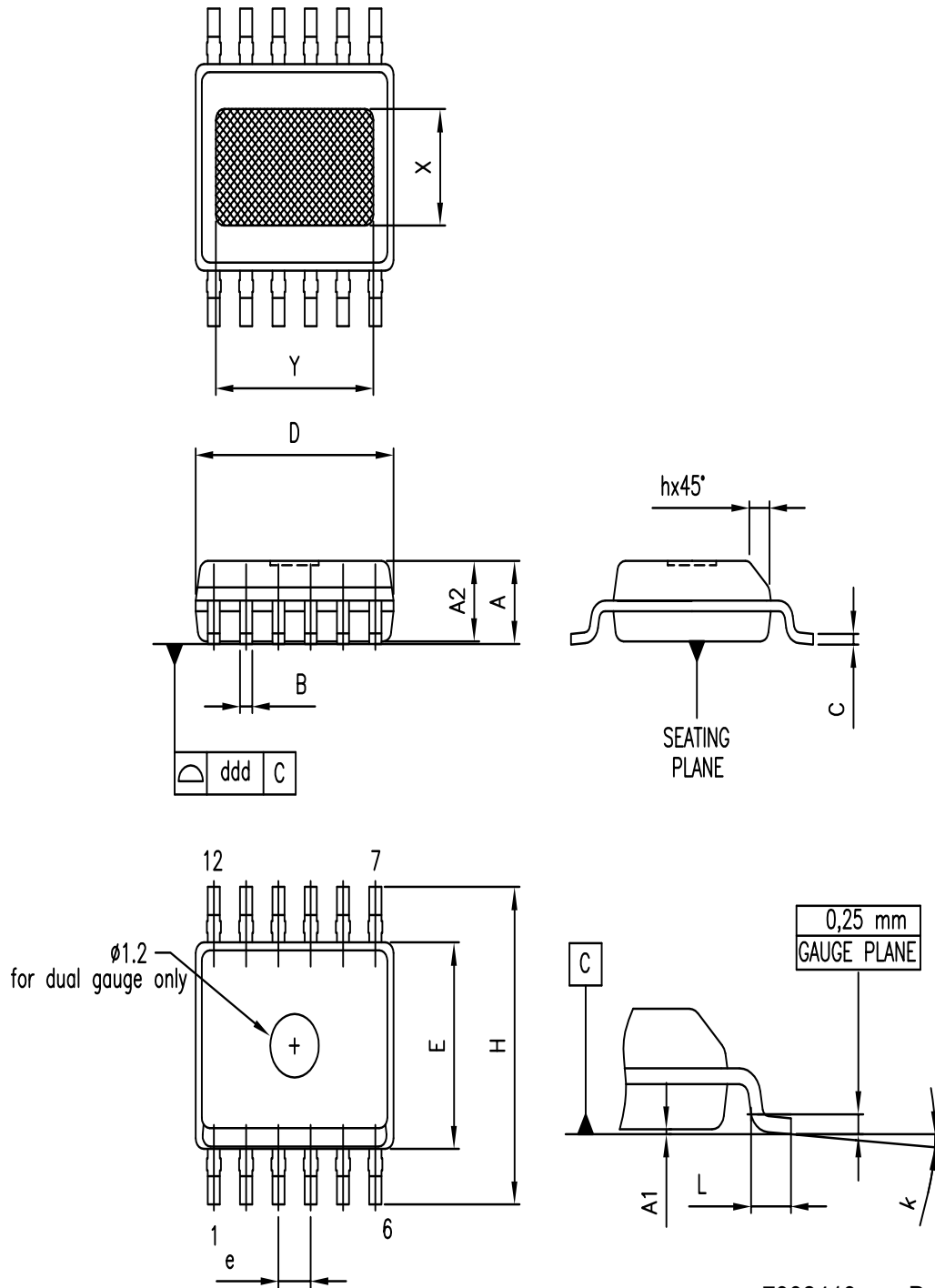
## 8 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 8.1 PowerSSO12 package information

Figure 13. PowerSSO12 package outline



7392413 rev. D

Table 11. PowerSSO12 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.250		1.700
A1	0.000		0.100
A2	1.100		1.600
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.55
L	0.400		1.270
k	0d		8d
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Note: Dimension D doesn't include mold flash protrusions or gate burrs. Mold flash protrusions or gate burrs don't exceed 0.15 mm in total both side.

Figure 14. PowerSSO12 recommended footprint

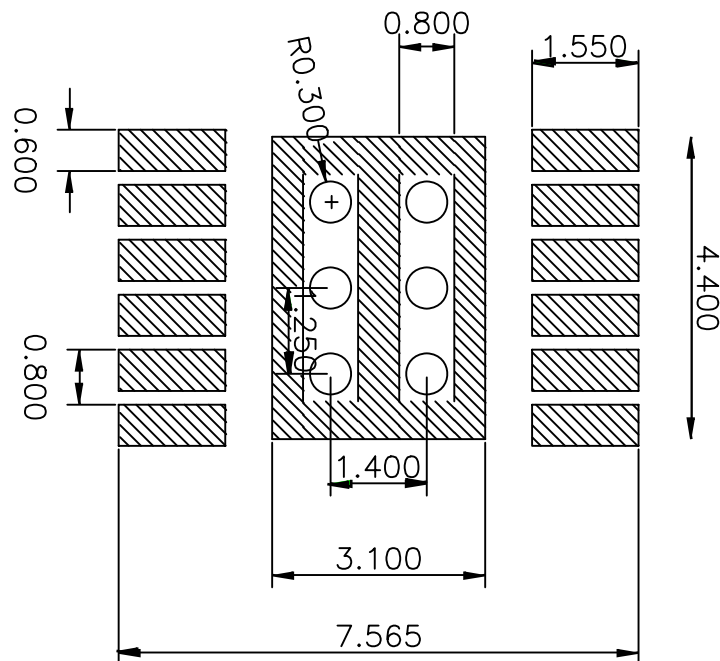


Figure 15. PowerSS012 tape packing information [mm]

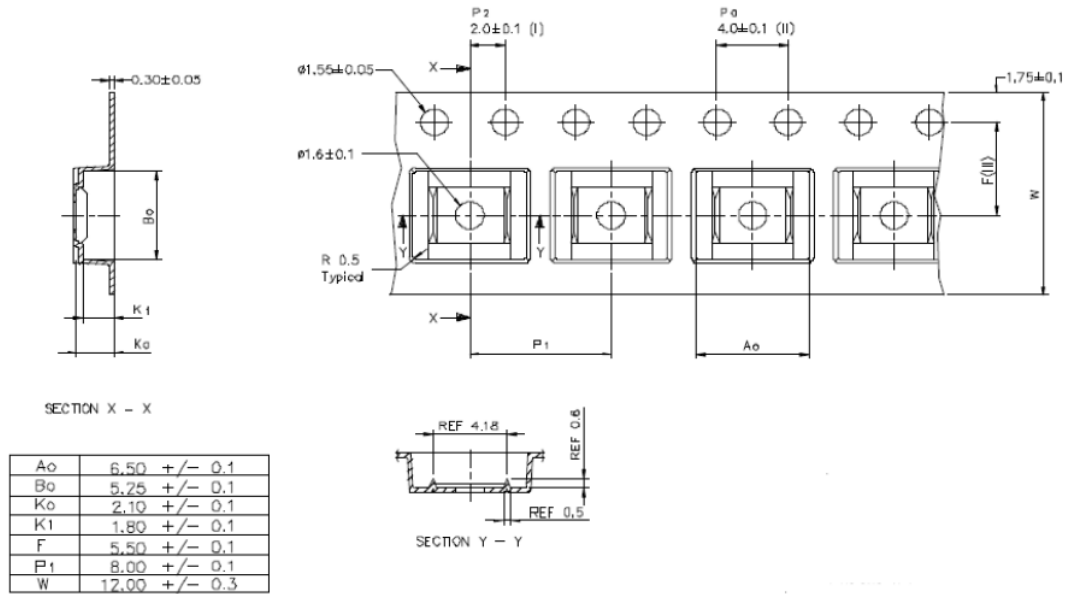
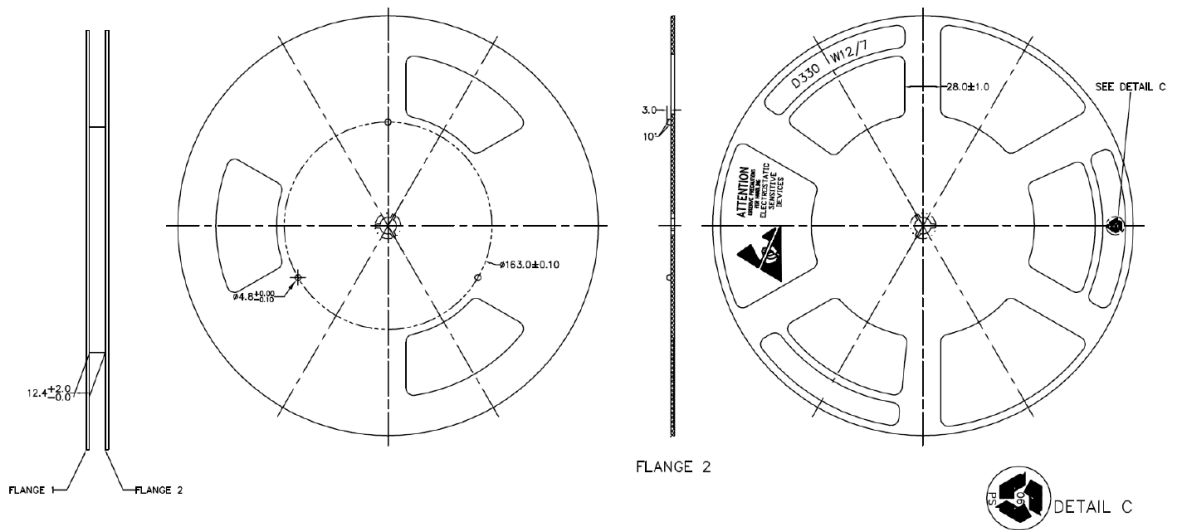


Figure 16. PowerSS012 reel packing information [mm]



- NOTES :
1. MATERIAL : POLYSTYRENE (BLACK)
  2. ANTISTATIC COATED
  3. FLANGE WARPAGE : 3 MM MAXIMUM
  4. ALL DIMENSIONS ARE IN MM
  5. ESD - SURFACE RESISTIVITY -  $10^9$  TO  $10^{11}$  OHMS/SQ.
  6. GENERAL TOLERANCE :  $\pm 0.25$  MM
  7. TOTAL THICKNESS OF REEL: 18.4 MAX.
  8. MOLD NO: TX12-07-A3

## Revision history

**Table 12. Document revision history**

Date	Revision	Changes
23-Apr-2020	1	Initial release.
26-Jun-2020	2	IPS161HF RPN added to document
03-Mar-2021	3	Minor changes in <a href="#">Section Applications</a>
29-Mar-2021	4	Updated $I_{LGND}$ maximum value in <a href="#">Table 4</a>
30-Jul-2021	5	Updated thermal data in <a href="#">Table 3</a> according to Jedec conditions.

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