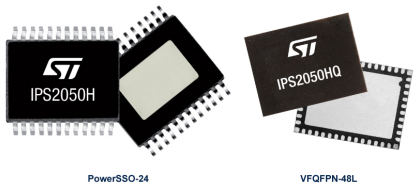
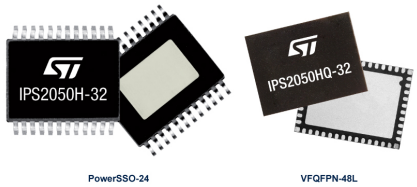
IPS2050H, IPS2050H-32

High efficiency, high-side switch with extended diagnostics and smart driving for capacitive loads





Features

- 8 V to 60 V operating supply voltage range
- Operating output current: 2.4 A (IPS2050H/HQ) or 5.6 A (IPS2050H-32/HQ-32) per channel
- Smart driving of capacitive load
- Fast demagnetization of inductive loads
- Under-voltage lock-out
- V_{CC} over-voltage protection
- Per-channel overload and over-temperature protection
- Case over-temperature protection
- Ground disconnection protection
- Per channel overload/over-temperature event diagnostic pins
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- Packages: PowerSSO-24 and VFQFPN-48L 8x6x0.9 mm

Applications

- Programmable logic control
- Vending machines
- Industrial PC peripheral input/output
- Numerical control machines
- General high-side switch applications

Product status link
IPS2050H
IPS2050H-32

Product label
SUSTAINABLE TECHNOLOGY

Description

The IPS2050H/HQ and IPS2050H-32/HQ-32 are dual high-side switch ICs able to drive capacitive, resistive or inductive loads with one side connected to ground.

The very low $R_{DS\text{-}ON}$ (≤ 50 mΩ up to T_J = 125 °C) makes the IC suitable for applications with up to 2.4 A (IPS2050H/HQ) or 5.6 A (IPS2050H-32/HQ-32) steady state operating current.

Each output channel is independently protected against junction over-temperature events by a junction temperature sensor, and a further temperature sensor is included to monitor case temperature, so an overheated output channel can only be turned back ON when the case temperature returns below the reset temperature.

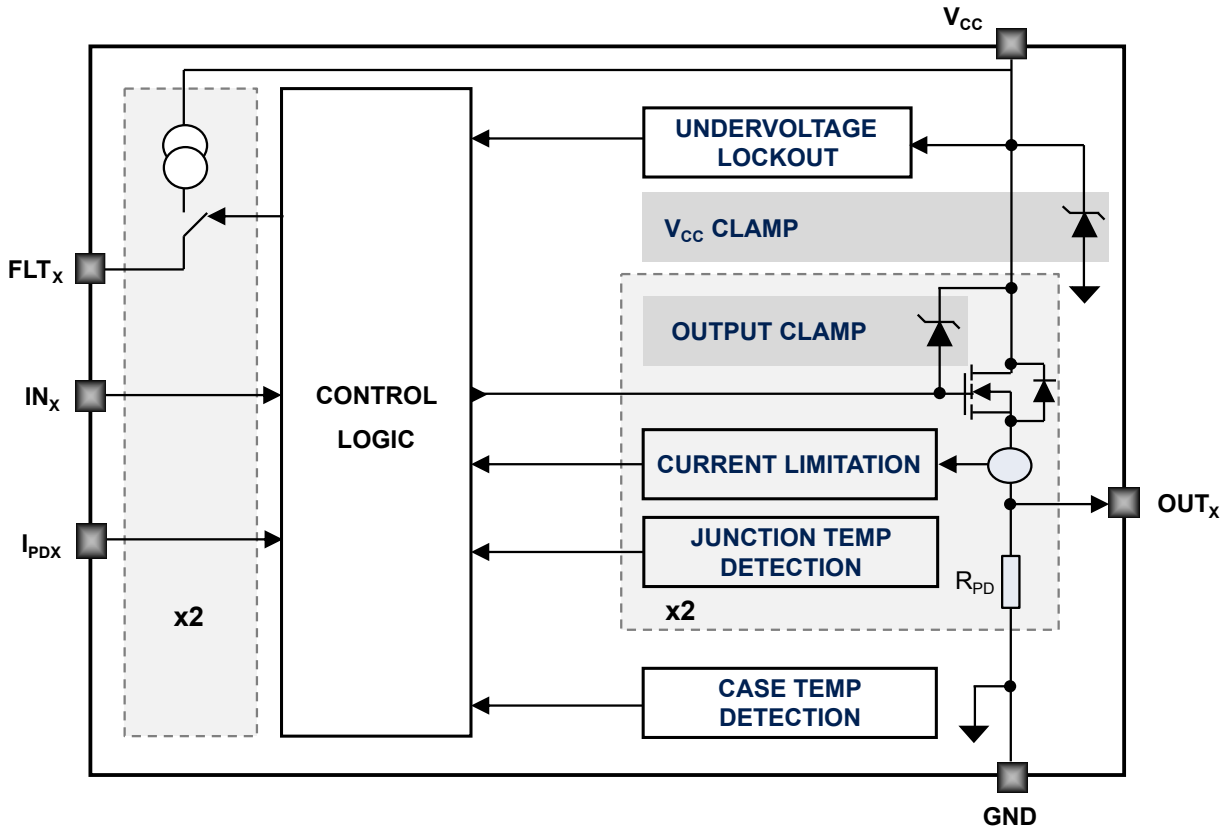
The embedded per-channel overload protection circuit monitors the output current and, on triggering of the activation threshold ($I_{PK\text{-}X}$), starts modulating the impedance of the output switch to limit the output current to $I_{LIM\text{-}X}$, for both IC and load protection.

The IC offers two different sets of activation threshold and limitation levels ($I_{PKH\text{-}X}$, $I_{LIMH\text{-}X}$ and $I_{PKL\text{-}X}$, $I_{LIML\text{-}X}$) for smart driving of capacitive loads (such as bulb lamps) and loads with initial peak current requirements.

The IC diagnostics is based on two FAULT pins (current source), one for each channel. Each FAULT pin is activated by an overload or an over-temperature event on the related channel.

1 Block diagram

Figure 1. IPS2050H/HQ, IPS2050H-32/HQ-32 block diagram



2 Pin connection

Figure 2. Pin connections (top through view)

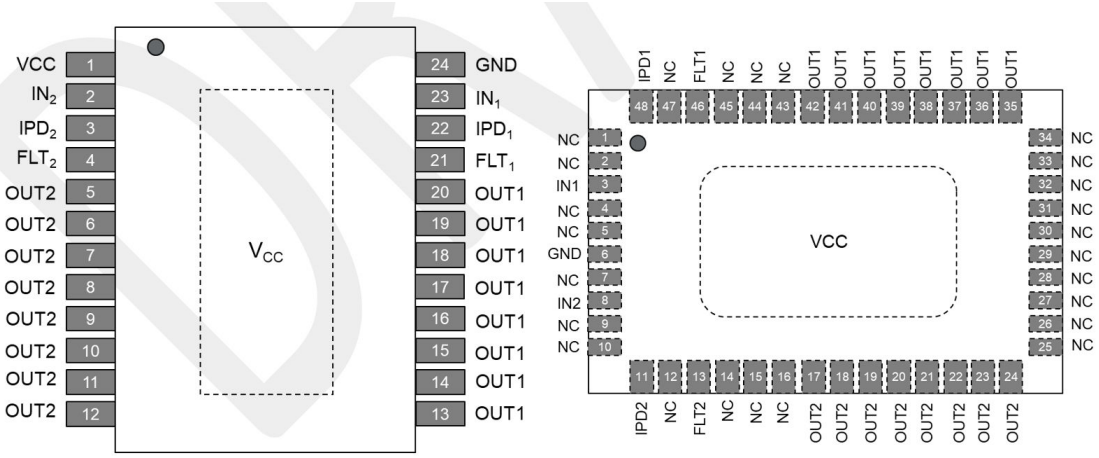


Table 1. Pin descriptions

Pin no.		Name	Description
PSSO24	VFQFPN-48L		
1, exposed pad	exposed pad	V_{CC}	Supply voltage
2	8	IN_2	Channel 2 input
3	11	IPD_2	Channel 2 initial current duration / level selector. Connect to GND by a capacitor to set duration of I_{PKH-2} (see Section 7.3 and Table 9 / Table 10). Connect to IN_2 by a 220 kΩ resistor to disable initial I_{PKH-2} threshold on channel 2 (the over-current limit for channel 2 is only I_{PKL-2}). Connect to GND by a 10 kΩ resistor to disable I_{PKL-2} on channel 2 (the over-current threshold for channel 2 is only I_{PKH-2}).
4	13	FLT_2	Fault (Overload or Over-temperature) diagnostic pin for channel 2. Can't be left floating: if not used, connect to GND by a 1.5kΩ resistor.
5 to 12	17 to 24	OUT_2	Channel 2 power stage output Short the pins on the same net of the application board
13 to 20	35 to 42	OUT_1	Channel 1 power stage output Short the pins on the same net of the application board
21	46	FLT_1	Fault (Overload or Over-temperature) diagnostic pin for channel 1. Can't be left floating: if not used, connect to GND by a 1.5kΩ resistor.
22	48	IPD_1	Channel 1 initial current duration / level selector. Connect to GND by a capacitor to set duration of I_{PKH-1} (see Section 7.3 and Table 9 / Table 10). Connect to IN_1 by a 220 kΩ resistor to disable initial I_{PKH-1} threshold on channel 1 (the over-current limit for channel 1 is only I_{PKL-1}). Connect to GND by a 10 kΩ resistor to disable I_{PKL-1} on channel 1 (the over-current threshold for channel 1 is only I_{PKH-1}).
23	3	IN_1	Channel 1 input

Pin no.		Name	Description
PSSO24	VFQFPN-48L		
24	6	GND	Device ground
-	1 to 5; 7 to 10; 12; 14 to 16; 25 to 34; 43 to 45; 47	NC	Internally not connected. If necessary, these pins can be routed in the application.

Note: Leaving IPD_X floating is equivalent to a 1 µs duration for I_{PKH-X}.

3 Absolute maximum ratings

Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to 65	V
I_{CC}	Maximum DC reverse current (from GND to V_{CC})	-250	mA
I_{OUT}	Output stage current	Internally limited	A
$-I_{OUT}$	Reverse current (from OUT to V_{CC})	5	A
V_{IN}	IN pin voltage	-0.3 to V_{CC}	V
I_{IN}	IN pin current	-10/+10	mA
V_{PD}	I_{PD} pin voltage	-0.3 to 5.5	V
I_{PD}	I_{PD} pin current	-1/+10	mA
V_{FAULT}	FLT pins voltage	-0.3 to 5.5	V
I_{FAULT}	FLT pins current	-1[(1)]/+10	mA
E_{AS}	Single pulse avalanche energy, two channels driven simultaneously (T_{AMB} = 125 °C, V_{CC} = 24 V, I_{OUT} = 2 A)	1.3[(2)]	J
		1.0[(3)]	J
P_{TOT}	Power Dissipation at T_C = 25 °C	Internally limited	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Junction Operating Temperature	Internally limited	°C
T_C	Case Operating Temperature	-40 to 150	°C

1. *intended as worst case when IC is in normal operation (no fault)*
2. *IPS2050H / IPS2050H-32*
3. *IPS2050HQ / IPS2050HQ-32*

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	PSSO24	VFQFPN-48L	Unit
$R_{th(JC)}$ (1)	Thermal resistance junction-case per channel	0.7	1	°C/W
$R_{th(JA)}$ (2)	Thermal resistance junction-ambient	22	26	°C/W

1. *Rth between the die and the bottom case surface measured by cold plate as per JESD51.*
2. *JESD51-7.*

5 Electrical characteristics

(8 V < V_{CC} < 60 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{UVON}	Under-voltage ON threshold	-	6.9	-	8	V
V_{UVOFF}	Under-voltage OFF threshold	-	6.5	-	7.8	V
V_{UVH}	Under-voltage hysteresis	-	0.15	0.5	-	V
I_{SOFF}	Supply current in OFF state	IN_X = GND, OUT_X = open load	-	0.5	0.95	mA
I_{SON}	Supply current in ON state	V_{CC} = 24V	1.95	2.6	3.2	mA
		V_{CC} = 36V	2.05	2.7	3.3	mA
		V_{CC} = 60V	2.25	2.9	3.5	mA

Table 5. Output stage

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{DSON}	On-state resistance	V_{CC} = 24 V, R_{LOAD} = 12 Ω, @ T_J = 25 °C	-	25	30	mΩ
		V_{CC} = 24 V, R_{LOAD} = 12 Ω, @ T_J = 125 °C	-	-	50	mΩ
$V_{OUT(OFF)}$	OFF state output voltage	V_{IN} = 0 V, I_{OUT} = 0 A	-	-	2	V
$I_{OUT(OFF)}$	OFF state output current	V_{IN} = 0 V, V_{OUT} = 0 V	-	-	10	µA

Table 6. Switching

(V_{CC} = 24 V; -40 °C < T_J < 125 °C, R_{LOAD} = 12 Ω, input rise time < 0.1 µs)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Rise time		-	25	50	µs
t_f	Fall time		-	15	30	µs
$t_{PD(L-H)}$	Propagation delay time IN to OUT, low to high			14	25	µs
$t_{PD(H-L)}$	Propagation delay time IN to OUT, high to low		-	33	60	µs
$t_{D(VCCON)}$	Propagation delay time IN to OUT at power-on	V_{IN} = V_{CC} and rising from 0 to 24 V	150	500	1600	µs

Figure 3. **Timing**

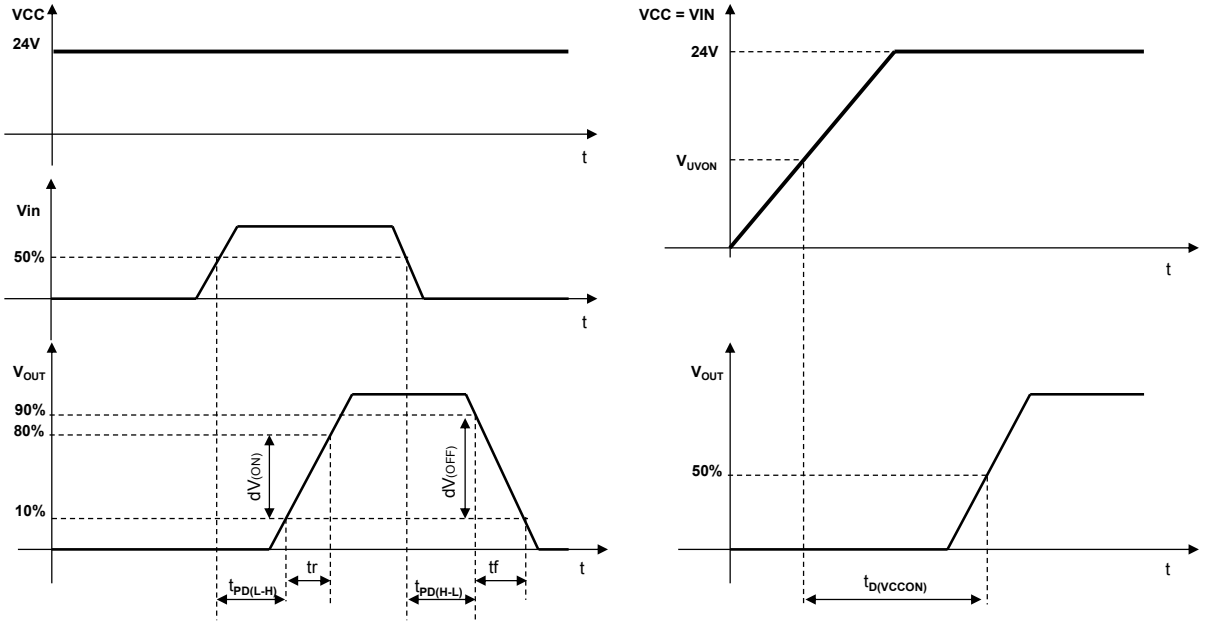


Table 7. **Input pin (IN1 or IN2)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input pin low level voltage	-	-	-	0.8	V
V_{IH}	Input pin high level voltage	-	2.2	-	-	V
$V_{I(HYST)}$	Input pin hysteresis voltage	-	-	0.4	-	V
I_{IN}	Input pin current	$V_{IN} = V_{CC}$ = 36V	-	-	200	µA
		$V_{IN} = V_{CC}$ = 60V	-	-	600	

Table 8. **Diagnostic pins (FLT_1, FLT_2)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IH_{FLT}	Diagnostic pins source current in fault condition.	V_{FLT} = 1 V (fault condition active)	-2	-3	-4	mA
		V_{FLT} = 5 V (fault condition active)	-0.4	-0.7	-1.0	
IL_{FLT}	Diagnostic pins leakage current	Normal operation V_{CC} = 60 V	-	-	-25	µA
BT_{FLT}	Diagnostic pins blanking time	-	60	-	400	µs
VCL_{FLT}	Diagnostic pins clamp voltage	I_{FLT} = +1 mA	6	6.8	8	V
		I_{FLT} = -1 mA	-	-	0.7	

Table 9. IPS2050H/HQ overload protections

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Overload with Dual Threshold Protection: I_{PD} pin to GND by C_{PD} (470 pF ≤ C_{PD} ≤ 470 nF); see Section 7.3.1						
I_{PKH-X}	Initial overcurrent activation threshold for channel x	V_{CC} = 24 V	-	11.5	-	A
I_{LIMH-X}	Initial overcurrent limitation level for channel x		6.1	8.8	11.5	A
D_{PKX}	Time limit of Initial overcurrent for channel x		-	215*C_{PD} [nF]	-	µs
I_{PKL-X}	Steady state overcurrent activation threshold for channel x		-	5.2	-	A
I_{LIML-X}	Steady state overcurrent limitation level for channel x		2.5	3.5	4.5	A
I_{HYS}	Steady state output Current limitation hysteresis		-	0.3	-	A
$I_{LIML-OFF}$	Steady state overcurrent limitation deactivation threshold		-	I_{LIML} - I_{HYS}	-	A
Overload with Single Level (Lowest) Protection: I_{PD} pin connected to IN by 220 kΩ resistor; see Section 7.3.2						
I_{PKL-X}	Steady state overcurrent activation threshold for channel x	V_{CC} = 24 V	-	5.2	-	A
I_{LIML-X}	Steady state overcurrent limitation level for channel x		2.5	3.5	4.5	A
I_{HYS}	Steady state output Current limitation hysteresis		-	0.3	-	A
$I_{LIML-OFF}$	Steady state overcurrent limitation deactivation threshold		-	I_{LIML}-I_{HYS}	-	A
Overload with Single Level (Highest) Protection: I_{PD} pin connected to GND by 10 kΩ resistor; see Section 7.3.3.						
I_{PKH-X}	Initial overcurrent activation threshold for channel x	V_{CC} = 24 V	-	11.5	-	A
I_{LIMH-X}	Initial overcurrent limitation level for channel x		6.1	8.8	11.5	A

Table 10. IPS2050H-32/HQ-32 overload protections

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Overload with Dual Threshold Protection: I_{PD} pin to GND by C_{PD} (470 pF ≤ C_{PD} ≤ 470 nF); see Section 7.3.1						
I_{PKH-X}	Initial overcurrent activation threshold for channel x	V_{CC} = 24 V	-	19.8	-	A
I_{LIMH-X}	Initial overcurrent limitation level for channel x		12.5	17.9	23.2	A
D_{PKX}	Time limit of Initial overcurrent for channel x		-	215*C_{PD} [nF]	-	µs
I_{PKL-X}	Steady state overcurrent activation threshold for channel x		-	10.5	-	A
I_{LIML-X}	Steady state overcurrent limitation level for channel x		5.7	8.0	10.4	A
I_{HYS}	Steady state output Current limitation hysteresis		-	0.3	-	A
$I_{LIML-OFF}$	Steady state overcurrent limitation deactivation threshold		-	I_{LIML} - I_{HYS}	-	A
Overload with Single Level (Lowest) Protection: I_{PD} pin connected to IN by 220 kΩ resistor; see Section 7.3.2						
I_{PKL-X}	Steady state overcurrent activation threshold for channel x	V_{CC} = 24 V	-	10.5	-	A
I_{LIML-X}	Steady state overcurrent limitation level for channel x		5.7	8.0	10.4	A
I_{HYS}	Steady state output Current limitation hysteresis		-	0.3	-	A
$I_{LIML-OFF}$	Steady state overcurrent limitation deactivation threshold		-	I_{LIML}-I_{HYS}	-	A
Overload with Single Level (Highest) Protection: I_{PD} pin connected to GND by 10 kΩ resistor; see Section 7.3.3.						
I_{PKH-X}	Initial overcurrent activation threshold for channel x	V_{CC} = 24 V	-	19.8	-	A
I_{LIMH-X}	Initial overcurrent limitation level for channel x		12.5	17.9	23.2	A

Figure 4. **High (left) and Low (right) I_{LOAD} control activation thresholds (I_{PK}) and limitation levels (I_{LIM})**

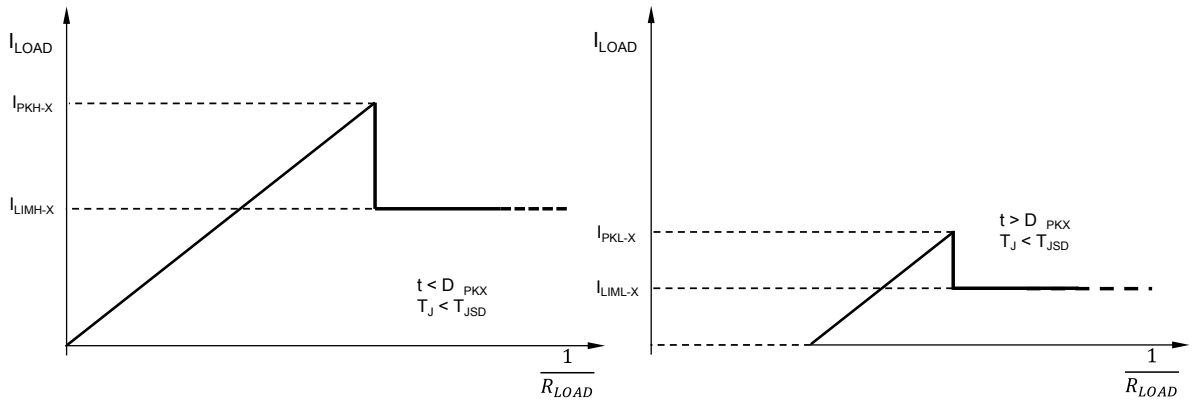


Table 11. **Other protections**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Overtemperature protections						
T_{JSD}	Junction temperature shutdown	-	150	170	190	°C
T_{JR}	Junction temperature reset	-	-	150	-	°C
T_{JHYS}	Junction temperature hysteresis	-	7	20	-	°C
T_{CSD}	Case temperature shutdown	-	-	130	-	°C
T_{CR}	Case temperature reset	-	-	110	-	°C
T_{CHYS}	Case temperature hysteresis	-	-	20	-	°C
Ground disconnection/Wire break						
I_{LGND}	GND disconnection output current	V_{INX} = Vcc = 24 V, V_{OUT} = 0 V	-	-	0.5	mA
VCC overvoltage						
V_{CLAMP}	V_{CC} Clamp Voltage	I_{CC} ≤ 10 mA	65.5	70.0	73.5	V
Demagnetization of inductive load						
V_{DEMAG}	Demagnetization Voltage	I_{OUT} = 0.5 A, Load ≥ 10 mH	Vcc-76	Vcc-72.5	Vcc-68	V

6 Output Logic

Table 12. Output stage truth table

(L=pin voltage Low, H=pin voltage High, X=not determined)

	IN_X	OUT_X	FLT_X
Normal Operation	L H	L H	L L
Overload	L H	L X(1)	L H
Junction over-temperature	L H	L L	L H
Case over-temperature	L H	L L(2)	L H(2)
UVLO	L H	L L	X X

1. *Pin voltage = I_{OUT} * R_{LOAD}*
2. *Channels with $T_J > T_{JSD}$ are forced off and the related FLT are activated*

Figure 5. Typical application diagram with opto-couplers

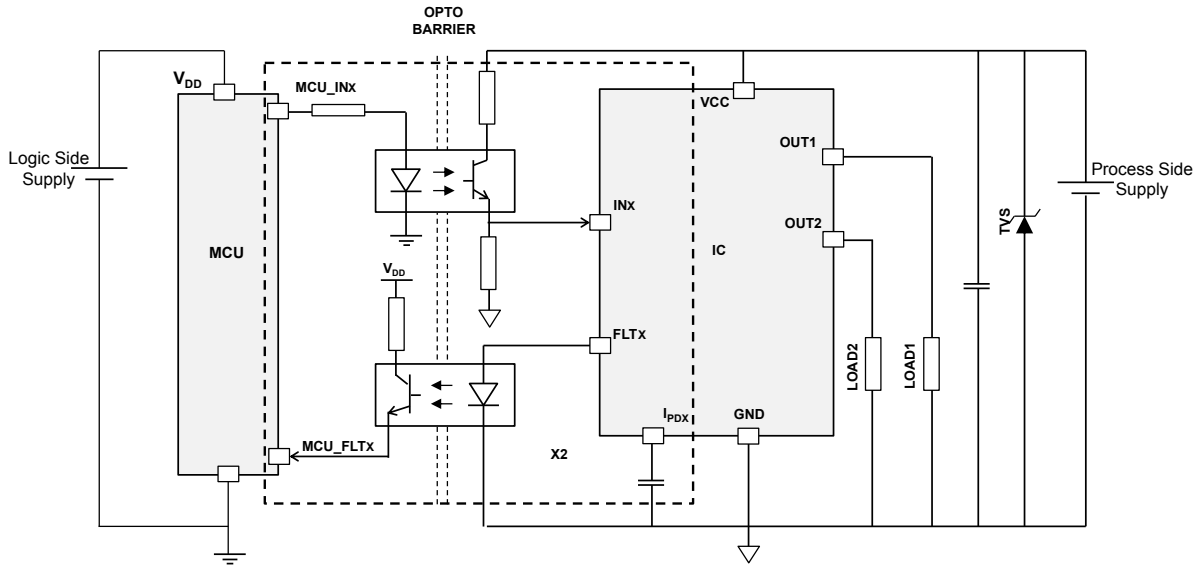
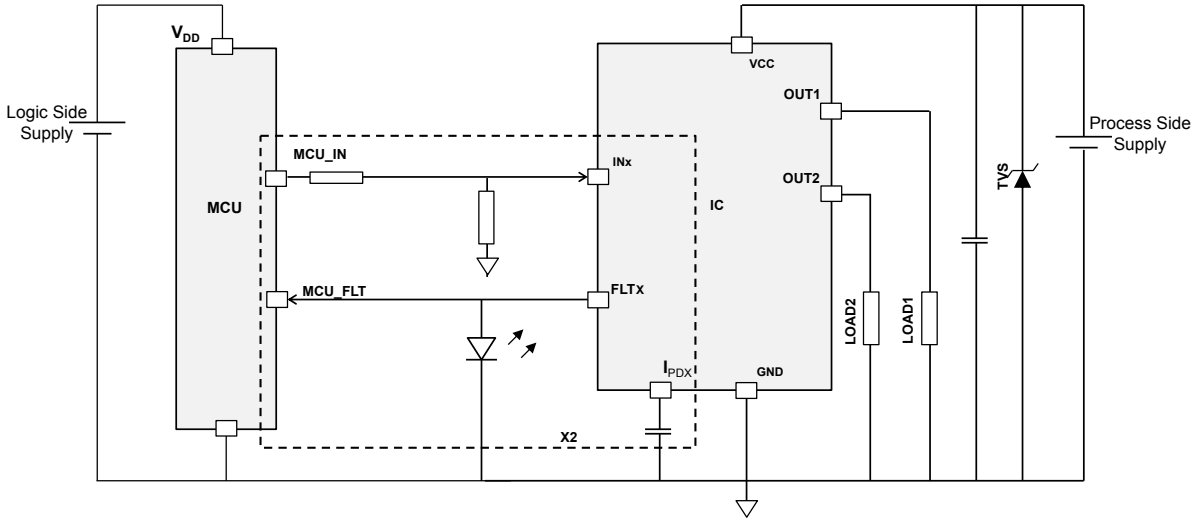


Figure 6. **Typical application diagram without opto-couplers**



7 Protections and diagnostic

The IC integrates several protections to help the design of robust applications.

7.1 Under-voltage lock-out

The IC is turned off if the voltage on V_{CC} pin falls below the turn-off threshold (V_{UVOFF}). Normal operation restarts after V_{CC} exceeds the turn-on threshold (V_{UVON}). Turn-on and turn-off thresholds are defined in Table 4.

7.2 Over-temperature

The device is protected against overheating in case of overload conditions. During the driving period (when the MCU is forcing the IN_X pin high), if the output is overloaded, the device suffers two different thermal stresses, one related to the junction temperature of each output channel, and the other related to the whole case temperature.

The two thermal faults (Thermal Junction and Thermal Case) have different trigger thresholds: T_{JSD} and T_{CSD}, respectively.

Usually, in thermal stress conditions due to overload, the junction thermal shutdown is the first protection that is activated: each output channel (OUT_X) is turned off when its junction temperature (T_{JX}) is higher than the activation threshold (T_{JSD}) and turned back on when it goes below the reset threshold (T_{JR}). This behavior continues while overload on the output persists. When the thermal protection is active for OUT_X, the related FLT_X (current source) becomes active accordingly.

If the thermal protection is active and the temperature of the case (T_C) increases over the case protection threshold (T_{CSD}), then the thermal case protection is activated and the output is switched off until the junction temperature of each channel in fault and case temperature fall below the respective reset thresholds (T_{CR} and T_{JR}). The FLT_X pins are active even when thermal case events occur.

Figure 7 shows the thermal protection behavior, while Figure 8 and Figure 9 show typical temperature trends and output vs. input state.

Figure 7. **Thermal protection flowchart**

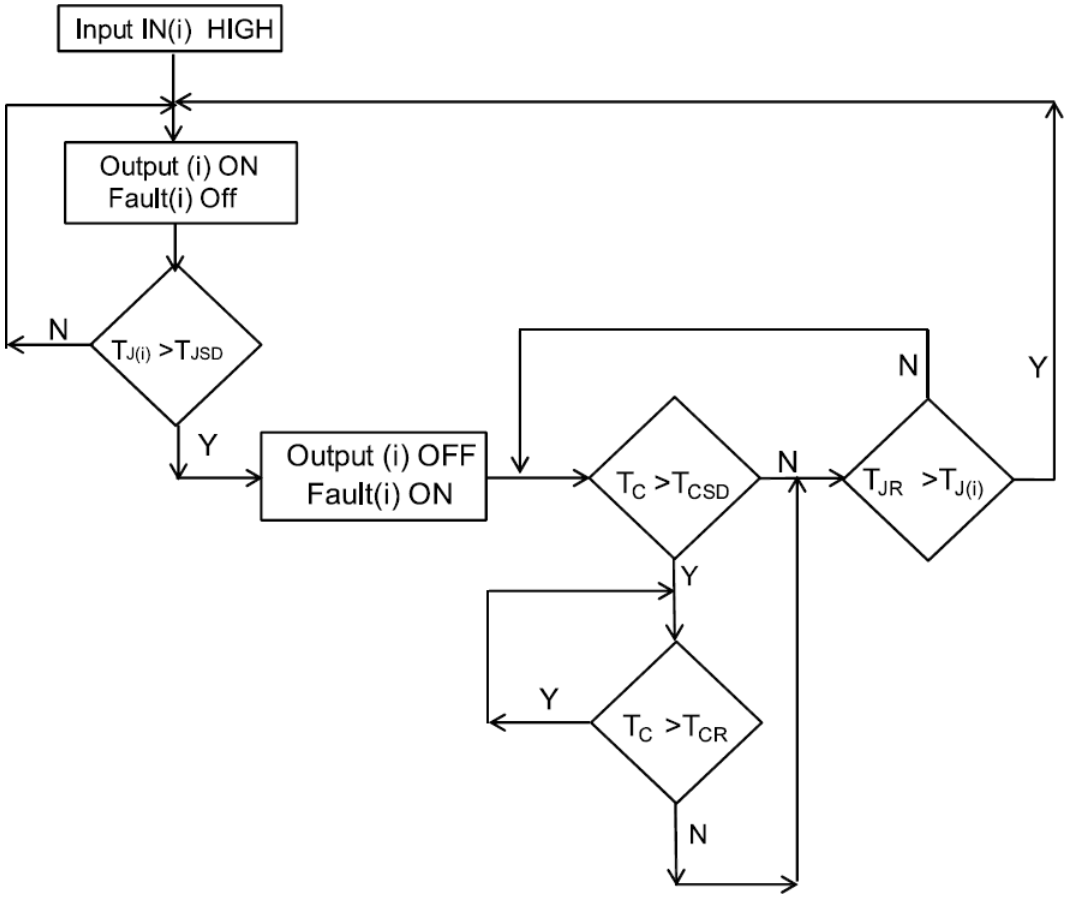


Figure 8. **Thermal protection plot, T_J > T_{JSD}**

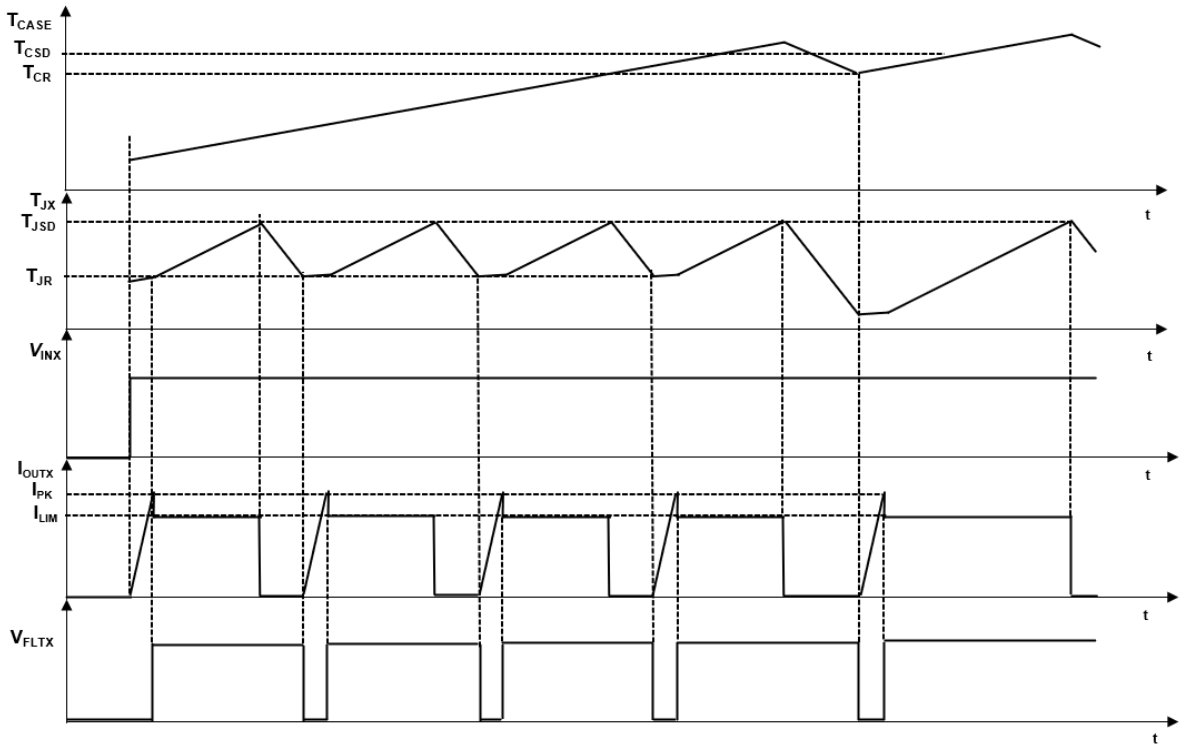
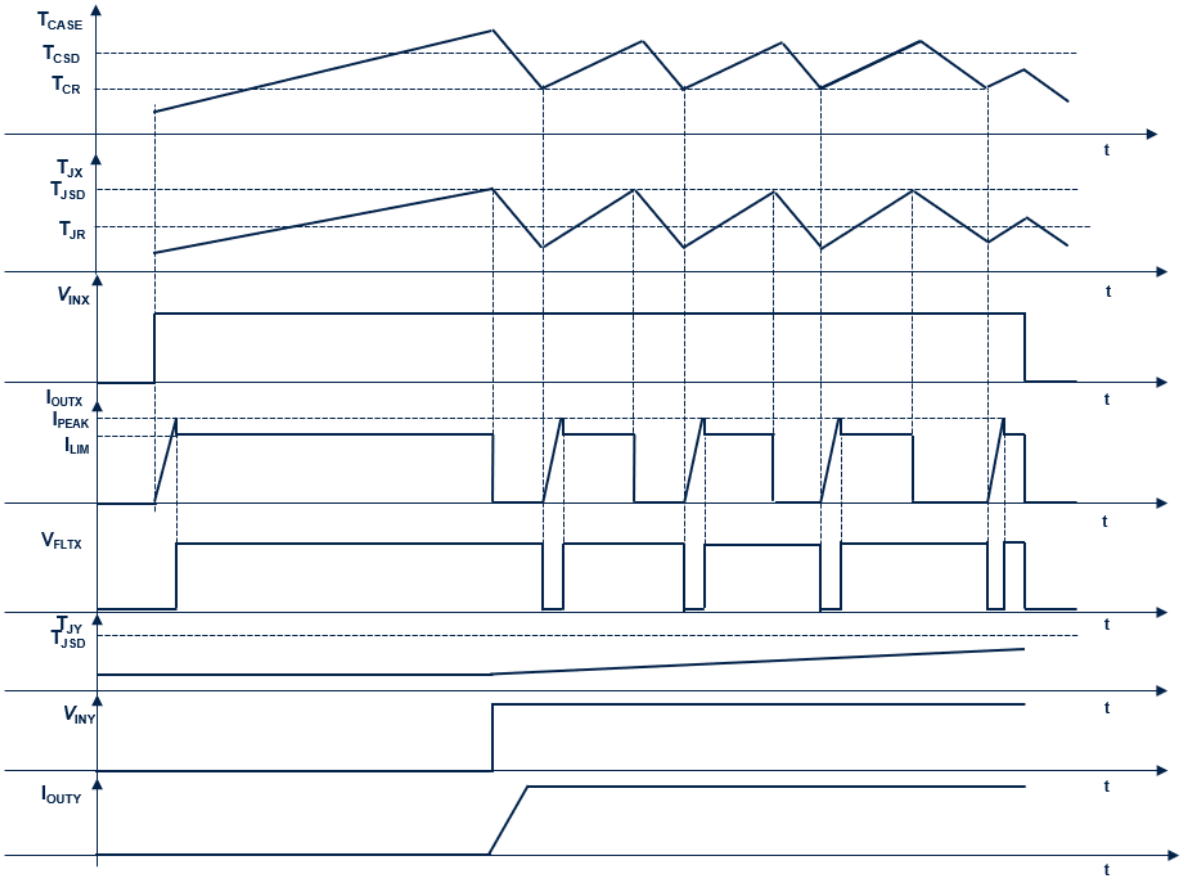


Figure 9. **Thermal protection plot, $T_C > T_{CSD}$**



7.3 Overload

The IC integrates two independent overload protection circuits (one for each output channel) consisting of an output current sensing section and an output current limitation section.

When the output channel is ON, the sensing circuitry monitors the current supplied to the load: if the activation threshold (I_{PK-X}) is triggered, then the current limitation control circuitry is activated to limit output current to the current limitation level (I_{LIM-X}) and FLT_X pin is activated until the overload condition is removed.

The IC allows the user to set both single and dual activation thresholds for each channel. See the following sections for details and Table 9 / Table 10 for specific activation thresholds and limitation levels.

Note that while an output channel operates below its activation threshold, the power dissipation can be calculated by $R_{ON} * I_{OUT}^2$, but when the current limitation circuit is activated, power dissipation increases and can be calculated by $V_{DS} * I_{LIM-X}$, where V_{DS} is the voltage drop between OUT_X and V_{CC} pins of the IC. In order to protect the IC against thermal stress, the overtemperature protection is always active and retains the highest priority.

7.3.1 Overload protection with dual threshold

This case is activated when the pin I_{PDX} is connected to GND by a capacitor (C_{PD}) and the IC works with two activation thresholds I_{PKH-X} and I_{PKL-X}.

The I_{PKH-X} is active only in the limited time frame between the L-H transition of the IN_X signal and the D_{PKX} delay defined by the following design rule:

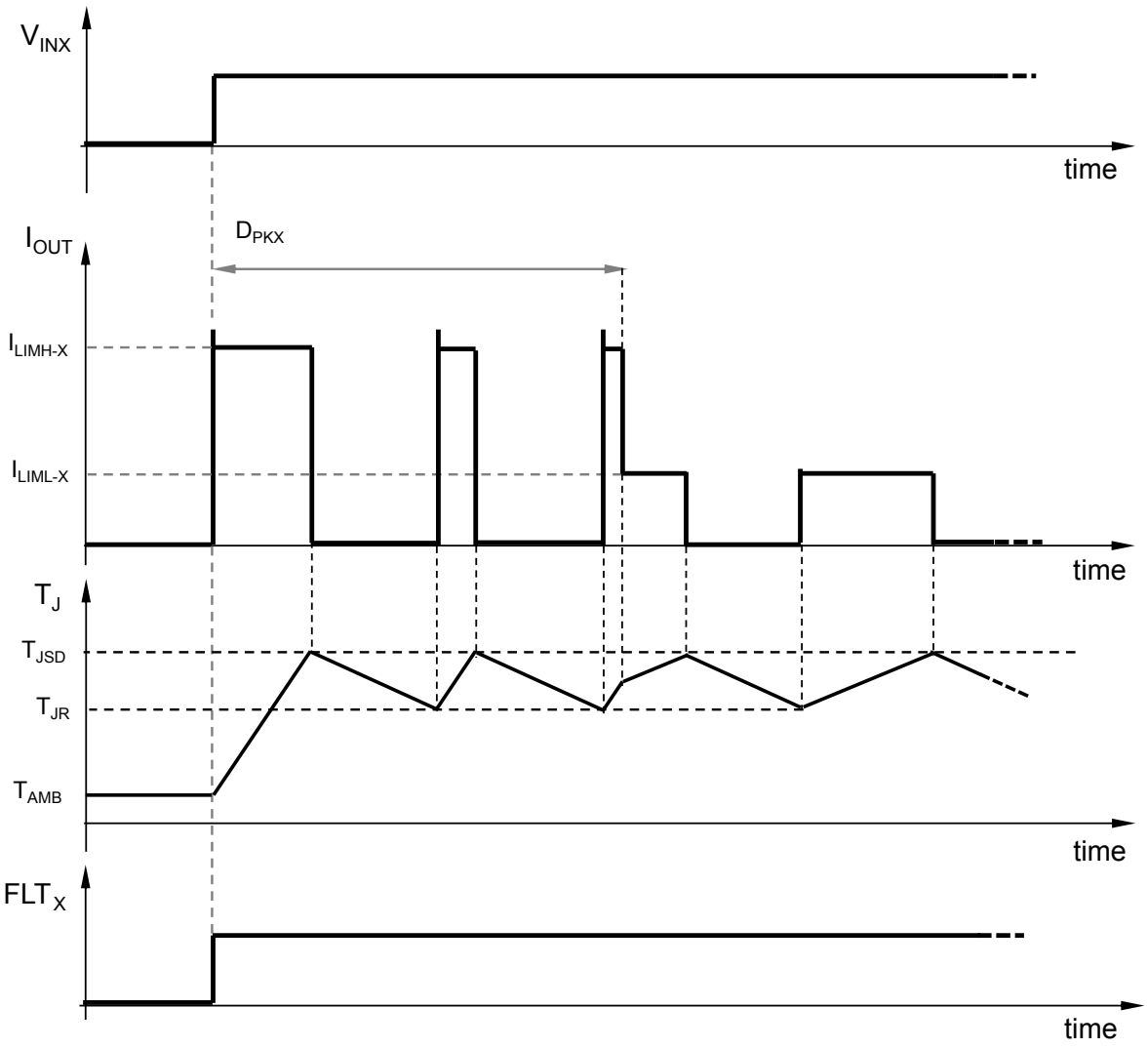
$$D_{PKX}\,[\mu s] = 215 \times CPD\,[nF]$$

The above design rule is valid in the range 470 pF ≤ C_{PD} ≤ 470 nF (see Table 9 / Table 10).

If the I_{PKH-X} is triggered within the D_{PKX} time frame, then the output current is limited to I_{LIMH-X}.

After D_{PKX} has elapsed, the IC operates with I_{PKL-X} activation threshold and I_{LIML-X} limitation level, respectively.

Figure 10. Short-circuit behavior with dual threshold ($T_{CASE} < T_{CSD}$)



7.3.2 Overload protection with single (low) threshold

The user can set the activation threshold to I_{PKL-X} and the limitation level to I_{LIML-X} by connecting the I_{PDX} pin to the related IN_X pin with a 220 KΩ resistor.

This condition is equivalent to setting D_{PKX} = 0 µs.

Note: Leaving I_{PDX} floating is equivalent to having an initial peak duration of 1 µs.

7.3.3 Overload protection with single (high) threshold

The user can set the activation threshold to I_{PKH-X} and the limitation level to I_{LIMH-X} by connecting the I_{PDX} pin to GND with a 10 KΩ resistor.

7.4 V_{CC} disconnection protection

V_{CC} disconnection involves the disconnection of the module from the supply line. When this condition is detected, the output channel can be driven normally until the voltage on VCC pin remains higher than the UVLO threshold.

In case of inductive load, if the V_{CC} is disconnected while the channel is active, the energy stored in the inductance is discharged through the power switch thanks to the integrated demagnetization circuit.

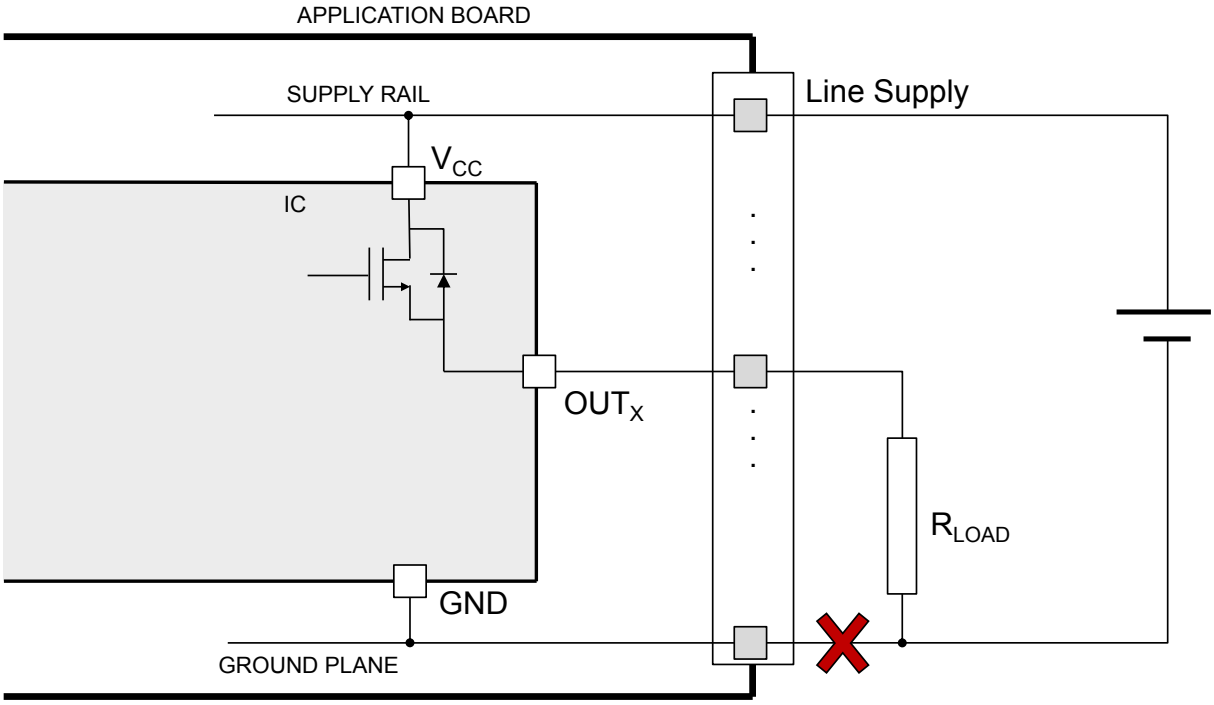
7.5 GND disconnection protection

GND disconnection is the disconnection of the module from the reference line. When this condition occurs, the output channel is turned off regardless of the input status.

When this event occurs, the IC continues working normally until the voltage between VCC and GND pins of the IC results ≥ V_{UVOFF}. The voltage on the GND pin of the IC rises up to the supply rail voltage level. In case of a GND disconnection event, a current (I_{LGND}) flows through OUT pin.

For an inductive load, if the GND is disconnected while the output channel is active, the current flows through the power, which is activated by an active clamp as if the input had been deactivated.

Figure 11. Ground disconnection



8 Active clamp

Active clamp is also known as Fast Demagnetization of inductive loads or Fast Current Decay. When a high-side driver turns off an inductance, an under-voltage on output is detected.

The OUT pin is pulled-down to V_{CC}-V_{DEMAG}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at ~V_{DEMAG} until the load energy has been dissipated. The energy is dissipated in both IC internal switch and load resistance.

Figure 12. Active clamp equivalent principle schematic

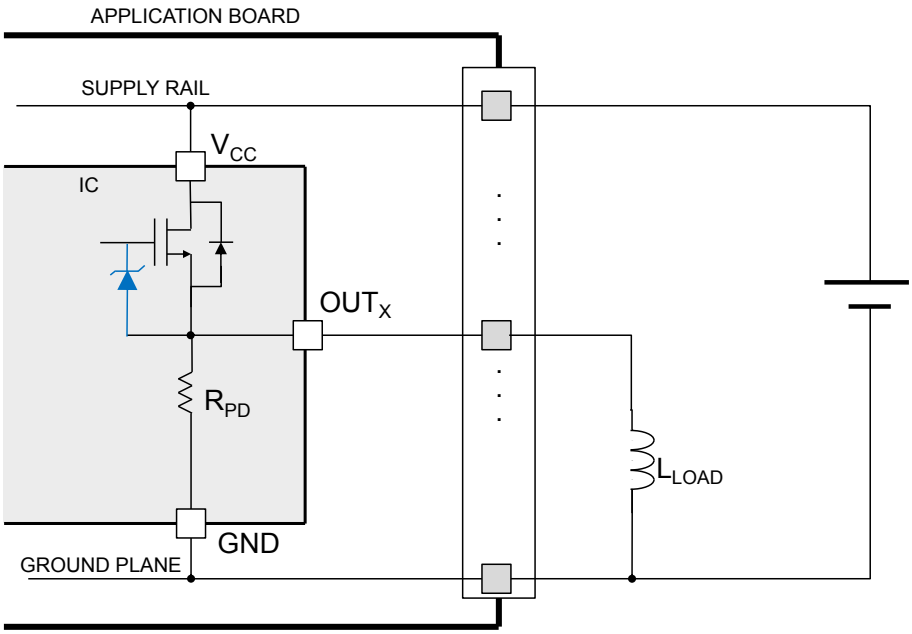


Figure 13. Typical demagnetization: E vs I (single pulse, two channels driven simultaneously) at V_{CC} = 24 V and T_{AMB} = 125 °C

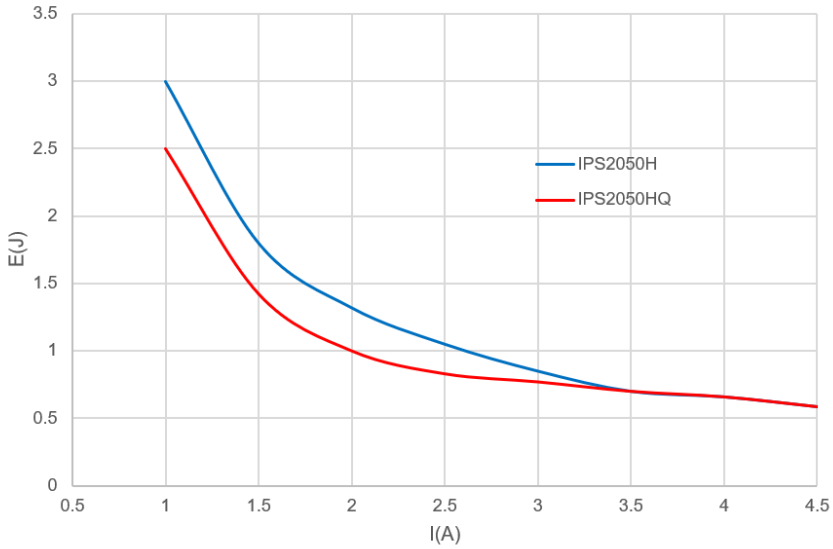
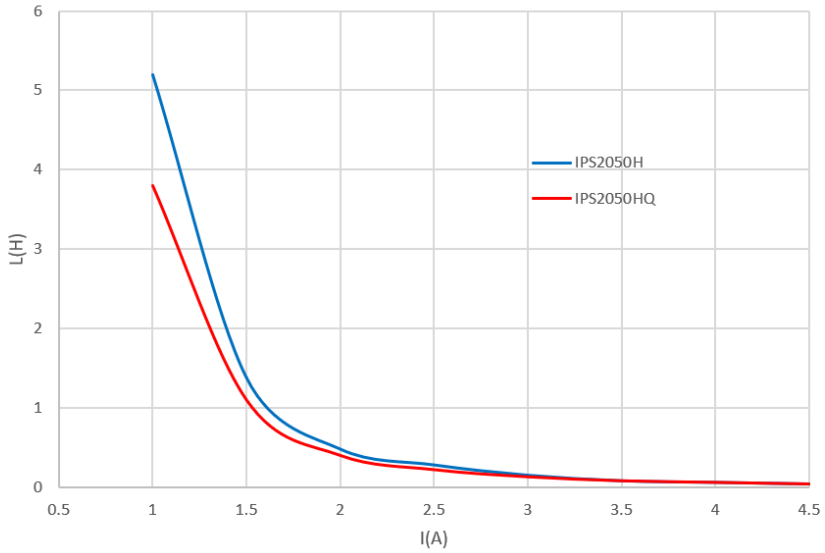


Figure 14. Typical demagnetization: L vs I (single pulse, two channels driven simultaneously) at V_{CC} = 24 V and T_{AMB} = 125 °C



9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Package mechanical data

Figure 15. **PowerSSO-24 package dimensions**

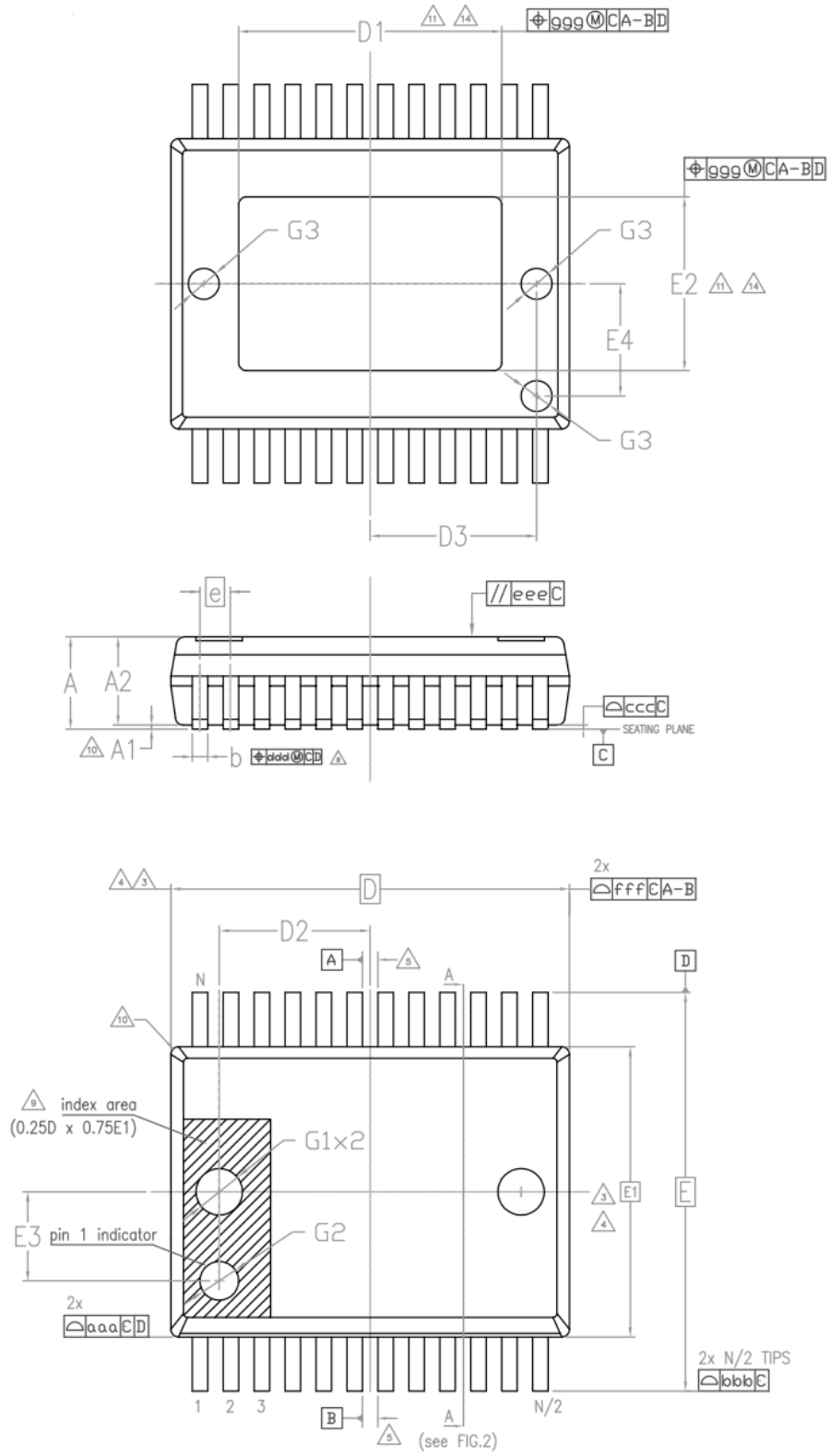


Figure 16. **PowerSSO-24 package, section A-A**

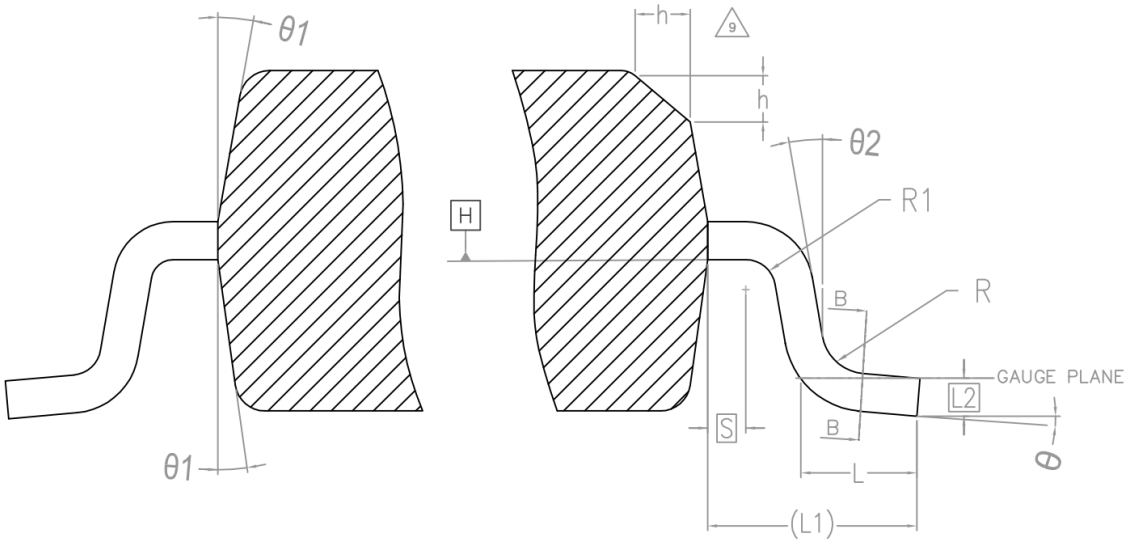


Figure 17. **PowerSSO-24 package, section B-B**

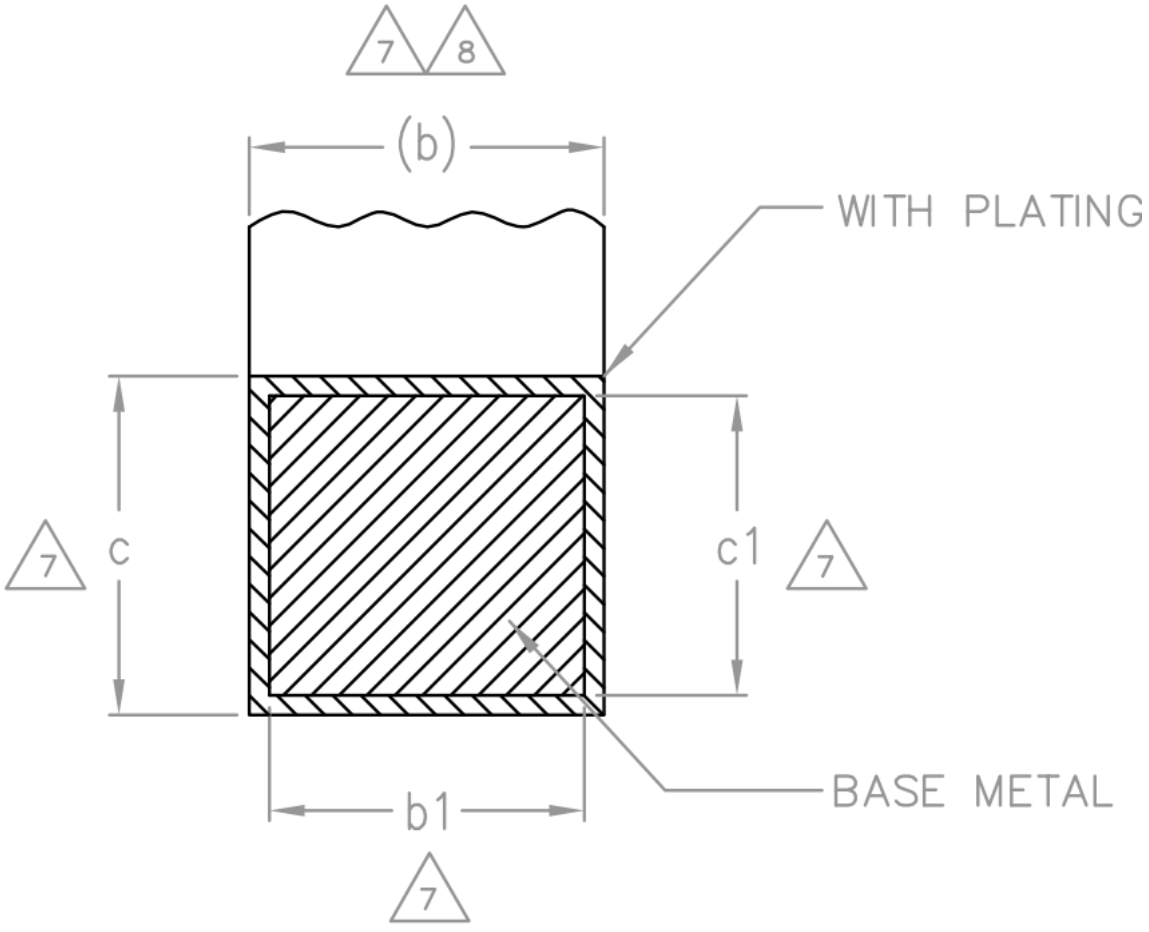


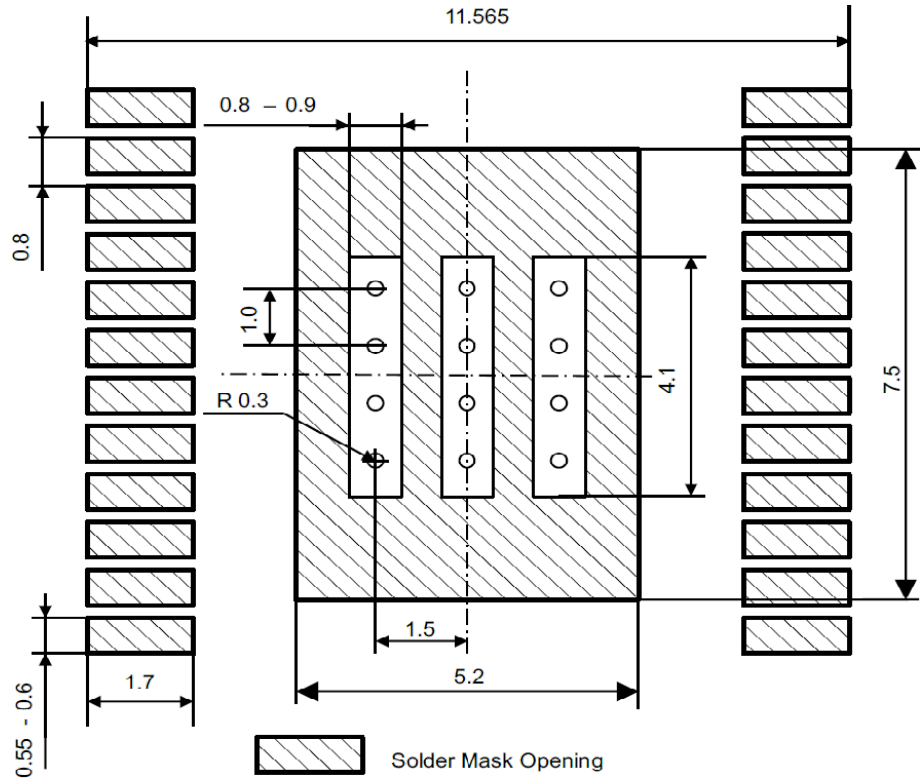
Table 13. **PowerSSO-24 mechanical data**

Symbol	[mm]		
	Min.	Nom.	Max.
Θ	0°	-	7°
Θ1	5°	-	10°
Θ2	0°	-	-
A	-	-	2.42
A1	0.005	-	0.09
A2	2.23	2.28	2.33
b	0.375	-	0.45
b1	-	0.40	-
c	0.24	-	0.30
c1	0.20	0.20	0.30
D		10.30 BSC	
D1	6.60	-	7.00
D2	-	3.65	-
D3	-	4.30	-
e		0.80 BSC	
E		10.30 BSC	
E1		7.50 BSC	
E2	4.60	-	5.00
E3	-	2.30	-
E4	-	2.90	-
G1	-	1.20	-
G2	-	1.00	-
G3	-	0.80	-
h	0.30	-	0.40
L	0.60	0.70	0.85
L1		1.40 REF	
L2		0.25 BSC	
N		24	
R	0.30	-	-
R1	0.20	-	-
S	0.25	-	-

Table 14. **Tolerance of forms and positions**

Symbol	Tolerance of forms and positions
aaa	0.20
bbb	0.20
ccc	0.10
ddd	0.20
eee	0.10
fff	0.20
ggg	0.15

Figure 18. **PowerSSO-24 suggested footprint [mm]**



STMicroelectronics is not responsible for PCB-related issues. The footprint shown in the above figure is a suggestion which may differ from the customer PCB supplier design rules.

Figure 19. **VFQFPN-48L package dimensions**

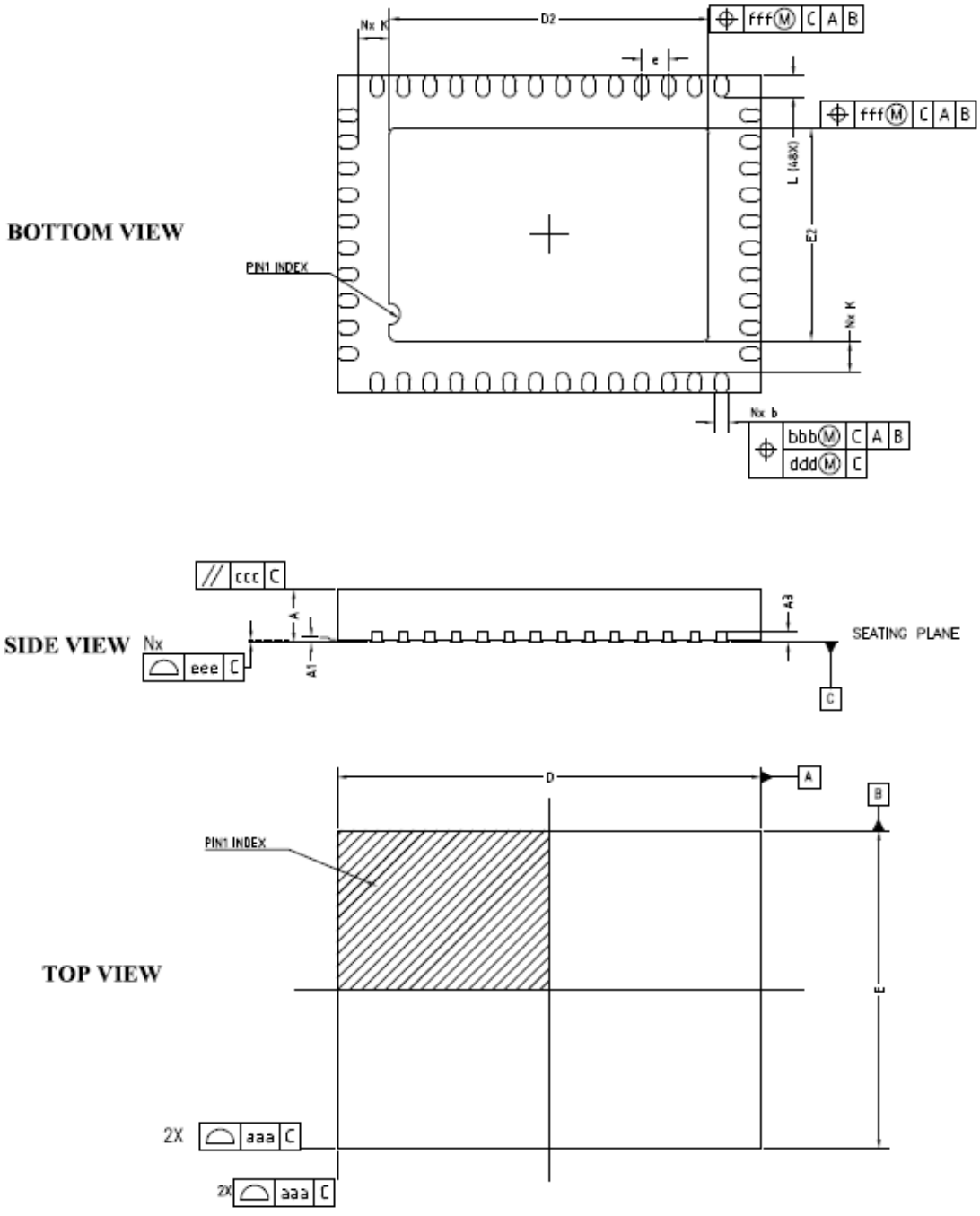


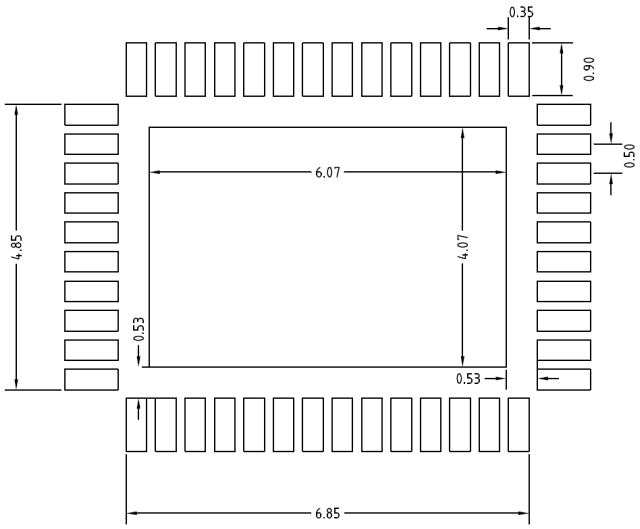
Table 15. **VFQFPN-48L mechanical data**

Symbol	[mm]		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3		0.20 REF.	
b	0.20	0.25	0.30
D		8.00 BSC	
e		0.50 BSC	
E		6.00 BSC	
D2	5.97	6.02	6.07
E2	3.97	4.02	4.07
L	0.365	0.40	0.435
k	0.53	-	-
N		48	

Table 16. **Tolerance of forms and positions**

Symbol	Tolerance of forms and positions
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Figure 20. **VFQFPN-48L suggested footprint [mm]**



10 Packing information

10.1 Packing mechanical data

Figure 21. **PowerSSO-24 tube shipment (no suffix)**

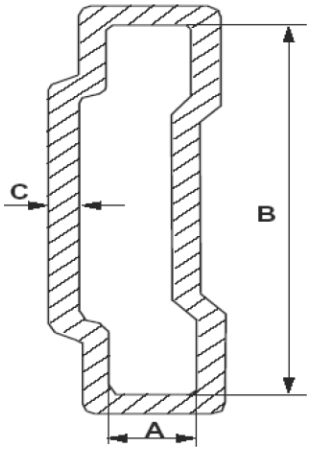


Table 17. **PowerSSO-24 tube shipment information**

All dimensions are in mm

Description	Value
Base quantity	49
Bulk quantity	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

Figure 22. **PowerSSO-24 reel shipment**

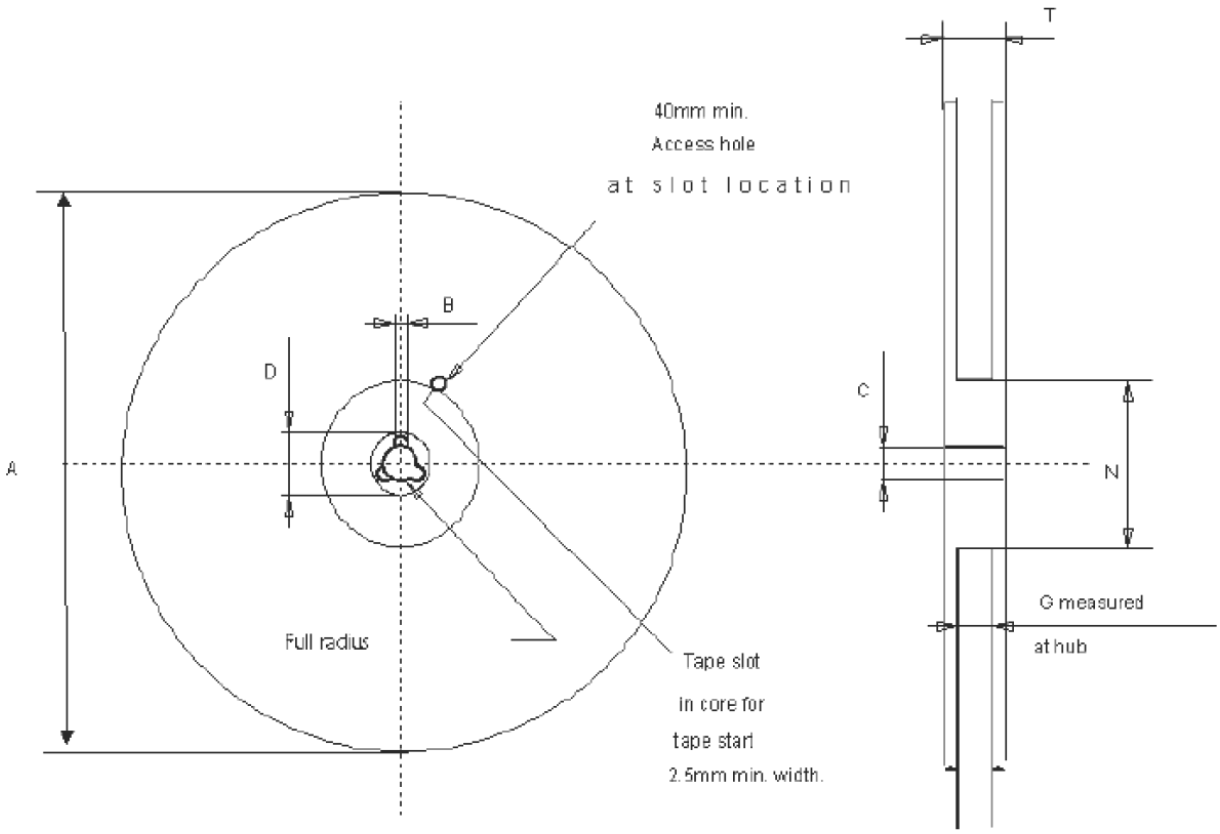


Table 18. **PowerSSO-24 reel information**

All dimensions are in mm

Description	Value
Base quantity	1000
Bulk quantity	1000
A (max.)	330
B (min.)	1.5
C (±0.2)	13
F	20.2
G (2 ±0)	24.4
N (min.)	100
T (max.)	30.4

Figure 23. **PowerSSO-24 tape drawings**

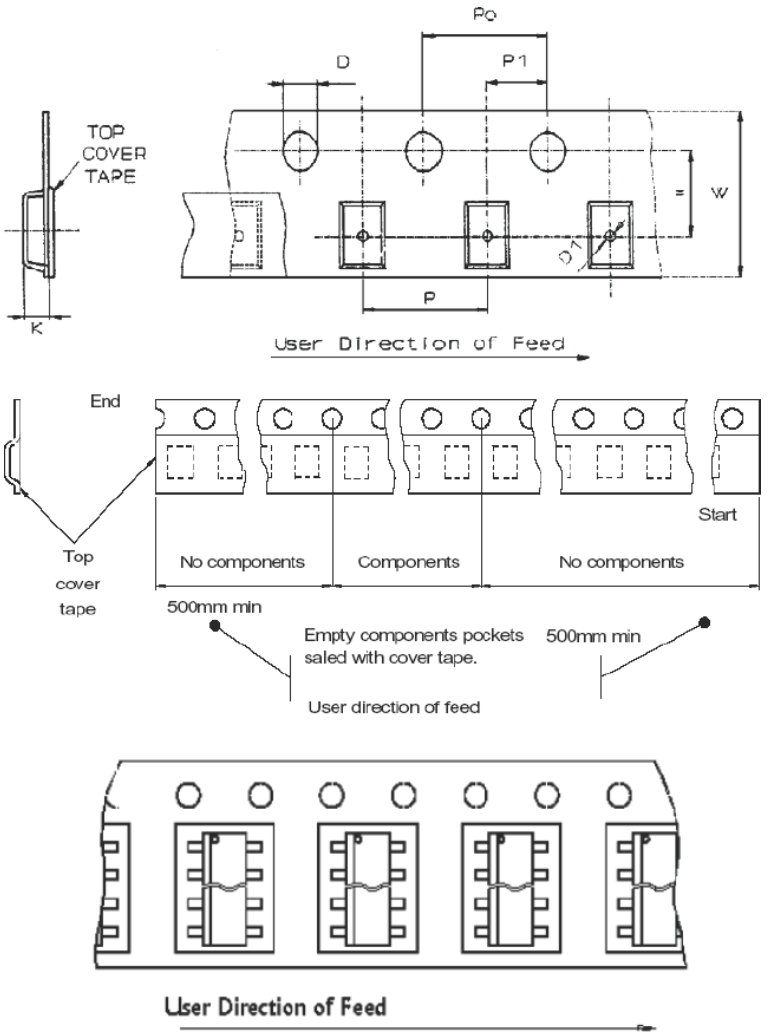


Table 19. **PowerSSO-24 tape dimension**

All dimensions are in mm

Description	Symbol	Value
Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: According to the Electronic Industries Association (EIA) standard 481 rev. A, Feb 1986.

Figure 24. **VFQFPN-48L reel shipment reference**

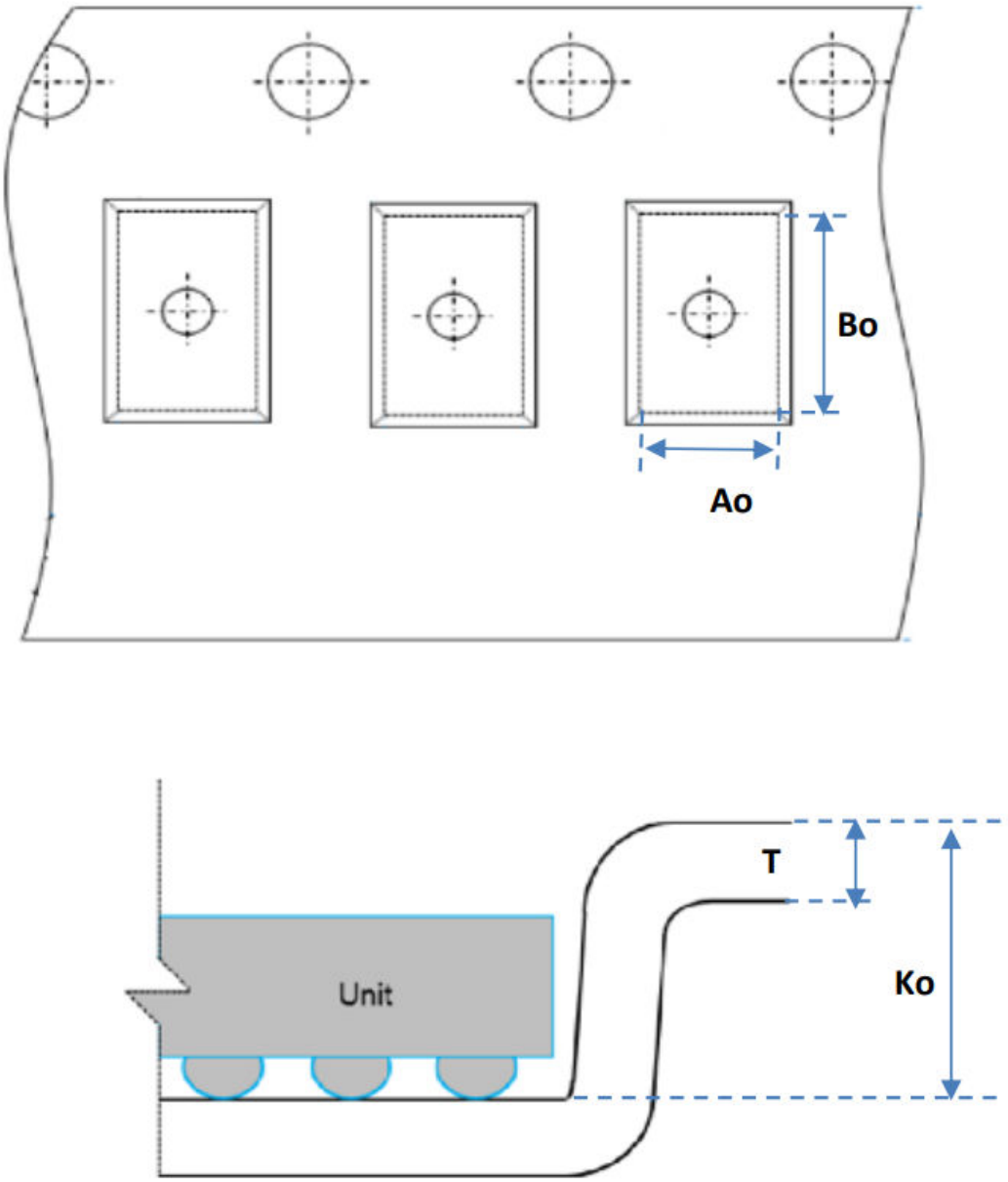
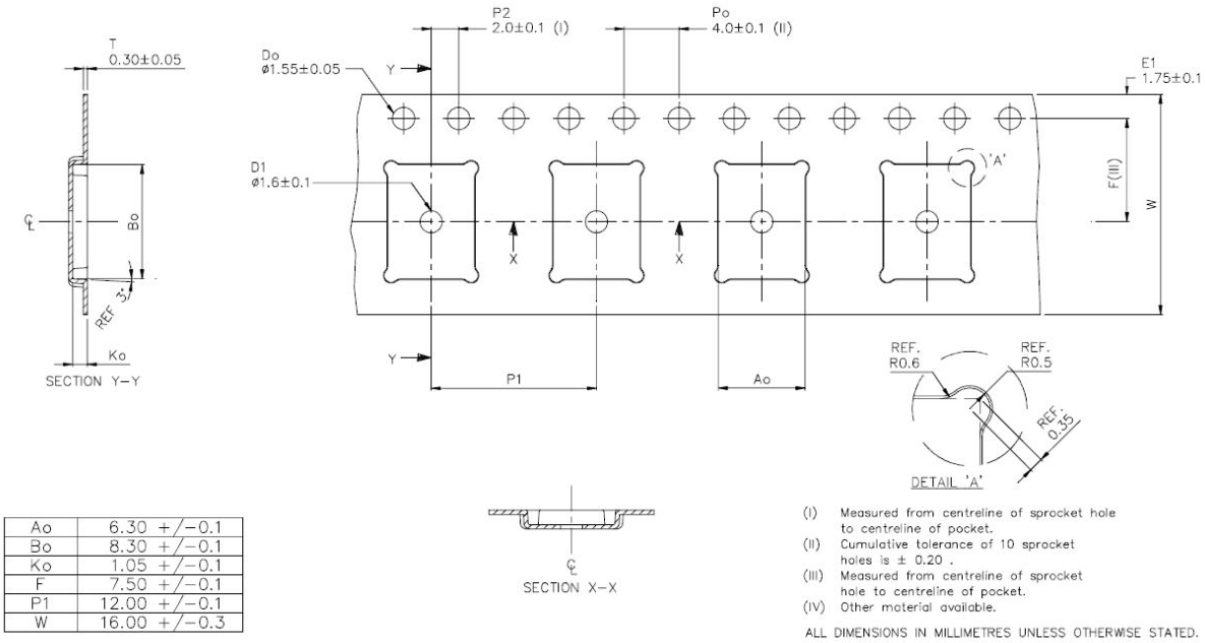


Table 20. **Standard SPC parameters**

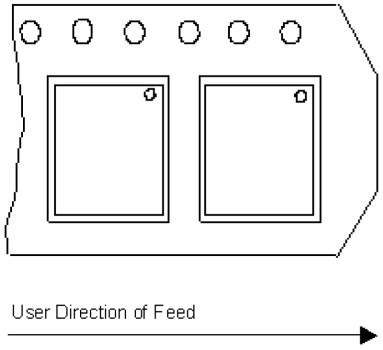
Item	Description
Ao	Pocket Length
Bo	Pocket Width
Ko	Pocket Depth
T	Tape Thickness

Figure 25. **VFQFPN-48L carrier tape dimensions**



Ao	6.30 +/−0.1
Bo	8.30 +/−0.1
Ko	1.05 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Figure 26. **VFQFPN-48L carrier tape, Pin 1 indication**



11 Ordering information

Table 21. **Ordering information**

Part number	Package	Packaging
IPS2050H	PowerSSO-24	Tube
IPS2050HTR		Tape and reel
IPS2050H-32		Tube
IPS2050HTR-32		Tape and reel
IPS2050HQ	VFQFPN-48L 8x6x0.9 mm	Tape and reel
IPS2050HQ-32		

Revision history

Table 22. **Document revision history**

Date	Version	Changes
15-Nov-2021	1	Initial release.
02-Dec-2021	2	Changed I_{SOFF} max. value in Table 4.
01-Aug-2022	3	Add QFN data: fig.2, 12, 15, 16, 20, 21, 22; tables 1, 2, 3, 14, 15, 19, 20. Divided table 9 in tables 9, 10, 11. Some minor changes.
26-Apr-2023	4	Modified Table 1; corrected Table 12; changed Figure 8 and Figure 9; add Figure 14. Changed Figure 15 and Table 13; add Figure 16 and Figure 17 ; some minor changes.
04-Jul-2023	5	Corrected RPNs and summary link table in cover page; added ST sub-brand in cover page; changed FLTx pin description in Table 1; changed package name to VFQFPN-48L.
05-Aug-2025	6	Corrected typo in Table 9 and Table 10.

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