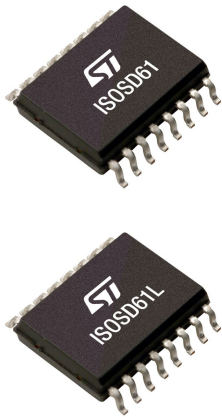


## 16-Bit isolated $\Sigma$ - $\Delta$ modulator, single-ended and LVDS interfaces



### Features

- Up to 25 MHz external clock input
- $\pm 320$  mV full scale analog input range
- 16 bits resolution, no missing codes
- 86 dB typical SNR
- -83 dB typical THD
- 13 bits typical ENOB
- Low Voltage Differential Signaling (LVDS) and Single - ended (TTL/CMOS) options
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  extended industrial temperature range
- SO-16 wide package
- 30 kV/ $\mu\text{s}$  typical High Common-mode transient immunity
- 6000 V<sub>PEAK</sub> Isolation Voltage V<sub>IOTM</sub>
- 1200 V<sub>PEAK</sub> Working Voltage V<sub>IORM</sub>

### Application

Current and voltage sensing in:

- Industrial motor control
- Solar inverter
- UPS
- Electric vehicle charger
- Factory automation
- Telecom and server power supply

#### Product status link

ISOSD61

#### Product label



### Description

The ISOSD61 is a galvanic isolated second order Sigma-Delta modulator based on embedded transformer coupling technology. It converts an analog input signal with maximum range of  $\pm 320\text{mV}$  into a high speed, 25 Msps, 1-bit digital data stream. The signal information can be rebuilt by means of a digital filtering. The modulator is isolated from the digital I/O section through a high-speed isolated data coupling, whose performances are far better than other isolated transceivers like optocouplers.

# 1 Device overview

Figure 1. ISOSD61L Block diagram

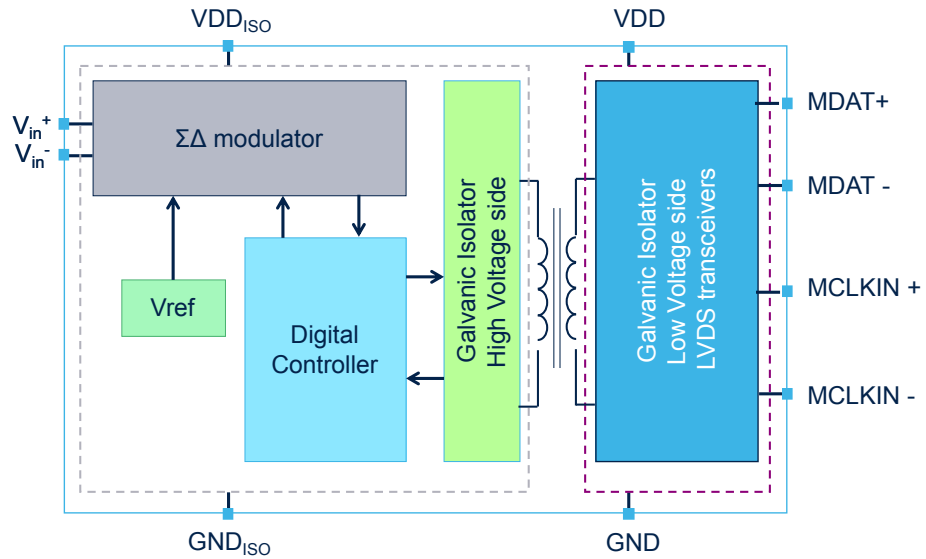
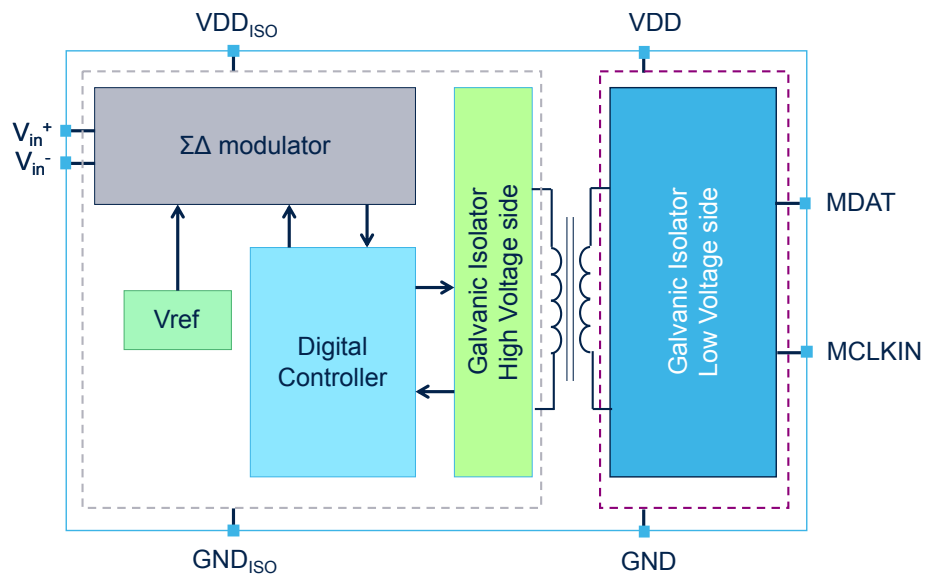
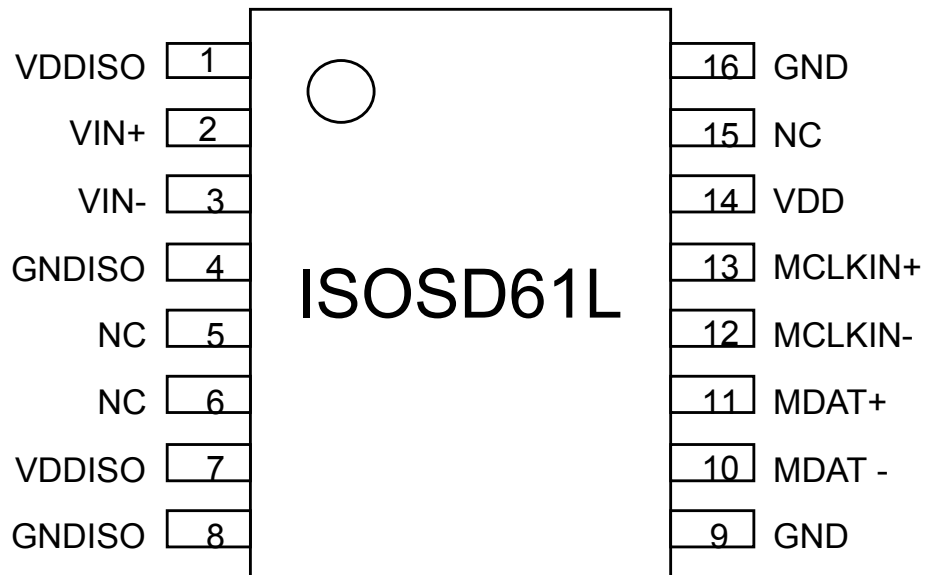
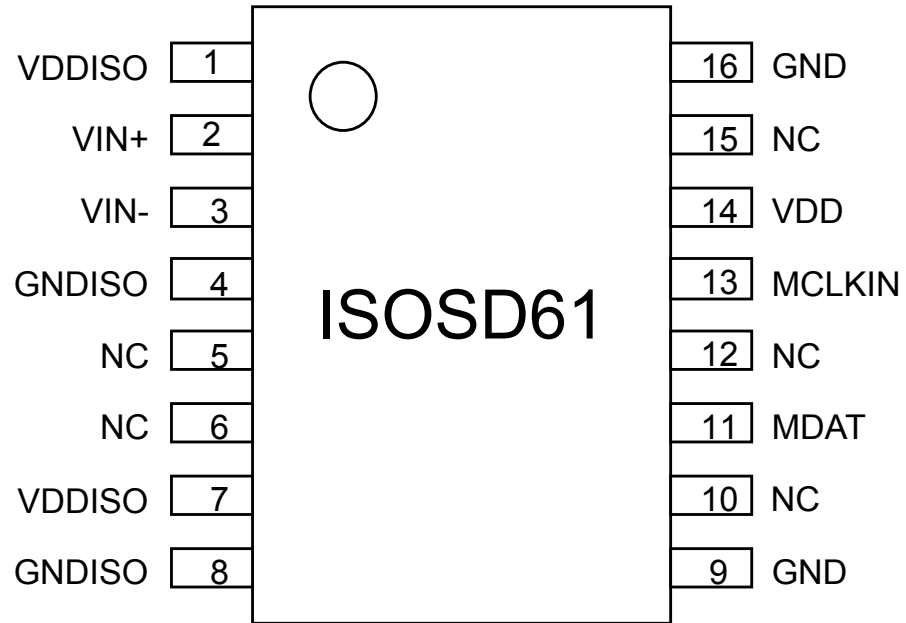


Figure 2. ISOSD61 Block diagram



## 2 Pin description

Figure 3. Pin connection



**Table 1. Pin description**

Pin No.	Pin name	Pin description (ISOSD61L)	Pin description (ISOSD61)
1	VDDISO	VDD high voltage side	VDD high voltage side
2	VIN+	Positive analog input	Positive analog input
3	VIN-	Negative analog input	Negative analog input
4	GNDISO	GND high voltage side	GND high voltage side
5	NC <sup>(1)</sup>		
6	NC <sup>(1)</sup>		
7	VDDISO	VDD high voltage side	VDD high voltage side
8	GNDISO	GND high voltage side	GND high voltage side
9	GND	GND low voltage side	GND low voltage side
10	MDAT-	Serial data output-	NC
11	MDAT+/MDAT	Serial data output+	Serial data output
12	MCLKIN-	Clock input-	NC
13	MCLKIN+/MCLKIN	Clock input+	Clock input
14	VDD	VDD low voltage side	VDD low voltage side
15	NC		
16	GND	GND low voltage side	GND low voltage side

1. For test purpose only; it must be connected to GND in functional mode.

### 3 Device specifications

**Table 2. Isolation characteristics**

Description	Symbol	Test Conditions	Characteristic	Unit
Maximum Working Isolation Voltage	$V_{IORM}$	-	1200	$V_{PEAK}$
Input to Output Test Voltage In accordance with VDE 0884-11	$V_{PR}$	Method a, Type test	1920	$V_{PEAK}$
		$V_{PR} = V_{IORM} \times 1.6$ , $t_m = 10$ s		
		Partial discharge < 5 pC		
		Method b, 100 % Production test	2250	$V_{PEAK}$
		$V_{PR} = V_{IORM} \times 1.875$ , $t_m = 1$ s		
Partial discharge < 5 pC				
Transient Overvoltage (Highest Allowable Overvoltage)	$V_{IOTM}$	$t_{ini} = 60$ s, Type test	6000	$V_{PEAK}$
Maximum Surge Test Voltage	$V_{IOSM}$	Type test	6000	$V_{PEAK}$
Isolation Resistance	$R_{IO}$	$V_{IO} = 500$ V at $T_S$ , Type test	$>10^9$	$\Omega$

**Table 3. UL 1577**

Description	Symbol	Characteristic	Unit
Isolation Withstand Voltage, 1min (Type test)	$V_{ISO}$	3535/5000	$V_{RMS}/V_{PEAK}$
Isolation Test Voltage, 1sec (100% production)	$V_{ISOtest}$	4242/6000	$V_{RMS}/V_{PEAK}$

**Table 4. Safety-limiting values (maximum values allowed in the event of a failure)**

Description	Symbol	Value	Unit
Case temperature	$T_S$	150	$^{\circ}\text{C}$
Input current	$I_{S, INPUT}$	100	mA
Output power	$P_{S, OUTPUT}$	1400	mW

**Table 5. Isolation and safety-related specifications**

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	CLR	8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (External Creepage)	CPG	8	mm	Measured from input terminals to output terminals, shortest distance path along body
Tracking Resistance (Comparative Tracking Index)	CTI	$\geq 400$	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group			II	Material Group (DIN VDE 0110, 1/89, Table 1)

**Table 6. Absolute maximum ratings**

Parameter	Symbol	Min.	Max.	Units
Storage temperature	$T_S$	-55	150	$^{\circ}\text{C}$

Parameter	Symbol	Min.	Max.	Units
Operating temperature	$T_A$	-40	125	°C
Supply voltage	$V_{DD}, V_{DDISO}$	-0.3	6	V
Steady-state input voltage	$V_{IN+}, V_{IN-}$	-0.3	$V_{DDISO} + 0.5$	V
Digital input/output voltages	MDAT+, MDAT- MCLKIN+, MCLKIN-	-0.3	3.6	V
Lead solder temperature			260 for 10 s.	°C

**Table 7. Recommended Operating Conditions**

Parameter	Symbol	Min.	Max.	Units
Ambient operating temperature	$T_A$	-40	125	°C
VDD supply voltage	$V_{DD}$	3	5.5	V
VDDISO supply voltage	$V_{DDISO}$	4.5	5.5	V
Analog input voltage	$V_{IN+}, V_{IN-}$	-200	200	mV

**Table 8. Electrical specifications**

$V_{DD}=3$  V to 5.5 V,  $V_{DDISO} = 4.5$  to 5.5 V,  $V_{IN+} = -200$  mV to +200 mV,  $T_A=-40$  to 125 °C,  $f_{MCLKIN}=5$  to 25MHz unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
<b>STATIC CHARACTERISTICS</b>						
Resolution			16		bits	with SINC3 filter with OSR=256 and $V_{IN+}-V_{IN-}=200$ mV
Integral nonlinearity	INL		±3		LSB	
Differential nonlinearity	DNL		±0.2		LSB	No missing codes
Offset error	$V_{VOS}$		-0.8		mV	
Offset drift vs. temperature	$TCV_{VOS}$		1.5	4.5	µV/°C	
Offset drift vs. $V_{DDISO}$			200		µV/V	
Gain error	$G_E$			±1.0	%	
Gain error drift vs. Temperature	$TCG_E$		60		ppm/°C	
Gain error drift vs. $V_{DDISO}$			600		µV/V	
<b>ANALOG INPUTS</b>						
Full-scale differential voltage input range	FSR	-320		+320	mV	$V_{IN} = V_{IN+} - V_{IN-}$
Average input bias current	$I_{INA}$		-0.5		µA	$V_{DDISO} = 5$ V, $V_{DD} = 5$ V, $V_{IN+} = 0$ V;
	$I_{INA}$		40	50	µA	$V_{DDISO} = 5$ V, $V_{DD} = 5$ V, $V_{IN+} = 300$ mV;
Input capacitance	$C_{INA}$		10		pF	Across $V_{IN+}$ or $V_{IN-}$ to GNDISO
<b>DYNAMIC CHARACTERISTICS</b>						
Signal-to-noise ratio	SNR		86		dB	
Signal-to-(noise + distortion) ratio	SNDR		80		dB	

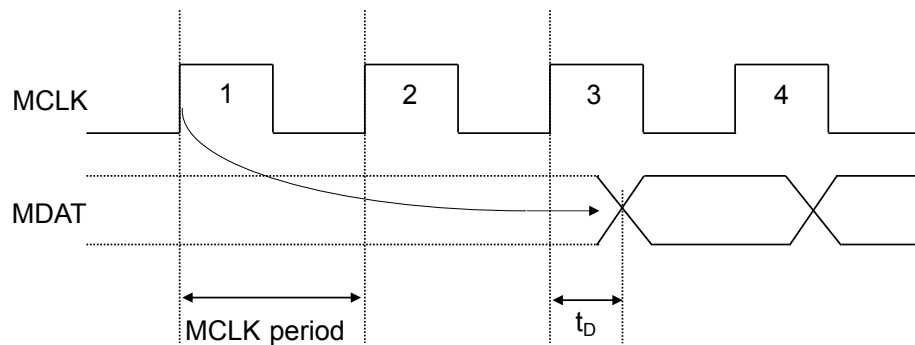
Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Effective number of bits	ENOB		13		bits	
Spurious free dynamic Range	SFDR		83		dB	
Total harmonic distortion	THD		-83		dB	
Common-mode transient immunity	CMTI	25	30		kV/ $\mu$ s	Transient Pulse repetition frequency up to 100 KHz
<b>POWER SUPPLY</b>						
VDDISO supply current	$I_{DDISO}$		35		mA	@ 25 MHz
			30		mA	@ 10 MHz
VDD supply current	$I_{DD}$		13		mA	$V_{DD} = 5\text{ V}$ , $f_{MCLKIN} = 25\text{ MHz}$
			11		mA	$V_{DD} = 5\text{ V}$ , $f_{MCLKIN} = 10\text{ MHz}$
			12.5		mA	$V_{DD} = 3.3\text{ V}$ , $f_{MCLKIN} = 25\text{ MHz}$
			10.5		mA	$V_{DD} = 3.3\text{ V}$ , $f_{MCLKIN} = 10\text{ MHz}$

1. Guaranteed by characterization

Table 9. Timing specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Modulator clock input frequency	$f_{CK}$	5		25	MHz	Clock duty cycle 48% to 52%
Data delay after rising edge of CK	$t_D$	5		20	ns	CL = 15 pF

Figure 4. Timing sequence diagram



The data is provided to the MDAT output 2 clock cycles after the effective sampling instant.

**Table 10. LVDS transmitter signaling specifications (ISOSD61L)**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Output voltage high	$V_{OH}$	-0.3		1475	mV	$R_{LOAD} = 110 \Omega \pm 20\%$
Output voltage low	$V_{OL}$	925			mV	$R_{LOAD} = 110 \Omega \pm 20\%$
Output differential voltage	$ V_{OD} $	240		420	mV	$R_{LOAD} = 110 \Omega \pm 20\%$
Output offset voltage	$V_{OS}$	1125	1200	1275	mV	$R_{LOAD} = 110 \Omega \pm 20\%$
Output current	$I_O$	2.2		3.7	mA	$R_{LOAD} = 110 \Omega \pm 20\%$
LVDS load impedance, single ended	$R_L$	80	110	140	$\Omega$	$V_{CM} = 1 V$ and $1.4 V$
$R_L$ mismatch between both channels	$\Delta R_L$			10	%	
MDAT rise time	$t_{LH}$	0.5		5	ns	$R_{LOAD} = 110 \Omega \pm 20\%$ $C_{LOAD} = 30 pF$
MDAT fall time	$t_{HL}$	0.5		5	ns	$R_{LOAD} = 110 \Omega \pm 20\%$ $C_{LOAD} = 30 pF$

**Table 11. LVDS receiver signaling specifications**

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage range	$V_R$	-0.3		3.6	V	$R_{LOAD} = 110 \Omega \pm 20\%$
Common mode voltage <sup>(1)</sup>	$V_C$	0.05		2.4 <sup>(2)</sup>	V	$R_{LOAD} = 110 \Omega \pm 20\%$
Differential input voltage <sup>(3)</sup>	$ V_i $	100			mV	$R_{LOAD} = 110 \Omega \pm 20\%$
Differential input hysteresis voltage <sup>(4)</sup>	$ V_{HYS} $	25			mV	$R_{LOAD} = 110 \Omega \pm 20\%$
Differential input capacitance	$C_i$			5	pF	$R_{LOAD} = 110 \Omega \pm 20\%$
Bias resistors <sup>(5)</sup>	$R_{PULLUP}/$ $R_{PULLDOWN}$	140	200	260	k $\Omega$	

- $V_C$  is defined as the voltage that is mid-way between  $V_H$  and  $V_L$ .
- This parameter is guaranteed with  $V_{dd} > 4 V$ .
- $|V_i|$  defines the minimum differential voltage that is guaranteed to be recognized as a valid input, 1 or 0, by the receiver.
- $|V_{hys}|$  defines the minimum voltage separation between the actual  $|V_i|$  rising and falling thresholds.
- A pullup resistor is present between the minus LVDS input and  $V_{3.3}$ , and a pulldown resistor is present between plus LVDS input and GND in order to force a '0' value if the LVDS input is floating.



**Table 12. Single-ended input and output signaling specifications (ISOSD61)**

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input high voltage	$V_{IH}$	2			V	$V_{DD} = 3.3\text{ V}$
		$V_{DD} \times 0.7$			V	$V_{DD} = 5\text{ V}$
Input low voltage	$V_{IL}$			0.8	V	$V_{DD} = 3.3\text{ V}$
				$V_{DD} \times 0.3$	V	$V_{DD} = 5\text{ V}$
Input current	$I_{IND}$		$\pm 0.5$		$\mu\text{A}$	
Input capacitance	$C_{IND}$		6		pF	
Output high voltage	$V_{OH}$	$V_{DD} - 0.06$	$V_{DD} - 0.04$		V	$V_{DD} = 5\text{ V}$ , $I_{OUT} = -0.2\text{ mA}$
		$V_{DD} - 0.05$	$V_{DD} - 0.03$			$V_{DD} = 3.3\text{ V}$ , $I_{OUT} = -0.2\text{ mA}$
Output low voltage	$V_{OL}$		0.01	0.02	V	$I_{OUT} = 0.2\text{ mA}$

**Table 13. Package characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
IC junction-to-ambient thermal resistance	$\theta_{JA}$		80		$^{\circ}\text{C}/\text{W}$	On a 2s2p JEDEC board in free air as per JEDEC JESD51, $T_A = 25^{\circ}\text{C}$

## 4 Terminology

### Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

### Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

### Offset error

Offset error is the deviation of the center scale code from the ideal scale code corresponding to 0 V differential input voltage.

### Gain error

The gain is the derivative of the digital output code vs. the input signal. Graphically, for the output code vs. input signal transfer function (an ideal straight line), the gain is the slope of such function. The gain error is the % difference between the measured slope and the expected one.

### Signal-to-Noise-and-Distortion Ratio (SINAD or SNDR)

SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the RMS value of the sine wave, and noise is the RMS sum of all non-fundamental AC signals up to half the sampling frequency ( $f_S / 2$ ), including harmonics.

### Signal-to-Noise Ratio (SNR)

SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the RMS amplitude of the fundamental. Noise is the RSM sum of all non-fundamental AC signals up to half the sampling frequency ( $f_S/2$ ).

The ratio is dependent on the number of quantization levels in the conversion: the greater the number of levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-Noise Ratio} = (6.02N + 1.76) \text{ [dB]}$$

Therefore, for a 12-bit converter, the SNR is 74 dB.

### Isolation transient immunity

The isolation transient immunity specifies the rise and fall speed of a transient pulse applied across the isolation barrier, beyond which clock or data is corrupted.

### Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of harmonics to the fundamental. The THD stated in this datasheet is defined as:

$$\text{THD} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:  $V_1$  is the RMS amplitude of the fundamental.  $V_2, V_3, V_4, V_5,$  and  $V_6$  are the RMS amplitudes of the second through the sixth harmonics. The result is in dB.

### Spurious Free Dynamic Range (SFDR)

SFDR is defined as the ratio of the RMS value of the AC Noise Peak (up to  $f_S / 2$ ) to the RMS value of the fundamental.

### Effective Number of Bits (ENOB)

ENOB is defined by:

$$\text{ENOB} = (\text{SINAD} - 1.76) / 6.02 \text{ [bits]}$$

### Noise free code resolution

Noise free code resolution represents the resolution in bits for which there is no code flicker. The noise free code resolution for an N-bit converter is defined as

$$\text{Noise free code resolution} = \log_2 \left( \frac{2^N}{\text{Peak-to-peak Noise}} \right) \text{ [bits]}$$

The peak-to-peak noise in LSBs is measured with  $V_{IN+} = V_{IN-} = 0 \text{ V}$ .

### Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output with an input differential sine wave,  $P_D$ , to the power of an input peak-to-peak sine wave applied to the common-mode voltage of  $V_{IN+}$  and  $V_{IN-}$ ,  $P_{CM}$ , as:

$$CMRR (dB) = 10 \log(P_D/P_{CM})$$

**Power Supply Rejection Ratio (PSRR)**

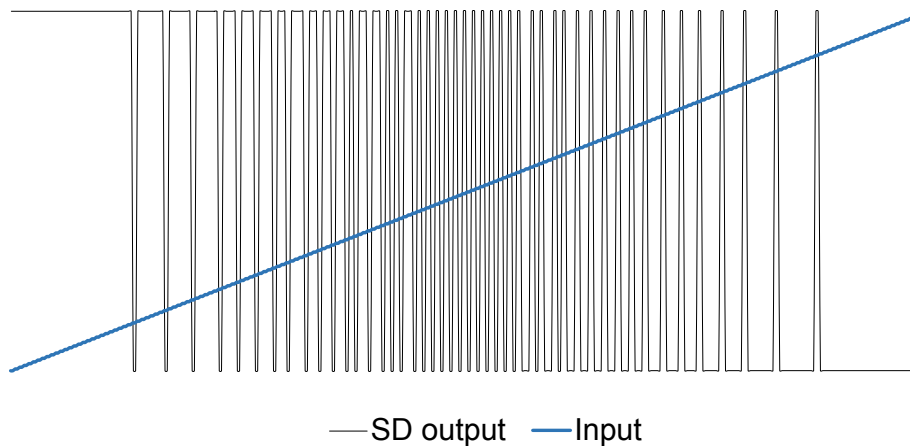
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the specified full-scale transition point due to a change in power supply voltage from the nominal value.

$$PSRR = 20 \log (\text{change in supply} / \text{change in output voltage})$$

## 5 Theory of operation

The differential analog input of the ISOSD61 implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The sample clock (MCLKIN) provided externally, is the clock signal for the conversion process as well as the output data-framing clock. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter.

**Figure 5. Sigma-Delta data stream vs. differential input voltage ramp**



A differential signal of 0 V results (ideally) in a stream of alternating 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. Any differential input voltage produces a stream whose ratio between 1s and the total number of pulses of the time is proportional to the ratio between the input voltage and the full-scale differential range (+320 mV - -320 mV= 640 mV). The correspondent equation is:

$$\frac{\text{nr of 1s}}{\text{tot nr of pulses}} = 0.5 + \frac{V_{in}}{640}$$

Where:  $V_{in}$ : input differential voltage [mV]; nr of 1s: count of 1 bit over a given time; tot nr of pulses: count of the total 1 and 0 bits over the given time.

This means for a maximum positive differential input signal +320 mV there would be only 1s (signal stuck at 1) and for a maximum negative of -320 mV only 0s (signal stuck at 0).

To decode the original information, the digital output stream must be digitally filtered and decimated. A recommended filter is the SINC3 3<sup>rd</sup> order decimator. The SINC3 filter can be easily realized, for instance, with a FPGA or an MCU like STM32.

### Analog inputs

The analog front-end of the modulator implements a differential switched capacitor circuitry, whose purpose is to sample and hold the analog signal every clock cycle. Like any A/D converter, to prevent the conversion of aliasing signal, in accordance to the Nyquist-Shannon theorem, a low-pass filter should be added at the analog inputs. Its cut- frequency should be below half the sampling frequency. The capacitors of this LP filter help to smooth the undershoots and overshoots of the internal switching capacitors. Every switching has a charge current injected, and the effective impedance of the analog inputs decreases with the clock frequency increasing. To avoid undesired signal voltage drops, the LP filter resistors should have a value in the order of tenth of ohms.

### Digital filtering

A typical filtering technique for sigma-delta modulators is the implementation of an SINC3 digital filter. The code below is an example of a generic SINC3 filter written for GNU Octave that can be easily ported to other languages or systems:

```
function [output, output_dec]=sinc3_generic(in)
%in is 1xsamples
%output is 1xsamples
%output_dec is 1x(samples/dec_fact)
```

```

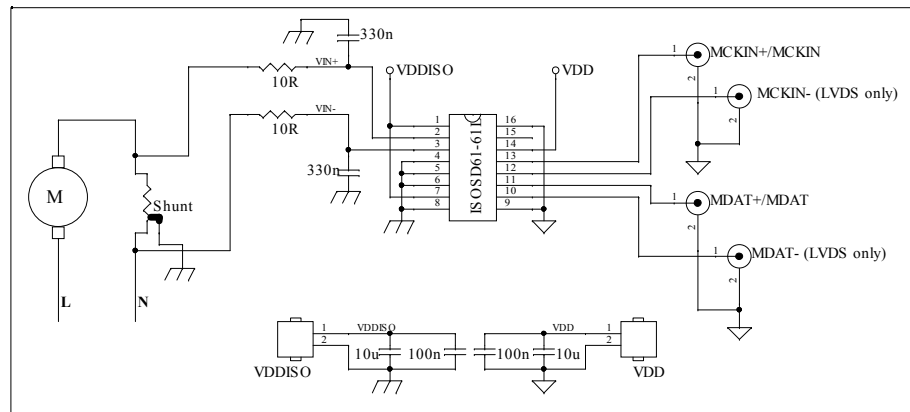
nbits = 25;
accbits = 46; %minimum accumulator size
dutbits = 16;
stages = 3;
dec_fact = 256;
dim = size(in);
samples = dim(2);
feed_state = zeros(1,stages);
fwd_state = zeros(1, stages);
i = 1;
out_feed_state = 0;
for k=1:samples
if ( i > 1 )
output(k) = round(out_feed_state * 2^((dutbits-1)));
else
output(k) = 0;
end
if ( k == dec_fact*i )
output_dec(i) = round(out_feed_state * 2^((dutbits-1)));
in_fwd = feed_state(stages);
fwd_sum = 0;
for s=1:stages
fwd_sum += fwd_state(s);
end
out_feed_state = in_fwd - fwd_sum;
si = stages;
while(si > 1)
fwd_sum = 0;
for s=1:(si-1)
fwd_sum += fwd_state(s);
end
fwd_state(si) = in_fwd - fwd_sum;
si--;
end
fwd_state(1) = in_fwd;
i++;
end
si = stages;
while(si > 1)
feed_state(si) = feed_state(si) + feed_state(si-1);
si--;
end
feed_state(1) = feed_state(1) + in(k)* 2^(-(nbits-1));
end
end

```

#### Application Design Tips

In [Figure 6](#) below a typical application schematics is shown:

Figure 6. Typical application schematics



Large use of capacitors on both VDDiso and VDD supply pins for decoupling is strongly recommended.

Though the device can withstand high transients across the isolation barrier, the application designer must take care of board coupling between the analog front-end and the digital back-end domains. They must also take design actions in order to avoid any loss of clearance and creepage distances. Failure to ensure these can lead to severe permanent damage.

The analog input tracks should be kept symmetrical and equalized in impedance, to minimize additional offset.

The use of ground planes for noise reduction is recommended.

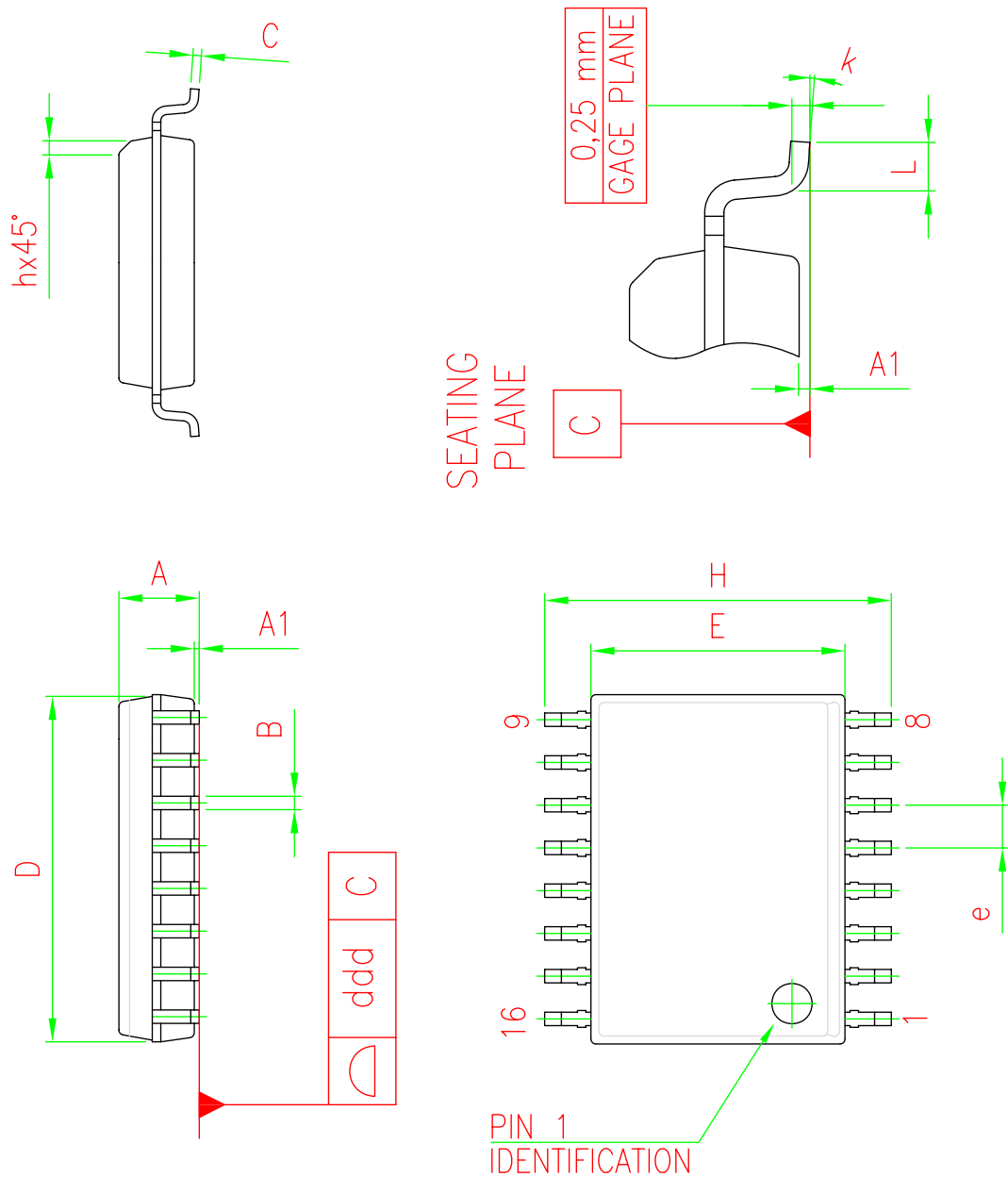
For LVDS digital interfacing, the use of termination resistors (typically 100 ohm) is recommended.

## 6 Package description

The ISOSD61/61L is hosted in an SO-16 wide package. The mechanical drawing is shown below.

**Figure 7. Mechanical drawing**

TITLE : PLASTIC SMALL OUTLINE PACKAGE 16L WIDE  
PACKAGE CODE : Y7



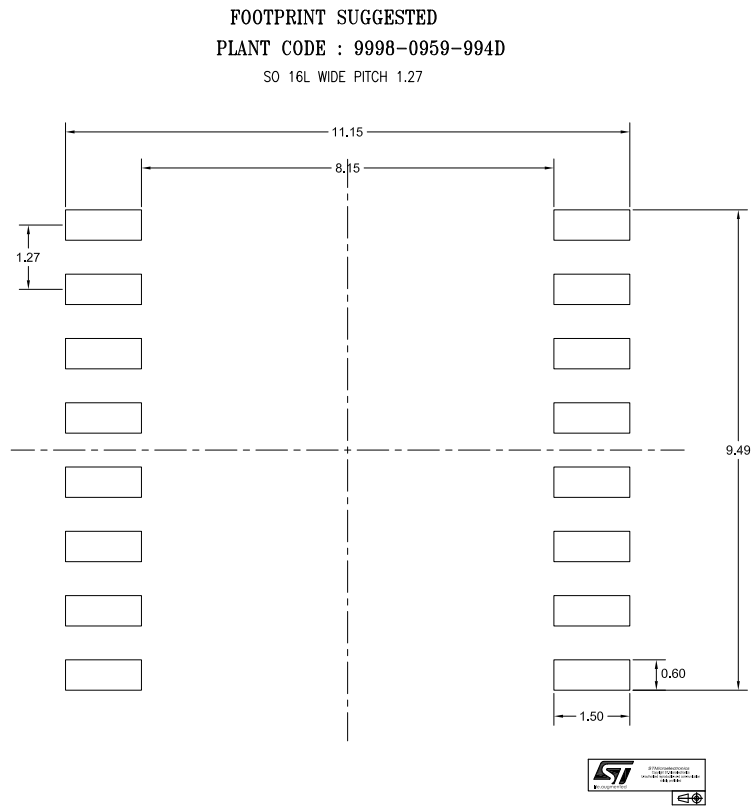
**Table 14. Package dimensions**

Dimensions							
Param.	Databook (mm)			Drawing (mm)			Notes
	Min.	Typ.	Max.	Min.	Typ.	Max.	
<b>A</b>	2.35		2.65	2.36		2.50	
<b>A1</b>	0.10		0.30	0.12	0.15	0.18	
<b>B</b>	0.33		0.51	0.375	0.40	0.425	
<b>C</b>	0.23		0.32			0.292	
<b>D</b>	10.10		10.50	10.35	10.38	10.41	(1)
<b>E</b>	7.40		7.60	7.52	7.55	7.58	
<b>e</b>		1.27			1.27		
<b>H</b>	10		10.65	10.20	10.30	10.40	
<b>h</b>	0.25		0.75		0.35		
<b>L</b>	0.40		1.27	0.60		0.75	
<b>k</b>	0		8	2	4	6	DEGREES
<b>ddd</b>			0.10			0.06	

1. Dimension D does not include mold flash, protrusions or gate burrs.  
 Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per side.



Figure 8. Recommended footprint



## 7 Ordering information

**Table 15. Device summary**

Order code	Package	Package Marking	Packing
ISOSD61	SO16W	ISOSD61	Tray
ISOSD61TR	SO16W	ISOSD61	Tape and Reel
ISOSD61L	SO16W	ISOSD61L	Tray
ISOSD61LTR	SO16W	ISOSD61L	Tape and Reel

## Revision history

**Table 16. Document revision history**

Date	Version	Changes
11-Jan-2021	1	Initial release.
26-Jan-2021	2	Added <a href="#">Table 15. Device summary</a>
10-Mar-2021	3	Deleted wrong hyperlinks.
03-May-2021	4	Modified <a href="#">Section Features</a> and <a href="#">Figure 8. Recommended footprint</a>
21-Jun-2021	5	Modified <a href="#">Table 2. Isolation characteristics</a> and added <a href="#">Table 3. UL 1577</a>
01-Dec-2021	6	Modified <a href="#">Table 4. Safety-limiting values (maximum values allowed in the event of a failure)</a>

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