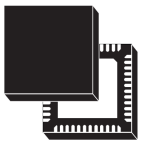
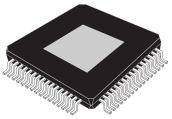
L5964

Datasheet

Automotive monolithic dual step-down switching regulator with LDO



VQFPN-48 (7x7 mm)



LQFP64

Maturity status link
L5964

Features

- AEC-Q100 qualified
- Two step-down synchronous switching voltage regulators with internal power switches:
  - Output voltage selectable by external divider (feedback voltage at 0.9 V)
  - Minimum and maximum output is limited by minimum and maximum duty cycle
  - Internal high-side/ low-side NDMOS
  - 270 kHz and 2.2 MHz selectable free-run frequencies
  - 125 kHz < f < 2.3 MHz synchronization range at SYNCIN pin
  - Programmable current limits at 2 A and 4.5 A (> 2 A requires the addition of external schottky diodes)
  - Independent hardware enabling pins
  - Independent supply inputs
  - 180° phase shift between outputs
  - Synch out 90° phase shift vs DC-DC1
  - Programmable switching frequency divider by 1, 2, 4, 8 between the two regulators
- Independent voltage supervisors/power-goods with selectable thresholds through external pin:
  - two available thresholds for UV/OV/PG signals: 90-120-95% or 80-110-85% (output voltage percentage)
- Soft-start, thermal protection
- One standby/linear regulator:
  - Output selectable with external resistor divider till 10 V
  - Soft start, hardware enable pin
  - 250 mA maximum current capability
  - Standby operative mode
  - Programmable power good thresholds (85% or 95% output voltage percentage)
  - Thermal protection
- Microcontroller reset with programmable duration, activated by output under voltage or watchdog fault
- External High Side Driver enable pin
- One integrated window watchdog (5 ms ≤ window ≤ 50 ms, with ± 20% tolerance)
- Short circuit protected outputs
- Low external components number
- Thermal shutdown junction temperature 150°C

Description

L5964 is a dual step-down switching regulator with internal power switches and a low drop-out linear/standby regulator. All the regulators have independent supply voltages, enables, power goods and thermal protections.

The switching regulators have selectable voltage supervisors and power goods, and selectable current limits. The LDO has power good and fixed current limitation.

The two DC-DC converters can work in free-run condition, with frequency selectable between two values, 270 kHz or 2.2 MHz, or synchronize themselves to an external clock (SYNCIN pin). They are 180° out of phase, while the synchronization output signal (SYNCOUT pin) is 90° out of phase with the first regulator. The phase shift simplifies the use of two ICs in the same application (4 DC/DC regulators).

DC-DC1 and DC-DC2 current limits can be independently set through the pins OCPSET1 and OCPSET2 respectively. Two current limits are available, 2 A (1.7 A min) and 4.5 A (3.7 A min).

For operation >2 A, Schottky diodes vs ground should be placed as close as possible to PHASE1/2 pins. These diodes should sustain 20 V, 2 A at room temperature and have less than 0.5 V forward voltage.

The high operating frequency allowed by the synchronization input helps to reduce AM and FM interferences and grants the use of small and low cost inductors and capacitors.

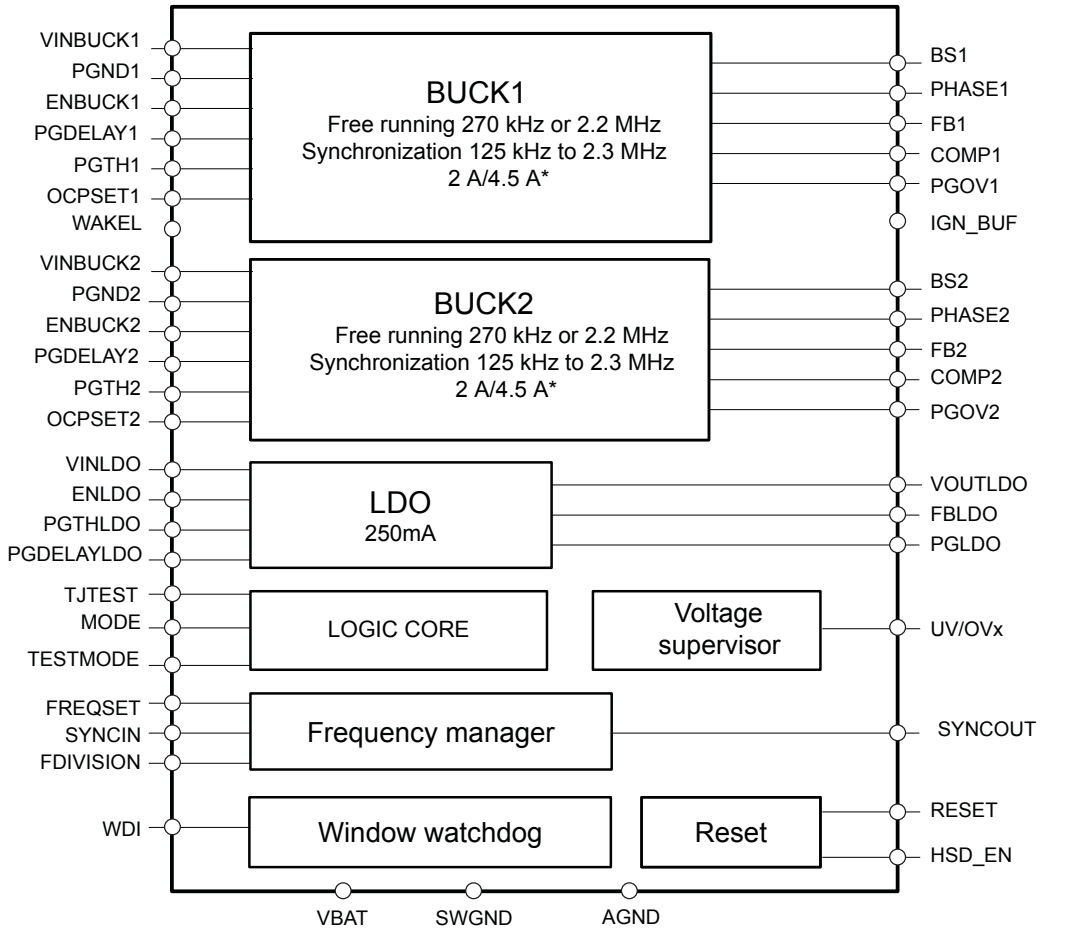
The L5964 can manage the microcontroller supply. A configurable reset output and a configurable watchdog input are available.

This IC finds application in the automotive segment, where load dump protection and wide input voltage range are mandatory. L5964 has been qualified for car passenger cars, with a standard 14 V battery. The total quiescent current, when both DC/DCs and LDO are disabled, is less than 10 µA.

The product is available in LQFP64 exposed pad up and in VQFPN48 slug down package. The slug, whenever possible, has to be connected to the ground plane.

1 Simplified, general block diagram

Figure 1. Simplified, general block diagram



* > 2 A operation requires the addition of external Schottky diodes

GADG2411171534PS

2 Pin description

2.1 LQFP64 pins description

Figure 2. **LQFP64 pinout (bottom view)**

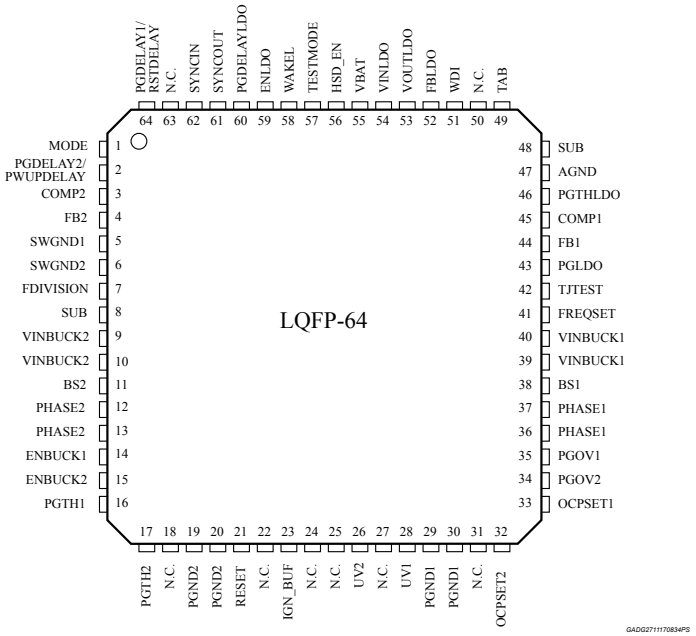


Table 1. **LQFP64 pin list**

N#	Pinname	Pin type	Pin description
1	MODE	IN	Working mode: Pin floating sets the working Mode to Normal; shorted to AGND sets the Microcontroller Mode.
2	PGDELAY2/ PWUPDELAY	IN	DC/DC2 Power good output delay time adjustable by connecting a capacitor from PGDELAY2 to AGND. In Microcontroller Mode, a capacitor sets the power up delay, from reset to watchdog input.
3	COMP2	IN/OUT	DC/DC2 Error amplifier output for compensation network connection.
4	FB2	IN/OUT	DC/DC2 Output feedback. Connected to an error amplifier that compares the feedback voltage to the internal reference voltage.
5	SWGND1	GROUND	DC/DC analog blocks ground (Switching ground).
6	SWGND2	GROUND	DC/DC analog blocks ground (Switching ground).
7	FDIVISION	IN	Frequency divider setting to make DC/DC2 working at a frequency that is 1/1, 1/2, 1/4 or 1/8 of DC/DC1 one.
8	SUB	GROUND	Device substrate ground.
9	VINBUCK2	SUPPLY	DC/DC2 power supply connection.
10	VINBUCK2	SUPPLY	DC/DC2 power supply connection.
11	BS2	OUT	Boot-strap capacitor connection for DC/DC2.
12	PHASE2	OUT	DC/DC2 power stage output (for external inductor and boot-strap capacitor connection).
13	PHASE2	OUT	DC/DC2 power stage output (for external inductor and boot-strap capacitor connection).
14	ENBUCK1	IN	DC/DC1 enable (active high).
15	ENBUCK2	IN	DC/DC2 enable (active high).

N#	Pinname	Pin type	Pin description
16	PGTH1	IN	Power good threshold setting for DC/DC1. Pin floating sets the threshold to 95% of Vout; shorted to AGND sets the threshold to 85% of Vout.
17	PGTH2	IN	Power good threshold setting for DC/DC2. Pin floating sets the threshold to 95% of Vout; shorted to AGND sets the threshold to 85% of Vout.
18	N.C.	-	Not Connected.
19	PGND2	GROUND	Power ground of DC/DC2. Connected to internal low-side source.
20	PGND2	GROUND	Power ground of DC/DC2. Connected to internal low-side source.
21	RESET	OUT	Reset signal to Microprocessor in Microcontroller Mode: in Normal mode is kept in high impedance state. Open-drain output.
22	N.C.	-	Not Connected.
23	IGN_BUF	OUT	DC/DC1 status (ON/OFF) echo to Microprocessor in Microcontroller Mode:in Normal Mode is kept in high impedance. Open-drain output.
24	N.C.	-	Not Connected.
25	N.C.	-	Not Connected.
26	UV2	OUT	Under-voltage DC/DC2 signal. Open-drain output.
27	N.C.	-	Not Connected.
28	UV1	OUT	Under-voltage DC/DC1 signal. Open-drain output.
29	PGND1	GROUND	Power ground of DC/DC1. Connected to internal low-side source.
30	PGND1	GROUND	Power ground of DC/DC1. Connected to internal low-side source.
31	N.C.	-	Not Connected.
32	OCPSET2	IN	Programmable OCP setting for DC/DC2. Pin floating sets the overcurrent threshold to 4A; shorted to AGND sets the threshold to 2 A.
33	OCPSET1	IN	Programmable OCP setting for DC/DC1. Pin floating sets the overcurrent threshold to 4A; shorted to AGND sets the threshold to 2 A.
34	PGOV2	OUT	Over-voltage DC/DC2 signal. Open-drain output.
35	PGOV1	OUT	Over-voltage DC/DC1 signal. Open-drain output.
36	PHASE1	OUT	DC/DC1 power stage output (for external inductor and boot-strap capacitor connection).
37	PHASE1	OUT	DC/DC1 power stage output (for external inductor and boot-strap capacitor connection).
38	BS1	OUT	Boot-strap capacitor connection for DC/DC1.
39	VINBUCK1	SUPPLY	DC/DC1 power supply connection.
40	VINBUCK1	SUPPLY	DC/DC1 power supply connection.
41	FREQSET	IN	Programmable internal PWM frequency for DC/DC. Pin floating sets the frequency to 2M Hz; shorted to AGND sets the frequency to 250 kHz and inhibits FDIVISION.
42	TJTEST	OUT	Device junction temperature information.
43	PGLDO	OUT	LDO regulator Power good output. Open-drain output.
44	FB1	IN/OUT	DC/DC1 Output feedback. Connected to error amplifier that compares the feedback voltage to the internal reference voltage.
45	COMP1	IN/OUT	DC/DC1 Error amplifier output for compensation network connection.
46	PGTHLDO	IN	Power good threshold setting for LDO. Pin floating sets the threshold to 95% of VOUTLDO; shorted to AGND sets the threshold to 85% of VOUTLDO.
47	AGND	GROUND	Device analog ground.
48	SUB	GROUND	Device substrate ground.
49	TAB	-	Device slug connection.
50	N.C.	-	Not Connected.

N#	Pinname	Pin type	Pin description
51	WDI	IN	Watchdog input from Microcontroller. Internal Pull Down.
52	FBLDO	IN/OUT	LDO regulator output feedback.
53	VOUTLDO	OUT	LDO regulator output.
54	VINLDO	SUPPLY	LDO regulator power supply.
55	VBAT	SUPPLY	Dedicated high voltage supply for reference blocks.
56	HSD_EN	OUT	Enable signal for external High Side switch (active low). Only active in microcontroller mode, high impedance in normal mode.
57	TESTMODE	IN	TESTMODE pin, reserved use. Connect to ground.
58	WAKEL	IN	Wake-up signal to enable DC/DC1 in OR internally with ENBUCK1 pin (ignored in Normal Mode, active low in Microcontroller Mode).
59	ENLDO	IN	LDO regulator enable (active high).
60	PGDELAYLDO	IN	LDO Power good output delay time adjustable by connecting a capacitor to AGND.
61	SYNCOUT	OUT	External Switching clock output signal.
62	SYNCIN	IN	External clock input connection. Connect an external clock at SYNCIN for frequency synchronization.
63	N.C.	-	Not Connected.
64	PGDELAY1/ RSTDELAY	IN	DC/DC1 Power good output delay time adjustable by connecting a capacitor from PGDELAY1 to AGND. In Microcontroller Mode, a capacitor sets the power up delay, from reset to watchdog input.

2.2 VQFPN-48 pins description

Figure 3. **VQFPN-48 pinout (bottom view)**

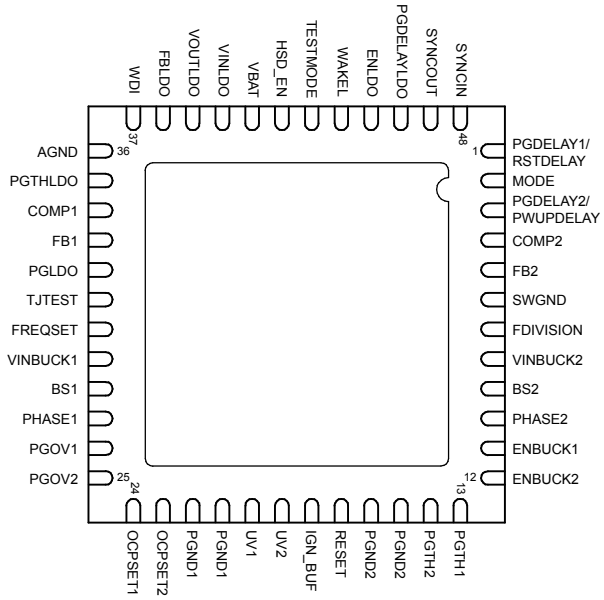


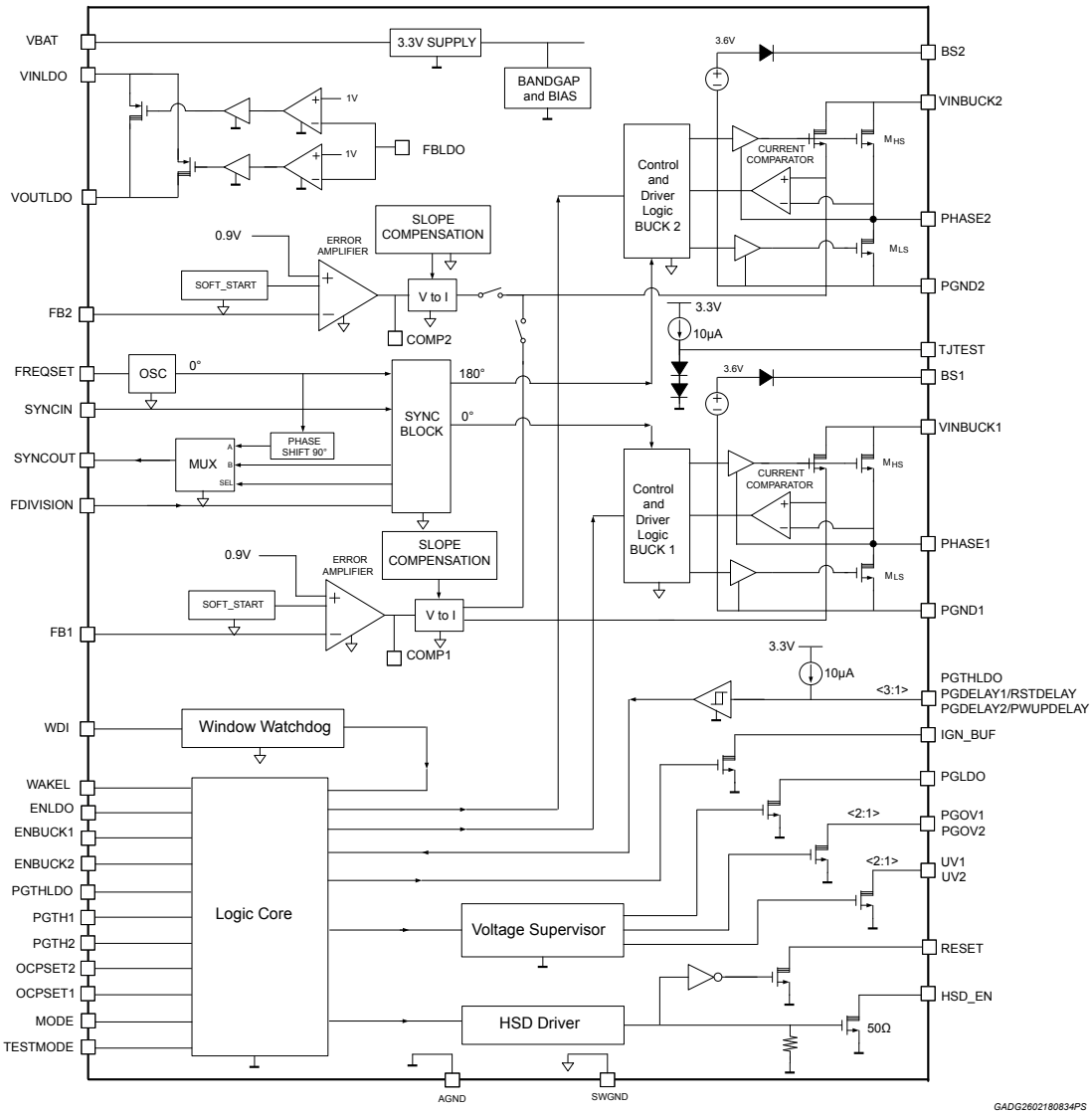
Table 2. **VQFPN-48 pin list**

N#	Pin name	Pin type	Pin description
1	PGDELAY1/ RSTDELAY	IN	DC/DC1 Power good output delay time adjustable by connecting a capacitor from PGDELAY1 to AGND. In Microcontroller Mode, a capacitor sets the power up delay, from reset to watchdog input.
2	MODE	IN	Working mode: pin floating sets the working Mode to Normal; shorted to AGND sets the Microcontroller Mode.
3	PGDELAY2/ PWUPDELAY	IN	DC/DC2 Power good output delay time adjustable by connecting a capacitor from PGDELAY2 to AGND. In Microcontroller Mode, a capacitor sets the power up delay, from reset to watchdog input.
4	COMP2	IN/OUT	DC/DC2 Error amplifier output for compensation network connection.
5	FB2	IN/OUT	DC/DC2 Output feedback. Connected to an error amplifier that compares the feedback voltage to the internal reference voltage.
6	SWGND	GROUND	DC/DC analog blocks ground (Switching ground).
7	FDIVISION	IN	Frequency divider setting to make DC/DC2 working at a frequency that is 1/1, 1/2, 1/4 or 1/8 of DC/DC1 one.
8	VINBUCK2	SUPPLY	DC/DC2 power supply connection.
9	BS2	OUT	Boot-strap capacitor connection for DC/DC2.
10	PHASE2	OUT	DC/DC2 power stage output (for external inductor and boot-strap capacitor connection).
11	ENBUCK1	IN	DC/DC1 enable (active high).
12	ENBUCK2	IN	DC/DC2 enable (active high).
13	PGTH1	IN	Power good threshold setting for DC/DC1. Pin floating sets the threshold to 95% of Vout; shorted to AGND sets the threshold to 85% of Vout.
14	PGTH2	IN	Power good threshold setting for DC/DC2. Pin floating sets the threshold to 95% of Vout; shorted to AGND sets the threshold to 85% of Vout.
15	PGND2	GROUND	Power ground of DC/DC2. Connected to internal low-side source.
16	PGND2	GROUND	Power ground of DC/DC2. Connected to internal low-side source.

N#	Pin name	Pin type	Pin description
17	RESET	OUT	Reset signal to Microprocessor in Microcontroller Mode: in Normal mode is kept in high impedance state. Open-drain output.
18	IGN_BUF	OUT	DC/DC1 status (ON/OFF) echo to Microprocessor in Microcontroller Mode:in Normal Mode is kept in high impedance. Open-drain output.
19	UV2	OUT	Under-voltage DC/DC2 signal. Open-drain output.
20	UV1	OUT	Under-voltage DC/DC1 signal. Open-drain output.
21	PGND1	GROUND	Power ground of DC/DC1. Connected to internal low-side source.
22	PGND1	GROUND	Power ground of DC/DC1. Connected to internal low-side source.
23	OCPSET2	-	Programmable OCP setting for DC/DC2. Pin floating sets the overcurrent threshold to 4 A; shorted to AGND sets the threshold to 2 A
24	OCPSET1	-	Programmable OCP setting for DC/DC1. Pin floating sets the overcurrent threshold to 4 A; shorted to AGND sets the threshold to 2 A
25	PGOV2	OUT	Over-voltage DC/DC2 signal. Open-drain output.
26	PGOV1	OUT	Over-voltage DC/DC1 signal. Open-drain output.
27	PHASE1	OUT	DC/DC1 power stage output (for external inductor and boot-strap capacitor connection).
28	BS1	OUT	Boot-strap capacitor connection for DC/DC1.
29	VINBUCK1	SUPPLY	DC/DC1 power supply connection.
30	FREQSET	IN	Programmable internal PWM frequency for DC/DC. Pin floating sets the frequency to 2M Hz; shorted to AGND sets the frequency to 250 kHz.
31	TJTEST	OUT	Device junction temperature information.
32	PGLDO	OUT	LDO regulator Power good output. Open-drain output.
33	FB1	IN/OUT	DC/DC1 Output feedback. Connected to error amplifier that compares the feedback voltage to the internal reference voltage.
34	COMP1	IN/OUT	DC/DC1 Error amplifier output for compensation network connection.
35	PGTHLDO	IN	Power good threshold setting for LDO. Pin floating sets the threshold to 95% of VOUTLDO; shorted to AGND sets the threshold to 85% of VOUTLDO.
36	AGND	GROUND	Device analog ground.
37	WDI	IN	Watchdog input from Microcontroller. Internal Pull Down.
38	FBLDO	IN/OUT	LDO regulator output feedback.
39	VOUTLDO	OUT	LDO regulator output.
40	VINLDO	SUPPLY	LDO regulator power supply.
41	VBAT	SUPPLY	Dedicated high voltage supply for reference blocks.
42	HSD_EN	OUT	Enable signal for external High Side switch (active low). Only active in microcontroller mode, high impedance in normal mode.
43	TESTMODE	IN	TESTMODE pin, reserved use. Connect to ground.
44	WAKEL	IN	Wake-up signal to enable DC/DC1 in OR internally with ENBUCK1 pin (ignored in Normal Mode, active low in Microcontroller Mode).
45	ENLDO	IN	LDO regulator enable (active high).
46	PGDELAYLDO	IN	LDO Power good output delay time adjustable by connecting a capacitor to AGND.
47	SYNCOUT	OUT	External Switching clock output signal.
48	SYNCIN	IN	External clock input connection. Connect an external clock at SYNCIN for frequency synchronization.

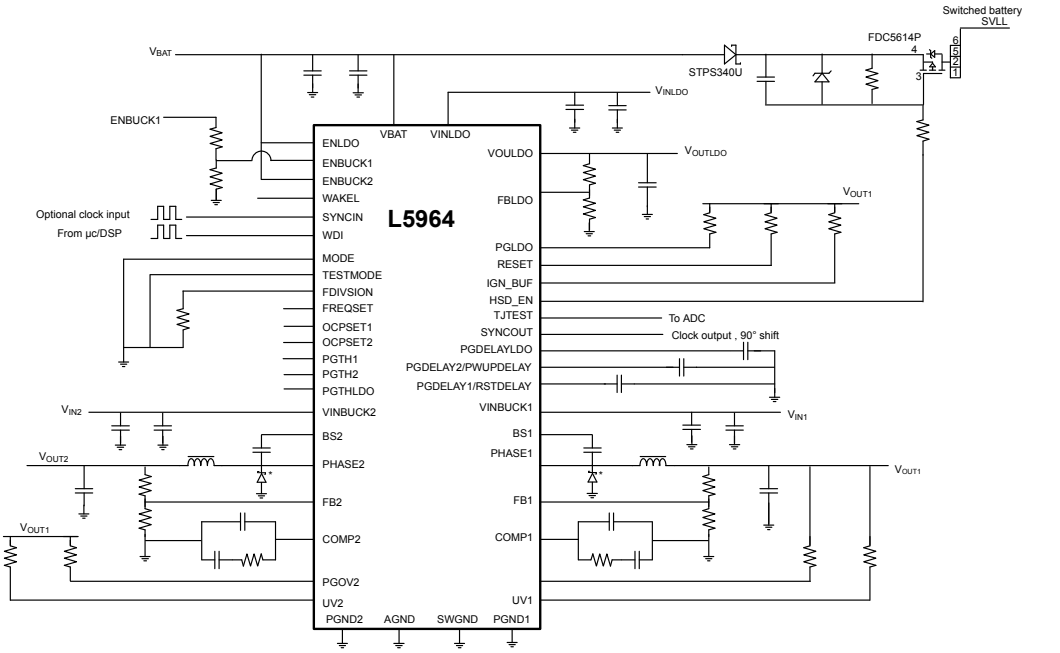
3 Block diagram

Figure 4. **Block diagram**



4 Applications diagram

Figure 5. Application circuit (microcontroller mode)



* a 20 V, with less than 0.5 V forward voltage, and 2 A at room temperature Schottky diode to ground is required as close as possible to the phase pin, to enable > 2 A current capability

GADG2711170847PS

5 Electrical specifications

5.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Pinname / symbol	Parameter	Value	Unit
VBAT, VINBUCK1,2,VINLDO, PHASE1,2	Maximum transient supply voltage	-0.3 to +40	V
ENBUCK2,WAKEL, ENLDO,HSD_EN	Enable pins voltage	-0.3 to +40	V
PGND1/2,AGND, SWGND, TAB	Ground pins voltage	-0.3 to +0.3	V
VOUTLDO,PGLDO, PGOV1,2, UV1,2	LDO regulator output, Power Good signals, under voltage signals	-0.3 to 12	V
BS1,2	Boot-strap capacitor pins	-0.3 to VINBUCK1,2+4.6	V
FB1, FB2, FBLDO, COMP1,2, PGDELAY1,2,PGDELAYLDO	Regulators pins	-0.3 to +4.6	V
ENBUCK1, PGTHLDO, PGTH12, GND12, OCPSET12, FREQSET,SYNCIN, SYNCOUT, FDIVISION, TJTEST, RESET, MODE, WDI, IGN_BUF, TESTMODE	Other I/O pins maximum voltage	-0.3 to +4.6	V
Top	Operating ambient temperature range	-40 to +105	°C
Tstg	Storage temperature range	-55 to +150	°C
Tj	Junction temperature	150	°C

5.2 Operating voltage

Table 4. Operating voltage

Pinname / symbol	Parameter	Value	Unit
VBAT, VINBUCK1,2,, VINLDO, PHASE1,2, VOUTLDO	Operating input voltage	-0.3 to +26	V
ENBUCK2, WAKEL, ENLDO, EN_HSD	Enable pins voltage	-0.3 to +26	V
ENBUCK1	Enable pin voltage	-0.3 to +3.6	V
VOUTLDO,PGLDO,PGOV1,2, UV1,2	LDO regulator output, Power Good signals, under voltage signals	-0.3 to 10	V
BS1,2	Boot-strap capacitor pins	-0.3 to VINBUCK1,2 + 3.6	V
FB1, FB2, FBLDO, COMP1,2, PGDELAY1,2,PGDELAYLDO	Regulators pins	-0.3 to +3.6	V
PGTHLDO, PGTH12, OCPSET12, FREQSET,SYNCIN, SYNCOUT, FDIVISION, TJTEST, RESET, MODE, WDI, IGN_BUF, TESTMODE	Other I/O pins operating voltage	-0.3 to +3.6	V
Top	Operating ambient temperature range	-40 to +105	°C
Tstg	Storage temperature range	-55 to +150	°C
Tj	Junction temperature	150	°C

5.3 Thermal data

Table 5. Thermal data (LQFP64)

Symbol	Parameter	Typ	Max	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-to-case	1.25	1.6	°C/W

Table 6. Thermal data (VQFPN-48)

Symbol	Parameter	Board	Value	Unit
Rthj-a-2s	Thermal resistance junction-to-ambient (Max)	2s	66	°C/W
Rthj-a-2s2p		2s2p	32	°C/W
Rthj-a-2s2pv		2s2p+vias	26	°C/W

5.4 Electrical characteristics

V_{VBAT} = 14.4 V, $V_{INBUCK1/2}$ = 14.4 V, V_{VINLDO} = 14.4 V, T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Battery Supply						
V_{VBAT}	Battery voltage operatingrange	-	3.3	-	26	V
$I_{SHUTDOWN}$	Shutdown mode powersupply current	V_{VBAT} = V_{VINLDO} = $V_{VINBUCK1}$ = $V_{VIBUCKN2}$ = 14.4V V_{ENLDO} = $V_{ENBUCK1}$ = $V_{ENBUCKN2}$ = Low; V_{WAKEUP} = High	-	3	5	µA
$I_{STANDBY\_LDO}$	LDO standby mode powersupply current	V_{VBAT} = V_{VINLDO} = $V_{VINBUCK1}$ = $V_{VIBUCKN2}$ = 14.4 V = V_{ENLDO}, $V_{ENBUCK1}$ = $V_{ENBUCKN2}$ = Low; V_{WAKEUP} = High,No Load	-	35	45	µA
OV_{VBAT}, OV_{VNBUCK}, OV_{VNLDO},	Over voltage lockout threshold	V_{VBAT} Rising	30	32	34	V
		V_{VBAT} Falling	28	30	32	V
UV_{VBAT}	Under voltage lockout threshold	V_{VBAT} Rising	2.8	3	3.2	V
		V_{VBAT} Falling	2.7	2.9	3.1	V
Buck converters Enable						
Normal mode						
$V_{EN1/2}$	ENBUCK1/2 threshold, oscillator, BUCK On	$V_{ENBUCK1/2}$ Rising	1.5	1.7	1.9	V
		$V_{ENBUCK1/2}$ Falling	1	1.3	1.6	V
$I_{EN1/2\_LEAKAGE}$	ENBUCK1/2 leakage current	$V_{ENBUCK1}$ = 3.3 V, $V_{ENBUCK2}$ = 14 V	-	1	2	µA
Microcontroller mode						
E_{n_Tmin}	Highl evel duration of ENBUCK1 enable	-	20	70	150	µs
I_{EN1}	ENBUCK1 leakage current	-	-	3.5	5	µA
WAKEL						
V_{WAKEL}	WAKEL Threshold, BUCK1 On	WAKEL Falling	0.8	1	1.3	V
		WAKEL Rising	1.5	1.8	2.1	V
I_{WAKEL}	WAKEL Leakage Current	WAKEL = 0 V	-	1.5	3	µA
Buck converter						
$V_{VIN1/2}$ $OVV_{IN1/2}$	Operating range	-	3.3	-	26	V
$HYS_{OVVinbuck}$	Hysteresis	-	-	0.4	-	V
$UV_{Vinbuck}$	Under voltage lockout threshold	$V_{VINBUCK1/2}$ Rising @ Vout = 1.2 V	2.7	3.0	3.3	V
		$V_{VINBUCK1/2}$ Falling @ Vout = 1.2 V	2.6	2.9	3.2	V
$V_{FB1/2\_VFB1/2}$	Feedback voltage	-	880	900	920	mV
ΔV_{LOADR}	Load regulation	Load = 0.3 A to 1.5 A	-	0.1	-	mV
$\Delta V_{LINER\_VFB1/2}$	Line regulation	$V_{VIN1/2}$ = 3.3 V to 26 V	-	0.1	-	mV
$\Delta V_{FB1/2}$/ $V_{FB1/2}$	$V_{FB1/2}$ undershoot	Load = 0.5 A ↔ 1.5 A, Δt = 10 µs		±5		%
		$V_{VIN1/2}$ = 8 V ↔ 18 V, Δt = 1 ms		±5		%
Ron_{HS}	High side switch on resistance	QFN package	-	75	90	mΩ
		LQFP package	-	90	110	
Ron_{LS}	Low side switch on resistance	QFN package	-	60	80	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Ron_{LS}	Low side switch on resistance	LQFP package	-	70	90	mΩ
$\Delta V_{FBSWx}/\Delta t$	FB pin Slope at Turn- on	Soft start time related	-	1	2	V/ms
Error amplifier						
g_m (1)	Error Amplifier Transconductance		-	1	-	mS
Oscillator						
f_{OSC}	Free-run switching frequency	FREQSET pin floating	2	2.2	2.4	MHz
		FREQSET pin connected to AGND	0.24	0.27	0.3	MHz
Peak current limit						
I_{PEAK_LIMIT}	Switch peak current limit	OCPSET1/2Floating (2)	3.7	4.5	-	A
		OCPSET1/2Connected to Ground (3)	1.7	2	-	A
Power Good and Power Good Delay for BUCK1/2						
$TH_{PG1/2}$	PGOV1/2 Threshold as FB Voltage Percentage	PGTH1/2 pin connected to AGND	80	85	92	%
		PGTH1/2 pin Floating	90	95	99.5	%
$V_{PG1/2L}$	PGOV1/2 Voltage Low	$I_{PGOV1/2}$ = 500 µA	-	0.1	0.2	V
$I_{PG1/2LEAKAGE}$	PGOV1/2 Leakage Current	$V_{PGOV1/2}$ = 5 V	-	-	1	µA
$t_{PG1/2}$	Delay for reporting a fault	C = 0 pF on PGDELAY 1,2 pin	-	1	-	µs
I_{PG_CHARGE}	PGDELAY1/2 Charging current		7	10	13	µA
$V_{THPGDLY1/2}$	PGDELAY1/2 Threshold		1.5	1.9	2.5	V
$t_{PG1/2}$	Power Good Delay Time	C = 100 pF on PGDELAY1,2 pin $t_{PG1/2} = C * V_{THPGDLY1/2} / I_{PG\_CHARGE}$	10	20	25	µs
OVand UV for BUCK1/2 output voltage						
$TH_{OV1/2}$	OV Threshold as Percentage of FB1/2 Voltage	PGTH1/2 connect to ground	105	110	115	%
		PGTH1/2 Floating	115	120	125	%
$HYS_{OV1/2}$	Hysteresis on OV1/2	PGTH1/2 pin floating/connected to AGND	4	6.5	8	%
$t_{OV1/2\_GLITCH}$	Glitch filter time for OV1/2	-	-	5	-	µs
$TH_{UV1/2}$	UV Threshold as Percentage of FB1/2 Voltage	PGTH1/2 Connect to Ground	72	80	84	%
		PGTH1/2 Floating	82	90	94	%
$HYS_{UV1/2}$	Hysteresis on UV1/2	PGTH1/2 pin floating/connected to AGND	-	2	4	%
$V_{UV1/2L}$	UV1/2 Voltage Low	IUV1/2 = 500 µA	-	0.1	0.2	V
$I_{UV\_LEAKAGE}$	UV1/2 Leakage Current	VUV1/2 = 5 V	-	-	1	µA
$t_{UV1/2\_GLITCH}$	Glitch Filter Time for UV1/2	-	5	6.5	10	µs
Synchronization						
f_{SYNC}	Frequency Range	50% Duty-cycle Wave on SYNCIN Pin	125	-	2300	kHz
-	SYNCIN Low Threshold	-	-	-	0.8	V
-	SYNCIN High Threshold	-	2	-	-	V
FDIVISION Pin						
R_{FDI}	Resistors connected to FDIVISON pin to set switching frequency of DC/DC2	60 kΩ <RFDI<80 kΩ	$f_{SWBUCK2}=1*f_{SWBUCK1}$			
		115 kΩ < RFDI<130 kΩ	$f_{SWBUCK2}=1/2*f_{SWBUCK1}$			

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{FDI}	Resistors connected to FDIVISON pin to set switching frequency of DC/DC2	170 kΩ < RFDI<178 kΩ	$f_{SWBUCK2}=1/4*f_{SWBUCK1}$			
		RFDI> 250 kΩ	$f_{SWBUCK2}=1/8*f_{SWBUCK1}$			
Thermal Shutdown for BUCK1/2						
TSD_{SWx}	Thermal shut-down temperature	Temperature Rising	155	165	175	°C
Hys_{TSDSWx}	Hysteresis on thermal shutdown temperature	-	-	8	-	°C
Linear regulator (LDO) enable						
V_{ENLDO}	ENLDO threshold, linear regulator on	V_{ENLDO} Rising	2.1	2.35	2.6	V
		V_{ENLDO} Falling	0.8	1	1.2	V
V_{ENLDO}	ENLDO threshold in standby mode	V_{ENLDO} Rising	5.0	5.5	6.0	V
I_{ENLDO}	ENLDO leakage current	V_{ENLDO} = 14 V 4 MOhm internal pull down	2	4	6	µA
Linear regulator (LDO)						
V_{VINLDO}	Input voltage range	-	3.3	-	26	V
UV_{VINLDO}	Over voltage lockout thresholdon VINLDO	V_{VINLDO} Falling	2.7	2.9	3.1	V
V_{FBLDO}	Feedback Voltage	Load Current = 250 mA (normal mode)	980	1000	1020	mV
		Load Current = 50 mA (st-by mode)	960	990	1020	mV
ΔV_{LOADR_FBLDO}	Load Regulation	ΔV_{FBLDO}, Load Current = 0 mA to 50 mA, $V_{VOUTLDO}$ = 1.5 V, Standby Mode	-2.5	-1	0	mV
		Load Current = 0 mA to 250 mA $V_{VOUTLDO}$ = 1.5 V, Normal Mode	-2	-0.8	0	mV
ΔV_{LINER_FBLDO}	Line regulation	ΔV_{FBLDO}, V_{VINLDO} = 3.5 V to 18 V, Load current = 50 mA	-	1	-	mV
ΔV_{FBLDO} / V_{FBLDO}	Undershoot/Overshoot	5 mA ↔ 250 mA Load Transition in Δt = TBD	-5	-	5	%
		8↔ 18 V V_{VINLDO} Transition in Δt = TBD	-5	-	5	%
Co	Output capacitance	-	3	-	-	µF
ESR	Output Capacitor ESR	-	-	-	0.2	Ω
$V_{DROPOUT\_LDO}$	Drop-out Voltage	$V_{VOUTLDO}$ = 3.3 V, Load current = 50 mA $V_{VOUTLDO}$ decreasing of 100 mV, Standby Mode	-	0.25	0.3	V
		$V_{VOUTLDO}$ = 3.3 V, Load current = 250 mA $V_{VOUTLDO}$ decreasing of 100 mV, Normal Mode	-	0.35	0.45	V
I_{LIMIT_DO}	Short circuit current limit	V_{OUTLDO} Shorted to Ground, Standby Mode	-	70	-	mA
		V_{OUTLDO} Shorted to Ground, Normal Mode	-	380	-	mA
$PSRR_{LDO}$	Power supply rejection ratio	Load Current = 50 mA, 10 Hz < f < 10 kHz 1Vac_{pp} on V_{INLDO}	50	-	-	dB
t_{SOFT_START}	Soft-start Period	-	150	250	350	µs
Thermal shutdown for linear regulator						

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TSD_{LDO}	Thermal Shut-down Temperature	Temperature rising	155	165	175	°C
HYS_{TSDLDO}	Hysteresis on Thermal Shutdown Temperature	-	-	8	-	°C
Power Good and Power Good Delay for linear regulator						
TH_{PGLDO}	PGLDO threshold as percentage of FBLDO voltage	PGTHLDO pin connected to AGND	83	87	91	%
		PGTHLDO pin floating	94	97	99.5	%
V_{PGLDOL}	PGLDO voltage low	I_{PGLDO} = 500 µA	-	0.1	0.2	V
$I_{LEAKAGE\_PGLDO}$	PGLDO leakage current	V_{PGLDO} = 5 V	-	-	1	µA
T_{PGLDO}	Delay for reporting a fault	C = 0 pF on PGLDO DELAY Pin	-	1	2	µs
T_{GLITCH_PGLDO}	Glitch Filter Time for PGLDO	-	10	14	17	µs
I_{PG_CHARGE}	PGDELAYLDO Charging Current	-	7	10	13	µA
$VTH_{PGLDODLY}$	PGDELAYLDO threshold	-	1.5	2	2.5	V
$t_{DLYPGLDO}$	PowerGood Delay Time	C = 100 pF on PGLDO DELAY Pin $t_{DLYPGLDO} = C * V_{THPGLDODLY}/I_{PG\_CHARGE}$	15	20	25	µs
High side driver enable						
V_{hsd_en}	Output voltage low	Load = 2 mA	-	0.1	0.2	V
Window watchdog						
V_{WDI}	Input high voltage	-	2	-	-	V
	Inputl ow voltage	-	-	-	0.8	V
T_{WD}	WDI minimum period	-	-	5	-	ms
	WDI maximum period	-	35	45	55	ms
	WDI Glitch immunity (1)	-	-	100	150	ns
RESET function						
V_{RESET}	Reset voltage	I_{RESET} = 500 µA	-	0.1	0.2	V
$T_{internal\_reset}$	Fixed internal reset time (4)	-	0.8	1	1.2	ms
$T_{DLYRESET}$	Delay time	C = 100 pF on RESET Pin	15	20	25	µs
$I_{LEAKAGE\_RESET}$	RESET leakage current	V_{RESET} = 3.3 V	-	-	1	µA
IGNITION BUFFER (IGN_BUF PIN)						
IGNBUF Output leakage		BUCK1 on, microcontroller mode	-	0	1	µA
IGNBUF Output Voltage Low		BUCK1 off, microcontroller mode I_{IGN_BUF} = 500 µA	-	0.1	0.25	V

1. *Guaranteed by design.*
2. *A 20 V, with less than 0.5 V forward voltage, and 2 A at room temperature Schottky diode to ground is required as close to the phase pin as possible, to enable > 2 A current capability*
3. *Guaranteed by bench validation.*
4. *RESET time is the sum of $T_{internal\_reset}$ and T_{delay} . $T_{reset} = T_{internal\_reset} + T_{delay}$*

6 Functional description

6.1 Block description

6.2 Switching regulators

The two switching step-down converters have their own enable. The output voltage of the converters can be set by an external resistor divider, at the feedback pin.

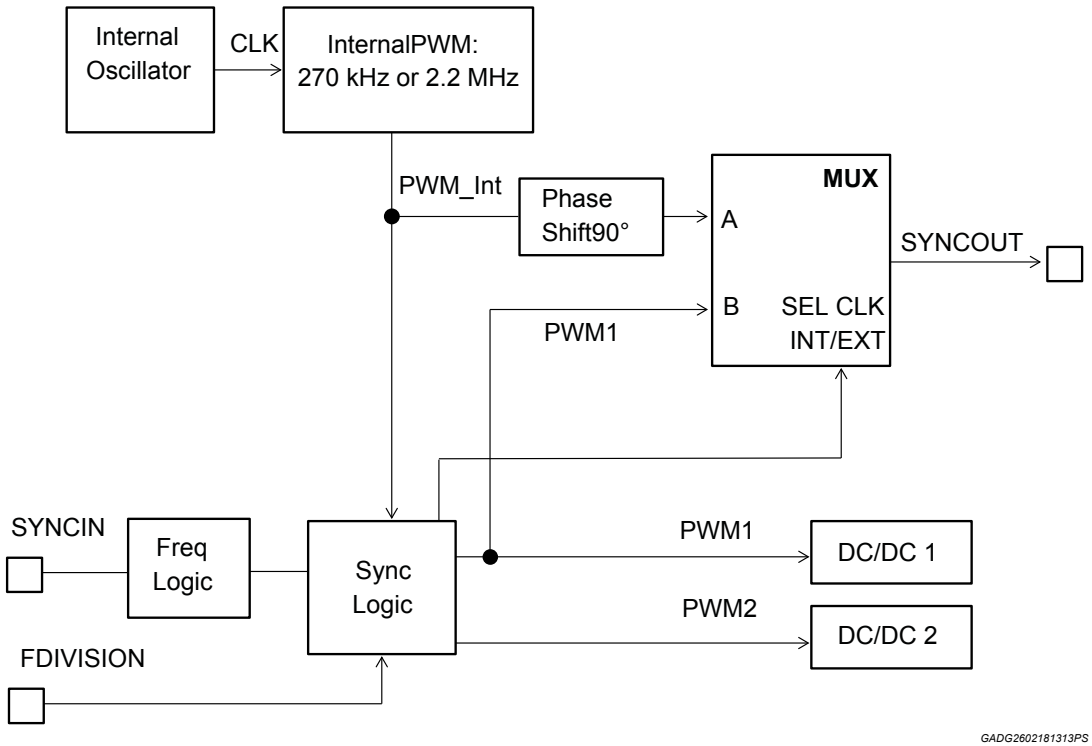
To reduce the inrush current during startup, an internal soft start is implemented. The total soft start time is about 900 µs and doesn't change with operating frequency.

Two free running frequencies can be selected by connecting FREQSET pin to ground (270 kHz) or leaving it floating (2.2 MHz). In order to consider EMC performance or synchronization needs at system level, the two DC/DCs can work with an external clock at the SYNCIN pin: the applied frequency is automatically adopted.

If two or more L5964 are used together, they can work in Master-Slave configuration: the function is implemented by a dedicated pin, SYNCOUT, which gives out the operating frequency of DC/DC1 phase shifted of 90° if two DC/DCs are working with internal free running frequency, otherwise SYNCOUT will follow SYNCIN pin (no phase shift). DC/DC1 and DC/DC2 always have 180° phase difference. DC/DC2 switching frequency can be the same or respectively 1/2, 1/4, 1/8 of DC/DC1 one: division factor is programmed by FDIVISION pin by connecting an external resistor to AGND.

The frequency divider is active only when the FREQSET pin is floating. In free run mode this happens when the switching frequency is set to 2 MHz. When the device is synchronized to an external clock, if the FREQSET pin is shorted to ground, the FDIVISION pin is inhibited.

Figure 6. PWM frequency management



6.3 Low drop out (LDO) linear regulator

Linear regulator normal mode

If ENLDO voltage is lower than 5 V the LDO works in Normal Mode, with output current capability up to 250 mA (see Figure 8 for reference).

The linear regulator shows quite low drop-out voltage, hence it can work with very low operating supply. Its output voltage VOUTLDO can be set by an external resistor divider connected to the feedback pin FBLDO. A dedicated power-good signal is available with 2 different selectable thresholds, which can be chosen acting on PGTHLO pin. If this pin is left floating, the threshold is set to 95% of the output voltage. If the pin is connected to AGND, the threshold is set to 85% of the regulated voltage. The delay of this signal can be adjusted by connecting a capacitor on PGDELAYLDO pin.

Figure 7. LDO diagram

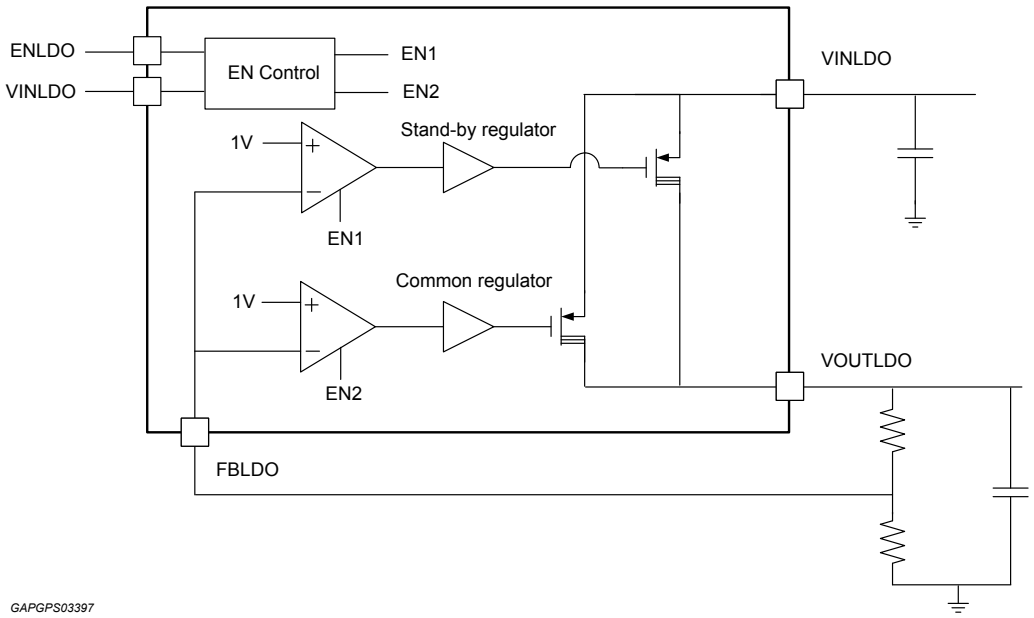
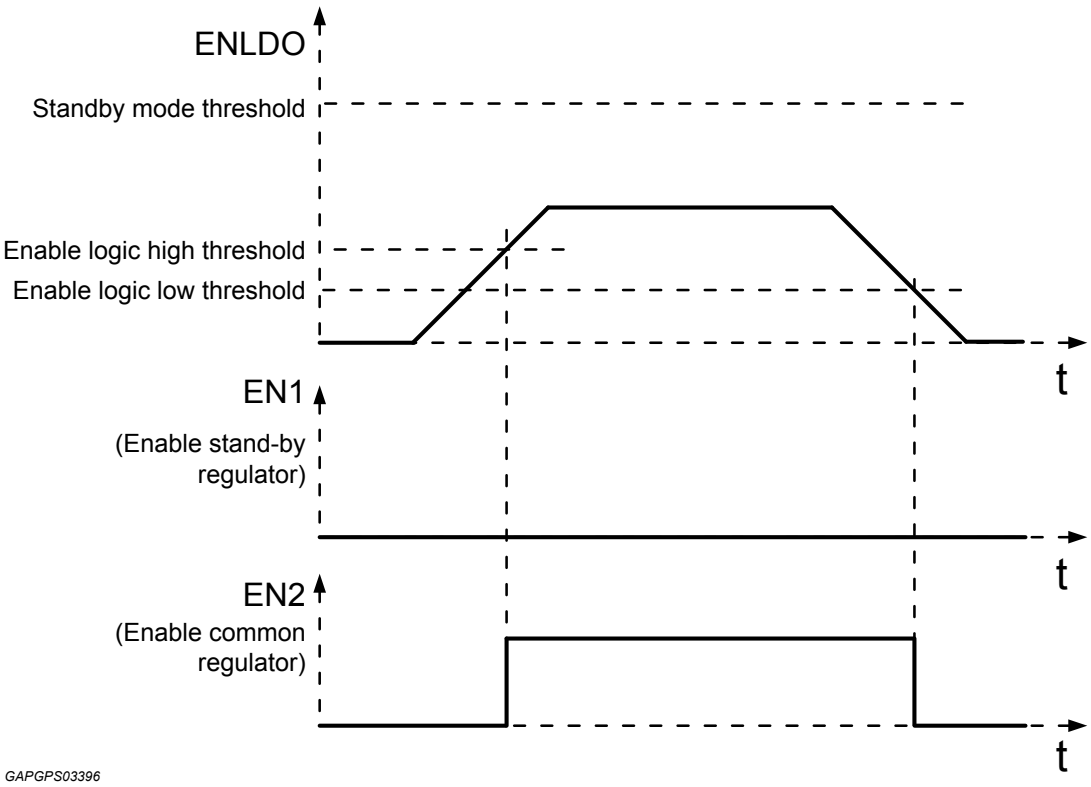


Figure 8. **Enable timing for LDO regulator in Normal Mode (ENLDO < 5 V)**



Linear regulator standby mode

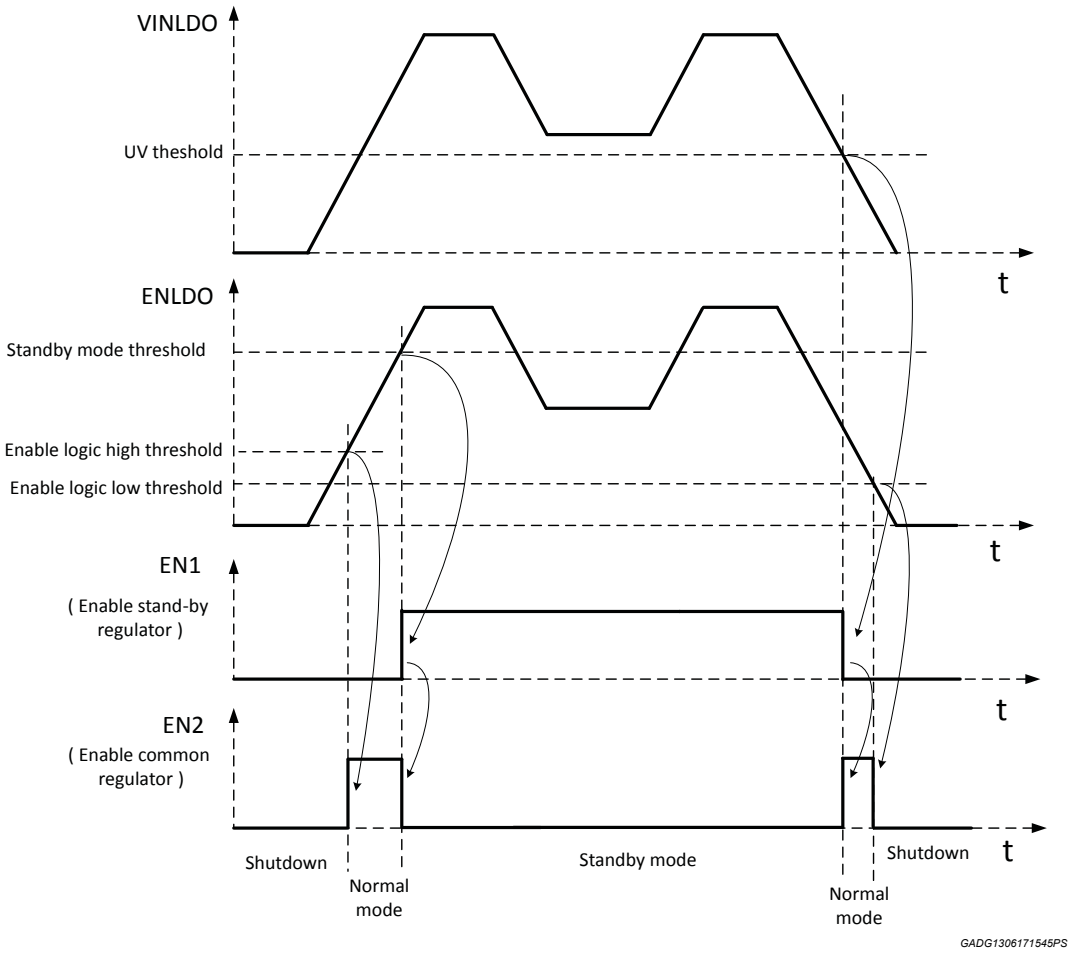
The linear regulator works as Standby Regulator when ENLDO is brought to a voltage higher than 5.5 V typ. Usually, in this working mode, VBAT, VINLDO and ENLDO are connected together, in order to switch on the standby regulator as soon as the battery voltage is present.

Standby Mode is latched with the rising edge of ENLDO until the under-voltage threshold of VINLDO is crossed, resetting the latch. An under-voltage of VBAT switches off the LDO.

In standby working condition the current capability is limited to 50 mA and current consumption from VINLDO is minimized. In Standby mode an external divider with resistors in the order of Mega Ohm is suggested, to further reduce supply current consumption.

If the power good, PGLDO, is used, it is recommended to connect it to VOUTLDO through a pull-up, in order to get a clean signal.

Figure 9. **Enable timing for standby regulator**

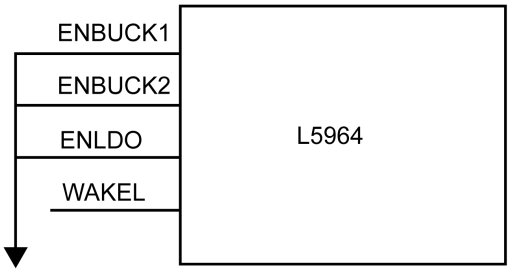


7 Working modes

7.1 Shutdown mode

If all the enable and wake up signals are not active, the device is in shutdown mode: all circuits are in off condition and current consumption from supply line is very low (10 µA).

Figure 10. Shutdown Mode configuration



7.2 Normal mode

Device working mode can be settled by shorting the MODE pin to AGND (Microcontroller Mode) or leaving it open (Normal Mode).

Normal mode working condition allows each regulator to be turned ON/OFF by its enable pin: Power Up sequence can be managed according to each regulator power-good signal with programmable delay (PGDELAY1,2 and PGDELAYLDO) through an external capacitor (Cext) connected to the pin as shown in the below figure.

In this configuration, ENBUCK2 pin can have a direct connection to the battery. WAKEL pin is ignored, since internally floating (see Figure 11).

Figure 11. ENBUCK2 internal block diagram

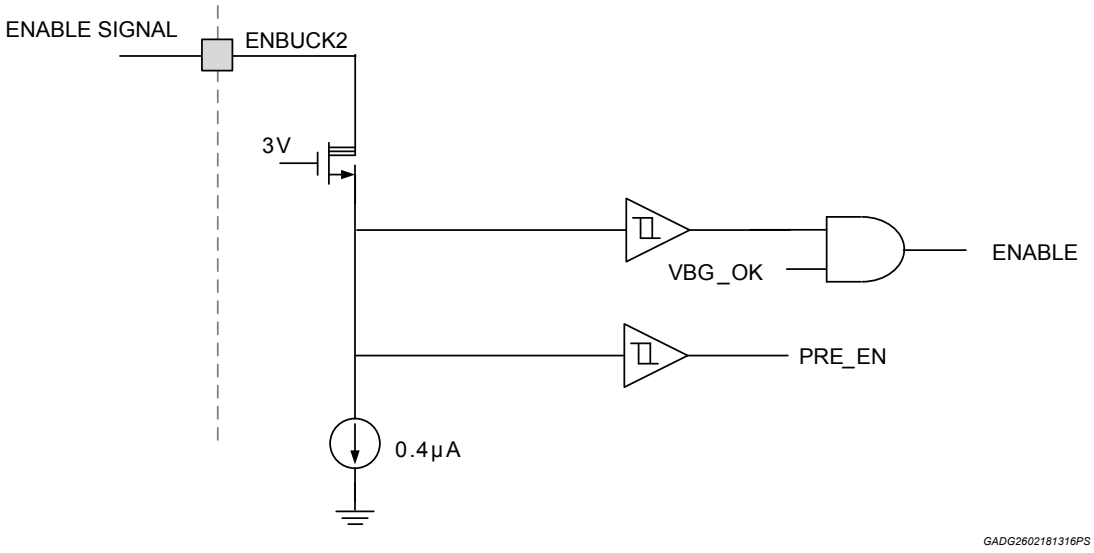
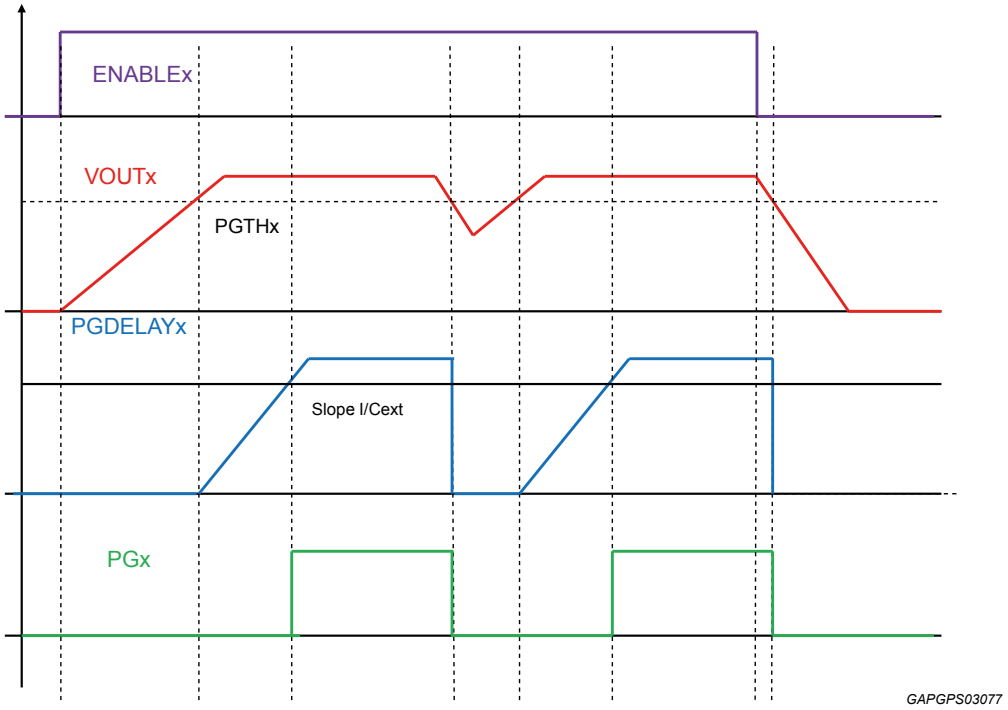


Figure 12. **Output signals behavior in normal mode**



In the table below relationship between capacitor value at PGDELAY pin and delay duration is shown:

Table 7. **Relationship between capacitor value at PGDELAY pin and delay duration**

C(PGDELAY1,2)	1 nF	10 nF	100 nF	470 nF	1 µF	10 µF
Power Good Delay Time 1/2	0.21ms	2.1ms	21ms	98.7ms	210ms	2.100s

Fault management

In case of under or over voltage detected at VINBUCK pin the correspondent DC/DC high side is switched off and turned on automatically at next PWM if the voltage is back to normal value. In case of under/over voltage at VBAT pin, both side switches are turned off and turned on automatically at next PWM when VBAT recovers to normal operating value.

To monitor DC/DC outputs, dedicated voltage detectors are integrated in L5964. There are 2 presets, which can be selected through PGTH12 pin, to decide detection voltage as output percentage. Each DC/DC has its own preset (PGTH1 and PGTH2).

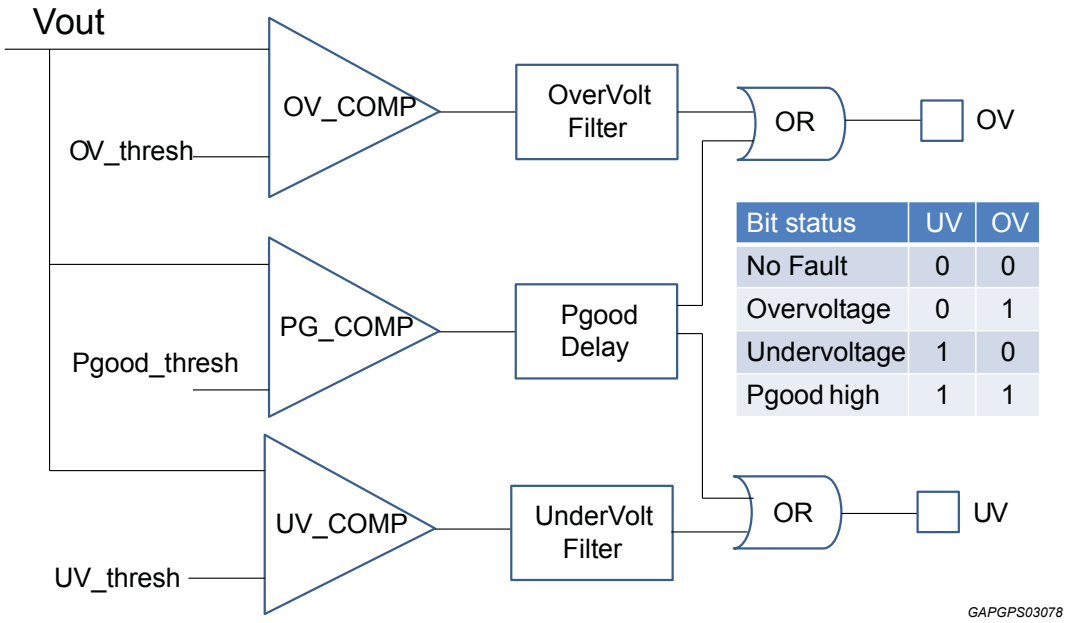
Table 8. **2 presets which can be selected through PGTH12 pin**

PGTHpin status	Prog/Threshold	UV	OV	Pgood
Floating	Prog1	90%	120%	95%
Shorted to AGND	Prog2	80%	110%	85%

UV1/2 and OV1/2 outputs are available: power-good1/2 status can be derived consequently (see Figure 13). Each power-good signal can be delayed by connecting a capacitor on PGDELAY1/2 pin. The LDO regulator has its own power-good signal PGLDO and PGDELAYLDO, but it has no UV/OV detection.

In case of output under voltage the fault is only detected and the device doesn't take any action. In case of output over voltage the High Side Power is switched off; when output decreases under the over voltage threshold, High Side is turned on automatically at next PWM. Under/over voltage information is available after filtering time at UV/OV pin; the fault is not latched.

Figure 13. **OV,UV functions**



Bit status	UV	OV
No Fault	0	0
Overvoltage	0	1
Undervoltage	1	0
Pgood high	1	1

Each DC/DC normally senses the output current and turn off the power stage when the peak is equal to the reference (current control mode). In case of over current in the inductor it is internally limited by control loop.

The over temperature (OT) protection works in the same way in both working modes: when OT is detected Power stage is switched off. It is turned on automatically when temperature decreases under low shutdown threshold. Each regulator has its own thermal sense and it is independently switched off.

7.3 Microcontroller mode

Microcontroller Mode (MODE pin connected to AGND) has been thought for L5964 to properly supply a Microcontroller; a dedicated power up phase is issued and main MCU signals like Reset and Watchdog are managed. In this mode the power-good delays are used differently respect to normal mode: PGDELAY1 is used to generate Reset duration, PGDELAY2 to generate the Power Up delay (TPU, from Reset rising edge to Watchdog input WDI sensitivity). Only LDO power-good signal will be delayed according to PGDELAYLDO, while power-good 1/2 signals (at PGOV1/2 pins) will show no delay.

Enable thresholds, V_H and V_L, can be chosen by the user in order to be compatible with different customer's requests.

R1 should be selected in order to satisfy the following equation (ENBUCK1 has an internal clamp to 5 V):

R1 > (V(ENABLE_SIGNAL)_MAX - 5 V) / ILIM

Where Ilim is the maximum current permissible in ENBUCK1 pin, 1 mA.

R2 is calculated from VH, VL and R1 in this way:

$$V_H = \frac{0.99\ V \cdot (R_2//(29.13k \cdot 0.8) + R_1)}{(R_2//(29.13k \cdot 0.8)) \cdot 0.6}$$

$$V_L = \frac{0.91\ V \cdot (R_2//1\ M + R_1)}{(R_2//1\ M) \cdot 0.6}$$

GADG2905171620PS

WAKEL pin is active and, like ENBUCK1, can enable DC-DC1 with the opposite logic (active low, in OR with ENBUCK1).

Watchdog input (WDI) is digitally checked by an internal counter. The device verifies the correct WDI frequency range (between 20 Hz and 200 Hz): it means that WDI pulse has to last at minimum 5 ms and maximum 50 ms (TWD), otherwise a watchdog fail is detected and a Reset will be issued (see Figure 14).

Figure 15 shows an example of Power Up phase: watchdog counter starts after the established power up delay is expired (normally starts at each WDI falling edge) and is reset at each WDI falling edge. If TWD is exceeded, then a WDI fail is detected.

Figure 14. ENBUCK1 internal block diagram in microcontroller mode

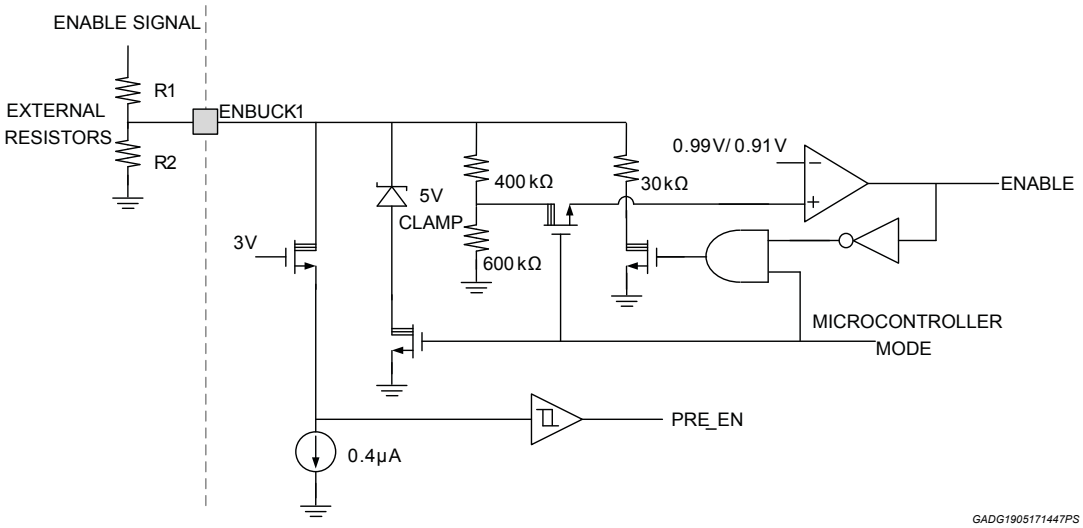
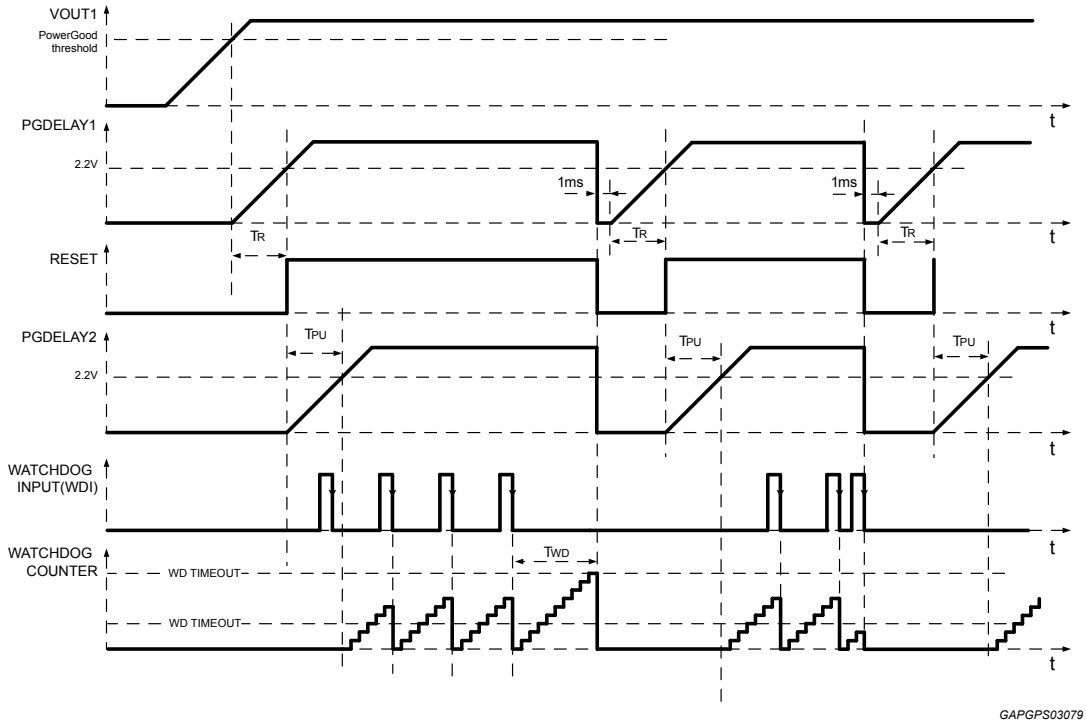


Figure 15. **Microcontroller mode power up phase**



In Microcontroller Mode, RESET and HSD_EN pins are active (in Normal mode they are in highimpedance state); HSD_EN pin is used to control an external PMOS High Side switch and will follow Reset behavior: if reset is asserted the external PMOS is turned OFF.

In the below table relationship between capacitor value at PGDELAY pin and Reset/Power Up duration is shown:

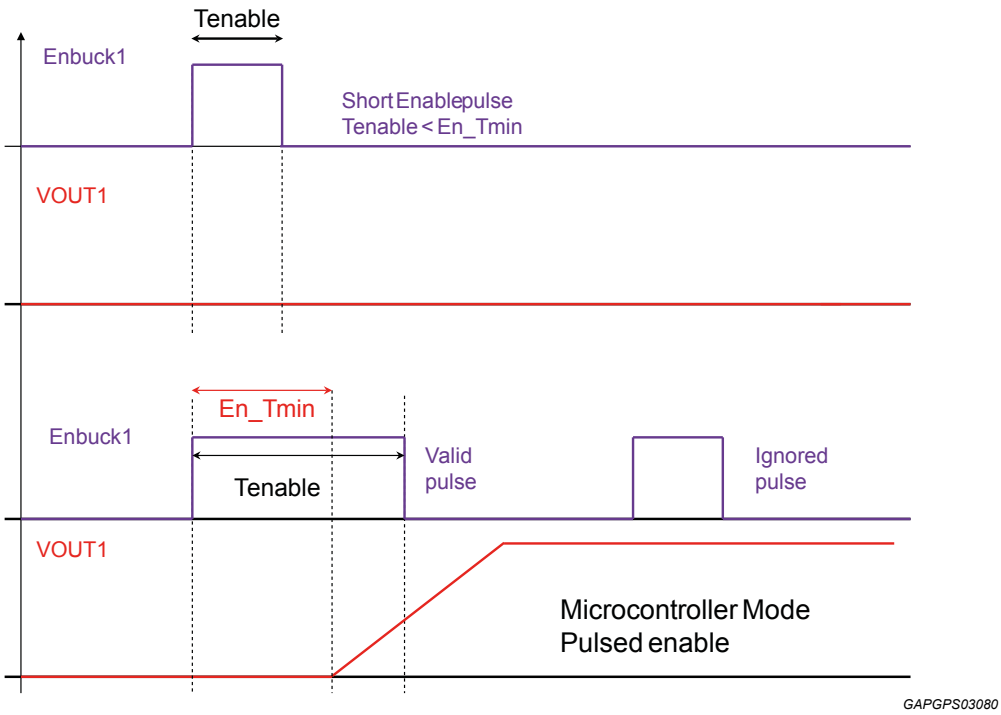
Table 9. **Relationship between capacitor value at PGDELAY pin and Reset/Power Up duration:**

C(PGDELAY1,2)	1 nF	10 nF	100 nF	470 nF	1µF	10 µF
Reset Time	1.21ms	3.1ms	22ms	99.7 ms	211 ms	2.101s
Power Up Delay, T_{PU}	0.21ms	2.1ms	21ms	98.7 ms	210ms	2.100s

Pulsed Enable function

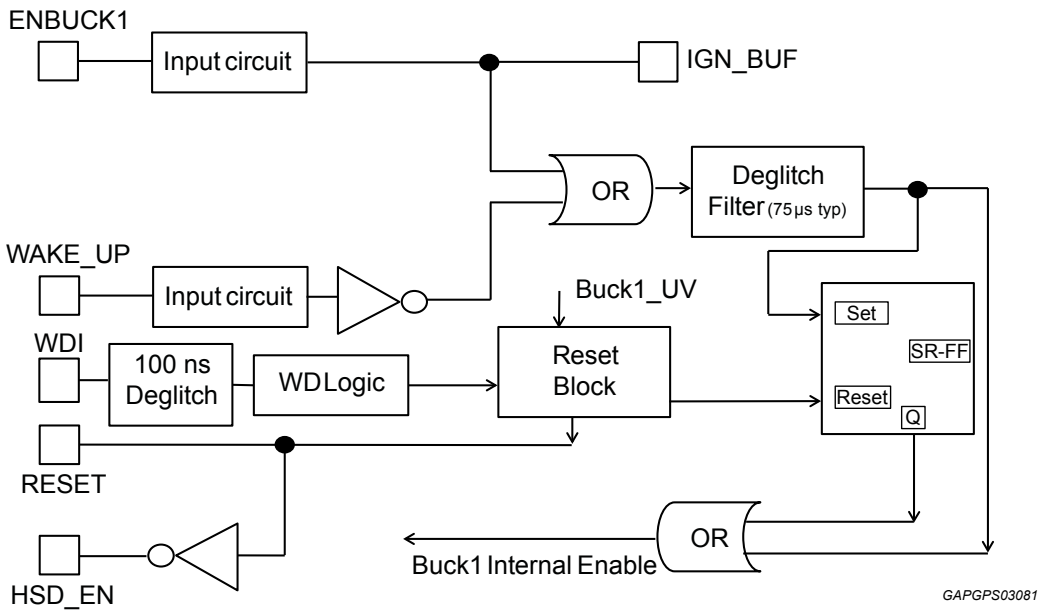
DC/DC1 enable pin (ENBUCK1) is considered valid even if it goes low after a certain time (pulsed enable). The following figure explains how the detection works: if the ENBUCK1 lasts for a time greater than En_Tmin (25 µs min - 125 µs max), then it is internally latched and used to start DC/DC1; then the regulator is kept in on condition, regardless of the ENBUCK1 status. If the regulator is ON and there are additional pulses on ENBUCK1 they will be ignored. A Reset event can reset the internal Enable latch (Watchdog fail or under voltage on DC/DC1 output).

Figure 16. **Pulsed enable function**



WAKEL pin behavior is expected to be the same (but active low) and is managed in the same way as ENBUCK1 pin to turn on DC/DC1. IGN_BUF is the level shifted non-inverted version of ENBUCK1 pin. It is an open-collector output.

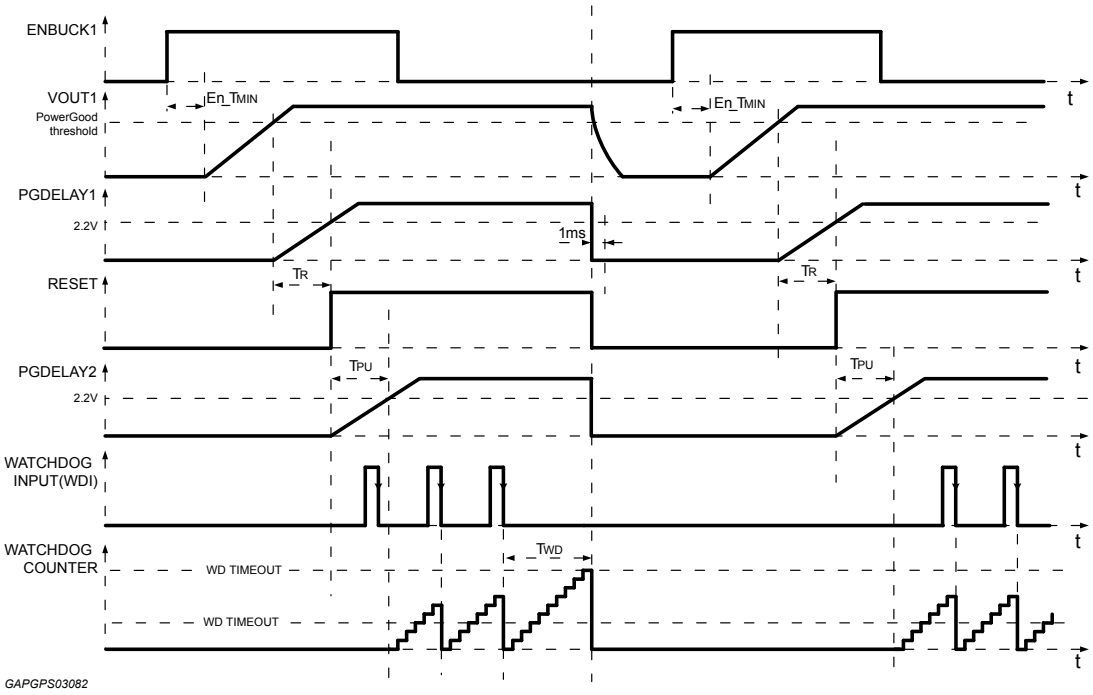
Figure 17. **Enable pin management**



Fault management

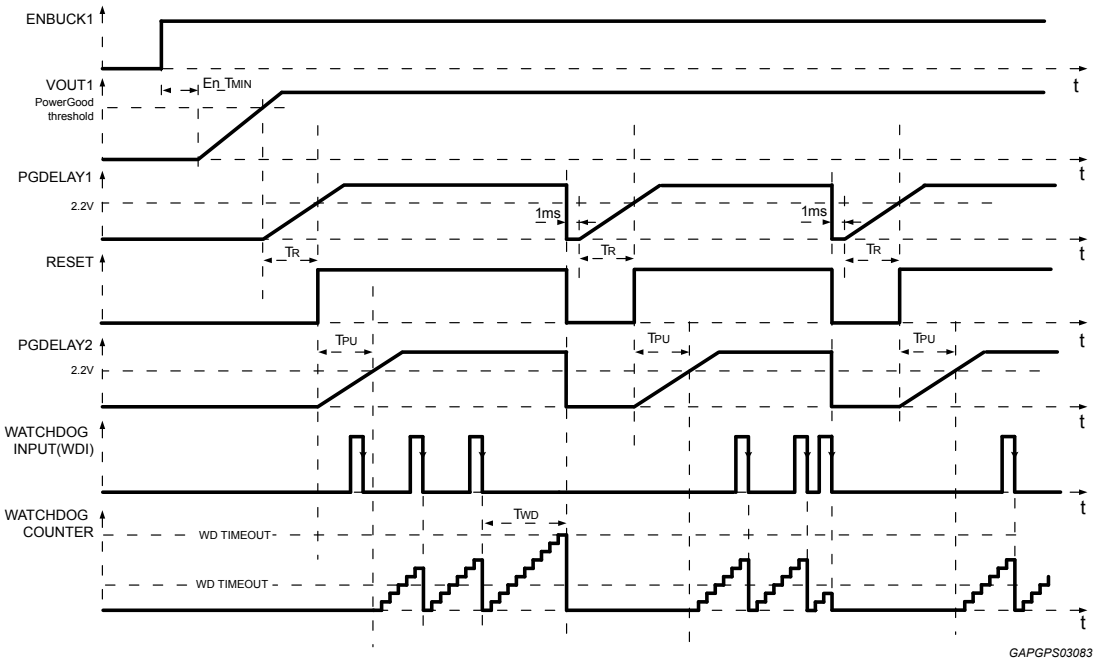
In Microcontroller Mode, after power up phase, WDI is continuously monitored: if a WDI fail occurs, the device reacts in the following way: a Reset is issued and, if ENBUCK1 is low and WAKEL is high, DC/DC1 is turned off and restarted at the next enable rising edge. A new power up phase is issued. Same behavior is expected in case of under voltage detected at DC/DC1 output.

Figure 18. WD fail management in microcontroller mode (1)



If ENBUCK1 is high or WAKEL is low and a WDI fault or under voltage fault occurs, L5964 generates a Reset (whose duration is TR) and the DC/DC1 remains on (see Figure 19).

Figure 19. WD fail management in microcontroller mode (2)



In Microcontroller Mode, if an Overtemperature occurs on DC/DC1 and the output decreases under UV threshold, a Reset is asserted. Fault is managed as described in Figure 18 and Figure 19.

The table below resumes Fault Management for all regulators in all working modes.

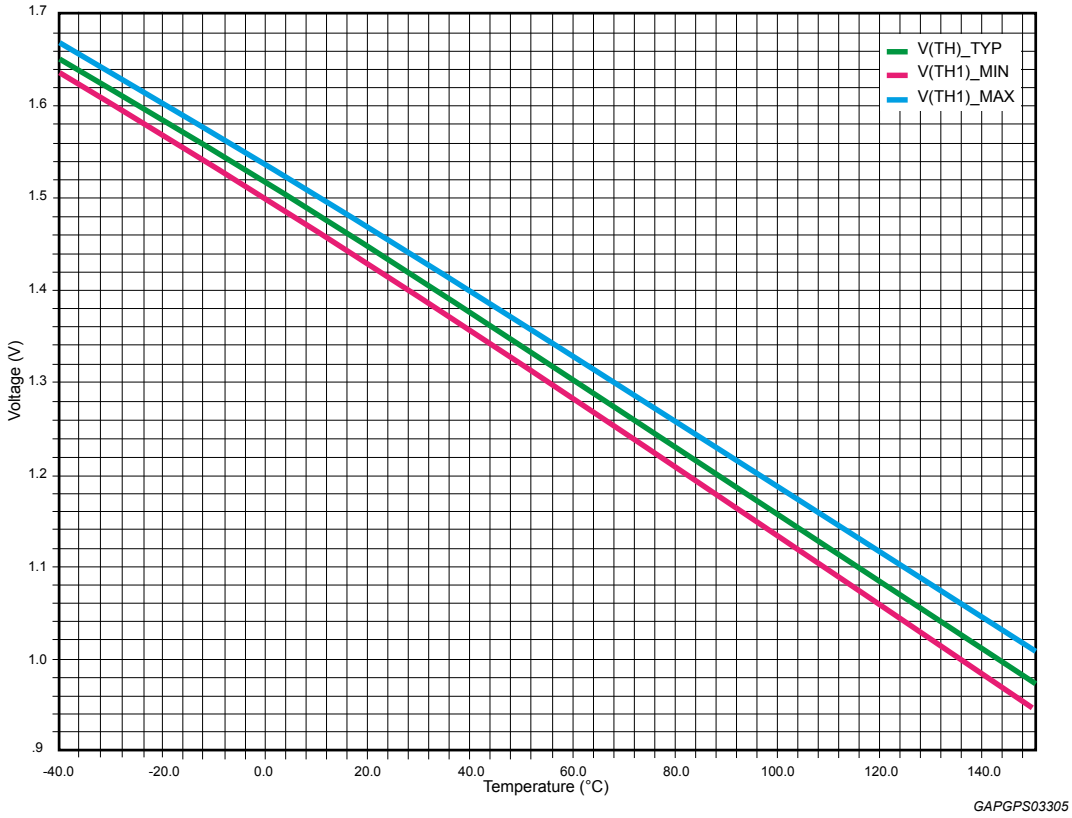
Table 10. Fault Management for all regulators in all working modes

WorkingMode	Fault	L5964B action
DC/DC: Normal	Vout OV	DC/DC high side is switched OFF after 10 µs (typ) of filtering time. High Side turned on again when output voltage returns to normal value (considering comparator hysteresis).
	Vout UV	No action (only detection after 10 µs (typ) of filtering time).
	Over temp	DC/DC high side is switched off and turned on again when temp becomes lower than shutdown threshold (considering hysteresis).
	Output short	Pulse by pulse current sensing and limiting (HS and LS)
	VBAT/VINBUCK OV	DC/DC high side is switched OFF after 5 µs (typ) of filtering time. High Side turned on again when input voltage returns to normal value (considering comparator hysteresis).
	VBAT/VINBUCK UV	DC/DC high side is switched OFF after 5 µs (typ) of filtering time. High Side turned on again when input voltage returns to normal value (considering comparator hysteresis).
LDO: Normal Standby mode	Over temp	LDO is switched off and turned on again when temp becomes lower than shutdown threshold (considering hysteresis).
	Output short	Current limit to 250 mA (normal mode). Current limit to 50 mA (Standby mode).
	VINLDO OV	It is only active in LDO Normal Mode. LDO switched off and switched on again when VINLDO returns to normal value.
	VBAT OV	It is only active in LDO Normal Mode. LDO switched off and switched on again when VBAT returns to normal value.
	VINLDO UV	LDO switched off and switched on again when VINLDO returns to normal value.
	VBAT UV	LDO switched off and switched on again when VBAT returns to normal value.
MCU mode DC/DC - LDO		RESET is asserted in case of DC/DC1 UV/OV. For all the other faults the action is the same as above.

Junction temperature information

L5964 provides at TJTEST pin a voltage directly proportional to the internal junction temperature. The relationship is reported below.

Figure 20. **TJTEST voltage vs junction temperature**



In the table below detailed values are provided:

Note: Values coming from corners simulation at Ibias = 10 µA.

Table 11. **TJTEST voltage vs junction temperature**

	Tj= -40°C	Tj= 0°C	Tj= 27°C	Tj= 100°C	Tj= 110°C	Tj= 120°C	Tj= 130°C	Tj= 140°C	Tj= 150°C	Tj= 160°C	Tj= 170°C	Tj= 180°C	Unit
Min	1.637	1.498	1.402	1.135	1.097	1.06	1.022	0.984	0.946	0.908	0.87	0.832	V
Typ	1.651	1.515	1.421	1.159	1.122	1.085	1.048	1.011	0.974	0.936	0.898	0.861	
Max	1.667	1.535	1.443	1.188	1.152	1.116	1.079	1.043	1.006	0.969	0.932	0.895	

8 Application information

8.1 Output inductor (L)

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of the maximum load current. For example, if a $\Delta I_L = I_{RIPPLE} = 0.3 \times I_{OUT(MAX)}$. Where, $I_{OUT(MAX)}$ is the maximum output current.

Then, the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW}\,\Delta I_L} V_{OUT}\,(1 - \frac{V_{OUT}}{V_{IN\,(MAX)}}) \quad (1)$$

Where, f_{SW} is the switching frequency, $V_{IN(MAX)}$ is the maximum input voltage. The peak current flowing in Inductor is $I_{L(PEAK)} = I_{OUT(MAX)} + \Delta I_L / 2$. If the Inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device. An inductor having saturation current higher than the device current limit has to be chosen.

8.2 Output capacitors (C_{OUT})

Output capacitors are selected to support load transients and output ripple current, as well as to get loop stability. The amount of voltage ripple can be calculated by the output ripple current flowing in the Inductor:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_L\,(ESR + \frac{1}{8 f_{SW} C_{OUT}}) \quad (2)$$

Usually the first term is dominant. However, if a ceramic capacitor (which is recommended) is adopted, the first term on the above equation can be neglected as the ESR value is very low.

$$C_{OUT\,(MIN)} = \frac{\Delta I_L}{8 f_{SW} \times (V_{OUT\,(RIPPLE)} - \Delta I_L \times ESR)} \quad (3)$$

For example, in case $V_{OUT} = 3.3$ V, $V_{IN} = 14$ V, $f_{SW} = 250$ kHz, $\Delta I_L = 0.3 \times 3.5$ A $= 1.05$ A, in order to have a $\Delta V_{OUT} = 5\% \times V_{OUT} = 0.165$V , a capacitor bigger than 3.3 µF is needed ignoring the ESR of the capacitor. In case of not negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value. The ESR can be minimized by simply adding more capacitors in parallel, or by using higher quality capacitors.

It is important to have a big enough output capacitor to sustain the output voltage during a load transient. The regulator usually needs time to maintain the output voltage during load transitions. Eq. (4) shows the minimum output capacitance needed in this case. This value does not take the ESR of the output capacitor into account in the output voltage change. High quality capacitors or lower ESR capacitors are recommended. The minimum output capacitance needed is also determined by the maximum energy stored in the inductor when a high current to low current transition occurs. The capacitance must be sufficient to absorb the change in inductor current as Eq. (5).

$$C_{OUT\,(MIN)} = \frac{(I_{OUT\,(MAX)} - I_{OUT\,(MIN)}) \times 2.5 T_{sw}}{\Delta V_{OUT}} \quad (4)$$

$$C_{OUT\,(MIN)} = \frac{L}{2} \times \frac{I_{OUT\,(MAX)}{}^2 - I_{OUT\,(MIN)}{}^2}{V_{OUT} \times \Delta V_{OUT}} \quad (5)$$

Where: $I_{OUT(MAX)}$ and $I_{OUT(MIN)}$ refer to the worst case load in the system and ΔV_{OUT} is the tolerance of the regulated output voltage.

Generally, if the minimum output capacitance satisfies Eq. (4) and Eq. (5), it is bigger enough to meet also Eq. (3). However, the final output capacitance should be the biggest one among them.

8.3 Input capacitors (C_{IN})

The input capacitors must be chosen to support the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitors must deliver the RMS current according to the below equation:

$$I_{RMS} > I_{OUT\,(MAX)} \sqrt{D(1-D)} \quad (6)$$

Where $I_{OUT(MAX)}$ is the maximum DC output current and D is the duty cycle. This function has a maximum at D = 0.5 and it is equal to $I_{OUT(MAX)}/2$.

Ceramic capacitors can deliver quite a bit of current but their total capacitance is relatively low. Electrolytic capacitors typically offer much more capacitance than ceramic capacitors, but can typically deliver a current of 100 to 500 mArms. So a good design will employ both types of capacitor with the ceramic capacitors placed closest to the input pins of the device.

As a result, ceramic capacitors which have very low ESR and inductance are the best for filtering the high frequency switching noise, and electrolytic capacitors are typically able to provide more current over extended periods of time where V_{IN} would otherwise droop.

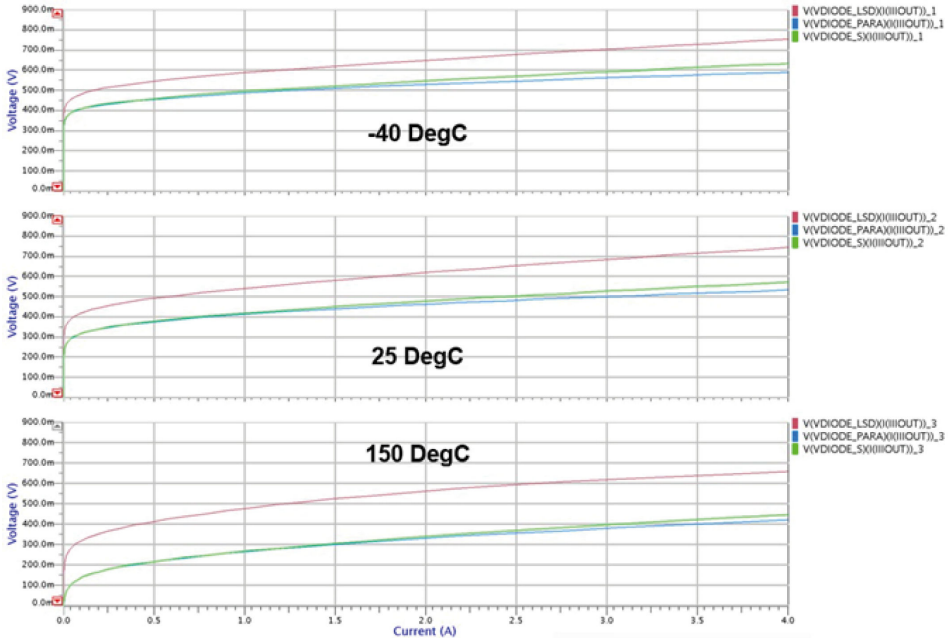
8.4 Bootstrap capacitor (C_{BS})

A bootstrap capacitor must be connected between the BSx and PHASEx pins to provide floating gate drive to the high-side MOSFET. For most applications 47 nF is sufficient. This should be a ceramic capacitor with a voltage rating of at least 6 V.

8.5 Schottky diode

When the L5964 needs to supply more than 2 A from a switching regulator, one Schottky diode has to be connected at each output of the DC-DC converter (cathode on PHASE1/PHASE2 pins, anode on PGND1/PGND2). The Schottky diode needs to have a breakdown voltage equal or higher than PHASE pin absolute maximum ratings of 40 V, with less than 0.5 V forward voltage at 2 A forward current at room temperature 25 °C. In order to keep the voltage drop within 0.5 V, the series resistance to the diode should be minimized, keeping short and large PCB connection between the diode and the phase pin, the diode and ground. Maximum parasitic capacitance that Schottky can add is 2 nF. Parasitic capacitor will affect the snubber. Figure 21 shows simulations in 3 conditions: the red line shows the L5964 alone, the blue line shows the Schottky STPS3L40UF alone and the green line shows the parallel of L5964 and STPS3L40UF. They are the worsts case conditions for both L5964 (highest current capability versus process spread) and Schottky (lowest current capability). Comparison is made at 3 temperatures. The blue line must be always lower than the red one: higher distance means higher protection. The green line close to blue line says that almost all the current flows through the Schottky diode.

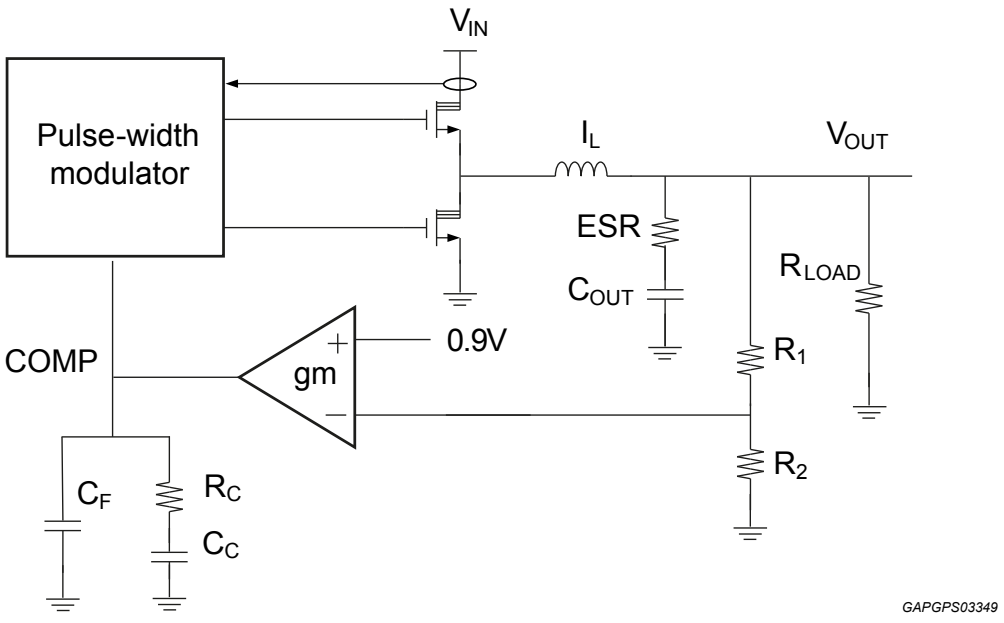
Figure 21. **Worstcase I/V characteristic of L5964, Schottky diode and L5964 protected with Schottky**



8.6 Compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the device is based on the peak current mode control, compatible with external RC compensation network. The error amplifier is a transconductance amplifier with large bandwidth, which is much larger than the closed-loop one.

Figure 22. **Basic control loop block diagram**



The above figure shows the closed loop system with a R_C compensation network. The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The loop transfer function is:

$$L(s) = \frac{V_{REF}}{V_{OUT}} \times G_{MOD}(s) \times G_{EA}(s) \quad (7)$$

Where: s is the angular frequency;

V_{REF} is the internal reference voltage, 0.9 V;

V_{OUT} is the output voltage of the converter; $G_{MOD}(s)$ is the transfer function of the modulator with C_{OUT} and R_{LOAD}. $G_{MOD}(s)$ forms a pole and a zero by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR as expressed in below equation:

$$G_{MOD}(s) = \frac{g_{mMOD} R_{LOAD} (1 + sESR \times C_{OUT})}{(1+sR_{LOAD} C_{OUT})} \quad (8)$$

gmMOD = 3.6S

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT\ MAX}} \quad (9)$$

The dominant pole is:

$$f_{pMOD} = \frac{1}{2\pi C_{OUT} (R_{LOAD} ESR)} \quad (10)$$

The zero is :

$$f_{zMOD} = \frac{1}{2\pi C_{OUT} ESR} \quad (11)$$

$G_{EA}(s)$ is the transfer function of the buck convertor from control to output. It forms two poles and a zero as expressed in the equation below:

$$G_{EA}(s) \approx \frac{g_{mEA} r_o (1+ sR_C C_C)}{(1+ sr_O C_C)(1+ sR_C C_F)} \quad (12)$$

Where:

g_{mEA} is the transconductance of the error amplifier, 1mS. r_O is the output resistance of error amplifier.

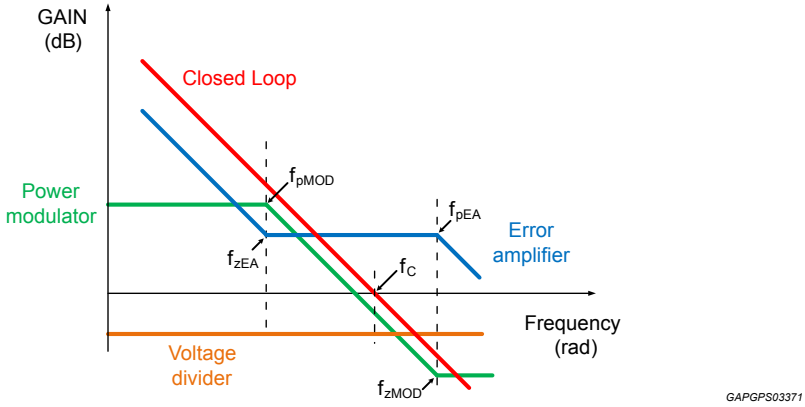
The zero is:

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C} \quad (13)$$

The option pole is:

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C} \quad (14)$$

Figure 23. **Simplified gain plot**



Application information

The zero f_{zEA} set by C_C and R_C cancel the pole f_{pMOD} set by R_{LOAD} and C_{OUT}.

The optional pole f_{pEA} set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency f_C, where the loop gain equals 1 (0 dB).

The power modulator has a DC gain set by g_{mMOD} x R_{LOAD}. g_{mMOD} is transconductance of modulator, it is about 3.6S. The following equations allow to approximate the value for the gain of the power modulator $GAIN_{MOD(DC)}$.

$$GAIN_{MOD(DC)} = g_{mMOD} \times R_{LOAD} \quad (15)$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error-amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD(fC)} = GAIN_{MOD(DC)} \times \frac{f_{pMDO}}{f_C} \quad (16)$$

The guidelines for calculation of network:

1. Choose a value for fC,usually between $f_{SW}/5$ and $f_{SW}/10$.
2. Choose resistor divider R1 and R2 to set the desired V_{OUT}.
3. Calculate the value of R_C as follows:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times GAIN_{MOD(fC)}} \quad (17)$$

4. Set the error-amplifier compensation zero formed by R_C and CC (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C} \quad (18)$$

5. If f_{zMOD} is less than $5f_C$, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C} \quad (19)$$

8.7 Power good delay time setting

The PGDELAY1 and PGDEALY2 pins are multipurpose pin that provide a delay function of power good output when chip is out of microcontroller mode. There is an internal 10 µA current source to charge up the external delay capacitor. The delay time is set by :

$$T_{DLY} = \frac{2.2V}{10\mu A} C_{DLY} \quad (20)$$

Where:

C_{DLY} is the external delay capacitor.

8.8 Watch dog delay time setting

The PGDELAY1 and PGDEALY2 pins are multipurpose pins that do not provide a delay function of power good output when chip is in microcontroller mode. The PGDELAY1 set the reset duration time (T_R) and PGDEALY2 set the power up delay time (T_{UP}).

$$T_R = \frac{2.2V}{10\mu A} C_{DLY} \quad (21)$$

$$T_{UP} = \frac{2.2V}{10\mu A} C_{DLY} \quad (22)$$

Where:

C_{DLY} is the external delay capacitor.

9 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

Figure 24. LQFP64 (10x10x1.4 mm exp. pad up) package outline

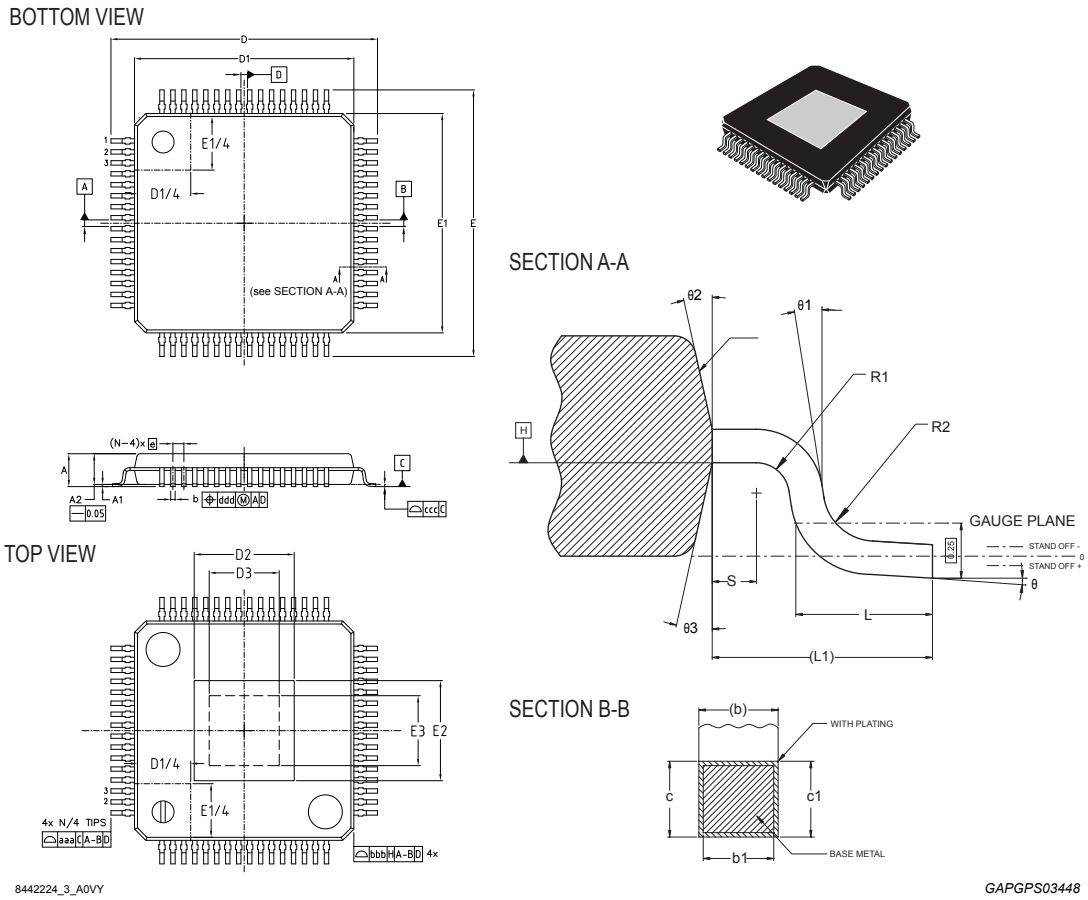
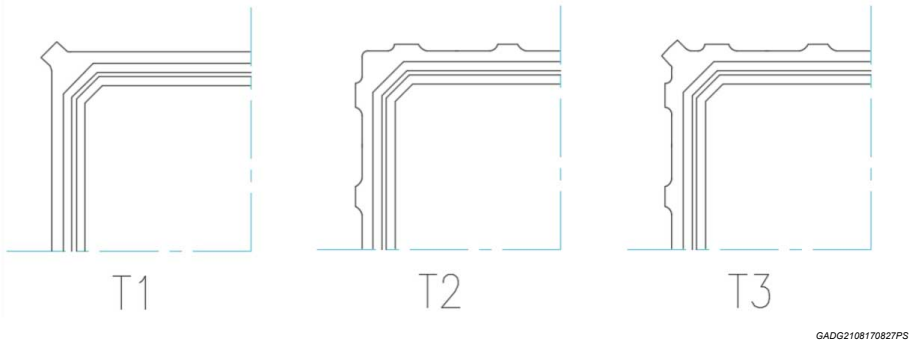


Table 12. **LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data**

Symbol	Dimensionsin mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	6°
Θ1	0°	9°	12°
Θ2	11°	12°	13°
Θ3	11°	12°	13°
A	-	-	1.49
A1	-0.04	-	0.04
A2	1.35	1.4	1.45
b	-	-	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	0.127	0.16
D	12.00 BSC		
D1(1)(2)	10.00BSC		
D2	**See VARIATIONS**		
e	0.50BSC		
E	12.00BSC		
E1(1)(2)	10.00BSC		
E2	**See VARIATIONS**		
L	0.45	0.60	0.75
L1	1.00REF		
N	-	64	-
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	-	0.20	-
bbb	-	0.20	-
ccc	-	0.08	-
ddd	-	0.08	-
VARIATIONS			
Padoption 6.0x6.0 (T1-T3)(3)			
D2	-	-	6.61
E2	-	-	6.61
D3	4.8	-	-
E3	4.8	-	-

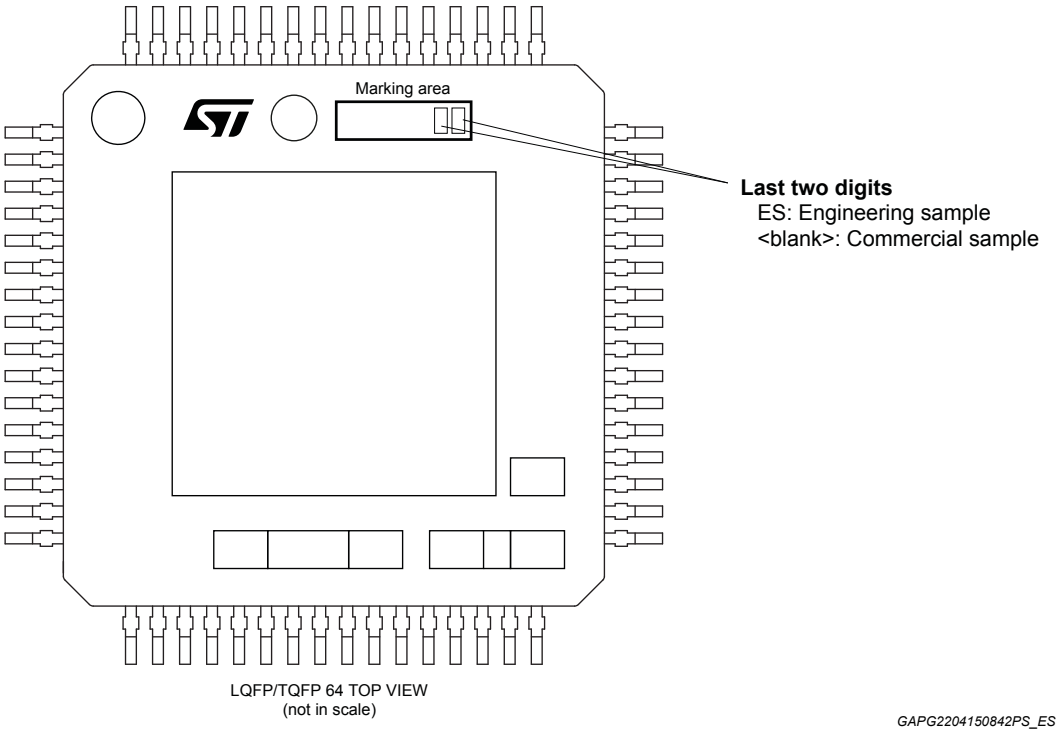
1. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusion is “0.25 mm” per side.
2. The Top package body size may be smaller than the bottom package size by much as 0.15 mm.

3. Number, dimensions and position of shown groves are for reference only:



9.2 Package marking information

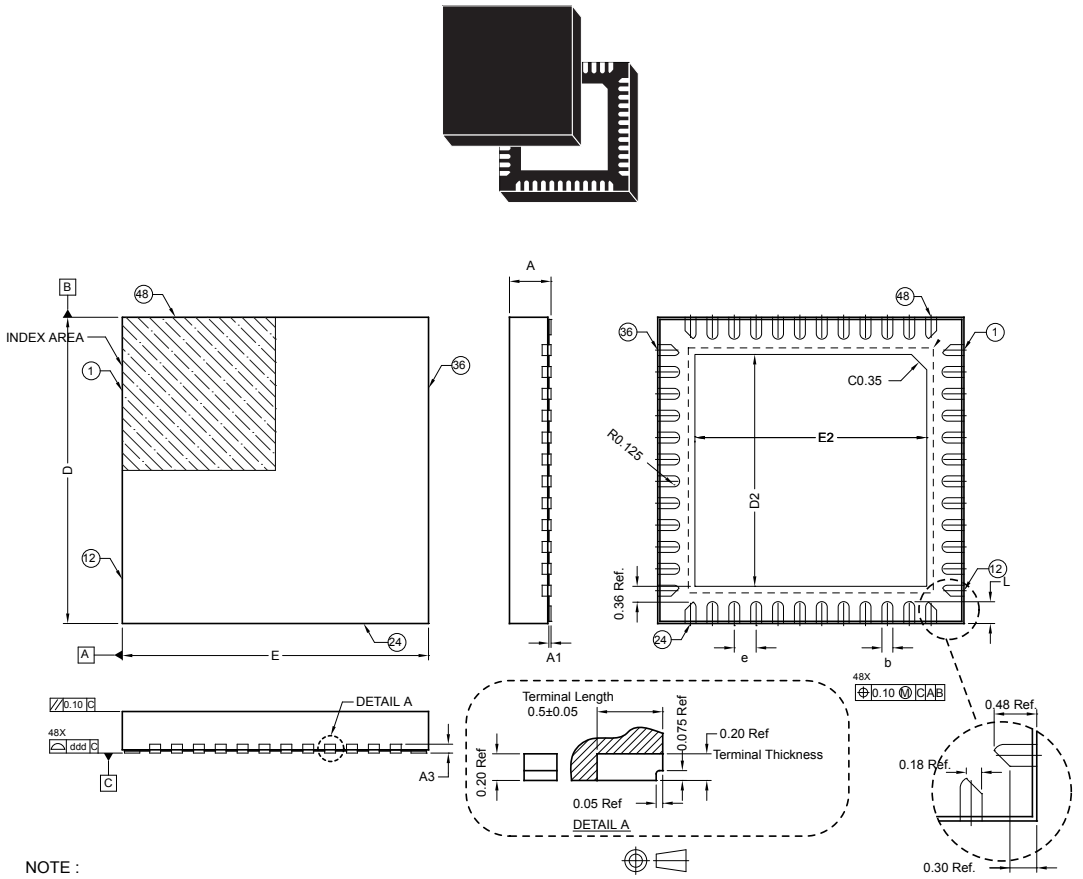
Figure 25. **LQFP64 (10x10x1.4 mm exp. pad up) marking information**



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

9.3 VFQFPN-48 (7x7x1.0 mm - opt. D) package information

Figure 26. **VFQFPN-48 (7x7x1.0 mm - opt. D) package outline**



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. REFER JEDEC MO-220.

7446345_G_V0 (Opt. C)

GAPGPS03449

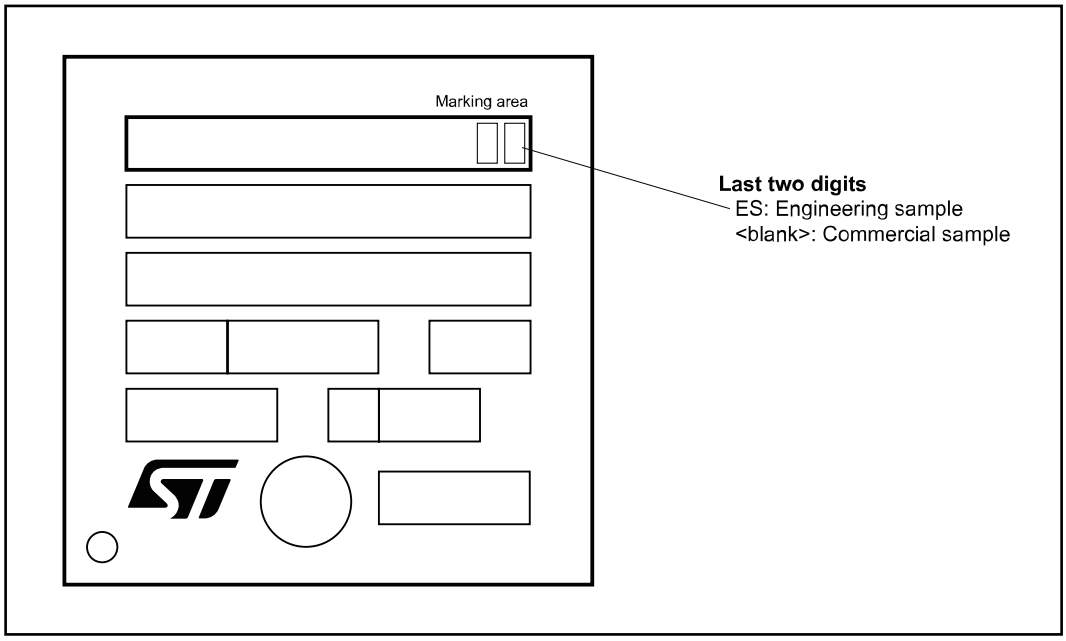
Table 13. **VFQFPN-48 (7x7x1.0 - opt. D) package mechanical data**

Ref	Dimensions					
	Millimeters			Inches [1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.85	0.95	1.05	0.0335	0.0374	0.0413
A1	-	-	0.05	-	-	0.0020
A2	-	0.75	-	-	0.0295	-
A3	-	0.200	-	-	0.0079	-
b	0.15	0.25	0.35	0.0059	0.0098	0.0138
D	6.80	7.00	7.15	0.2697	0.2756	0.2815
D2	5.15	5.30	5.45	0.2028	0.2087	0.2146
E	6.85	7.00	7.15	0.2697	0.2756	0.2815
E2	5.15	5.30	5.45	0.2028	0.2087	0.2146
e	0.45	0.50	0.55	0.0177	0.0197	0.0217
L	0.45	0.50	0.55	0.0177	0.0197	0.0217
ddd	-	-	0.08	-	-	0.0031

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*

9.4 VFQFPN-48 (7x7x1.0) marking information

Figure 27. **VFQFPN-48 (7x7x1.0) marking information**



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

10 Ordering information

Table 14. **Ordering information**

Part number	Package	Packing
L5964L-TY	LQFP64	Tray
L5964L-TR		Tape and reel
L5964Q-TY	VQFPN-48	Tray
L5964Q-TR		Tape and reel

Revision history

Table 15. **Document revision history**

Date	Version	Changes
02-Dec-2025	1	Initial release.

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.