L9965C/L99BM2C

Datasheet

Current, voltage, charge, and isolation monitor for HV battery packs

TQFP48
7x7x1 mm

Product status link
L9965C, L99BM2C

Product summary		
Order code	**Package**	**Packing**
L9965C-TR	TQFP48	Tape and reel
L99BM2C-TR		

Features

- L9965C: AEC-Q100 qualified
- L9965C Functional Safety: ISO26262 compliant, ASIL-D systems ready, documentation available
- Temperature grade 1: -40°C to +125°C operating temperature range
- HBM ESD classification level 2
- CDM ESD classification level C4B
- 2 independent current sense ADCs
    - 18-bit resolution
    - Input range = ±100 mV
    - <0.1% gain error, <1 LSB offset
    - Integrated programmable digital filtering with cut-off frequency from 3.5 kHz to 5 Hz for instantaneous current measurement
    - Fully redundant architecture with cross-check on every current sample
- Integrated Coulomb Counter
- Fully redundant short circuit detector with programmable threshold and ultrafast reaction time
- 2 programmable (level/PWM encoded) FAULT outputs
- Programmable DCDC converter controller to enable fast and flexible DC-link precharge
- 10 gate pre-drivers also compatible with optocouplers
- 11 fully differential analog inputs
- 7 configurable GPIO
- SPI and I2C Controller peripherals to interface up to two external EEPROM, L9965P/L99BM2P pyro driver sensors
- SPI Target for direct MCU interface
- 3.3V (VTREF) and 5V (V5V) LDOs for external sensors supply and biasing
- Embedded NVM for configuration parameters storage and runtime configuration integrity check
- Ultrafast vertical interface peripheral for isolated communication
- Compatible with 18S L9965A/L99BM218 cell monitoring chip with a max desynchronization time of 7 µs at system level

Applications

- Automotive battery monitoring systems
- Energy storage systems
- UPS

Description

The L9965C/L99BM2C is a current, voltage, charge, and isolation monitor for HV battery packs.

The devices belong to the L9965/L99BM2 family for high-voltage battery management systems monitoring and control.

1 Overview

The L9965C/L99BM2C is a current, voltage, charge and isolation monitor for HV battery packs.

It is part of the L9965/L99BM2 chipset for battery management systems and can be inserted as an addressable element of the same isolated daisy chain (VIF).

It monitors instantaneous pack current by means of an external shunt resistor and provides current measurements synchronized with battery cells voltage when used in conjunction with L9965A/L99BM218 cell monitoring chip. Current is also integrated over time to accumulate pack charge information.

The L9965C/L99BM2C also monitors pack current to detect overcurrent and short-circuit events.

Current measurement function and short-circuit detection are fully redundant and embed safety checks, targeting highest FuSa targets in demanding systems (ASIL D for automotive applications).

The IC also features 10 gate predrivers to drive external FETs and optocouplers.

They can be used in conjunction with 11 analog inputs to perform fully differential voltage measurements, monitoring several key voltages in the HV system (e.g., DC-Link connectors, charger connectors, etc.) and the isolation between battery terminals and chassis (with ASIL-A compliance for automotive applications).

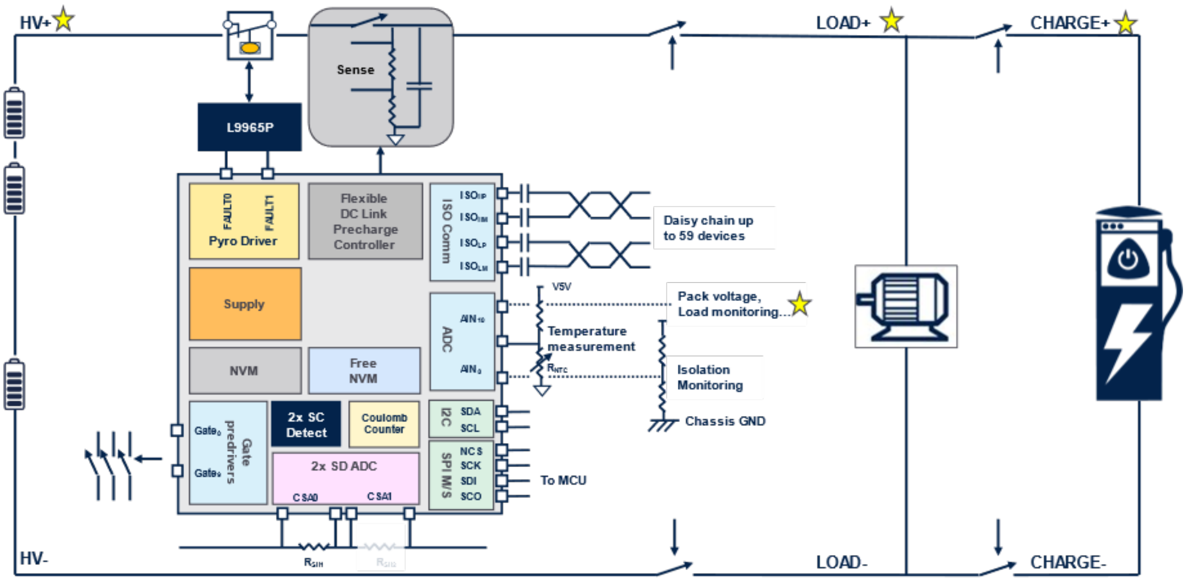
Voltage ADC supports both absolute and ratiometric measurements to provide maximum flexibility and accuracy for temperature measurement via external NTCs.

The L9965C/L99BM2C integrates 5V and 3.3V LDOs available for biasing external sensors and supplying companion chips such as ST automotive EEPROMs. A SPI Controller and an I2C Controller allow interfacing the IC with external sensors and EEPROMs.

The devices are designed to enable easy and reliable interaction with the L9965P/L99BM2P respectively, a companion pyroswitch driver. The chipset is designed to achieve ultra-fast detection and reaction to short-circuit failures.

The device embeds a fully configurable DC-link precharge controller algorithm to implement fast active charge of the DC-Link. The active precharge controller provides an alternative and cost-effective solution to traditional passive RC network that requires a very large high-power resistor, with a saving in the BOM and in the PCB space.

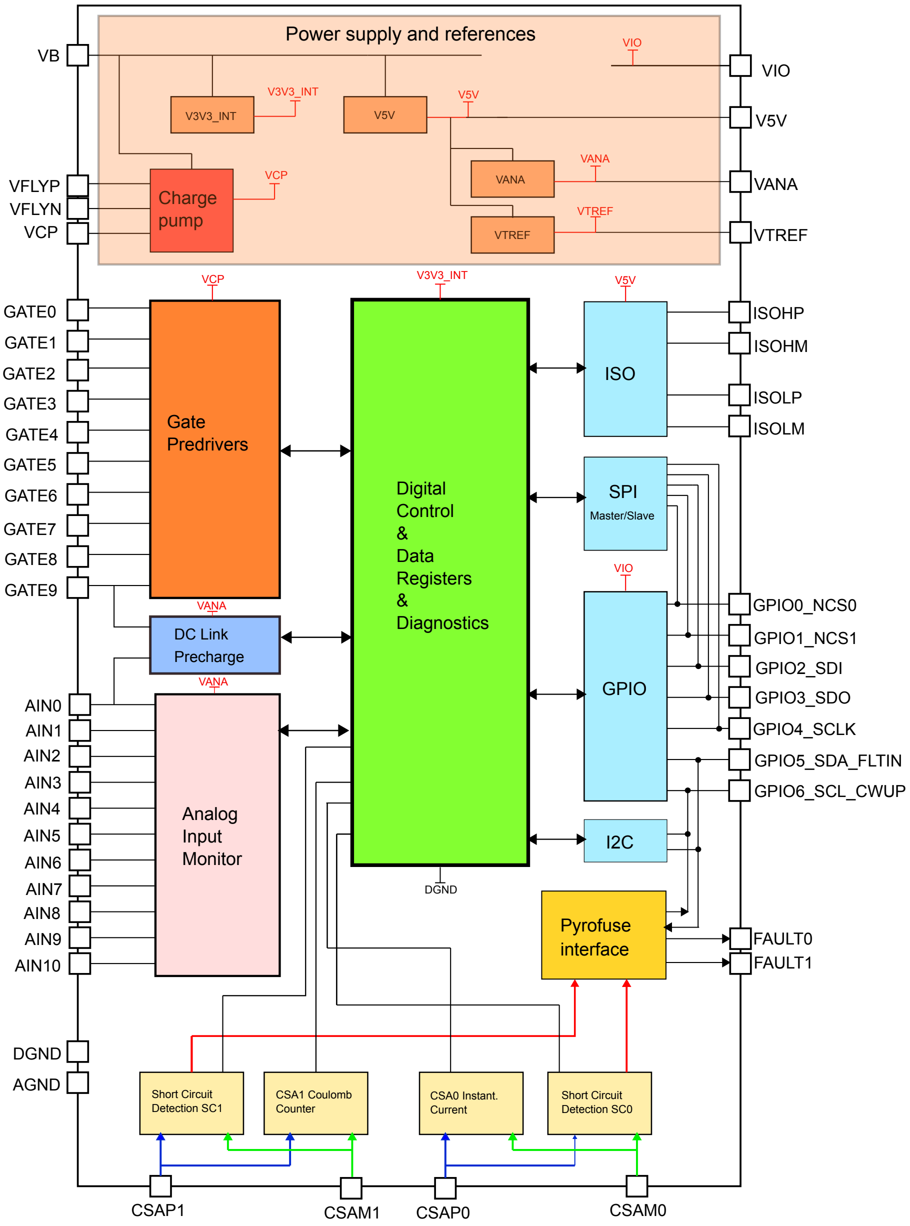
Figure 1. L9965C/L99BM2C battery pack controller



2 Block diagram and pin description

2.1 Block diagram

Figure 2. L9965C/L99BM2C Block diagram



2.2 Pin description

Figure 3. L9965C Pinout (top view)

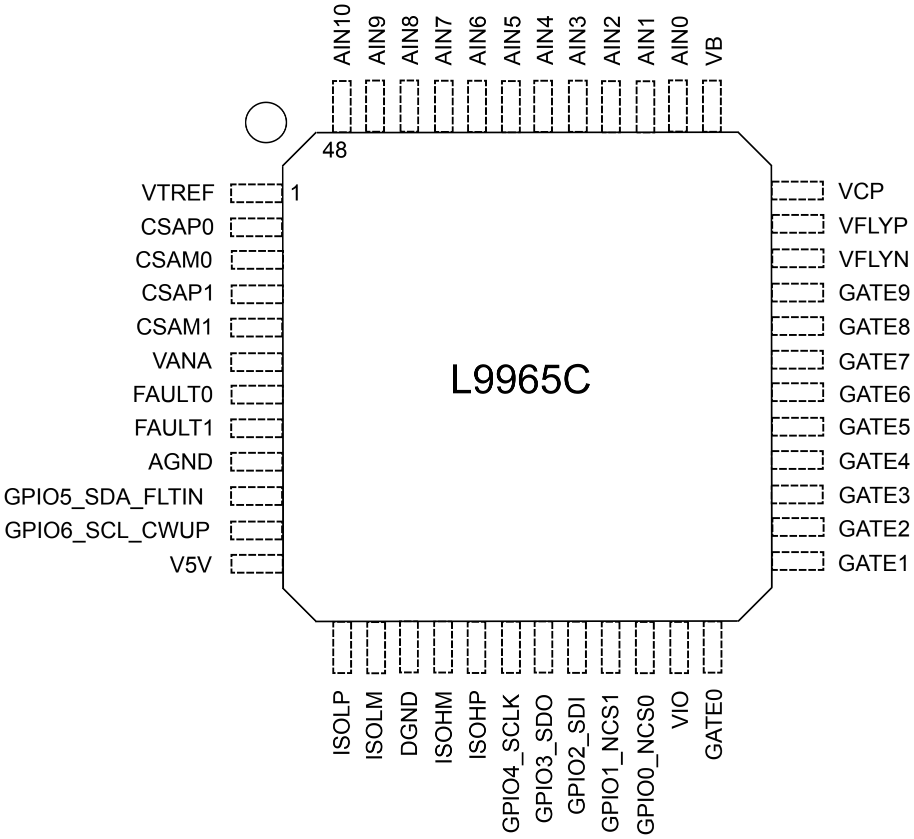


Figure 4. **L99BM2C Pinout (top view)**

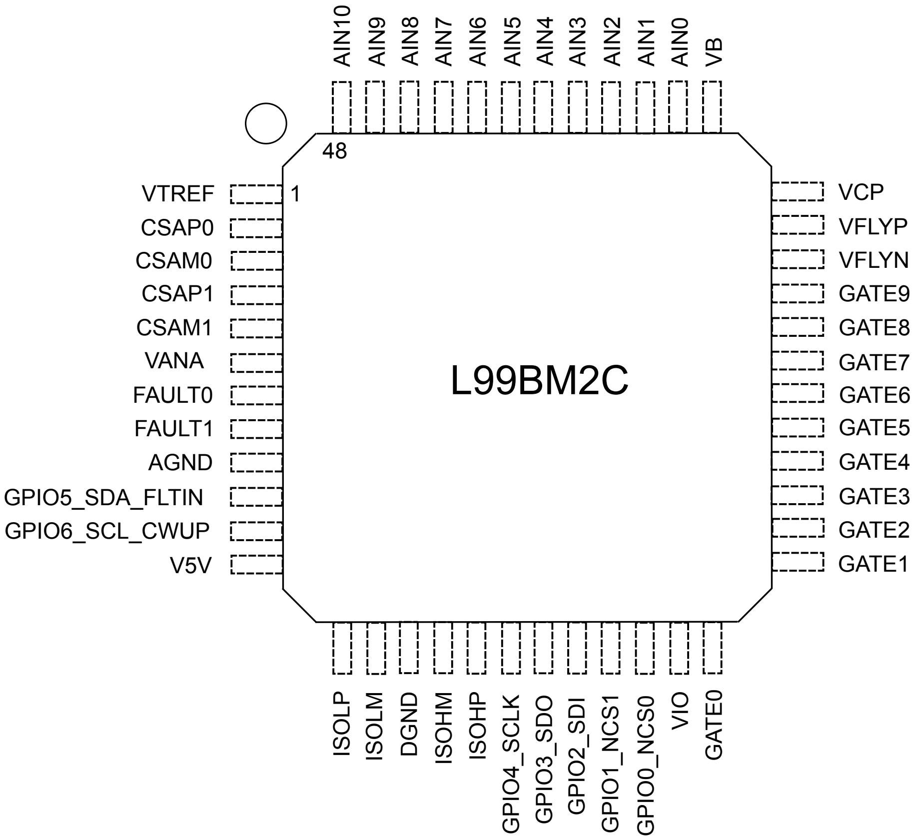


Table 1. **Pin function**

Pin #	Pin name	Description	Pin type	Pin category
1	VTREF	3V3 LDO for external use	Regulator out	Local
2	CSAP0	Current sense line	Analog input	Local
3	CSAM0	Current sense line	Analog input	Local
4	CSAP1	Current sense line	Analog input	Local
5	CSAM1	Current sense line	Analog input	Local
6	VANA	3V3 LDO for internal use	Regulator out	Local
7	FAULT0	Fault output (push-pull)	Digital output	Local
8	FAULT1	Fault output (push-pull)	Digital output	Local
9	AGND	Analog Ground	GND	Global
10	GPIO5_SDA_FLTIN	General purpose I/O or I2C Data or Fault Input	Analog input/digital I/O	Local
11	GPIO6_SCL_CWUP	General purpose I/O or I2C Clock or Cyclic Wakeup output	Analog input/digital I/O	Local
12	V5V	5V LDO	Regulator out	Local
13	ISOLP	VIF pin	Analog I/O	Global
14	ISOLM	VIF pin	Analog I/O	Global
15	DGND	Digital Ground	GND	Global
16	ISOHM	VIF pin	Analog I/O	Global
17	ISOHP	VIF pin	Analog I/O	Global
18	GPIO4_SCLK	General purpose I/O or SPI Clock	Digital I/O	Local

Pin #	Pin name	Description	Pin type	Pin category
19	GPIO3_SDO	General purpose I/O or SPI Data output	Digital I/O	Local
20	GPIO2_SDI	General purpose I/O or SPI Data Input	Digital I/O	Local
21	GPIO1_NCS1	General purpose I/O or SPI Chip Select	Digital I/O	Local
22	GPIO0_NCS0	General purpose I/O or SPI Chip Select	Digital I/O	Local
23	VIO	Digital output buffer supply	Supply	Local
24	GATE0	Gate Predriver output	Predriver output	Local
25	GATE1	Gate Predriver output	Predriver output	Local
26	GATE2	Gate Predriver output	Predriver output	Local
27	GATE3	Gate Predriver output	Predriver output	Local
28	GATE4	Gate Predriver output	Predriver output	Local
29	GATE5	Gate Predriver output	Predriver output	Local
30	GATE6	Gate Predriver output	Predriver output	Local
31	GATE7	Gate Predriver output	Predriver output	Local
32	GATE8	Gate Predriver output	Predriver output	Local
33	GATE9	Gate Predriver output, Pre-charge controller Predriver output	Predriver output	Local
34	VFLYN	Charge Pump flying capacitor	Charge pump pin	Local
35	VFLYP	Charge Pump flying capacitor	Charge pump pin	Local
36	VCP	Charge Pump tank	Regulator out	Local
37	VB	Battery supply	Supply	Global
38	AIN0	Analog input, Pre-charge controller sensing input	Analog input	Local
39	AIN1	Analog input	Analog input	Local
40	AIN2	Analog input	Analog input	Local
41	AIN3	Analog input	Analog input	Local
42	AIN4	Analog input	Analog input	Local
43	AIN5	Analog input	Analog input	Local
44	AIN6	Analog input	Analog input	Local
45	AIN7	Analog input	Analog input	Local
46	AIN8	Analog input	Analog input	Local
47	AIN9	Analog input	Analog input	Local
48	AIN10	Analog input	Analog input	Local
49	EP	Exposed Pad. Connect to AGND		N.A.

2.3 Unused pins

Unused GPIOs (GPIOx) shall be connected to AGND. They shall be left programmed as analog input via CFG_GPIO.GPIO<x>_CONF.

Unused VIF ports (ISOxP – ISOxM pair) shall be terminated with R_{TERM}.

Unused GATEx outputs shall be terminated with pull-down resistors connected to AGND (470 kΩ is a proper value), and shall be kept disabled, as by default.

Unused AINx input shall be connected to AGND.

3 Device ratings

3.1 Electrical ratings

The following section describes the different operational ranges.

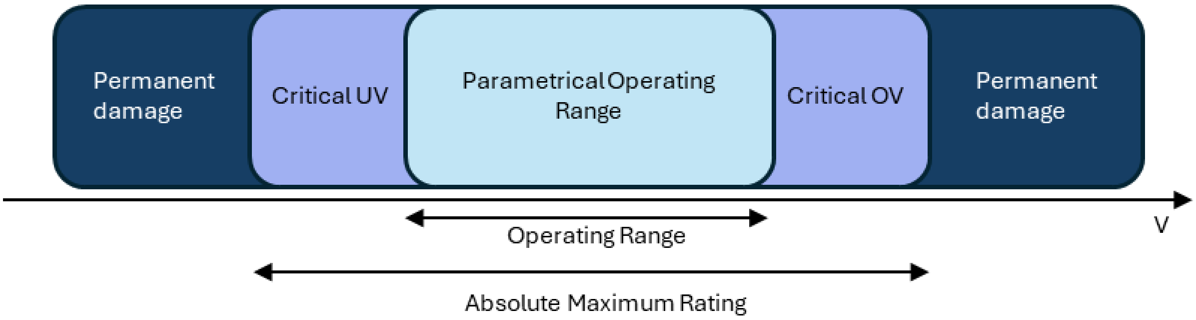
For each device pin:

- **Operating Range (OR):** within this range functions operate as specified and without parameter deviations. All the device's electrical parameters are tested and guaranteed in this range and are valid over the whole junction temperature operating range, unless otherwise specified.
- **Absolute Maximum Rating range (AMR):** within this range functions may not operate properly. However, the IC is not damaged. Exposure to AMR conditions for extended periods may affect device reliability. Exceeding any AMR may cause permanent damage to the integrated circuit.

Note: Currents are noted with a positive sign when flowing into a pin.

Note: Integrated protections and diagnostics are designed to prevent device destruction under the fault conditions described in the specification. Fault conditions are considered to be out of normal operating range. Protection functions are not designed for continuous repetitive operation.

Figure 5. **Pin voltage ranges**



All electrical parameters of the device, unless otherwise noted, are tested and guaranteed in the conditions specified in the table below.

Table 2. **Electrical ratings**

Param	Description	Test Cond	AMR MIN	OR MIN	OR TYP	OR MAX	AMR MAX	Unit	Notes
Power Supplies									
V_{VB}	VB: voltage range	vs. AGND	-0.3	6		18	24	V	
V_{V5V}	V5V: voltage range	vs. AGND	-0.3		5		min(7, V_{VB} +0.3)	V	Regulated voltage
V_{VANA}	VANA: voltage range	vs. AGND	-0.3		3.3		min (4.6, V_{V5V} + 0.3)	V	Regulated voltage
V_{VTREF}	VTREF: voltage range	vs. AGND	-0.3		3.3		min (4.6, V_{V5V} + 0.3)	V	Regulated voltage
V_{VCP}	VCP: voltage range	vs. AGND	V_{VB}-0.3		V_{VB}+5		V_{VB} + 12	V	Regulated voltage
V_{VFLYP}	VFLYP: voltage range	vs. AGND	V_{VB}-0.3				V_{VB} + 12	V	

Param	Description	Test Cond	AMR MIN	OR MIN	OR TYP	OR MAX	AMR MAX	Unit	Notes
V_{VFLYN}	VFLYN: voltage range	vs. AGND	Max (-0.3; V_{VB} - 10)				V_{VB}+ 0.3	V	
V_{VIO}	VIO: voltage range	vs. AGND	-0.3	3		5.5	7	V	
Grounds									
V_{DGND}	DGND: voltage range	vs. AGND	-0.3	-0.1		0.1	0.3	V	
Analog Inputs									
V_{AINx}	AIN0..AIN10: voltage range	vs. AGND	-0.3	0		V_{VB}	24	V	
Current sense									
V_{CSAx}	CSAP, CSAM: voltage range	vs. AGND	-1	-0.125		+0.125	4.6	V	
Gate predrivers									
V_{GATEx}	GATE0…GATE10: voltage range	vs. AGND	-0.3	0		min(V_{GATE_CLAMP},V_{VCP})	V_{VCP} + 0.3	V	
GPIOs									
V_{GPIOx}	GPIO0…GPIO6: voltage range	vs. AGND	-0.3	0		V_{V5V}	V_{VIO} + 0.3	V	
Fault lines									
V_{FAULTx}	FAULT0…1: voltage range	vs. AGND	-0.3	0		3.6	min (4.6, V_{VANA} + 0.3)	V	
ISO signals									
V_{ISOx} (1)	ISOLM, ISOLP, ISOHM, ISOHP: voltage range	vs. AGND	-9	0		V_{V5V}	18	V	

1. *These limits are intended to ensure:*
   - *DPI EMC on ISOx pins*
   - *BCI EMC on ISOx pins*
   - *Hotplug on ISOx pins*
   - *ESD 4kV HBM on ISOx pins*

3.2 ESD ratings

Table 3. ESD protection

Test Type	Pin	Value	Unit
HBM(1)	All pins	± 2	kV
HBM(1)(2)	VB, AGND, DGND, ISOHP, ISOHM, ISOLP, ISOLM	±4	kV
CDM(3)	All pins	±500	V
CDM(3)	Corner pins	±750	V
Latch-up (4)	All pins	±100	mA

1. *HBM (Human Body Model) according to AEC-Q100-002.*
2. *Each pin is tested vs GND pins connected together.*

3. *CDM (Charged Device Model) according to AEC-Q100-011.*
4. *Latch-up test according to AEC-Q100-004 Class 2, Level A.*

3.3 Thermal ratings

All electrical parameters of the device, unless otherwise noted, are tested and guaranteed in the conditions specified in the table below.

Table 4. Temperature ranges and thermal data

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating temperature (ECU environment)	-40		125	°C
T_j	Operating junction temperature	-40		150	°C
T_{stg}	Storage temperature	-40		150	°C
$R_{Th\ j\text{-}a}$	Thermal resistance junction-to-ambient (1) (2)		27		°C/W

1. *Evaluated according to Jedec JESD51-2,-5,-7 guideline with a 2s2p thermally enhanced PCB.*
2. *Even assuming a high ambient temperature (T_{amb}=125°C), the increase due to power dissipation, considering the reference application model, is not higher than 5°C. In a worst-case scenario, the final junction temperature Tj= 130°C is well below the maximum allowed value.*

4 Current consumption

The L9965C/L99BM2C is supplied by the VB pin, which is then used to generate all the regulated supplies.

When used in BEV/PHEV systems, the IC is usually placed in the HV battery junction box, where all the different supply derivation lines are managed via independent contactors or solid-state relays.

The IC is usually supplied by means of an isolated DC/DC converter feeding from the 12V LV supply (reinforced isolation). Alternatively, a functionally isolated DC-DC converter may be used to generate the VB supply from the HV battery pack. In most demanding systems, a wired-OR combination of the two supplies may be necessary.

Table 5. **Current consumption**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$I_{VB\_BASE\_SLP0}$	Base current consumption from VB pin, with all resources enabled and in idle state	DEEP SLEEP, -40°C ≤ T_{amb} ≤ +85°C			10	µA	
$I_{VB\_BASE\_SLP1}$		DEEP SLEEP, +85°C ≤ T_{amb} ≤ +125°C			17	µA	
$I_{VB\_STBY\_CAL0}$		STANDBY, CC_STBY_CAL_EN = 0			235	µA	
$I_{VB\_STBY\_CAL1}$		STANDBY, CC_STBY_CAL_EN = 1			250	µA	
$I_{VB\_BASE\_NORM}$		NORMAL, I_{V5V_EXT} = 0, I_{VTREF_EXT} = 0			3	mA	
$I_{VB\_DELTA\_SCx}$	Delta current from VB when one Short Circuit detection is enabled	NORMAL, SC<x>_EN=1 FAULT<x>_MODE = 0			100	µA	
$I_{VB\_DELTA\_CSA\_INST}$	Delta current from VB when the instantaneous current ADC is enabled	NORMAL, CSA continuously converting			350	µA	
$I_{VB\_DELTA\_CC}$	Delta current from VB when the Coulomb Counter ADC is enabled	NORMAL, CC continuously converting			150	µA	
$I_{VB\_DELTA\_ADCV}$	Delta current from VB when the voltage ADC is converting	Voltage ADC continuously converting			800	µA	
$I_{VB\_DELTA\_GATE}$	Delta current from VB when one GATE pre-driver is enabled	GATE<x> not in HiZ			40	µA	
$I_{VB\_DELTA\_COMM}$	Delta current consumption from VB pin when communication is ongoing	One VIF port continuously transmitting. Using recommended BOM			13	mA	VB
$I_{VB\_DELTA\_V5V}$	Delta current from VB when external load is applied to V5V	Guaranteed by characterization, I_{SOURCE} from 1mA to 2mA	-5.5			µA/mA	VB
$I_{VB\_DELTA\_VTREF\_SOURCE}$	Delta current from VB when external load is applied to VTREF	Guaranteed by characterization, I_{SOURCE} from 1mA to 2mA	-42			µA/mA	VB
$I_{VB\_DELTA\_VTREF\_SINK}$		Guaranteed by characterization, I_{SINK} from 500uA to 1mA			3.5	µA/mA	VB
$I_{VB\_DELTA\_PRECHG}$	Delta current from VB when the pre-charge function is running	Not including the dynamic current due to the external FETs Qg			7	mA	VB
$I_{VB\_DELTA\_GPO}$	Delta current from VB when one GPIO is programmed as digital output	GPO<x> = 1			60	µA	

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
I_{VIO_GPO}	Leakage from VIO	All GPIOs disabled and in HiZ			1	µA	
$I_{VIO\_DELTA\_GPO}$	Delta current from VIO when one GPIO is programmed as digital output	GPO<x> = 1			230	µA	

5 Functional description

5.1 Device functional states

Figure 6 shows all the possible L9965C/L99BM2C states.

Figure 6. Device functional states

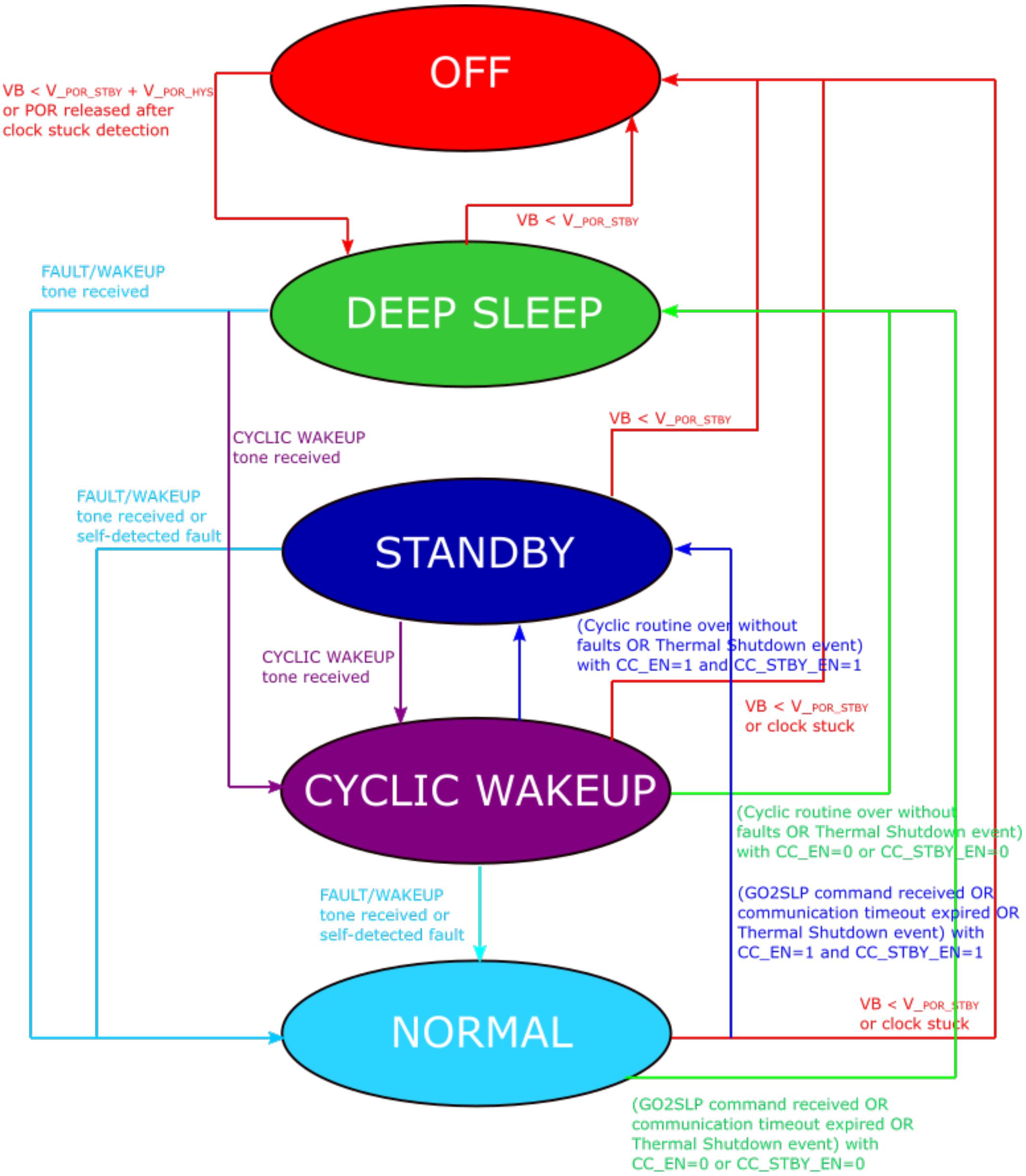


Table 6 summarizes the functional state behaviors, describing the transitions and the resources active in each operating state.

Table 6. Device functional states

State	Purpose	Reached from	Condition	Active resources
OFF	Device OFF	Any state	When VB voltage falls below the POR threshold	None

State	Purpose	Reached from	Condition	Active resources
DEEP SLEEP	Ultra-low power state for managing long inactivity periods	NORMAL	(GO2SLP command received OR communication timeout expired OR Thermal Shutdown event) with CFG_FOR_STBY_LOGIC.CC_EN = 0 or CFG_FOR_STBY_LOGIC.CC_STBY_EN = 0	Wake up Via VIF Wake up via SPI Target
		CYCLIC WAKEUP	(Cyclic routine over without faults OR Thermal Shutdown event) with CFG_FOR_STBY_LOGIC.CC_EN = 0 or CFG_FOR_STBY_LOGIC.CC_STBY_EN = 0	
		OFF	When VB rises above the POR threshold + hysteresis, or when the POR is released after a clock stuck detection.	
STANDBY	Low power state for managing battery idle state	NORMAL	(GO2SLP command received OR communication timeout expired OR Thermal Shutdown event) with CFG_FOR_STBY_LOGIC.CC_EN = 1 and CFG_FOR_STBY_LOGIC.CC_STBY_EN = 1	All resources active in DEEP SLEEP + Charge/ Discharge Detection Wakeup (CC_WUP)
		CYCLIC WAKEUP	(Cyclic routine over without fault OR Thermal Shutdown event) with CFG_FOR_STBY_LOGIC.CC_EN = 1 and CFG_FOR_STBY_LOGIC.CC_STBY_EN = 1	
CYCLIC WAKEUP	To perform cyclic diagnostics during low power operation	DEEP SLEEP	Wakeup by Cyclic Wakeup	All resources fully operating, except Communication Timeout (COMM_TIM), Short Circuit Detection, Clock Monitor Self-Test and Overcurrent Detection. Isolated Vertical Interface (VIF) partially available (passthrough from ISOL to ISOH disabled)
		STANDBY	Wakeup by Cyclic Wakeup	
NORMAL	Full operation	DEEP SLEEP	Wakeup by MCU, Wakeup by Fault, Wakeup via SPI Target.	All resources fully operating
		STANDBY	Wakeup by MCU, Wakeup by Fault, Wakeup via SPI Target, Self-Wakeup	
		CYCLIC WAKEUP	Wakeup by MCU, Wakeup by Fault, Self-Wakeup	

Transition from NORMAL to low power states occurs whenever a GO2SLP is commanded. To do so, the MCU has to write the 0xCC code in the SPECIAL_KEY field. The IC answers with the register content feedback, as for a usual write operation in VIF communication, where the device has been addressed with its VIF ID (not valid for broadcast command). Immediately after that, it moves to the low power state.

The POR_MAIN_ASSERTED latch indicates that a transition from NORMAL/CYCLIC WAKEUP to any other low power state (STANDBY/DEEP SLEEP/OFF) has occurred. The POR_SLEEP_ASSERTED indicates that a transition to OFF state has occurred. At the first power-up both flags (POR_MAIN_ASSERTED and POR_SLEEP_ASSERTED) are asserted.

5.2 Power-up sequence

A short procedure, recommended for correctly switching on the IC, is shown. The device is supposed to be used for the first time; it means that

- all the bits and fields in the registers have the default values.
- no device ID has been stored in the Non-Volatile Memory. The device holds, for VIF_ID, the default value of 0x00.

The following procedure can be used on both cases of L9965C/L99BM2C used in a stand-alone application (communication through SPI Target interface), or connected in daisy chain on the VIF bus.

Procedure 1: Power-up sequence

1. Supply VB with a voltage higher than the POR threshold. The device is expected to do the transition from OFF to DEEP SLEEP State.
2. A first wake-up frame (or tone) can be sent. The device is awakened up and the three LDOs (VTREF, VANA and V5V) are all switched ON. However, after the Communication Timeout expiration (2s is the default value), the device is expected to come back to DEEP SLEEP because
    a. The Communication Timeout is enabled by default. The device waits a valid frame before the timeout expiration.
    b. The communication is, in any case, not possible, since no device ID has been assigned to the device. The device can only accept broadcast commands (which are addressed with DEV_ID=0x00, as explained in Broadcast Write)
3. Before the timeout expiration, a broadcast command must be sent assigning to the 6-bit field VIF_ID_CFG.VIF_ID the desired <x> value of the VIF_ID. Considering that VIF_ID_CFG register is protected by lock field, the unlock procedure shall be applied (Procedure 11: Configuration Lock/Unlock).
4. User can check if the addressing has been successfully concluded. It is possible reading a register, setting for DEV_ID on MOSI frame the previously assigned <x> value. The device is expected to answer, with DEV_ID=<x> in MISO frame.
5. Optionally, the Communication Timeout can be disabled putting DEV_GEN_CFG_1.COMM_TIM_EN=0. The unlock procedure must be applied also in this case.

5.3 Power supply

The L9965C/L99BM2C is equipped with a comprehensive set of power supply units for feeding both internal and external components.

5.3.1 Main supply (VB)

The VB pin is the main supply. This line:

- Feeds the 5V LDO (5V)
- Feeds the 3V3 Standby LDO (V3V3 STBY)
- Feeds the Charge Pump (VCP)

5.3.1.1 Diagnostics

Table 7. **VB pin diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VB UV	If the V_{VB} voltage falls below $V_{VB\_UV\_TH}$ the fault is acknowledged.	DIAG_STATUS1.VB_UV flag is set	If the V_{VB} voltage rises above $V_{VB\_UV\_TH}$ + $V_{VB\_UV\_HYS}$, the VB_UV flag can be cleared by MCU	None	Blanked during wakeup sequences, until NORMAL/ CYCLIC WAKEUP states are reached Not maskable

5.3.1.2 Electrical parameters

Table 8. **VB supply electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{VB\_UV\_TH}$	VB Undervoltage Threshold		4.75	5	5.25	V	VB
$V_{VB\_UV\_HYS}$	VB Undervoltage hysteresis		85		185	mV	VB
$T_{VB\_UV\_FIL}$	VB Undervoltage filter time		17	20	23	µs	VB

5.3.2 Charge pump (VCP)

The charge pump:

- Feeds the internal analog circuitry for biasing of the Gate Pre-Drivers (GATEx)
- Feeds the internal analog circuitry for biasing the Analog Input Monitor (AINx)

5.3.2.1 Diagnostics

Table 9. **Charge pump diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
CP UV	If the V_{VCP} voltage falls below $V_{VCP\_UV\_TH}$ for an interval longer than $T_{VCP\_UV\_FIL}$ the VCP_UV fault is acknowledged.	DIAG_STATUS1.VCP_UV flag is set	If the V_{VCP} voltage rises above $V_{VCP\_UV\_TH}$ + $V_{VCP\_UV\_HYS}$ for an interval longer than $T_{VCP\_UV\_FIL}$, the VCP_UV flag can be cleared by MCU	None	Blanked during wakeup sequences, until NORMAL/ CYCLIC WAKEUP states are reached. Not maskable
CP OV	If the V_{VCP} voltage rises above $V_{VCP\_OV\_TH}$ for an interval longer than $T_{VCP\_OV\_FIL}$ the VCP_OV fault is acknowledged.	DIAG_STATUS1.VCP_OV flag is set	If the V_{VCP} voltage falls below $V_{VCP\_OV\_TH}$ - $V_{VCP\_OV\_HYS}$ for an interval longer than $T_{VCP\_OV\_FIL}$, the VCP_OV flag can be cleared by MCU	None	Not maskable

5.3.2.2 Electrical parameters

Table 10. **VCP electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{VCP_HIGH}	Regulated voltage	V_{VB} in OR range	V_{VB}+4		V_{VB}+7.5	V	VCP
V_{VCP_LOW}		Guaranteed by design, 4.3V < V_{VB} < 6V	V_{VB}+2.8		V_{VB}+6.5	V	VCP
I_{VCP_LOAD}	DC current capability	Design info			1.5	mA	VCP
f_{VCP}	Switching frequency	Design info		62.5		kHz	VCP
η_{VCP_HIGH}	Charge pump rescaling factor for current	Design info, V_{VB} in OR range	0.4			mA/mA	VB, VCP
$V_{VCP\_UV\_TH}$	Charge pump UV threshold		2		3.5	V	VCP-VB
$V_{VCP\_UV\_HYS}$	Charge pump UV threshold hysteresis		100			mV	VCP-VB
$T_{VCP\_UV\_FIL}$	Charge pump UV filter time		17	20	23	µs	VCP
$V_{VCP\_OV\_TH}$	Charge pump OV threshold		8		12	V	VCP-VB
$V_{VCP\_OV\_HYS}$	Charge pump OV threshold hysteresis		190			mV	VCP-VB
$T_{VCP\_OV\_FIL}$	Charge pump OV filter time		17	20	23	µs	VCP

5.3.3 5V LDO (V5V)

This 5V LDO:

- Is fed by VB main supply
- Feeds the 3V3 Analog LDO (VANA)
- Feeds the 3V3 Reference LDO (VTREF)
- Feeds the Isolated Vertical Interface (VIF)
- Can be used to feed the Digital Output Buffer Supply (VIO)

5.3.3.1 *Diagnostics*

Table 11. **V5V LDO diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
V5V UV	If V_{V5V} falls below $V_{V5V\_UV\_TH}$ for an interval longer than $T_{V5V\_UV\_OV\_FIL}$, the V5V UV fault is acknowledged	DIAG_STATUS1.V5V_UV flag is set	If V_{V5V} rises above $V_{V5V\_UV\_TH} + V_{V5V\_UV\_HYS}$ for an interval longer than $T_{V5V\_UV\_OV\_FIL}$, the V5V_UV flag can be cleared by MCU	None	Blanked during wakeup sequences, until NORMAL/ CYCLIC WAKEUP states are reached Not maskable
V5V OV	If V_{V5V} rises above $V_{V5V\_OV\_TH}$ for an interval longer than $T_{V5V\_UV\_OV\_FIL}$, the V5V OV fault is acknowledged	DIAG_STATUS1.V5V_OV flag is set	If V_{V5V} falls below $V_{V5V\_OV\_TH} - V_{V5V\_OV\_HYS}$ for an interval longer than $T_{V5V\_UV\_OV\_FIL}$, the V5V_OV flag can be cleared by MCU	None	Not maskable
V5V OC	If I_{V5V} rises above $I_{TH\_OC\_V5V}$ for a time longer than $T_{FLT\_OC\_V5V}$ filter time	DIAG_STATUS2.V5V_OC flag is set	If I_{V5V} falls below $I_{TH\_OC\_V5V}$ for a time longer than $T_{FLT\_OC\_V5V}$ filter time, the V5V_OC flag can be cleared by MCU	None	Blanked during wakeup sequences, until NORMAL/ CYCLIC WAKEUP states are reached Not maskable
V5V OT	If T_J rises above $T_{TH\_TSD\_V5V}$ for a time longer than $T_{FLT\_TSD\_V5V}$ filter time	No flag	If T_J falls below $T_{TH\_TSD\_V5V}$- $T_{TH\_HYS\_TSD\_V5V}$ for a time longer than $T_{FLT\_TSD\_V5V}$ filter time	None	Not maskable

5.3.3.2 *Electrical parameters*

Table 12. **V5V electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{V5V}	Regulated voltage	NORMAL, All operating lines and loads	-2%	5	+2%	V	V5V
I_{V5V_EXT}	Current capability for external applications		-10			mA	V5V
I_{V5V_LIM}	Current limitation	NORMAL, V_{V5V} = 0V	-220		-80	mA	V5V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{V5V\_LINE\_REG}$	Transient line regulation	Line step from minimum to maximum operating VB, dV/dt = 1V/us, All loads, Guaranteed by design	-6		+6	%	V5V
$dV_{V5V\_LOAD\_REG}$	Transient load regulation	Load step from minimum to maximum operating current, di/dt = 3mA/us, All lines, Guaranteed by design	-5		+5	%	V5V
$T_{V5V\_SOFT\_START}$	Soft start timing	From 10% to 90% of $V_{V5V,}$ Guaranteed by design			200	µs	V5V
$PSRR_{V5V}$	Power Supply Rejection Ratio	V_{NOISE} = 100mV_{pp} on $V_{VB,}$ f_{NOISE} = 400kHz, V_{VB} > 7V. Guaranteed by design	60			dB	V5V
$V_{V5V\_UV\_TH}$	V5V Undervoltage Threshold		4.25		4.75	V	V5V
$V_{V5V\_UV\_HYS}$	V5V Undervoltage hysteresis		50		150	mV	V5V
$V_{V5V\_OV\_TH}$	V5V Overvoltage Threshold		5.4		6	V	V5V
$V_{V5V\_OV\_HYS}$	V5V Overvoltage hysteresis		50		150	mV	V5V
$T_{V5V\_UV\_OV\_FIL}$	UV/OV filter time		17	20	23	µs	V5V
$T_{FLT\_OC\_V5V}$	V5V overcurrent monitor, detection filter time	Digital filter	17	20	23	µs	V5V
$I_{TH\_OC\_V5V}$	V5V overcurrent monitor, threshold current		-220		-80	mA	
$T_{FLT\_TSD\_V5V}$	V5V thermal shut-down, detection filter time	Digital filter	17	20	23	µs	
$T_{TH\_TSD\_V5V}$	V5V thermal shut-down, threshold equivalent temperature	High threshold voltage	172	180	188	°C	
$T_{TH\_ HYS\_TSD\_V5V}$	V5V thermal shut-down, threshold equivalent temperature, hysteresis			10		°C	

5.3.4 3V3 Analog LDO (VANA)

This 3.3V LDO:

- Is fed by 5V LDO (V5V)
- Is used for biasing internal analog circuitry

5.3.4.1 Diagnostics

Table 13. **VANA diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VANA UV	If the V_{VANA} voltage falls below $V_{VANA\_UV\_TH}$ for an interval longer than $T_{VANA\_UV\_FIL}$ the VANA_UV fault is acknowledged.	DIAG_STATUS1.VANA_UV flag is set	If the V_{VANA} voltage rises above $V_{VANA\_UV\ \_TH}$ + $V_{VANA\_UV\ \_HYS}$ for an interval longer than $T_{VANA\_UV\_FIL}$, the VANA_UV flag can be cleared by MCU	None	Blanked during wakeup sequences, until NORMAL/ CYCLIC WAKEUP states are reached Not maskable

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VANA OV	If the V_{VANA} voltage rises above $V_{VANA\_OV\_TH}$ for an interval longer than $T_{VANA\_OV\_FIL}$ the VANA_OV fault is acknowledged.	DIAG_STATUS1.VANA_OV flag is set	If the V_{VANA} voltage falls below $V_{VANA\_OV\_TH}$ - $V_{VANA\_OV\_HYS}$ for an interval longer than $T_{VANA\_OV\_FIL}$, the VANA_OV flag can be cleared by MCU	None	Not maskable
VANA OC	If I_{VANA} rises above $I_{TH\_OC\_VANA}$ for a time longer than $T_{FLT\_OC\_VANA}$ filter time	DIAG_STATUS2.VANA_OC flag is set	If I_{VANA} falls below $I_{TH\_OC\_VANA}$ for a time longer than $T_{FLT\_OC\_VANA}$ filter time, the VANA_OC flag can be cleared by MCU	None	Not maskable

5.3.4.2 *Electrical parameters*

Table 14. VANA electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{VANA}	Regulated voltage	All operating lines and loads	-3%	3.3	+3%	V	VANA
$T_{VANA\_SOFT\_START}$	Soft start timing	From 10% to 90% of V_{VANA}, Guaranteed by design			450	us	VANA
$T_{FLT\_OC\_VANA}$	VANA overcurrent monitor, detection filter time	Digital filter	17	20	23	μs	
$I_{TH\_OC\_VANA}$	VANA overcurrent monitor, threshold current		-61		-30	mA	
$V_{VANA\_UV\_TH}$	VANA UV threshold	Tested in production	2.56	2.73	2.89	V	VANA
$V_{VANA\_UV\_HYS}$	VANA UV threshold hysteresis	Tested in production	22		42	mV	VANA
$T_{VANA\_UV\_OV\_FIL}$	VANA UV/OV filter time	Guaranteed by SCAN	17	20	23	us	VANA
$V_{VANA\_OV\_TH}$	VANA OV threshold	Tested in production	3.48	3.71	3.93	V	VANA
$V_{VANA\_OV\_HYS}$	VANA OV threshold hysteresis	Tested in production	25		60	mV	VANA

5.3.5 3V3 Standby LDO (V3V3 STBY)

This internal 3.3V LDO:

- Is fed by Main Supply (VB)
- Is used for supplying internal circuitry in STANDBY and NORMAL

When in undervoltage, it determines the POR_MAIN assertion.

5.3.6 3V3 Reference LDO (VTREF)

This regulator can be used to bias external sensors and voltage dividers.

5.3.6.1 Diagnostics

Table 15. VTREF diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VTREF UV	If the V_{VTREF} voltage falls below $V_{VTREF\_UV\_TH}$ for an interval longer than $T_{VTREF\_UV\_FIL}$ the VTREF_UV fault is acknowledged.	DIAG_STATUS1.VTREF_UV flag is set	If the V_{VTREF} voltage rises above $V_{VTREF\_UV\_TH}$ + $V_{VTREF\_UV\_HYS}$ for an interval longer than $T_{VTREF\_UV\_FIL}$, the VTREF_UV flag can be cleared by MCU	None	Blanked during wakeup sequences, until NORMAL/ CYCLIC WAKEUP states are reached Not maskable
VTREF OV	If the V_{VTREF} voltage rises above $V_{VTREF\_OV\_TH}$ for an interval longer than $T_{VTREF\_OV\_FIL}$ the VTREF_OV fault is acknowledged.	DIAG_STATUS1.VTREF_OV flag is set	If the V_{VTREF} voltage falls below $V_{VTREF\_OV\_TH}$ - $V_{VTREF\_OV\_HYS}$ for an interval longer than $T_{VTREF\_OV\_FIL}$, the VTREF_OV flag can be cleared by MCU	None	Not maskable

5.3.6.2 Electrical parameters

Table 16. VTREF electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{VTREF}	Regulated voltage	NORMAL, all static line and loads	-2%	3.3	+2%	V	VTREF
I_{VTREF_EXT}	Current capability for external applications	Design info	-5		1	mA	VTREF
$I_{VTREF\_LIM\_SOURCE}$	Current limitation in source	NORMAL, V_{VTREF} = 0V	-44		-20	mA	VTREF
$I_{VTREF\_LIM\_SINK}$	Current limitation in sink	NORMAL, V_{VTREF} = 3.6V	5		15	mA	VTREF
$dV_{VTREF\_LOAD\_SOURCE}$	Transient load regulation, sourcing	Load step from minimum to maximum operating current, di/dt = 3mA/us, All lines. Guaranteed by design	-2		+2	%	VTREF
$dV_{VTREF\_LOAD\_SOURCE}$	Transient load regulation, sinking	Load step from minimum to maximum operating current, di/dt = 3mA/us, All lines. Guaranteed by design	-1		+1	%	VTREF
dV_{VTREF_LINE}	Transient line regulation	Line step on V5V from minimum to maximum operating voltage, dV/dt = 1V/us, All loads. Guaranteed by design	-1		+1	%	VTREF
$T_{VTREF\_SOFT\_START}$	Soft start timing	From 10% to 90% of $V_{VTREF,}$ Guaranteed by design			450	µs	VTREF
$PSRR_{VTREF}$	Power Supply Rejection Ratio	V_{NOISE} = 10mV_{pp} on $V_{V5V,}$ f_{NOISE} = 400kHz, Guaranteed by design	60			dB	VTREF
VVTREF_UV_TH	VTREF UV threshold		2.56	2.73	2.89	V	VTREF
$V_{VTREF\_UV\_HYS}$	VTREF UV threshold hysteresis		22		42	mV	VTREF
$T_{VTREF\_UV\_FIL}$	VTREF UV filter time		17	20	23	µs	VTREF
$V_{VTREF\_OV\_TH}$	VTREF OV threshold		3.48	3.71	3.93	V	VTREF

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{VTREF\_OV\_HYS}$	VTREF OV threshold hysteresis		25		60	mV	VTREF
$T_{VTREF\_OV\_FIL}$	VTREF OV filter time		17	20	23	µs	VTREF

5.3.7 Digital output buffer supply (VIO)

This supply input is used to bias the output stage of the GPIOx pins. It can be connected to either 5V or 3.3V. The 5V LDO (V5V) can be used for supplying VIO to 5V level. Optionally, an external 3.3V supply can be provided. Device 3V3 LDOs are not suitable for supplying VIO.

5.4 Oscillators

This section describes the device oscillators.

5.4.1 Low frequency standby oscillator (OSCI_STBY)

The low frequency standby oscillator operates at f_{STBY_OSC} and is active when the device is in NORMAL, STANDBY and CYCLIC WAKEUP states.

5.4.1.1 Electrical parameters

Table 17. Standby oscillator electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
f_{STBY_OSC}	Oscillator frequency		460	500	540	kHz	

5.4.2 High frequency main oscillator (OSCI_MAIN)

The high frequency main oscillator operating at f_{MAIN_OSC} and active only in NORMAL and CYCLIC WAKEUP states.

Outside the oscillator's frequency operating range, the power up and down transitions and related timing may be affected. A frequency drift can be detected by the oscillator monitor as described in the dedicated section.

5.4.2.1 Electrical parameters

Table 18. Main oscillator electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
f_{MAIN_OSC}	Oscillator frequency		15.04	16	16.96	MHz	

5.4.3 Oscillator monitor

When in NORMAL or CYCLIC WAKEUP, the main and standby oscillators are monitoring each other. In case of frequency drift detection, the OSC_FAIL flag is set (cleared upon read).

In case either of the two oscillators is stuck, POR_SLEEP_N and POR_MAIN_N are asserted. So, all the device configurations are restored to their default value and POR_SLEEP_ASSERTED and POR_MAIN_ASSERTED flags are set. MCU may attempt a retry performing the wakeup sequence. The oscillator stuck fault is detected within TOSCI_STUCK_TIMEOUT time.

The oscillator monitor is BISTed at each wakeup from low power states to NORMAL. In case of failure, the DIAG_STATUS2.CLOCK_MON_SELFTEST_FAIL is set (cleared upon read). This flag has to be checked at least 12 ms after the power-up.

5.4.3.1 *Electrical parameters*

Table 19. **Oscillator monitor electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$f_{OSC\_MON\_ERR}$	Oscillator delta frequency threshold		25		36	%	
$T_{OSCI\_STUCK\_TIMEOUT}$	Oscillator stuck detection timeout			2		ms	

5.5 Ground loss monitor (GNDMON)

To detect failures in grounding, the IC integrates a ground loss monitor. Such diagnostic is available on-demand to cover latent failures. It can be enabled programming GND_LOSS_ENABLE = 1.

5.5.1 Diagnostics

Table 20. **Ground loss monitor diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
AGND/ DGND LOSS	If a differential voltage greater than $V_{GND\_LOSS\_TH}$ arises between AGND and DGND for an interval longer than $T_{GND\_LOSS\_FIL}$, the DIAG_STATUS1. GND_LOSS_FAIL fault is acknowledged	The GND_LOSS_FAIL flag is set	If the differential voltage between AGND and DGND falls below $V_{GND\_LOSS\_TH}$ for an interval longer than $T_{GND\_LOSS\_FIL}$, the GND_LOSS_FAIL can be cleared by MCU	None	GND_LOSS_ENABLE masks diagnostic execution. When disabled, the GND_LOSS_FAIL flag can always be cleared This diagnostic is only active in NORMAL and CYCLIC WAKEUP

5.5.2 Electrical parameters

Table 21. **Ground loss monitor characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{GND\_LOSS\_TH}$	Ground loss detection threshold		100	200	300	mV	AGND, DGND
$T_{GND\_LOSS\_FIL}$	Ground loss detection filter time		240	300	360	us	AGND, DGND

5.6 Current sense ADCs (CSAPx/CSAMx)

The IC features two pairs of CSA pins, implementing a fully differential sensing architecture. Such pairs can be respectively used as follows:

- CSAP0/CSAM0 pair shall be used for sensing the instantaneous pack current. Such ADC is fully synchronized to the L9965/L99BM2 BMIC voltage ADCs.
- CSAP1/CSAM1 pair shall be used for performing Coulomb Counting with a 2nd, independent, ADC.

In order to achieve high ASIL ratings at system level, it is recommended to adopt a dual shunt approach with independent external analog front-end.

CSA pairs can also be connected to the same shunt resistor, but the analog front ends shall still be independent in order to maximize performances.

5.6.1 Common electrical parameters

This section lists common electrical parameters of the CSAs connected to both CSAx pairs.

5.6.1.1 *Electrical parameters*

Table 22. Current sense ADC electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{DIFF_FS}	ADC full scale differential input voltage, CSAP-CSAM	Design info	-125		125	mV	CSAPx, CSAMx
V_{DIFF_OP}	ADC operating differential input voltage, CSAP-CSAM	Design info	-100		100	mV	CSAPx, CSAMx
V_{CSA_CM}	ADC common mode input voltage, (CSAP+CSAM)/2	Design info	-100		100	mV	CSAPx, CSAMx
N_{BIT_CSA}	ADC bit number: encoding is in 2’s complement	Design info		18		bit	CSAPx, CSAMx
V_{CUR_RES}	CSA resolution (LSB)	Design info, effective range [+/- 125mV]		0.95e-6 = $0.25/2^{18}$		V	CSAPx, CSAMx
R_{CSA_DIFF}	CSA input differential impedance	Guaranteed by design	5			MΩ	CSAPx, CSAMx

5.6.2 Instantaneous current measurement ADC (CSAP0/CSAM0)

The IC offers the possibility to acquire pack instantaneous current using the CSA connected to the CSAP0/ CSAM0 pair.

This CSA can be enabled programming CFG_DIAG.CUR_INST_EN = 1 and is available only in NORMAL state.

The trigger is designed to be sensitive to broadcast commands triggering cells conversion on L9965A/L99BM218 (CMD1.SOC = 1 with CMD1.ADC_INST_CONV = 1). The SOC/ADC_INST_CONV fields of L9965C/L99BM2C is placed at the same address and in the same position of the SOC/VOLT_CONV bits in L9965A/L99BM218. This implementation guarantees enhanced synchronization between cell voltage samples acquired by L9965A/ L99BM218 and pack current acquired by L9965C/L99BM2C: both acquisition triggers are only desynchronized by the VIF command latency, which is negligible: less than $T_{DESYNCH\_INST\_CSA\_BMIC}$

The acquisition starts $T_{CUR\_INST\_START}$ after the receival of the trigger command. It lasts $T_{CUR\_INST\_FILTER}$, which is programmable using the CUR_INST_FIL field. Moreover, a third time $T_{CUR\_INST\_CAL}$ is necessary to post-elaborate the conversion data. The total conversion time is:

$T_{curr\_inst\_conv} = T_{CUR\_INST\_START} + T_{CUR\_INST\_FILTER} + T_{CUR\_INST\_CAL}$.

It has been designed to be synchronized with the cell and battery ADCs of L9965A/L99BM218.

Note: *To ensure proper synchronization at system level, the MCU shall apply the same configuration for the filtering windows of L9965A/L99BM218 and L9965C/L99BM2C.*

A new Start of Conversion (SOC) command cannot interrupt or re-start an ongoing conversion, and the command is discarded.

Result of the last instantaneous current acquisition is available in the CUR_INST 18-bit field (register CSA_INST_MEAS), along with the corresponding DIAG_CSA_SC.DATA_READY_CSA_INST bit (clear-on-read), and it is encoded in 2’s complement. Register data is always available in NORMAL, but it is reset once the device moves to any low power state.

5.6.2.1 *Electrical parameters*

Table 23. Instantaneous current measurement electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{CUR\_INST\_START}$	ADC settling time			60(1)		µs	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_000}$	Instantaneous current ADC filter time (field CUR_INST_FIL in register CFG_CSA_INST)	CUR_INST_FIL = 000		136 (1)		µs	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_001}$		CUR_INST_FIL = 001		264 (1)		µs	CSAP0, CSAM0

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{CUR\_INST\_FILTER\_010}$	Instantaneous current ADC filter time (field CUR_INST_FIL in register CFG_CSA_INST)	CUR_INST_FIL = 010		1.04 (1)		ms	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_011}$		CUR_INST_FIL = 011		2.08 (1)		ms	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_100}$		CUR_INST_FIL = 100		4.16 (1)		ms	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_101}$		CUR_INST_FIL = 101		8.32 (1)		ms	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_110}$		CUR_INST_FIL = 110		16.64 (1)		ms	CSAP0, CSAM0
$T_{CUR\_INST\_FILTER\_111}$		CUR_INST_FIL = 111		99.84 (1)		ms	CSAP0, CSAM0
$T_{CUR\_INST\_CAL}$	ADC post-calibration time			27 (1)		µs	CSAP0, CSAM0
$CSA_{INST\_OFFSET\_ERR}$	CSA Offset Error, Including post-soldering and ageing effects(2)	CSAP and CSAM inputs shorted on PCB, with 0V common mode, Guaranteed by test bench characterization	-1		1	LSB	CSAP0, CSAM0
$CSA_{INST\_LOW\_RANGE\_ERR0}$	Total Conversion Error in low range, Including post-soldering and ageing effects(2)	0 mV < |CSAP-CSAM| < 2mV, -40°C ≤ Tamb ≤ +125°C, Guaranteed by test bench characterization	-3		3	LSB	CSAP0, CSAM0
$CSA_{INST\_GAIN\_ERR\_0}$	CSA Gain Error, including nonlinearities, Including post-soldering and ageing effects(2)	2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, -40°C < T_{AMB} < +125°C	-0.1		0.1	%	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_000}$	Standard deviation over a population of 100 samples, T_{AMB}	CUR_INST_FIL = 000		9.9		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_001}$		CUR_INST_FIL = 001		8		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_010}$		CUR_INST_FIL = 010		4.9		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_011}$		CUR_INST_FIL = 011		3.1		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_100}$		CUR_INST_FIL = 100		2.1		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_101}$		CUR_INST_FIL = 101		1.5		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_110}$		CUR_INST_FIL = 110		1		μV_{RMS}	CSAP0, CSAM0
$V_{CSA\_INST\_NOISE\ \_111}$		CUR_INST_FIL = 111		0.5		μV_{RMS}	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_000}$	Current ADC 3dB cutoff frequency. Design info about ideal filter behaviour	CUR_INST_FIL = 000		5405		Hz	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_001}$		CUR_INST_FIL = 001		2784		Hz	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_010}$		CUR_INST_FIL = 010		707		Hz	CSAP0, CSAM0

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$F_{CUT\_INST\_CUR\_FILTER\_011}$	Current ADC 3dB cutoff frequency. Design info about ideal filter behaviour	CUR_INST_FIL = 011		276.9		Hz	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_100}$		CUR_INST_FIL = 100		121		Hz	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_101}$		CUR_INST_FIL = 101		56.7		Hz	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_110}$		CUR_INST_FIL = 110		27.4		Hz	CSAP0, CSAM0
$F_{CUT\_INST\_CUR\_FILTER\_111}$		CUR_INST_FIL = 111		4.4		Hz	CSAP0, CSAM0
$T_{DESYNCH\_INST\_CSA\_BMIC}$	Max. desynchronization between SOC triggers of instantaneous current acquired by L9965C/L99BM2C CSA and instantaneous voltage acquired by the farthest L9965A/ L99BM218 (58th device of the daisy chain). The parameter is including also a 50ns wire propagation delay between each unit.	Application info	-7.2		7.2	µs	CSAP0, CSAM0

1. *parameters affected by clock main uncertainty*
2. *Single samples are characterized by a superimposed gaussian noise, with zero-mean and $V_{CSA\_INST\_NOISE}$ standard deviation*

5.6.3 Coulomb Counting ADC (CSAP1/CSAM1)

The Coulomb Counting operation requires the MCU to track the charge added/subtracted from the battery pack over time. The IC helps tracking the charge variation ΔQ in the battery pack by continuously acquiring and accumulating the current. This significantly reduces the MCU reading rate, simplifying user SW.

The Coulomb Counting function exploits a dedicated, independent ADC operating on CSAP1/CSAM1 pair. To enable it and the related accumulation function, the CFG_FOR_STBY_LOGIC.CC_EN bit must be set. The ADC starts acquiring data after the T_{CC_START} settling time. When Coulomb Counting is active, the CSA1 ADC is enabled and continuously running: a new acquisition starts upon completion of the previous conversion.

Current samples are continuously accumulated in the CUR_CC_MSB and CUR_CC_LSB fields (registers CUR_CC_MSB and CUR_CC_LSB_CNT), while the CUR_CC_LSB_CNT .CC_SAMPLE_CNT counts the number of samples stored in the accumulator.

To prevent temporal incoherence between samples accumulated in the Coulomb Counter registers, the $T_{CUR\_CC\_FILTER}$ setting is sampled upon CC_EN rising edge. Changing $T_{CUR\_CC\_FILTER}$ on the fly is not allowed.

The internal accumulator size N_{SAMPLE_CNT} has been designed to retain data without saturating for an interval lasting at least $(2^{NSAMPLE\_CNT}-1) * (T_{CUR\_CC\_FILTER\_XX} - 2.08ms)$[1]. MCU shall periodically poll the Coulomb Counter to retrieve the charge information, but the accumulator size guarantees very relaxed polling periods: the minimum time interval without saturating the accumulator is in the [17.32-142.27]s range, corresponding respectively to 70ms and 560ms filter options. This helps reducing the amount of data transmitted on the VIF bus, thus also improving current consumption.

The following procedure (Procedure 2: Coulomb Counter readout) shall be followed to ensure proper data synchronization between accumulator and sample counter:

Procedure 2: Coulomb Counter readout

1. MCU reads CUR_CC_MSB register
   a. A snapshot of CUR_CC internal accumulator (LSB part) is loaded into the CUR_CC_LSB field.
   b. A snapshot of internal sample counter is loaded into the CC_SAMPLE_CNT field.
   c. The CUR_CC internal accumulator is cleared.
   d. The internal sample counter is cleared
2. MCU reads the CUR_CC_LSB_CNT register.

Periodical read of the Coulomb Counter can be useful for the following purposes:

- In algorithms relying directly on the CC for determining the SOC
- In algorithms exploiting Kalman filters for tracking the SOC. The periodical read of the CC helps evaluating the average current value, which can be used to adapt the process noise covariance matrix, thus improving the accuracy of the cell model estimators.

Disabling the Coulomb Counter by setting CC_EN = 0 doesn't reset the accumulator. MCU shall follow the readout procedure described above to empty the Coulomb Counter.

The Coulomb Counting routine may refer to a known previous charge $Q(t_0)$ and apply the following equation:

Coulomb Counting algorithm

$$\begin{cases} Q(t_k) = Q_{t0} + \Delta Q = Q_{t0} + \Delta T \sum_{k=1}^{K} I_{CELL}(k) = Q_{t0} + \frac{T_{CUR\_FILTER}}{R_{SHUNT}} \sum_{k=1}^{K} V_{\mathrm{DIFF}}(k) \\ \sum_{k=1}^{K} V_{\mathrm{DIFF}}(k) = CC\_ACC^{*}V_{CUR\_RES} \end{cases} \tag{1}$$

Where:

- V_{DIFF} = CSAP1-CSAM1
- CC_ACC is the accumulator, encoded in 2's complement.
- R_{SHUNT} is the external shunt resistor mounted between CSAP1 and CSAM1

Then, the $Q(t_k)$ just evaluated becomes the $Q(t_0)$ for the next iteration.

The CC_SAT read-only flag reports the status of the sample counter. It saturates when the register holds $2^{NSAMPLE\_CNT}$-1 and a new sample is generated. In such case, the CC_SAT is set to '1'. Meanwhile, the accumulation is stopped and CUR_CC internal accumulator and internal sample counter are frozen.

To obtain the real acquisition window time, the formula is:

CC_SAMPLE_CNT*(CUR_CC_FIL - 2.08ms) (*)

Note: [1] *When CC_EN goes from 0 to 1, only the first sample is acquired after CUR_CC_FIL.*

5.6.3.1 *Electrical parameters*

Table 24. **Coulomb Counter electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
N_{ACC}	Coulomb Counter accumulator size	Design info		26		bit	CSAP1, CSAM1
N_{SAMPLE_CNT}	Coulomb Counter sample counter size	Design Info		8		bit	CSAP1, CSAM1
T_{CC_START}	Coulomb Counter settling time			240 (1)		µs	CSAP1, CSAM1
$T_{CUR\_CC\_FILTER\_00}$	Programmable current Sense sample acquisition time for Coulomb Counter accumulator (2 bit), CUR_CC_FIL field in CFG_FOR_STBY_LOGIC register	CUR_CC_FIL = 00		68.64 (1)		ms	CSAP1, CSAM1
$T_{CUR\_CC\_FILTER\_01}$		CUR_CC_FIL = 01		135.2 (1)		ms	CSAP1, CSAM1
$T_{CUR\_CC\_FILTER\_10}$		CUR_CC_FIL = 10		268.32 (1)		ms	CSAP1, CSAM1
$T_{CUR\_CC\_FILTER\_11}$		CUR_CC_FIL = 11		534.56 (1)		ms	CSAP1, CSAM1

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$CSA_{CC\_OFFSET\_ERR}$	CSA Offset Error, Including post-soldering and aging effects(2).	CSAP and CSAM inputs shorted on PCB, with 0V common mode, Guaranteed by test bench characterization	-1		1	LSB	CSAP1, CSAM1
$CSA_{CC\_LOW\_RANGE\_ERR0}$	Total Conversion Error in low range, Including post-soldering and ageing effects(2).	NORMAL or STANDBY with CC_STBY_CAL_EN = 1, 0 mV < |CSAP-CSAM| < 2mV, -40°C ≤ Tamb ≤ +105°C, Guaranteed by test bench characterization	-3		3	LSB	CSAP1, CSAM1
$CSA_{CC\_LOW\_RANGE\_ERR1}$		NORMAL or STANDBY with CC_STBY_CAL_EN = 1, 0 mV < |CSAP-CSAM| < 2mV, +105°C ≤ Tamb ≤ +125°C, Guaranteed by test bench characterization	-11		11	LSB	CSAP1, CSAM1
$CSA_{CC\_LOW\_RANGE\_ERR2}$		STANDBY, CC_STBY_CAL_EN = 0, 0 mV < |CSAP-CSAM| < 2mV, -40°C < T_{AMB} < +105°C	-7		7	LSB	CSAP1, CSAM1
$CSA_{CC\_LOW\_RANGE\_ERR3}$		STANDBY, CC_STBY_CAL_EN = 0, 0 mV < |CSAP-CSAM| < 2mV, -+105°C < T_{AMB} < +125°C	-16		16	LSB	CSAP1, CSAM1
$CSA_{CC\_GAIN\_ERR\_0}$	CSA Gain Error, including nonlinearities Including post-soldering and ageing effects(2).	NORMAL, 2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, -40°C < T_{AMB} < +105°C	-0.1		0.1	%	CSAP1, CSAM1
$CSA_{CC\_GAIN\_ERR\_1}$		NORMAL, 2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, +105°C < T_{AMB} < +125°C	-0.5		+0.5	%	CSAP1, CSAM1
$CSA_{CC\_GAIN\_ERR\_2}$		STANDBY, CC_STBY_CAL_EN = 0, 2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, -40°C < T_{AMB} < +105°C	-0.3		0.3	%	CSAP1, CSAM1
$CSA_{CC\_GAIN\_ERR\_3}$		STANDBY, CC_STBY_CAL_EN = 1, 2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, -40°C < T_{AMB} < +105°C	-0.1		0.1	%	CSAP1, CSAM1
$CSA_{CC\_GAIN\_ERR\_4}$		STANDBY, CC_STBY_CAL_EN = 1, 2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, +105°C < T_{AMB} < +125°C	-0.5		0.5	%	CSAP1, CSAM1
$CSA_{CC\_GAIN\_ERR\_5}$		STANDBY, CC_STBY_CAL_EN = 0, 2mV < |CSAP-CSAM| < $V_{DIFF\_RANGE\_OP}$, +105°C < T_{AMB} < +125°C	-1		1	%	CSAP1, CSAM1

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{CSA\_CC\_NOISE\_00}$	Standard deviation over a population of 100 samples, T_{AMB}	CUR_CC_FIL = 00		1		μV_{RMS}	CSAP1, CSAM1
$V_{CSA\_CC\_NOISE\_01}$		CUR_CC_FIL = 01		0.7		μV_{RMS}	CSAP1, CSAM1
$V_{CSA\_CC\_NOISE\_10}$		CUR_CC_FIL = 10		0.5		μV_{RMS}	CSAP1, CSAM1
$V_{CSA\_CC\_NOISE\_11}$		CUR_CC_FIL = 11		0.5		μV_{RMS}	CSAP1, CSAM1

1. *parameters affected by clock standby uncertainty*
2. *Single samples are characterized by a superimposed Gaussian noise, with zero-mean and V_{CC_NOISE} standard deviation*

5.6.4 CSA cross-check (X-CHECK)

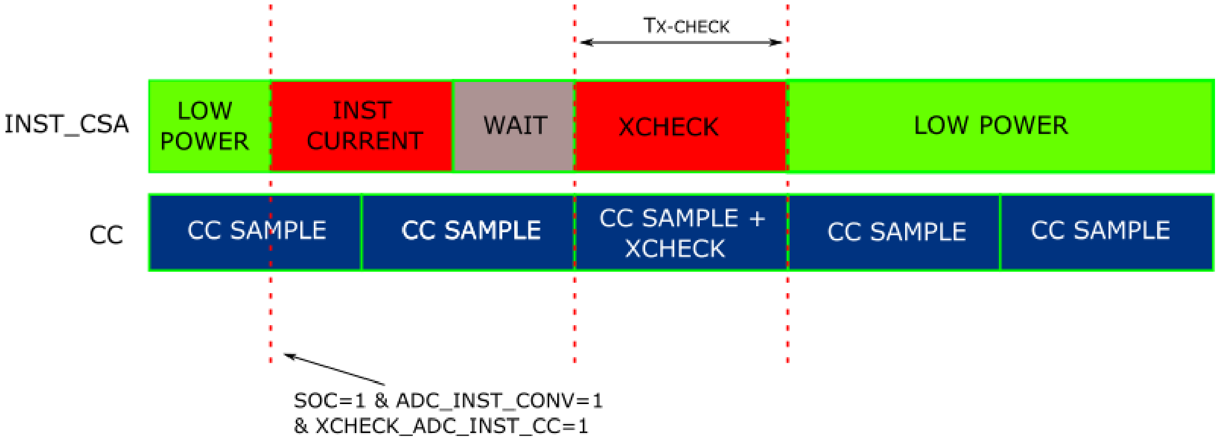
When both the instantaneous current measurement ADC (CSAP0/CSAM0) and the Coulomb Counting ADC (CSAP1/CSAM1) are enabled (CFG_DIAG.CUR_INST_EN = 1 and CFG_FOR_STBY_LOGIC.CC_EN = 1), a real-time cross-check between instantaneous samples can be performed.

- In NORMAL, samples are cross-checked whenever the MCU issues a conversion command featuring CMD1.SOC = 1 and CMD1.XCHECK_ADC_INST_CC = 1 in the same frame
- The x-check is performed automatically upon each transition to CYCLIC WAKEUP.

When only the instantaneous current measurement ADC (CSAP0/CSAM0) is enabled (CFG_DIAG.CUR_INST_EN = 1 and CFG_FOR_STBY_LOGIC.CC_EN = 0), and the MCU issues a command featuring CMD1.SOC = 1, CMD1ADC_INST_CONV = 1 and CMD1.XCHECK_ADC_INST_CC = 1 in the same frame, CSA0 conversion and X-CHECK are not performed.

Performing the x-check does not alter the instantaneous current measurement thread, nor the synchronicity with L9965A/L99BM218 cell voltage measurement. In fact, as shown in Figure 7, the instantaneous current sample is acquired immediately, while the x-check is delayed aligning the instantaneous CSA to the Coulomb Counter running in background.

Figure 7. **CSA & CC X-Check**



The WAIT time duration in Figure 7 can vary between $T_{CUR\_INST\_START}$ and ($T_{CUR\_INST\_FILTER\_010}$ + $T_{CUR\_INST\_START}$).

The x-check conversion lasts $3T_{CUR\_INST\_FILTER\_010}$ (the result is available after the additional time required for the calibration $T_{CUR\_INST\_CAL}$) and follows this strategy:

- If both samples are greater than 2048 LSB, the following condition is checked:

Cross-check condition (high range)

$$\begin{cases} if\left|CUR_{INST_{CSA0}}\right| \geq \left|CUR_{INST_{CC}}\right| = \; = \; > \left|CUR_{INST_{CSA0}} - CUR_{INST_{CC}}\right| \leq \dfrac{\left|CUR_{INST_{CSA0}}\right|}{X_{CHECK_{HIGH_{TH}}}} \\ if\left|CUR_{INST_{CSA0}}\right| < \left|CUR_{INST_{CC}}\right| = \; = \; > \left|CUR_{INST_{CSA0}} - CUR_{INST_{CC}}\right| \leq \dfrac{\left|CUR_{INST_{CC}}\right|}{X_{CHECK_{HIGH_{TH}}}} \end{cases} \tag{2}$$

- If the absolute value of at least one sample is less or equal than 2048 LSB, the following condition is checked:

Cross-check condition (low range)

$$\left|CUR_{INST_{CSA0}} - CUR_{INST_{CC}}\right| \leq X_{CHECK_{LOW_{TH}}} \tag{3}$$

To confirm the diagnostic execution, the DIAG_STATUS2.XCHECK_ADC_INST_CC_END latch (cleared upon read) is set when the check is over. In case one of the conditions above is not verified, the DIAG_STATUS2.XCHECK_ADC_INST_CC_FAIL latch is set (cleared upon read).

It is possible to verify the integrity of cross-check circuit requiring a self-test procedure, by setting the field CMD2.XCHECK_CSA_SELFTEST=1 (write only command). When the routine is accomplished, the flag DIAG_STATUS2.XCHECK_CSA_SELFTEST_END is asserted, and the check result is available on the bit DIAG_STATUS2.XCHECK_CSA_SELFTEST_FAIL (both clear-on-read).

During the self-test all the functional flags related to cross-check are not masked; they shall be cleared at the end of the routine.

During the cross-check execution, CC_EN and CUR_INST_EN settings must not be modified.

5.6.4.1 *Electrical parameters*

Table 25. **X-Check electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$X_{CHECK\_LOW\_TH\_00}$	Programmable x-check threshold for low range (2 bit) – XCHECK_LOW_TH 2-bit field in CFG_DIAG register	XCHECK_LOW_TH = 00 (default)		40		LSB	CSAP1, CSAM1, CSAP0, CSAM0
$X_{CHECK\_LOW\_TH\_01}$		XCHECK_LOW_TH = 01		70		LSB	CSAP1, CSAM1, CSAP0, CSAM0
$X_{CHECK\_LOW\_TH\_10}$		XCHECK_LOW_TH = 10		100		LSB	CSAP1, CSAM1, CSAP0, CSAM0
$X_{CHECK\_LOW\_TH\_11}$		XCHECK_LOW_TH = 11		255		LSB	CSAP1, CSAM1, CSAP0, CSAM0
$X_{CHECK\_HIGH\_TH\_00}$	Programmable x-check threshold for high range (2 bit) – XCHECK_HIGH_TH 2-bit field in CFG_DIAG register	XCHECK_HIGH_TH = 00		16			CSAP1, CSAM1, CSAP0, CSAM0
$X_{CHECK\_HIGH\_TH\_01}$		XCHECK_HIGH_TH = 01 (default)		32			CSAP1, CSAM1, CSAP0, CSAM0

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$X_{CHECK\_HIGH\_TH\_10}$	Programmable x-check threshold for high range (2 bit) – XCHECK_HIGH_TH 2-bit field in CFG_DIAG register	XCHECK_HIGH_TH = 10		64			CSAP1, CSAM1, CSAP0, CSAM0
$X_{CHECK\_HIGH\_TH\_11}$		XCHECK_HIGH_TH = 11		8			CSAP1, CSAM1, CSAP0, CSAM0

5.6.5 Overcurrent detection (OVC)

The IC can protect the battery pack from overcurrent events due to overload conditions in both charge and discharge directions.

Each current sample continuously acquired by the Coulomb Counting and each instantaneous current sample acquired via Instantaneous Current Measurement are compared to programmable digital thresholds:

- CSA_OVC_TH.OVC_DCHG_TH (8-bit) sets the overcurrent threshold in discharge.
- CSA_OVC_TH.OVC_CHG_TH (8-bit) sets the overcurrent threshold in charge.

If either of the two CSA detects an overcurrent condition, the corresponding OVC_CHG_x and OVC_DCHG_x flags are set (DIAG_CSA_SC register).

The MCU is supposed to intervene and take appropriate reaction. Such diagnostic is not intended to trigger a pyro-fuse shot via the FAULTx lines, since the current to be eventually interrupted lies within the safety range of the mechanical relays and it is not expected to rise indefinitely like in short-circuit events.

To avoid false detections, overcurrent thresholds must only be modified while CFG_DIAG.OVC_EN = 0 and CFG_FOR_STBY_LOGIC.CC_EN = 0.

This diagnostic can be enabled via OVC_EN bit and covers the failures listed in Table 26.

5.6.5.1 Diagnostics

Table 26. Overcurrent diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Overcurrent in Charge (Instantaneous CSA)	If (CSAP0 - CSAM0) < $V_{OVC\_CHG\_TH}$ the OVC_CHG_0 fault is acknowledged	DIAG_CSA_SC.OVC_CHG_0 flag is set	If (CSAP0 - CSAM0) > $V_{OVC\_CHG\_TH}$, OVC_CHG_0 flag can be cleared by MCU	None	CUR_INST_EN masks measurement execution for CSA0. When disabled, the OVC_CHG_0 flag can always be cleared. OVC_EN masks diagnostic execution. When disabled, the OVC_CHG_0 flag can always be cleared. This diagnostic is available only in NORMAL
Overcurrent in Discharge (Instantaneous CSA)	If (CSAP0 – CSAM0) > $V_{OVC\_DCHG\_TH}$, the OVC_DCHG_0 fault is acknowledged	DIAG_CSA_SC.OVC_DCHG_0 flag is set	If (CSAP0 – CSAM0) < $V_{OVC\_DCHG\_TH}$, the OVC_DCHG_0 flag can be cleared by MCU	None	CUR_INST_EN masks measurement execution for CSA0. When disabled, the OVC_DCHG_0 flag can always be cleared.

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
					OVC_EN masks diagnostic execution. When disabled, the OVC_DCHG_0 flag can always be cleared. This diagnostic is available only in NORMAL
Overcurrent in Charge (CC)	If (CSAP1 – CSAM1) < $V_{OVC\_CHG\_TH}$ the OVC_CHG_1 fault is acknowledged	DIAG_CSA_SC.OVC_CHG_1 flag is set	If (CSAP1 – CSAM1) > $V_{OVC\_CHG\_TH}$, the OVC_CHG_1 flag can be cleared by MCU	None	CC_EN masks measurement execution for CSA1. When disabled, the OVC_CHG_1 flag can always be cleared. OVC_EN masks diagnostic execution. When disabled, the OVC_CHG_1 flag can always be cleared. This diagnostic is available only in NORMAL
Overcurrent in Discharge (CC)	If (CSAP1 – CSAM1) > $V_{OVC\_DCHG\_TH}$, the OVC_DCHG_0 fault is acknowledged	DIAG_CSA_SC.OVC_DCHG_1 flag is set	If (CSAP1 – CSAM1) < $V_{OVC\_DCHG\_TH}$, the OVC_DCHG_1 flag can be cleared by MCU	None	CC_EN masks measurement execution for CSA1. When disabled, the OVC_DCHG_1 flag can always be cleared. OVC_EN masks diagnostic execution. When disabled, the OVC_DCHG_1 flag can always be cleared. This diagnostic is available only in NORMAL

5.6.5.2 *Electrical parameters*

Table 27. Overcurrent electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{OVC\_CHG\_TH}$	Programmable Overcurrent in Charge threshold (8 bit); $V_{OVC_{CHG_{TH}}} = -512V_{CUR\_RES}*CODE$		-125		0	mV	CSAPx, CSAMx
$V_{OVC\_DCHG\_TH}$	Programmable Overcurrent in Discharge threshold (8 bit); $V_{OVC_{DCHG_{TH}}} = 512V_{CUR\_RES}*CODE$		0		125	mV	CSAPx, CSAMx

5.6.6 Charge/discharge detection wakeup (CC_WUP)

L9965C/L99BM2C is able to monitor pack current while in STANDBY state, in order to detect leakage conditions in both charge and discharge directions. This diagnostic is not available in other FSM states.

This feature can be activated having the Coulomb Counter enabled (CC_EN = 1) and setting CFG_FOR_STBY_LOGIC.CC_STBY_EN = 1. A Communication Timeout or Go To Sleep command then moves the device to STANDBY.

When L9965C/L99BM2C moves to STANDBY from NORMAL/CYCLIC WAKEUP:

- the Coulomb Counter accumulator (CUR_CC internal accumulator) and internal sample counter are reset and disabled (regardless of CC_EN and CC_STBY_EN bit) to start from a zero-charge initial condition.
- A T_{CC_BLANK} blanking timer is started during which the CC ADC is disabled.
- Once T_{CC_BLANK} expires, the CC ADC is re-enabled. The transition to STANDBY is over.

While in STANDBY:

- The Coulomb Counter accumulator (CUR_CC internal accumulator) and internal sample counter are kept under reset.
- The CC ADC continuously monitors its shunt (after the settling time TCC_START), converting the CSAP1/CSAM1 pair with the programmed $T_{CUR\_CC\_FILTER\_XX}$ filter.
- The conversion result is compared to the $V_{CC\_WAKEUP\_TH}$ threshold: if higher, a leakage is detected. The diagnostic covers both charge/discharge leakage as the check is performed on the absolute value of the signal. Leakage detection leads to self-wakeup in NORMAL state for FAULT notification.

When L9965C/L99BM2C moves from STDBY/SLEEP to NORMAL:

- The CC ADC is disabled till the device complete the transition to NORMAL state.
- At this point, if CC_EN = 1, the CC ADC is re-enabled along with the Coulomb Counter accumulator (CUR_CC internal accumulator) and internal sample counter.
- The transition to NORMAL is over. The leakage diagnostic is disabled.

When L9965C/L99BM2C moves from CYCLIC WAKEUP to NORMAL:

- No T_{CC_BLANK} blanking timer is applied. If CC_EN = 1, at the end of the cyclic procedure, the CC ADC is kept enabled along with the Coulomb Counter accumulator (CUR_CC internal accumulator) and internal sample counter.

To guarantee the integrity of the diagnostic functions in STANDBY, the IC shall be periodically moved to CYCLIC WAKEUP. This is achieved programming a suitable cyclic wakeup interval in the L9965T/L99BM2T transceiver. The periodicity of the cyclic wakeup shall be consistently higher than $T_{CC\_BLANK} + T_{CUR\_CC\_FILTER\_XX} + T_{CYCLIC\_ROUTINE\_DURATION}$, to guarantee that the device holds the STANDBY state for enough time to acquire at least one current sample. Otherwise, the diagnostic is not performed correctly as no current sample is processed.

When L9965C/L99BM2C moves to CYCLIC WAKEUP:

- The CC ADC is disabled and then enabled according to the CYCLIC WAKEUP routine timing. During the Open load diagnostic it is disabled, then it is enabled if CC_EN = 1 so to allow the x-check versus the instantaneous ADC.

This diagnostic covers the failures listed in Table 28.

5.6.6.1 *Diagnostics*

Table 28. **Charge/discharge wakeup monitor diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Charge/ Discharge detection	If $\|V_{CSAP1}-V_{CSAM1}\|$ reaches, or it is higher than $V_{CC\_WAKEUP\_TH}$, an excessive charge/ discharge condition is detected	The DIAG_STATUS_STBY.CC_WUP flag is set. The IC moves to NORMAL and sends a FAULT/WAKEUP frame	Once in NORMAL, the CC_WUP flag can be cleared by MCU	None	CC_EN masks diagnostic execution. When disabled, the CC_WUP flag can always be cleared. CC_STBY_EN masks diagnostic execution. When disabled, the CC_WUP flag can always be cleared

5.6.6.2 *Electrical parameters*

Table 29. Charge/discharge detection electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{CC\_WAKEUP\_TH}$	Coulomb Counter wakeup threshold (8 bit), $V_{CC_{WAKEUP_{TH}}} = V_{\mathrm{CUR\_}RES} * CODE$		0		255	LSB	CSAP1, CSAM1
T_{CC_BLANK}	CC ADC blanking time duration		0.8	1	1.2	ms	CSAP1, CSAM1

5.6.7 CSA_CC circuits redundancy for safety

For the compliance to safety requirements, CSA_CC filter block is made redundant. At this purpose, the microcontroller is expected to verify the coherence check results.

An integrity check is implemented, based on digital filter outputs matching verification. In NORMAL mode the check is automatically started as soon as CSA1 is enabled, and it is continuously running. The result is provided via SPI/VIF with DIAG_STATUS_STBY.XCHECK_CC_DATA_VALID_FAIL and DIAG_STATUS_STBY.XCHECK_CC_DATA_FAIL flags. Same applies to STANDBY state, where CSA1 is all time enabled. These flags are, however, masked if the Coulomb Counter ADC is not used. This avoids unwanted FSM transitions (i.e., from CYCLIC WAKEUP to NORMAL), when the Coulomb Counter is never used.

Moreover, in STANDBY, the self-wake-up detection circuit receives both digital filter outputs, that are expected to be fully equivalent in case no hardware failure is present. Self-wake-up is triggered when at least one of the two digital filter outputs is above detection threshold. In addition, in case a self-wake-up is triggered by an incoherent redundant logic decision, warning is given with DIAG_STATUS_STBY.XCHECK_PLS_WAKEUP_FAIL. The external MCU, in case of wake-up due to Charge-Discharge detection, shall verify the circuit integrity reading this flag.

5.7 Short-circuit detection

The L9965C/L99BM2C protects the battery pack from dangerous short-circuit conditions by sensing the voltage across external shunt resistors and operating with a fast detection time T_{SC_DET}.

Detection thresholds can be set programming the SC_TH_SEL 8-bit field in SC_SET_CFG register, and the programmed values are common to both current senses.

The programmability range is 20 – 200 LSB, corresponding to thresholds values in the range 25 – 250 mV. The device performances in terms of accuracy are not guaranteed if the thresholds values are programmed outside this range.

This diagnostic is enabled using SC<x>_EN bit and covers the failures listed in Table 30. When disabled, FAULTx outputs are put in HiZ and all related diagnostic and functions are not available.

Connections of the SC<x> diagnostics to the FAULT<x> lines are hard-wired:

- Short-circuit faults detected by the SC0 diagnostic are redirected on FAULT0 pin. The FAULT0 output is put in HiZ in case CFG_DIAG.SC0_EN = 0. An external pullup/pulldown resistor is needed to define the inactive state, which shall correspond to the “no fault” state in order to avoid inadvertent pyro-fuse fire in case of pin loss.
- Short-circuit faults detected by the SC1 diagnostic are redirected on FAULT1 pin. The FAULT1 output is put in HiZ in case CFG_DIAG.SC1_EN = 0. An external pullup/pulldown resistor is needed to define the inactive state, which shall correspond to the “no fault” state in order to avoid inadvertent pyro-fuse fire in case of pin loss.

Note: The L9965C/L99BM2C companion pyrodriver already embeds pullup/pulldown resistors on its trigger inputs.

When enabled, the SC detection is available only in NORMAL state, while it is disabled in other operating states.

Propagation delay from diagnostic assertion to FAULT<x> assertion is T_{SC_REACT} (in case of PWM-based encoding, however, latencies related to cycle completion shall be also considered, see also Figure 8).To avoid false detections, short-circuit thresholds shall only be modified while SC<x>_EN = 0.

5.7.1 FAULT signaling mode (FAULTx_MODE)

FAULTx outputs are only available in NORMAL state and can be configured to encode the fault status in different modes:

- FAULT_CFG.FAULT<x>_MODE = 0 sets the level-based encoding
  - Such a strategy enables ultralow current consumption in low-power strategies. This is the default configuration every time the device enters in NORMAL state.
- FAULT_CFG.FAULT<x>_MODE = 1 sets the PWM-based encoding.
  - The PWM-based encoding allows the L9965P/L99BM2P companion chip to continuously monitor the status of FAULTx lines, being capable of detecting stuck-at faults in real-time.

The FAULTx failure state can also be configured:

- FAULT<x>_LEVEL = 0 sets the failure state to low level or dc_{FAULT_LOW} duty cycle
- FAULT<x>_LEVEL = 1 sets the failure state to high level or dc_{FAULT_HIGH} duty cycle

To be robust against common cause failures, it is recommended to apply complementary failure states to FAULT0 and FAULT1.

Note: L9965P/L99BM2P companion pyrodriver inputs can be configured to be sensitive to any FAULT signaling mode and level.

Table 30 summarizes FAULTx output behavior according to the device state and different configurations.

Table 30. **FAULTx output behavior**

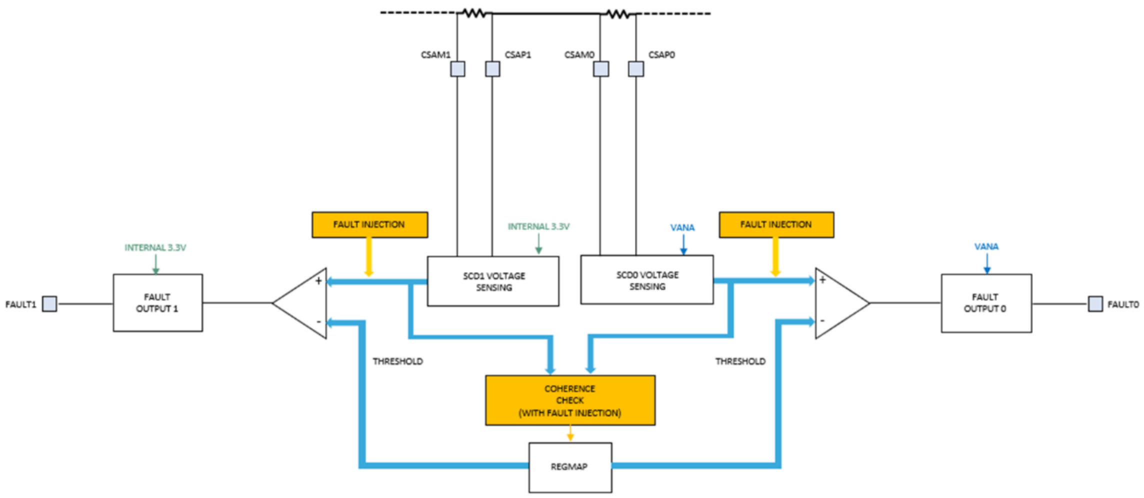
SC<x>_EN	FAULT<x>_MODE	FAULT<x>_LEVEL	Short-Circuit Fault	FAULTx
0	X	X	X	HiZ
1	0	0	No	High
1	0	0	Yes	Low
1	0	1	No	Low
1	0	1	Yes	High
1	1	0	No	75% duty
1	1	0	Yes	25% duty
1	1	1	No	25% duty
1	1	1	Yes	75% duty

5.7.2 Short-circuit fault injection (SC_ARM/SC_INJECT)

To comply with the latest ISO26262 requirements, two safety mechanisms are introduced (see also Figure 8):

- L9965C/L99BM2C implements fault injection from the input of Short-Circuit detection down to FAULTx outputs (available only with the level-based encoding, with only one input at the time - SC_ARM and SC_INJECT bits of CMD2 functional register);
- The coverage of the remaining path, from shunts to detection stages, is assured by the coherence check of shunt voltage sensing, based on the assumption that, in absence of hardware failure, the two measurements must be equivalent. The result of this cross-check is available on the flag DIAG_STATUS2.XCHECK_SC_CONV_FAIL. In addition, this cross-check feature can also be fault-injected (XCHECK_SC_CONV_FAULT_INJ bit of the CMD2 functional register).

Figure 8. **Fault injection principle**



To perform a Fault Injection the following steps (Procedure 3: Short-circuit fault injection) must be followed.

Procedure 3: Short-circuit fault injection

1. The MCU writes CMD2.SC_ARM=1 to arm the fault circuit injection trigger. At this point the time T_SC_INJECT_TIMEOUT is started.
2. The MCU can write into CMD2.SC_INJECT field to perform the injection on one of the two paths. The only admitted codes are 01 and 10 for injecting, respectively, the fault on SC0 and SC1 (00 and 11 are not admitted).
3. The MCU writes CMD2.SC_ARM=0 to end the fault injection. The injection must, in any cases, to be concluded before T_SC_INJECT_TIMEOUT expires; otherwise, it is ended by the timeout, and SC_ARM is reset to 0.

To prevent inadvertent pyrofuse deployment, it is not possible to inject faults simultaneously on the two SC paths. They need to be tested separately.

The manual fault injection procedure is recommended in the following application scenarios:

- When L9965C/L99BM2C is not paired to the L9965P/L99BM2P pyrofuse driver.
- In case the fault signaling mode is configured to PWM, the integrity of the SC diagnostic can be tested at powerup executing the manual fault injection procedure.

If FAULTx outputs are configured in level-mode, a real-time BIST can be performed setting FAULT<x>_CYCLIC_BIST = 1 (register FAULT_CFG). In such case, any on-demand BIST request is discarded.

5.7.3 Diagnostics

Table 31. **Short circuit in discharge diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Short Circuit in Discharge	If the (CSAPx – CSAMx) voltage raises above V_{SC_TH} for longer than T_{SC_DET}, the SC<x>_DCHG fault is acknowledged.	The DIAG_CSA_SC.SC<x>_DCHG flag is set The corresponding FAULTx line is asserted	If the CSAPx – CSAMx voltage falls below V_{SC_TH} for longer than T_{SC_DET}, the SC_DCHG flag can be cleared by MCU	FAULTx lines are released	SC<x>_EN masks diagnostic execution. When disabled, the SC<x>_DCHG flag can always be cleared SC<x>_FAULT_MSK masks reaction on the corresponding FAULTx line

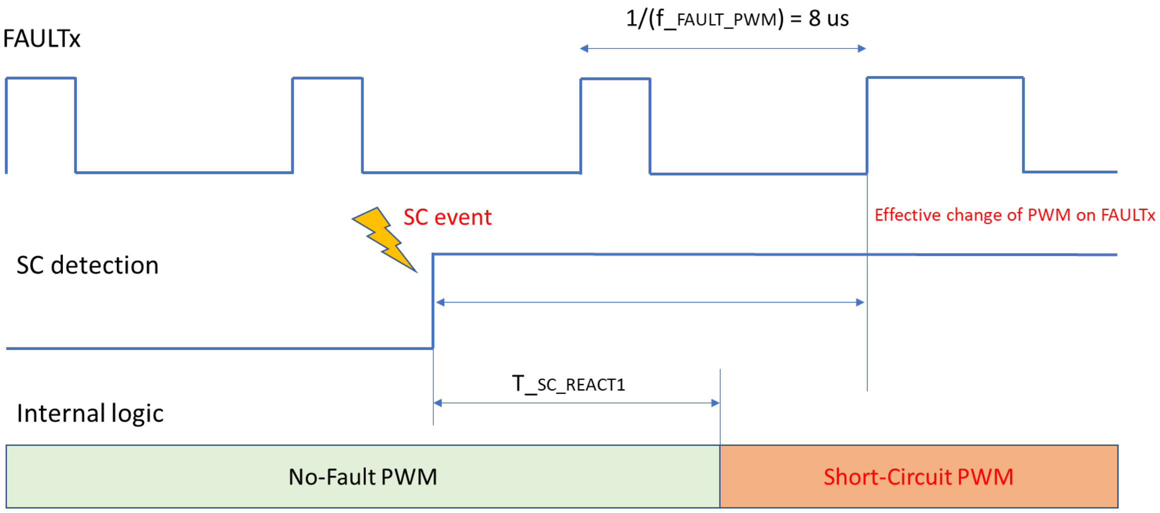
5.7.4 Electrical parameters

Table 32. Short-circuit diagnostic electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{SC_TH}	Short circuit threshold	The threshold value is calculated from SC_TH_SEL 8-bit field: V_{SC_TH} = VSC_TH_SEL * 1LSB, with 1LSB= 1.25 mV	25		250	mV	CSAPx, CSAMx
$V_{SC\_CM\_RANGE}$	Short-circuit diagnostic common mode input range, (CSAP+CSAM)/2	Design info	0		580	mV	CSAPx, CSAMx
dV_{SCD_IN}	Short-circuit detection, operating differential input range		0		250	mV	
T_{SC_DET}	Short-circuit diagnostic detection time	Voltage rising/falling with dV/dt = 250mV/ms on CSA pins			135	µs	CSAPx, CSAMx
$T_{SC\_INJECT\_TIMEOUT}$	Short-circuit injection timeout		81		127	ms	CSAPx, CSAMx
$T_{SC\_REACT\_0}$	Short-circuit reaction fault pin time	FAULT<x>_MODE = 0. From SC detection to FAULTx = 90% of final value, Pin loaded with 200pF			10	µs	CSAPx, CSAMx, FAULTx
$T_{SC\_REACT\_1}$		FAULT<x>_MODE = 1; (1); pin loaded with 200pF			10	µs	CSAPx, CSAMx, FAULTx
f_{FAULT_PWM}	Frequency of the PWM-encoded FAULTx output		-6%	125	+6%	kHz	FAULTx
dc_{FAULT_LOW}	FAULTx Low Duty-cycle in PWM-Encoded mode		5	25	45	%	FAULTx
dc_{FAULT_HIGH}	FAULTx High Duty-cycle in PWM-Encoded mode		55	75	95	%	FAULTx
V_{FAULT_LOW}	FAULTx Low logic level	I_{SINK} = 2mA			0.4	V	FAULTx
V_{FAULT_HIGH}	FAULTx High logic level	I_{SOURCE} = 2mA	2.4			V	FAULTx
$CODE_{ERR\_OS\_SCD}$	Short-circuit detection, total conversion threshold error, on all range		-6		6	LSB	

1. *In case of PWM encoding, the time from SC detection and the effective commutation to failure state duty cycle on FAULTx output could be longer than $T_{SC\_REACT\_1}$ because the last cycle codifying no-fault condition is entirely executed. See also Figure 9.*

Figure 9. **Short-circuit reaction time with FAULTx_MODE=1**



5.8 Interfacing with L9965P/L99BM2P pyrofuse driver

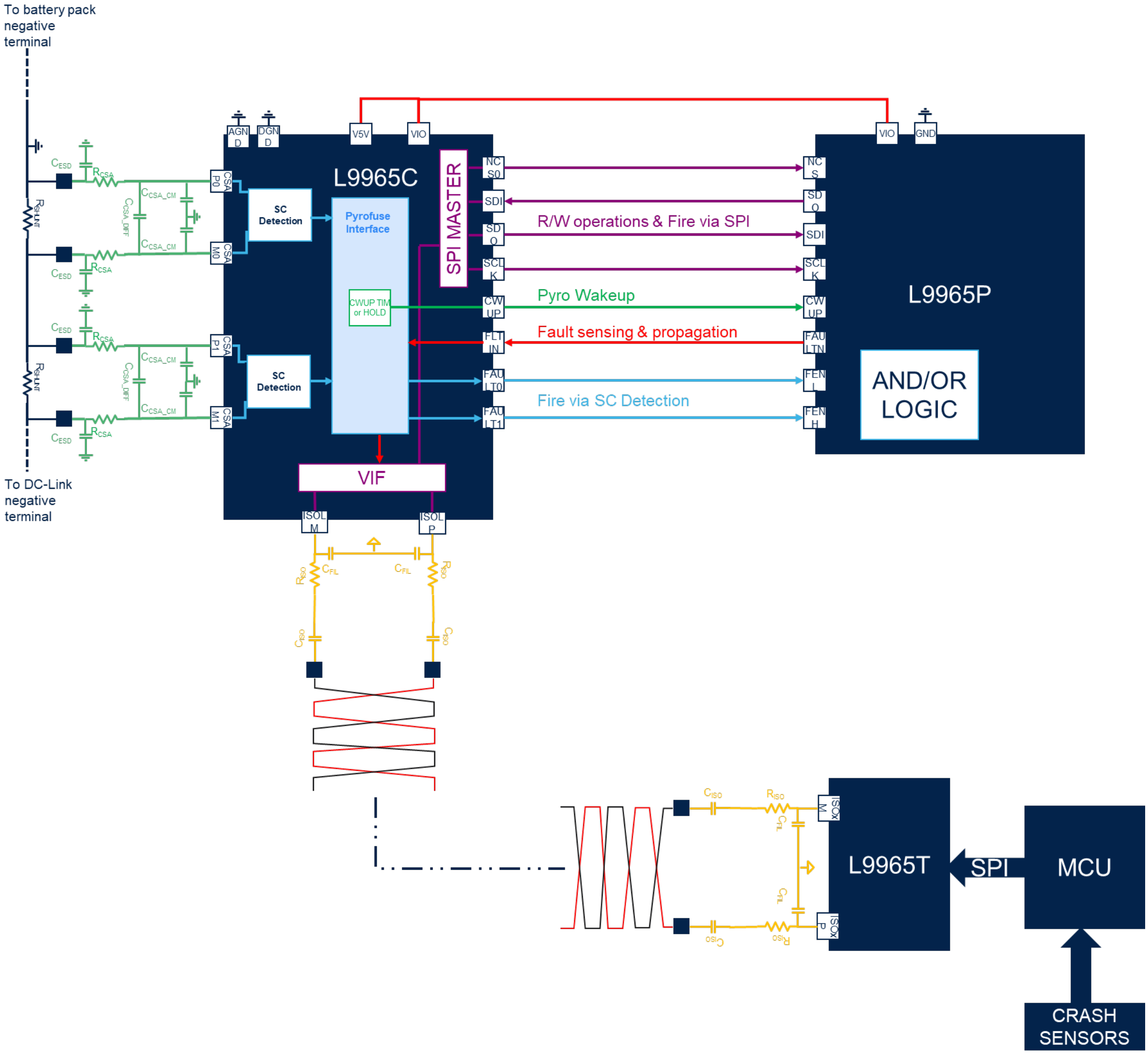
This section explains how the L9965C/L99BM2C can be interfaced with the L9965P/L99BM2P companion pyrofuse driver in order to maximize system performances and flexibility.

In the reference design shown in Figure 10, it is recommended to place the L9965C/L99BM2C and L9965P/L99BM2P on the same PCB, both grounded to the battery pack negative terminal. This ensures all interface pins are local to the ECU, which gives two main advantages:

- Minimizes reaction time to short-circuit: fault detection, propagation and reaction (deployment) all happens locally.
- Minimizes the residual FIT rate, as the occurrence of open/short failure on global lines is excluded by design.

It is recommended to supply both VIOs with 5V LDO (V5V)

Figure 10. **Interfacing L9965C/L99BM2C to L9965P/L99BM2P**



5.8.1 Communication interface

The L9965C/L99BM2C allows communicating with L9965P/L99BM2P via the SPI Controller peripheral. The MCU can access L9965P/L99BM2P using the Isolated Vertical Interface (VIF) and L9965C/L99BM2C as a bridge.

The SPI Controller can be used for:

- Performing L9965P/L99BM2P initialization and configuration.
- Performing periodic R/W operations needed for diagnostic purposes.
- Performing pyro-fuse deployment in case of crash or manual service disconnect.

Note: *Interfacing the L9965C/L99BM2C with an external EEPROM is still possible using a separate chip select pin (NCS1). The NCS1 pin can also be used for interfacing the L9965C/L99BM2C to a second L9965P/L99BM2P in applications requiring redundancy for safety and/or fail-operational purposes.*

5.8.2 Cyclic wakeup output (CWUP)

To manage L9965P/L99BM2P state transitions and put in place different power management strategies, L9965C/L99BM2C has been equipped with the CWUP output (active high).

To enable it, the GPIO6_SCL_CWUP shall be configured as CWUP programming CWUP_CFG.CWUP_EN = 1. When the L9965C/L99BM2C moves to a low-power state, the CWUP configuration is reset to its default and the output is left HiZ.

5.8.2.1 *Power management strategies*

Two power management strategies are available, as described in Table 33.

Table 33. **L9965P/L99BM2P power management strategies**

Power management strategy	L9965C/ L99BM2C State	L9965P/ L99BM2P State	CWUP Output	Configuration	Note
Full Power	NORMAL	NORMAL	Static high	CWUP_CFG.CWUP_EN = 1 CWUP_CFG.CWUP_HOLD = 1	This enables the quickest FTTI in critical applications, at a higher power consumption.
Low Power	NORMAL	CYCLIC WAKEUP (alternation between DEEP SLEEP and DIAG)	Pulse generation every T_{CWUP_PERIOD}	CWUP_CFG.CWUP_EN = 1 CWUP_CFG.CWUP_HOLD = 0 CWUP_CFG.CWUP_TIM_EN = 1 CWUP_CFG.TIM_TH_SEL = X	This enables optimized energy management while still guaranteeing a quick FTTI, compatible with most applications

The full power settings have higher priority than low-power ones: if CWUP_HOLD = 1, the CWUP output will be held high regardless of the CWUP timer running in background (CWUP_TIM_EN = 1). To put in place the low-power strategy, CWUP_HOLD shall be set low.

The system FTTI can be predicted using the following equations, accounting for all the delays involved between detection and deployment completion:

Estimation of FTTI for short-circuit detection & reaction

$$\begin{cases} T_{FTTI_{LOW_{POWER}}} = T_{SC_{FILTER}} + T_{SC_{REACT_x}} + T_{FENx_{FIL_{ANA}}} + T_{SELF_{WAKEUP_{L9965P}}} + T_{FENx_{DEGLITCH}} + T_{DEPLOY_{REACT}} + T_{DEPLOY_{PROFILE}} \\ T_{FTTI_{FULL_{POWER}}} = T_{SC_{FILTER}} + T_{SC_{REACT_x}} + T_{FENH_{DEGLITCH}} + T_{DEPLOY_{REACT}} + T_{DEPLOY_{PROFILE}} \end{cases} \quad (4)$$

Note: *Some timing parameters belong to L9965P/L99BM2P (refer to L9965P/L99BM2P DS). $T_{DEPLOY\_PROFILE}$ depends on the chosen pyrofuse.*

Typical FTTIs are ~650us in full-power strategy and ~1ms in low-power mode.

Unless the system requires a very aggressive FTTI the low-power strategy is usually the recommended one. Such strategy is based on the energy optimization paradigm which drives the whole L9965x chipset.

The L9965C/L99BM2C and L9965P/L99BM2P sensing and deployment chains spend most of their lifetime in idle state, but the integrity shall be cyclically checked in order to ensure readiness and functionality upon a short-circuit event.

Since the cyclic wakeup period may change during vehicle lifetime, all the CWUP related settings are not stored in the NVM. This enables MCU fine-tuning the power management strategy in order to implement a right trade-off between FTTI and energy efficiency.

5.8.2.2 *Electrical parameters*

Table 34. **CWUP electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{CWUP\_ON\_PULSE}$	Cyclic wakeup high pulse duration		90	100	125	µs	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_000}$	Cyclic wakeup pulse periodicity in NORMAL – TIM_TH_SEL, 3-bit field in CWUP_CFG_TIM_TH register	TIM_TH_SEL = 000	58		73	ms	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_001}$		TIM_TH_SEL = 001	117		145	ms	GPIO6_SCL_CWUP

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{CWUP\_PERIOD\_010}$	Cyclic wakeup pulse periodicity in NORMAL – TIM_TH_SEL, 3-bit field in CWUP_CFG_TIM_TH register	TIM_TH_SEL = 010	176		217	ms	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_011}$		TIM_TH_SEL = 011	294		361	ms	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_100}$		TIM_TH_SEL = 100	412		505	ms	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_101}$		TIM_TH_SEL = 101	530		649	ms	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_110}$		TIM_TH_SEL = 110	648		793	ms	GPIO6_SCL_CWUP
$T_{CWUP\_PERIOD\_111}$		TIM_TH_SEL = 111	766		938	ms	GPIO6_SCL_CWUP

5.8.3 Fault Input (FLTIN)

L9965P/L99BM2P features an open-drain FAULT output used for signaling faulty events to the controller. Up to two L9965P/L99BM2P can be connected in parallel and managed by L9965C/L99BM2C companion controller. In such case, all the L9965P/L99BM2P FAULT outputs can be joined together to form a wired-or fault line.

The L9965C/L99BM2C implements an active-low fault input (FLTIN) capable of decoding fault signals incoming from the aforementioned fault line and warning the BMS controller. Such functionality can be enabled programming FLTIN_CFG.FLTIN_EN = 1. Such bit is reset every time the IC moves to a low-power state.

5.8.3.1 *Fault detection and acknowledgment (FLTIN_DET)*

When enabled, FLTIN acts as an active-low fault input deglitched with $T_{FLTIN\_DEGLITCH}$. Independently on the power management strategy, whenever the FLTIN is detected low for longer than $T_{FLTIN\_DEGLITCH}$, the DIAG_CSA_SC.FLTIN_DET latch is set.

The fault acknowledgment procedure depends on the power management strategy:

- In full power mode, fault can be immediately acknowledged accessing L9965P/L99BM2P via SPI Controller.
- In low power mode, the L9965P/L99BM2P needs to be switched first to full power. Then, fault can be acknowledged via SPI Controller.

After the fault root cause has been acknowledged, and the FLTIN is detected high for longer than $T_{FLTIN\_DEGLITCH}$, the DIAG_CSA_SC.FLTIN_DET latch can be cleared on read.

5.8.3.2 *FLTIN line integrity check (FLTIN_TIMEOUT)*

As part of the system safety concept, L9965C/L99BM2C shall verify the fault notification capability of the L9965P/L99BM2P companion chip. This is achieved by means of the FLTIN line integrity check, which can be enabled programming FLTIN_CFG.FLTIN_INT_CHECK_EN = 1. Such bit is reset every time the IC moves to a low-power state.

When enabled, the integrity check can be executed:

- Continuously in full power mode (refer to Figure 11)
  - The $T_{FLTIN\_TIMEOUT}$ is started upon CWUP/FLTIN rising edge and it’s reset upon FLTIN low level
  - To refresh the timeout, L9965P/L99BM2P is expected to toggle its FAULTN output every T_{FAULTN_PERIOD}, generating a low pulse lasting T_{FAULTN_PULSE}
- Once per cycle in low power mode (refer to Figure 12 and Figure 13)
  - At each L9965P/L99BM2P cyclic wakeup, the $T_{FLTIN\_TIMEOUT}$ is started upon CWUP rising edge
  - To reset the timeout, L9965P/L99BM2P is expected to generate a single negative pulse lasting T_{FAULTN_PULSE} on the FLTIN line once awake.

In any configuration, in case the $T_{FLTIN\_TIMEOUT}$ timeout expires, the DIAG_CSA_SC.FLTIN_TIME_OUT latch is set.

Independently on the power management strategy, the T_{FAULTN_PULSE} in L9965P/L99BM2P has been designed smaller than $T_{FLTIN\_DEGLITCH}$ in order to allow distinguishing an integrity ack pulse from a real fault signal.

Whenever a fault occurs, the MCU is supposed to perform fault acknowledgment as described in Fault detection and acknowledgment (FLTIN_DET).

Figure 11. **FLTIN integrity check in full power mode**

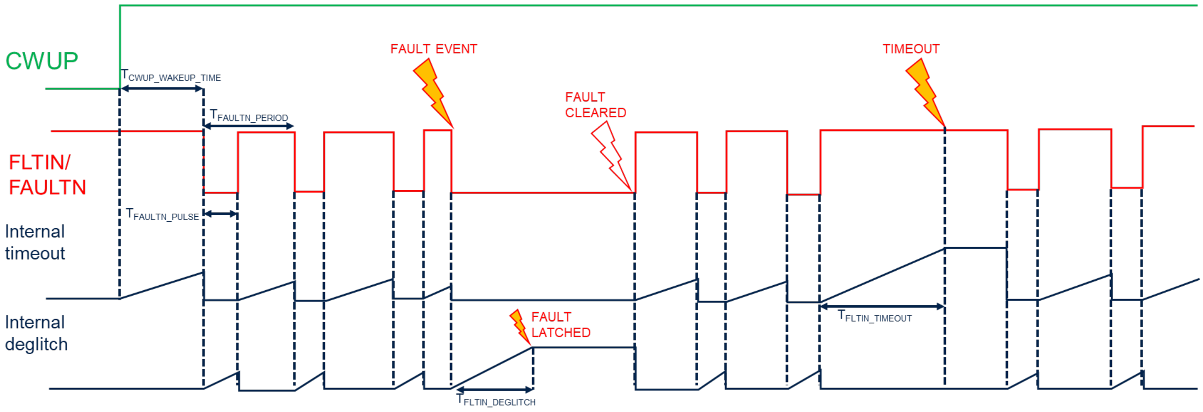


Figure 12. **FLTIN integrity check in low power mode (example of timeout detected by L9965C/L99BM2C)**

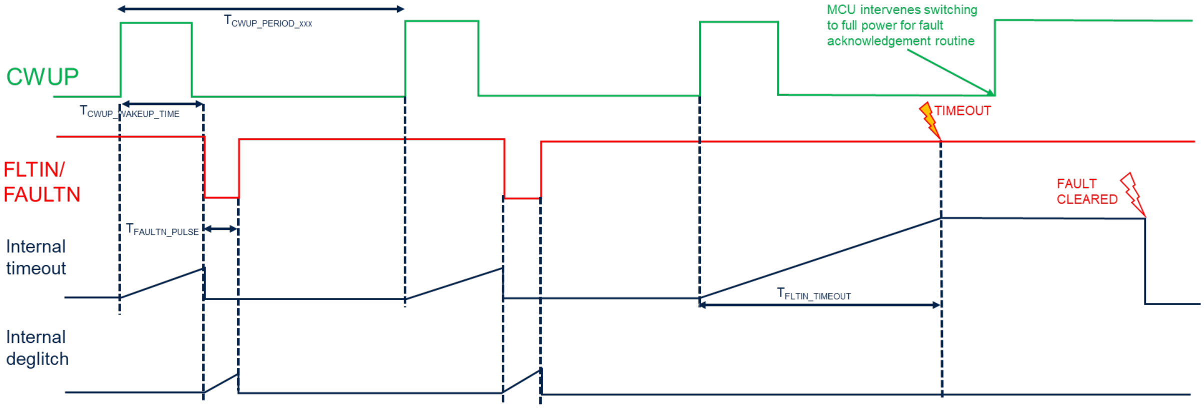
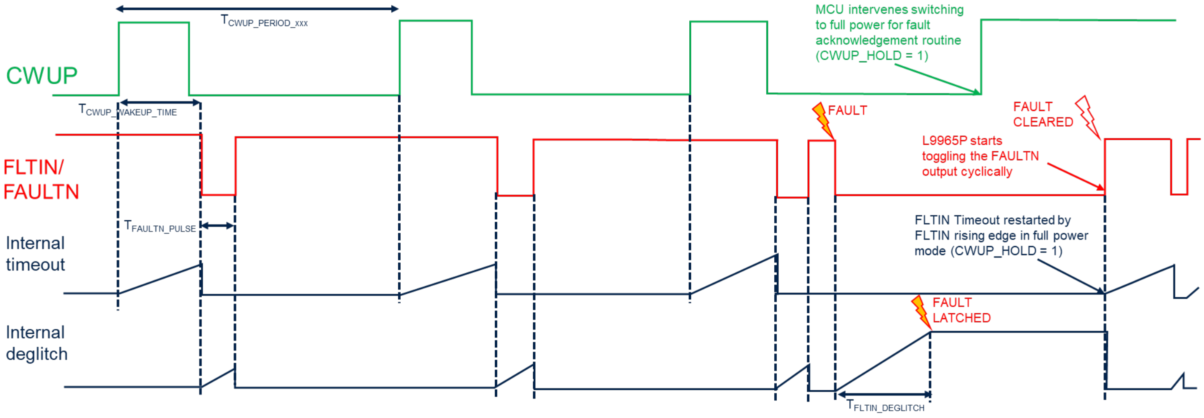


Figure 13. **FLTIN integrity check in low power mode (example of fault detected by L9965P/L99BM2P)**



5.8.3.3 *Diagnostics*

Table 35. **FLTIN diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
FLTIN Line Integrity Check fail	If the $T_{FLTIN\_TIMEOUT}$ expires the FLTIN_TIME_OUT fault is acknowledged	DIAG_CSA_SC.FLTIN_TIME_OUT flag is set	The FLTIN_TIME_OUT can always be cleared by MCU	The $T_{FLTIN\_TIMEOUT}$ is cleared but not restarted	FLTIN_EN masks diagnostic execution. When disabled, the FLTIN_TIME_OUT flag can always be cleared. FLTIN_INT_CHECK_EN masks diagnostic execution. When disabled, the FLTIN_TIME_OUT flag can always be cleared
FLTIN fault detection	If FLTIN holds the active level for longer than $T_{FLTIN\_DEGLITCH}$, the FLTIN_DET fault is acknowledged	DIAG_CSA_SC.FLTIN_DET flag is set	If FLTIN is detected high for longer than $T_{FLTIN_DEGLITCH}$the FLTIN_DET flag can be cleared by MCU	None	FLTIN_EN masks diagnostic execution. When disabled, the FLTIN_DET flag can always be cleared

5.8.3.4 *Electrical parameters*

Table 36. **FLTIN electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{FLTIN\_DEGLITCH}$	FLTIN input deglitch filter		34	40	46	µs	GPIO5_SDA_FLTIN
$T_{FLTIN\_TIMEOUT}$	FLTIN line integrity timeout		29		50	ms	GPIO5_SDA_FLTIN

5.8.4 Pyrofuse deployment outputs (FAULT0/FAULT1)

The L9965C/L99BM2C implements two independent fault outputs (FAULT0 and FAULT1), whose FAULT Signalling Mode (FAULTx_MODE) can be configured according to the application requirements.

To reach the highest ASIL level on pyrofuse deployment/non-deployment, both outputs should be used, connecting them to FENH/FENL inputs of the L9965P/L99BM2P driver. For better robustness against common cause failures, it is also recommended to adopt opposite levels encoding (e.g. FAULT0_LEVEL = 1 & FAULT1_LEVEL = 0, as shown in Figure 14).

The fault encoding mode (PWM or level-based), can instead be adjusted to reflect different BMS operating states.

Figure 14. **Pyro-Fuse deployment when both L9965C/L99BM2C is in NORMAL and L9965P/L99BM2P is in DEEP SLEEP state**

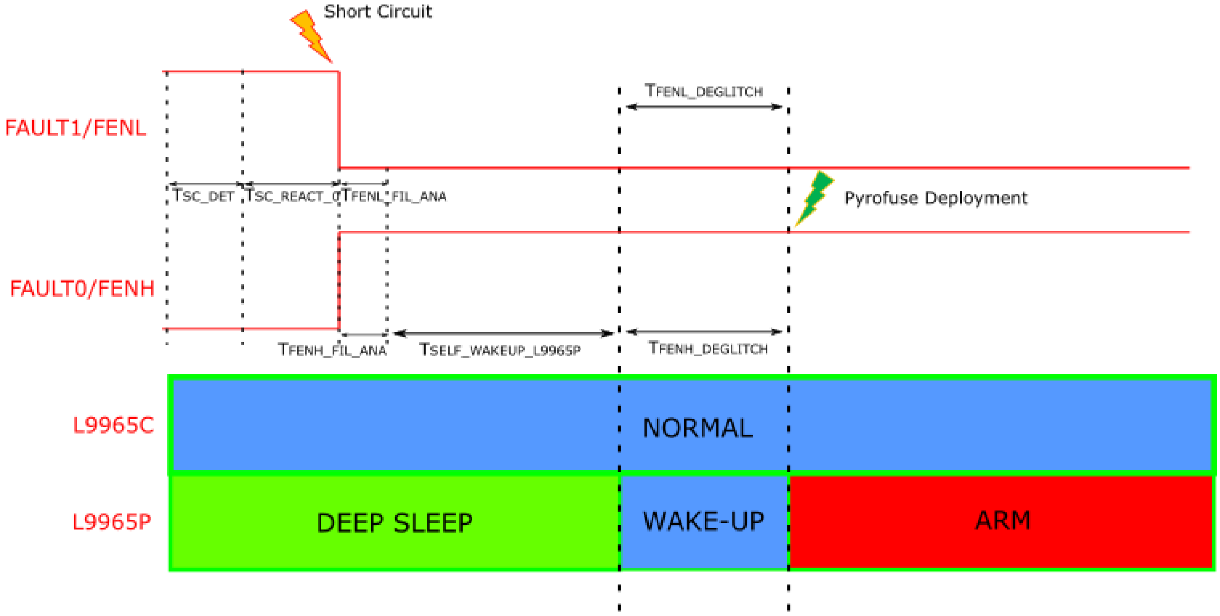
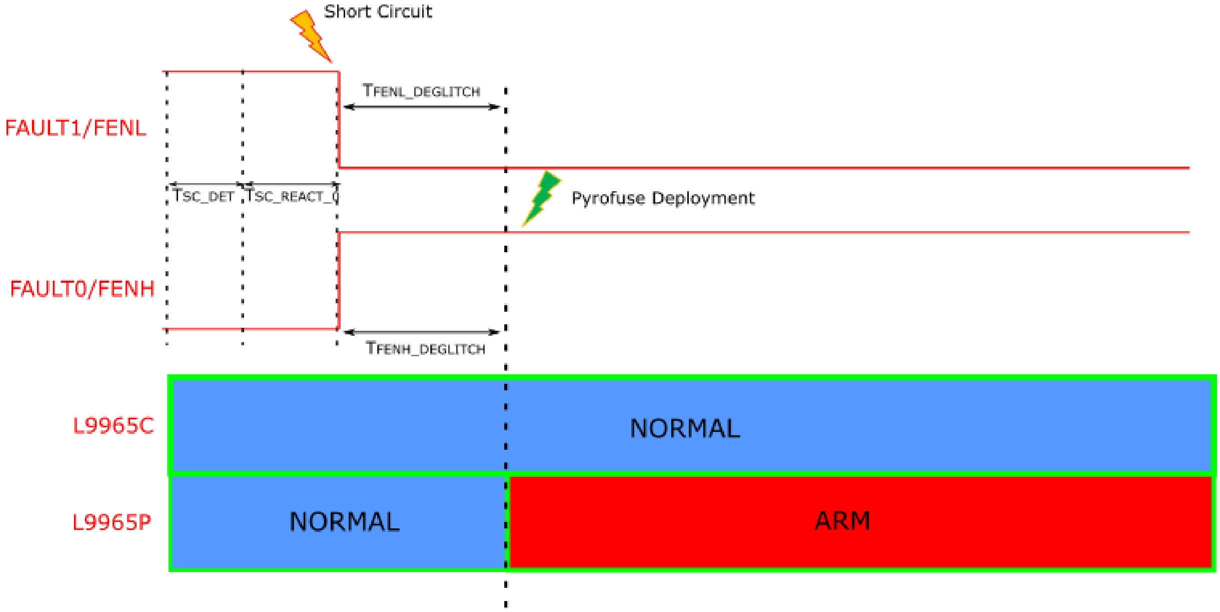


Figure 15. **Pyro-Fuse deployment when L9965C/L99BM2C is in NORMAL and L9965P/L99BM2P is in WAKEUP state**



5.8.4.1 *FAULT outputs line integrity check*

Similarly to the FLTIN Line Integrity Check (FLTIN_TIMEOUT), L9965P/L99BM2P companion chip also offers the possibility of verifying the integrity of FENH/FENL deployment lines.

Such functionality requires FLTIN_EN = 1

Depending on the power management strategy, such integrity check can be achieved applying different configurations listed in Table 37.

Table 37. **Configuration for FAULTx integrity check**

Power Management Strategy	L9965C/ L99BM2C State	L9965P/ L99BM2P State	FAULT<x> Output	Configuration	Checked Path	Note
Low_Power	NORMAL	CYCLIC WAKEUP (alternation between DEEP SLEEP and DIAG)	Level Mode	CWUP_CFG.CWUP_EN = 1 CWUP_CFG.CWUP_HOLD = 0 CWUP_CFG.CWUP_TIM_EN = 1 FAULT_CFG.FAULT<x>_MODE = 0 FAULT_CFG.FAULT<x>_CYCLIC_BIST = 1 FLTIN_CFG. FLTIN_EN = 1	SC<x> diagnostic + FAULT<x> output	These two methods enable cyclic check of the whole detection and signalling path, including the SC detection and excluding the digital deglitches. The methods rely on FLTIN received pulses to align FAULTx pulse generation. The flag of SC<x>_DCHG is not asserted during automatic integrity check.
Full_Power_1	NORMAL	NORMAL	Level mode	CWUP_CFG.CWUP_EN = 1 CWUP_CFG.CWUP_HOLD = 1 FAULT_CFG.FAULT<x>_MODE = 0 FAULT_CFG.FAULT<x>_CYCLIC_BIST = 1 FLTIN_CFG. FLTIN_EN = 1		
Full_Power_2	NORMAL	NORMAL	PWM-ing	CWUP_CFG.CWUP_EN = 1 CWUP_CFG.CWUP_HOLD = 1 FAULT_CFG.FAULT<x>_MODE = 1 FAULT_CFG.FAULT<x>_CYCLIC_BIST = X	FAULT<x> output	This enables continuous check of the signalling path, allowing quick detection of line stuck failures. As the FAULTx outputs are continuously toggling, the method does not rely on FLTIN received pulses to align FAULTx pulse generation
Full_Power_3	NORMAL	NORMAL	Level mode (with manual fault injection)	CWUP_CFG.CWUP_EN = 1 CWUP_CFG.CWUP_HOLD = 1 FAULT_CFG.FAULT<x>_CYCLIC_BIST = 0 FAULT_CFG.FAULT<x>_MODE = 0	Whole path: SC<x> diagnostic + deglitch + FAULT<x> output	This enables manual check of the whole fault sensing, filtering and propagation path. It is recommended to run such procedure at startup (refer to Short Circuit Fault Injection) During the fault injection procedure, the flag of SC<x>_DCHG is asserted.

Note: Regardless of the fault integrity check strategy, the short-circuit detection is always active and the SC<x>_DCHG flag is not masked during these checks.

The methods work as follows:

Low Power

In low-power mode, after having received the FLTIN negative pulse that confirms the integrity of the fault input line, L9965C/L99BM2C in turn generates confirmation pulses on the FAULTx outputs in order to allow L9965P/L99BM2P perform the same integrity check on its side (see Figure 16).

1. The IC continuously listens to the FLTIN line, waiting for each FLTIN rising edge in order to start the FAULTx integrity check pattern.

Note: Being based on the FLTIN rising edge sensing, this method requires L9965P/L99BM2P to generate periodic pulses on its FAULTN line.

2. If FAULT0_CYCLIC_BIST = 1 && FAULT0_MODE = 0, the logic waits for $T_{FAULTx\_LATENCY}$ and then toggles the SC0 diagnostic inputs, in order to generate a glitch on the FAULT0 output lasting T_{FAULTx_PULSE}.

Note: L9965P/L99BM2P recognizes such pulse as a validation of line integrity, but the corresponding FENH/FENL input is configured with a deglitch filter consistently higher than T_{FAULTx_PULSE}. This prevents inadvertent recognition of an arming condition.

3. If FAULT0_CYCLIC_BIST = 1 && FAULT0_MODE = 0, the IC acknowledges that FAULT0 has returned to its inactive level by sensing the corresponding edge.
4. If FAULT1_CYCLIC_BIST = 1 && FAULT1_MODE = 0, the logic waits for $T_{FAULTx\_LATENCY}$ and then toggles the SC1 diagnostic inputs, in order to generate a glitch on the FAULT1 output lasting T_{FAULTx_PULSE}.

Note: By doing so, the FAULT0/FAULT1 toggles are never aligned, so that a AND gating of the two conditions would never output dangerous fire commands. Additionally, also the FAULT1 line is deglitched on L9965P/L99BM2P with a filter consistently higher than T_{FAULTx_PULSE}.

If fault detection (FLTIN_DET = 1) occurs anytime during this procedure, the sequence is interrupted. The FSM is immediately reset and the FAULTx outputs return to their inactive state (provided that no short circuit is detected in the meantime). The sequence restarts from point “1” on the next trigger event (FLTIN rising edge).

Note: In Figure 17 there is an example with FAULT0_CYCLIC_BIST = 0. The steps “2” and “3” of the sequence are skipped and FAULT1 toggle occurs in place of FAULT0. The same would occur if FAULT0_MODE = 1 (PWM mode).

Full_Power_1

The behavior described for low-power mode (Figure 16) also applies to full power mode, if the FAULTx outputs are configured in level mode, as reported in Table 37. In this case, the only difference in respect to Figure 16 is represented by the CWUP signal being hold high (CWUP_HOLD = 1)

Full_Power_2

A third case is represented by full-power mode with FAULTx outputs encoded in PWM mode (see Figure 18).

1. In such case, the PWM generation on the FAULTx outputs is asynchronous in respect to the FLTIN received signal
2. Only the integrity of the FAULTx output is assessed, but SC diagnostic inputs are not toggled in real-time.

Full_Power_3

Finally, a manual short-circuit fault injection (SC_ARM/SC_INJECT) shall be executed at each system wakeup to verify the integrity of the whole propagation path.

Figure 16. **FAULTx lines integrity check in level mode**

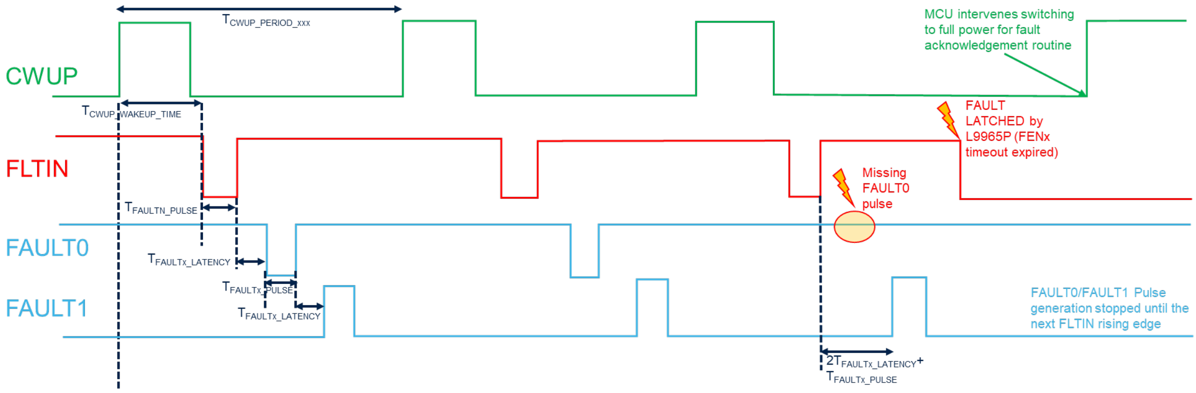


Figure 17. **FAULTx lines integrity check in level mode (example with FAULT0 cyclic BIST disabled)**

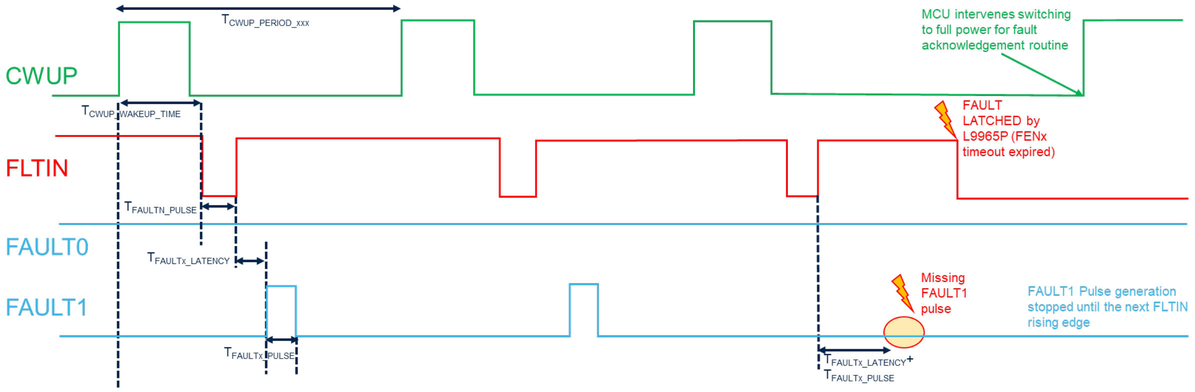
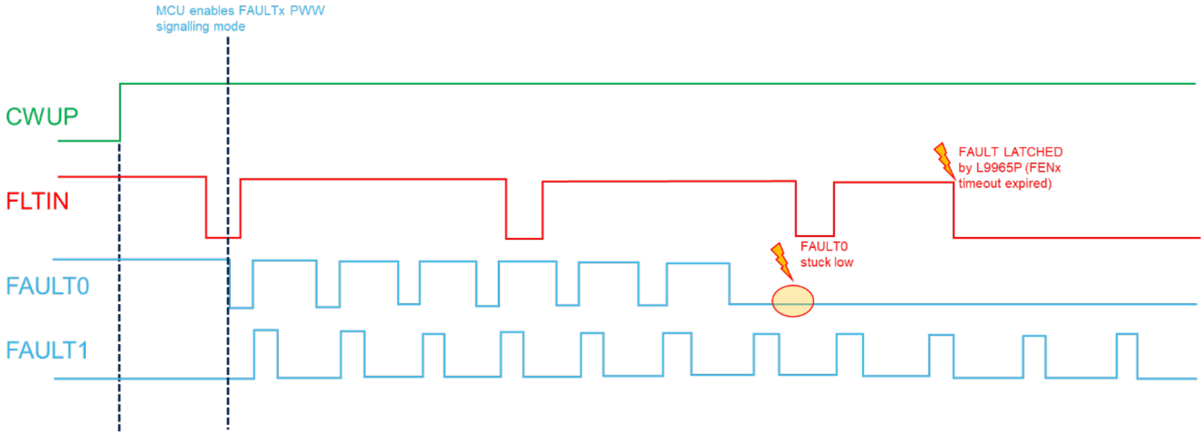


Figure 18. **FAULTx lines integrity check in PWM mode**



To prevent any misbehavior resulting in inadvertent pyro-fuse deploy, the different fault integrity check strategies are subject to a gating. The SC<x> detectors can only be toggled when specific “safe” configurations are applied.

5.8.4.2 *Electrical parameters*

Table 38. **FAULT0/FAULT1 integrity check electrical characteristics.**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
T_{FAULTx_PULSE}	FAULT0/FAULT1 integrity pulse duration		5	10	15	µs	FAULTx

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{FAULTx\_LATENCY}$	Delay between FLTIN rising edge and FAULT0 pulse. Delay between FAULT0 and FAULT1 integrity pulses		5	10	15	µs	FAULTx
C_{GPIO_EXT}	External bypass capacitor	Application information, including parasitic			240	pF	FAULTx

5.9 Current sense open load detection (CSA_OL)

To prevent failures in the Analog Front-End (AFE) from affecting fault detection capability, L9965C/L99BM2C offers the possibility to monitor the integrity of the connections to the CSA0 and CSA1 pin pairs.

All CSA pins are equipped with an open load diagnostic, whose execution is:

- On-demand while the device is in NORMAL
- Automatic at each transition to CYCLIC_WAKEUP

Such diagnostics are intended to cover failures in the analog front end affecting both Current Sense ADCs and CSA_CC Circuits Redundancy for Safety.

It is also possible to check if the Open Load diagnostic is in progress reading the flag CSA<x>_OPEN_BUSY (DIAG_CSA_SC register).

For the on-demand open load diagnostic, Procedure 4: Open load diagnostic must be followed:

Procedure 4: Open load diagnostic

1. MCU disables the Configuration Integrity Check (CONF_CRC) writing GENERAL_REG.CYC_CFG_CRC_DIS = 1
2. MCU removes the Configuration Lock
3. MCU disables the Short-Circuit Detection (SC) diagnostic on the CSAPx/CSAMx pin pair, writing CFG_DIAG.SC<x>_EN = 0
4. MCU disables the Instantaneous Current Measurement ADC (CSAP0/CSAM0) (CFG_DIAG.CUR_INST_EN = 0) and Coulomb Counting ADC (CSAP1/CSAM1) (CFG_FOR_STBY_LOGIC.CC_EN = 0)
5. MCU re-applies the Configuration Lock
6. MCU writes CMD2.CSA<x>_OL_DIAG = 1. At this point the IC enables the I_{CSA_OL} pullup currents on the CSAPx/CSAMx pin pair
7. MCU waits for 1.2*TCSA_OL_SET settling time (programmable via CFG_DIAG.CSA_OL_SET field). During this interval the CSA<x> Open Load comparator is masked
8. MCU reads back the status of CSA<x>OPEN latch. If a CSA_OL was previously detected two readings are required; the first one to clear the fault flag, the second one to read the current CSA_OL diagnosis.
   a. At the end of the TCSA_OL_SET settling time, the IC unmasks the open load comparator and, in case of failure, the CSA<x>_OPEN latch is set
   b. At the end of the TCSA_OL_SET settling time, the IC also disables the ICSA_OL pullup currents
9. MCU waits for 1.2*TCSA_OL_SET settling time to allow CSAPx/CSAMx pin voltage to settle down to the normal operating voltage
10. If no open load was detected
    a. MCU removes the Configuration Lock
    b. MCU re-enables the Short-Circuit Detection (SC) diagnostic on the CSAPx/CSAMx pin pair, writing SC<x>_EN = 1
    c. MCU re-enables the Instantaneous Current Measurement ADC (CSAP0/CSAM0) (CUR_INST_EN = 1) and Coulomb Counting ADC (CSAP1/CSAM1) (CC_EN = 1)
    d. MCU re-applies the Configuration Lock
    e. MCU re-enables the Configuration Integrity Check (CONF_CRC) writing CYC_CFG_CRC_DIS = 0
11. Otherwise, MCU reports the failure to the upper application level

5.9.1 Diagnostics

Table 39. **CSA open load diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
CSA<x> OPEN	If the voltage on either CSAM<x> or CSAP<x> pin raises above $V_{CSA\_OL\_TH}$ for a time interval longer than $T_{CSA\_OL\_TH}$, the CSA<x>_OPEN failure is acknowledged	The DIAG_CSA_SC.CSA<x>_OPEN flag is set	If the voltage on the affected pin falls below $V_{CSA\_OL\_TH}$ for a time interval longer than $T_{CSA\_OL\_TH}$, the CSA<x>_OPEN flag can be cleared by MCU	None	CUR_INST_EN = 1 masks diagnostic execution for CSA0. When diagnostic is disabled, the CSA0_OPEN flag can always be cleared CC_EN = 1 masks diagnostic execution for CSA1. When diagnostic is disabled, the CSA1_OPEN flag can always be cleared SC<x>_EN = 1 masks diagnostic execution for CSA<x>. When diagnostic is disabled, the CSA<x>_OPEN flag can always be cleared

5.9.2 Electrical parameters

Table 40. **CSA Open Load electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{CSA\_OL\_TH}$	CSA open load diagnostic threshold on CSAP and CSAM pins		1	1.2	1.4	V	CSAPx, CSAMx
$T_{CSA\_OL\_FIL}$	CSA open load comparator filter time		17	20	23	us	CSAPx, CSAMx
I_{CSA_OL}	CSA open load currents		-20%	100	+20%	µA	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_000}$	CSA open load diagnostic settling time – CSA_OL_SET, 3 bit field in CFG_DIAG register	CSA_OL_SET=000	20	25	30	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_001}$		CSA_OL_SET=001	40	50	60	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_010}$		CSA_OL_SET=010	60	75	90	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_011}$		CSA_OL_SET=011	80	100	120	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_100}$		CSA_OL_SET=100	110	125	145	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_101}$		CSA_OL_SET=101	135	150	170	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_110}$		CSA_OL_SET=110	158	175	198	ms	CSAPx, CSAMx
$T_{CSA\_OL\_SET\_111}$		CSA_OL_SET=111	180	200	225	ms	CSAPx, CSAMx

5.10 Analog input monitor (AINx)

While in NORMAL state, L9965C/L99BM2C monitors the AINx pins using a fully differential ADC, whose inputs can be connected to:

- Any of the AINx inputs
- AGND
- VTREF

Task execution is triggered on-demand programming AIN_CMD_CFG.VCONV = 1. When triggering a conversion, ADC differential inputs can be configured programming the AMUXP_CONF and AMUXN_CONF fields in the same frame, register AIN_CMD_CFG (refer to Table 41).

For instance, an absolute conversion of AIN5 input can be performed programming AMUXP_CONF = 0101 and AMUXN_CONF = 1101. A differential measurement of AIN4-AIN2 voltage can be triggered programming AMUXP_CONF = 0100 and AMUXN_CONF = 0010.

The differential voltage to be converted may be in the V_{AIN_RANGE} and can be referred to a floating common mode voltage, provided that the absolute pin voltages lie within the $V_{AIN\_ABS\_RANGE}$.

The ABS_RATIO bit (always written in the same frame) defines the conversion type:

- AIN_CMD_CFG.ABS_RATIO = 0 triggers a ratiometric measurement referred to 3V3 VTREF. It is recommended when using AINx input for measuring an NTC.
- AIN_CMD_CFG.ABS_RATIO = 1 triggers an absolute measurement.

The T_{VOLT_FILTER} acquisition window (programmable via AIN_CMD_CFG.TVOLT_FIL in the same frame) is applied to each sample. Longer acquisition windows results in a more robust filter ($F_{CUT\_VOLT\_FILTER}$ cutoff frequency).

Any ongoing conversion cannot be interrupted, and any asynchronous command triggering a new VADC start of conversion (VCONV) is discarded.

The conversion result is available in the AIN_MEAS field (AIN_MEAS register) and the update of the data is signaled through the flag DATA_READY_AIN (AIN_MEAS register).

The ADC can be BIST launched on-demand, writing CMD2.VADC_AIN_BIST = 1. The BIST procedure lasts $2T_{VOLT\_FILTER\_011}$ and includes the possibility of injecting a fault with CMD2.VADC_AIN_FAULT_INJ= 1, written in the same command frame.

Table 41. AMUX configuration

AMUXx_CONF	Input Connected To
0000	AIN0
0001	AIN1
0010	AIN2
0011	AIN3
0100	AIN4
0101	AIN5
0110	AIN6
0111	AIN7
1000	AIN8
1001	AIN9
1010	AIN10
1011	VTREF
1100	Reserved
1101	AGND
1110	Reserved
1111	Reserved

5.10.1 Diagnostics

Table 42. Analog input monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
ADC BIST FAIL	If the ADC BIST fails upon on-demand diagnostic, the VADC_AIN_BIST_FAIL fault is acknowledged. This fault is considered as valid if VADC_AIN_BIST_DONE is also asserted.	DIAG_STATUS1.VADC_AIN_BIST_FAIL flag is set	VADC_AIN_BIST_FAIL can be cleared by MCU read	None	Non maskable

5.10.2 Electrical parameters

Table 43. Cell Voltage Monitor electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
T_{AIN_START}	ADC settling time			20 (1)		µs	AINx
$V_{AIN\_RANGE\_1}$	AINx Differential Voltage Input Measurement Range	Design info, full scale range [-6.5;+6.5], Difference between any AIN_X and AIN_Y pin pair, ABS_RATIO = 1	-5.5		5.5	V	AINx
$V_{AIN\_RANGE\_0}$		Design info, ABS_RATIO = 0 Full scale range [-3.9; +3.9] @VTREF=3.3V	$-V_{VTREF}$		V_{VTREF}	V	AINx
$V_{AIN\_ABS\_RANGE}$	AINx Absolute pin voltage	Design info	0		VB	V	AINx
$V_{AIN\_RES\_1}$	AINx Measurement Resolution	Design info, ABS_RATIO = 1		198.4		µV	AINx
$V_{AIN\_RES\_0}$		Design info, ABS_RATIO = 0		119 @VTREF=3.3V		µV	AINx
N_{BIT_AIN}	ADC bit number	Design info		16		bit	AINx
R_{AIN_IN}	AINx input impedance	Guaranteed by design	40			MΩ	AINx
$AIN_{LOW\_RANGE\_ERR0}$	Total Conversion Error in low range, Including post-soldering and ageing effects(2).	0 mV < $\lvert V_{AINX} - V_{AINY}\rvert$ < knee_point_VADC, -40°C ≤ Tamb ≤ +105°C, Guaranteed by test bench characterization	-5		5	LSB	AINx
$AIN_{LOW\_RANGE\_ERR1}$		0 mV < $\lvert V_{AINX} - V_{AINY}\rvert$ < knee_point_VADC, +105°C ≤ Tamb ≤ +125°C, Guaranteed by test bench characterization	-13		13	LSB	AINx
$V_{AIN\_GAIN\_ERR\_0}$	ADC gain error, Including post-soldering and ageing effects. Including non-linearities(2).	knee_point_VADC < $\lvert V_{AINX} - V_{AINY}\rvert$ < V_{AIN_RANGE}, -40°C ≤ T_{amb} ≤ +105°C	-0.2		0.2	%	AINx

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$V_{AIN\_GAIN\_ERR\_0}$	ADC gain error, Including post-soldering and ageing effects. Including non-linearities(2).	knee_point_VADC < $\lvert V_{AINX} - V_{AINY}\rvert$ < V_{AIN_RANGE}, 105°C ≤ T_{amb} ≤ +125°C	-0.5		0.5	%	AINx
$V_{AIN\_NOISE\_000}$	Standard deviation over a 100 samples distribution at different Voltage ADC filter time (TVOLT_FIL 3-bit field in AIN_CMD_ CFG register), TAMB	TVOLT_FIL = 000		332		µVrms	AINx
$V_{AIN\_NOISE\_001}$		TVOLT_FIL = 001		296		µVrms	AINx
$V_{AIN\_NOISE\_010}$		TVOLT_FIL = 010		235		µVrms	AINx
$V_{AIN\_NOISE\_011}$		TVOLT_FIL = 011		100		µVrms	AINx
$V_{AIN\_NOISE\_100}$		TVOLT_FIL = 100		60		µVrms	AINx
$V_{AIN\_NOISE\_101}$		TVOLT_FIL = 101		60		µVrms	AINx
$V_{AIN\_NOISE\_110}$		TVOLT_FIL = 110		60		µVrms	AINx
$V_{AIN\_NOISE\_111}$		TVOLT_FIL = 111		60		µVrms	AINx
$T_{VOLT\_FILTER\_000}$		TVOLT_FIL = 000		0.532 (1)		ms	AINx
$T_{VOLT\_FILTER\_001}$		TVOLT_FIL = 001		1.064 (1)		ms	AINx
$T_{VOLT\_FILTER\_010}$		TVOLT_FIL = 010		2.128 (1)		ms	AINx
$T_{VOLT\_FILTER\_011}$		TVOLT_FIL = 011		4.256 (1)		ms	AINx
$T_{VOLT\_FILTER\_100}$		TVOLT_FIL = 100		8.512 (1)		ms	AINx
$T_{VOLT\_FILTER\_101}$		TVOLT_FIL = 101		17.024 (1)		ms	AINx
$T_{VOLT\_FILTER\_110}$		TVOLT_FIL = 110		34.048 (1)		ms	AINx
$T_{VOLT\_FILTER\_111}$		TVOLT_FIL = 111		68.096 (1)		ms	AINx
$F_{CUT\_VOLT\_FILTER\_000}$	Voltage ADC 3dB cutoff frequency at different Voltage ADC filter time (TVOLT_FIL 3-bit field in AIN_CMD_ CFG register)	TVOLT_FIL = 000		885		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_001}$		TVOLT_FIL = 001		416		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_010}$		TVOLT_FIL = 010		208		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_011}$		TVOLT_FIL = 011		104		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_100}$		TVOLT_FIL = 100		52		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_101}$		TVOLT_FIL = 101		26		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_110}$		TVOLT_FIL = 110		13		Hz	AINx
$F_{CUT\_VOLT\_FILTER\_111}$		TVOLT_FIL = 111		6.5		Hz	AINx
Knee_point_VADC		Design info, ABS_RATIO = 1		500		mV	AINx
Knee_point_VADC		Design info, ABS_RATIO = 0		250		mV	AINx

1. *Parameters affected by clock main uncertainty*
2. *Single samples are characterized by a superimposed Gaussian noise, with zero-mean and V_{AIN_NOISE} standard deviation*

5.10.3 Shunt temperature sensing

The IC supports temperature sensing by means of external NTCs, biased by Reference LDO (VTREF), and measured via Analog Input Monitor (AINx), using a ratiometric approach.

The Current Sense stages offer high accuracy, enabling reliable instantaneous current measurement and Coulomb Counting for SOC/SOH estimation. However, a residual error source is still represented by the shunt resistor temperature drift.

Even the most stable shunt resistors exhibit a 50ppm/°C temperature drift, so that calibration performed at room temperature may not recover the error over the whole temperature span. For instance, if the error is fully compensated @25°C, a residual error due to temperature drift ΔR_{TH} = 0.5% still exists when the ambient temperature is 125°C (max. operating value).

An NTC can be used for indirectly sensing the shunt inner temperature and perform resistance compensation, thus minimizing $\Delta R_{TH.}$

On Figure 31, connected to AIN10 pin, the reference circuit for NTC sensing is shown. Table 87 lists the recommended BOM, also for this measurement.

5.11 Gate predrivers (GATEx)

The L9965C/L99BM2C implements gate predrivers that can be used for driving external FETs.

By default, predriver stages are disabled and GATEx is in HiZ (GATE<x>_EN = 0). Any external switch has to be properly conditioned by means of external pullup/pulldown resistors (470kΩ resistors are recommended to comply with Charge Pump capability). The enable setting is not stored in the NVM and shall be refreshed by MCU every-time the device moves to NORMAL state.

Predrivers can be enabled programming GATE_PRDRV_EN.GATE<x>_EN = 1. When enabled, the GATEx outputs follow the corresponding GATE_CMD.GATE<x> command bit (default 0).

For every gate predriver, it is possible to select the pull-down current through a 2-bit field GATE<x>_PD (registers GATE_PRDRV_PD_0_TO_7 or GATE_PRDRV_PD_8_TO_9).

5.11.1 Electrical parameters

Table 44. **Gate predriver electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{GATE_ON}	GATEx pullup voltage			min(V_{GATE_CLAMP},V_{VCP})		V	GATEx
V_{GATE_CLAMP}	GATEx clamp voltage		16		20	V	GATEx
$C_{LOAD\_GATE\_09}$	Equivalent capacitive load	GATEx, x= 0-9, Application information			3.25	nF	GATEx
$C_{LOAD\_GATE\_10}$		GATE9 Application information, when used as pre-charge controller driver			130	pF	GATEx
$f_{SW\_GATE\_09}$	Pre-driver switching frequency	Application information, GATEx x= 0-9		10		Hz	GATEx
$f_{SW\_GATE\_10}$		Application information, GATE9 when used as pre-charge controller driver		100		kHz	GATEx
$I_{GATE\_PD\_00}$	GATEx pulldown current	GATE<x>_PD = 00, $V_{GATEx} \geq 2V$	-50%	1	+50%	mA	GATEx
$I_{GATE\_PD\_01}$		GATE<x>_PD = 01, $V_{GATEx} \geq 2V$	-50%	5	+50%	mA	GATEx
$I_{GATE\_PD\_10}$		GATE<x>_PD = 10, $V_{GATEx} \geq 2V$	-50%	10	+50%	mA	GATEx
$I_{GATE\_PD\_11}$		GATE<x>_PD = 11, $V_{GATEx} \geq 2V$	-50%	15	+50%	mA	GATEx
R_{GATE_PU}	Gate pre-driver, HS ON equivalent resistance	Calculated as ($V_{GPDRV\_HS\_ON\_H\_5mA}$-$V_{GPDRV\_HS\_ON\_H\_10mA}$)/(10mA-5mA)			130	Ohm	GATEx
$I_{GPDRV\_HS\_SAT}$	Gate pre-driver, HS saturation current	VGATEx=0V, VCP=25V (externally forced)	16	34	60	mA	GATEx

5.12 GPIOs

The device features 7 GPIOs pin, configurable according to Table 45:

Table 45. **GPIO configuration**

CFG_GPIO.GPIO<x>_CONF	Configuration
0	Generic digital input
1	Generic digital output

GPIOs can be used as simple I/Os driven/read via dedicated registers:

- When configured as digital output, the GPIOs can be driven according to the GPO_CMD.GPO<x> bit.
- The input buffer status can be read via GPI_READ.GPI<x> bit.
  - When configured as digital input, an internal weak pulldown/pullup can be configured programming CFG_GPIO.GPIO<x>_PU_PD.

Table 46. **GPIO weak pullup/pulldown configuration**

CFG_GPIO.GPIO<x>_PU_PD	Configuration
0	Weak pulldown ($R_{GPIO\_WK\_PD}$)
1	Weak pullup ($R_{GPIO\_WK\_PU}$)

Dedicated bit field can be used to force alternate special functions (see Table 47):

Table 47. **Alternate function activation**

SPI_VIF_CT.SPI_MODE	Configuration
00 (default)	SPI Target
01, 10	SPI disabled
11	SPI Controller
DEV_GEN_CFG_2.I2C_EN	**Configuration**
0 (default)	I2C disabled
1	I2C Controller
CWUP_CFG.CWUP_EN	**Configuration**
0 (default)	GPIO6_SCL_CWUP not configured as L9965P/L99BM2P Cyclic Wakeup Output (CWUP)
1	GPIO6_SCL_CWUP configured as L9965P/L99BM2P Cyclic Wakeup Output (CWUP)
FLTIN_CFG.FLTIN_EN	**Configuration**
0 (default)	GPIO5_SDA_FLTIN not configured as Fault Input (FLTIN)
1	GPIO5_SDA_FLTIN configured as Fault Input (FLTIN)

The alternate functions for Interfacing to L9965P/L99BM2P pyrofuse driver, have higher priority than the I2C Controller configurations:

- when CWUP_EN = 1, the GPIO6 is configured as CWUP regardless of the I2C_EN setting
- when FLTIN_EN = 1, the GPIO5 is configured as FLTIN regardless of the I2C_EN setting

Similarly, I2C_EN has higher priority than the standard GPIO configuration:

- when I2C_EN = 1, the GPIO5 and GPIO6 are configured as SDA and SCL respectively, regardless of the GPIO<x>_CONF

The following table summarizes the GPIO configurations in NORMAL state.

Table 48. GPIO configurations in NORMAL

PU = Pull-Up; PD = Pull-Down; OD = Open Drain; X = Don't care

PIN	GENERIC	SPI CONTROLLER (SPI_MODE)	SPI TARGET (SPI_MODE)	I2C CONTROLLER (I2C_EN)	CWUP (CWUP_EN)	FLTIN (FLTIN_EN)
GPIO0_NCS0	IN(PU/PD)/ OUT(1)	OUT	IN(PU)	X	X	X
GPIO1_NCS1	IN(PU/PD)/ OUT(1)	IN(PU/PD)/OUT (2)	X	X	X	X
GPIO2_SDI	IN(PU/PD)/ OUT(1)	IN(PD)	IN(PD)	X	X	X
GPIO3_SDO	IN(PU/PD)/ OUT(1)	OUT	OUT	X	X	X
GPIO4_SCLK	IN(PU/PD)/ OUT(1)	OUT	IN(PD)	X	X	X
GPIO5_SDA_FLTIN	IN(PU/PD)/ OUT(1)	X	X	INOUT(OD)	X	IN(PU)
GPIO6_SCL_CWUP	IN(PU/PD)/ OUT(1)	X	X	OUT(OD)	OUT	X

1. *Depending on configuration (GPIOx_CONF, GPIOx_PU_PD)*
2. *Depending on configuration (GPIO1_NCS1_EN). It can be used as generic GPIO if GPIO1_NCS1_EN=0*

Table 49 summarizes the GPIO management in DEEP SLEEP and STANDBY.

Table 49. GPIO configuration in DEEP SLEEP and STANDBY

PU = Pull-Up; PD = Pull-Down; OD = Open Drain; X = Don't care

PIN	1ST DEEP SLEEP	1ST NORMAL(1)	NTH DEEP SLEEP/STANDBY	NTH NORMAL
GPIO0_NCS0	IN(PU) for wake-up	IN(PU) for SPI Target	IN(PU) for wake-up only if SPI Target mode is configured; otherwise, PU	Latest configuration
GPIO1_NCS1	PU	IN(PD)	PU	Latest configuration
GPIO2_SDI	PD	IN(PD) for SPI Target	PD	Latest configuration
GPIO3_SDO	PD	OUT for SPI Target	PD	Latest configuration
GPIO4_SCLK	IN(PD) for wake-up	IN(PD) for SPI Target	IN(PD) for wake-up only if SPI Target mode is configured; otherwise, PD	Latest configuration
GPIO5_SDA_FLTIN	PU	IN(PD)	PU	Regmap configuration
GPIO6_SCL_CWUP	PD	IN(PD)	PD	Regmap configuration

1. *NVM configuration holding default factory values.*

Note: If VB is removed and the IC goes back to OFF state, the 1st DEEP SLEEP behaves as described in the table above. The 1st NORMAL configuration depends on the NVM content: if the NVM had been previously programmed, the configurations stored in the memory are re-downloaded and applied.

Table 50 summarizes the GPIO management in CYCLIC WAKEUP.

Table 50. GPIO configuration in CYCLIC WAKEUP

PU = Pull-Up; PD = Pull-Down; OD = Open Drain; X = Don't care

PIN	CYCLIC WAKEUP
GPIO0_NCS0	IN(PU) for wake-up only if SPI Target mode is configured; otherwise, PU
GPIO1_NCS1	PU

PIN	CYCLIC WAKEUP
GPIO2_SDI	PD
GPIO3_SDO	PD
GPIO4_SCLK	IN(PD) for wake-up only if SPI Target mode is configured; otherwise, PD
GPIO5_SDA_FLTIN	PU
GPIO6_SCL_CWUP	PD

Note: *This table is valid in the hypothesis that the IC has been previously programmed while in NORMAL state, with all configurations pushed in the NVM.*

5.12.1 Electrical parameters

Table 51. **GPIO electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{GPIOH}	GPIO high output value	I_{SOURCE} = 2mA	V_{VIO}-0.4			V	GPIOx
V_{GPIOL}	GPIO low output value	I_{SINK} = 2mA			0.4	V	GPIOx
V_{GPIOL_OD}	GPIO low output value in open-drain configuration	Valid for GPIO5_SDA_FLTIN and GPIO6_SCL_CWUP, I_{SINK} = 2mA			0.4	V	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
$R_{GPIO\_WK\_PU}$	GPIO weak pullup resistor to 3.3V	GPIO<x>_PU_PD = 1	0.4	1	1.6	MΩ	GPIOx
$R_{GPIO\_WK\_PU}$	GPIO weak pulldown resistor to GND	GPIO<x>_PU_PD = 0	0.4	1	1.6	MΩ	GPIOx
$V_{GPIO\_IN\_HIGH}$	GPIO high input level		2			V	GPIOx
$V_{GPIO\_IN\_HYS}$	GPIO input buffer hysteresis		0.1		0.5	V	GPIOx
$R_{GPIO\_EXT\_PU}$	GPIO external pullup resistor for open-drain configurations	Application information	-1%	4.7	+1%	kΩ	GPIOx
$I_{LEAK\_GPIO\_HiZ}$	GPIO leakage current in HiZ	PU/PD disabled, 0 < V_{GPIOx} < 5V	-0.5		0.5	uA	GPIOx

5.13 Communication with BMS controller

5.13.1 Physical Layer

The L9965C/L99BM2C implements two communication interfaces allowing BMS microcontroller access to internal registers and interaction with all the L9965x chained devices:

- SPI Target, described in SPI target.
  - Used by the controller to access the L9965C/L99BM2C device. Such interface is typically used when the IC is operates in a stand-alone application (e.g. 48V systems) along with the Master MCU which is local to the ECU.
- Isolated Vertical Interface (VIF), described in Isolated Vertical Interface (VIF).
  - Used by other L9965/L99BM2 devices, connected in daisy chain on the VIF bus, to communicate with the L9965C/L99BM2C device. The BMS Master is typically placed in a different voltage domain and needs an isolated communication interface to access each slave on the VIF bus.

At first power-up, both interfaces of L9965C/L99BM2C are available for performing Addressing Procedure. However, they are considered mutually exclusive during normal operation. After IC first configuration, only one interface shall be left enabled.

The IC does not manage concurrent access to registers via both physical layers, as there is no arbitration/ semaphore mechanism. As such, using the two interfaces simultaneously may result in unpredictable behavior and is not recommended

5.13.1.1 *SPI target*

The registers of the L9965C/L99BM2C can be accessed by the MCU when it is NORMAL state, performing read/ write operations through SPI.

SPI port is available for communication only in NORMAL functional state. In DEEP_SLEEP, STANDBY and CYCLIC_WAKEUP states only NCS and SCLK pins are active to recognize the wake-up sequence.

The SPI target peripheral pins and settings are described in Table 52.

Table 52. **SPI target pin description**

Pin	Function	I/O type	Notes	Active states
GPIO0_NCS0	Chip Select	Digital In	weak pullup R_{IN_PU}	DEEP_SLEEP, STANDBY and CYCLIC_WAKEUP (to recognize the wake-up sequence) NORMAL
GPIO2_SDI	Serial Data Input	Digital In	weak pulldown R_{IN_PD} (1)	NORMAL
GPIO3_SDO	Serial Data Output	Digital Out	The output buffer is connected to VIO	NORMAL
GPIO4_SCLK	Serial Clock	Digital In	weak pulldown R_{IN_PD} (1)	DEEP_SLEEP, STANDBY and CYCLIC_WAKEUP (to recognize the wake-up sequence) NORMAL

1. *Weak pull-down resistors on SDI and SCLK pins and weak pull-up on NCS pin are always enabled to address open failures.*

Table 53. **SPI target quick look overview**

Parameter	Description
Protocol	Out of frame
Single Frame Length	40 bit
Frame protection	6 bit CRC
Max. Frequency	2 MHz
CPOL	0
CPHA	1

The SPI communication is covered by several checks, described in Table 54. In case the frame received by L9965C/L99BM2C on SPI is not correct, it is discarded, the corresponding error bit is asserted in the status register COMM_ERR, and at successive SPI access an SPI ERROR frame is issued with a specific bit set according to the error.

Table 54. **SPI Errors**

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
SPI VIF_ID ERR	Wrong VIF ID in previous received frame	• Frame is discarded • VIF_ID_ERR = 1 in COMM_ERR • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
SPI COMM_CRC ERR	Wrong CRC in previous received frame	• Frame is discarded • COMM_CRC_ERR = 1 in COMM_ERR • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI WRONG_ADDR	Wrong address in previous received frame	• Frame is discarded • WRONG_ADDR = 1 in COMM_ERR • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI SHORT_FRAME	Short frame error (previous frame shorter than 40 bit)	• Frame is discarded • SHORT_FRAME = 1 in COMM_ERR • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI LONG_FRAME	Long frame error (previous frame longer than 40 bit)	• Frame is discarded • LONG_FRAME = 1 in COMM_ERR • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No

5.13.1.1.1 Electrical parameters

The SPI timings shown in are reported in .

Figure 19. **SPI Target timing diagram**

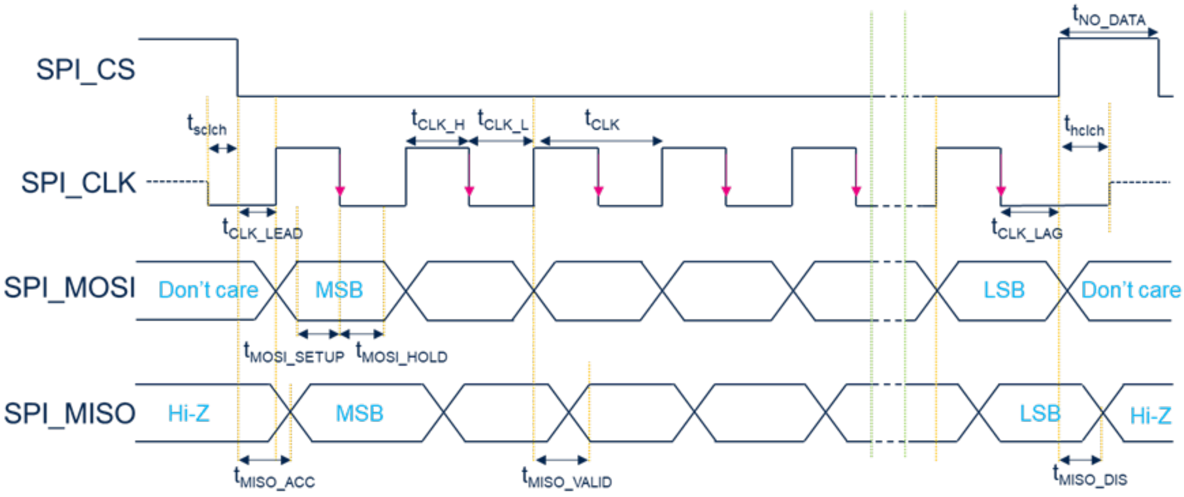


Table 55. **SPI Target electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	PIN
f_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info			2	MHz	NCS, SDI, SDO, SCLK
t_{CLK_L}	Time interval for CLK = LOW	Application info	210			ns	NCS, SDI, SDO, SCLK
t_{CLK_H}	Time interval for CLK = HIGH	Application info	210			ns	NCS, SDI, SDO, SCLK
t_{MISO_VALID}	Propagation delay (time passed after propagating SCLK edge @ at SDO active)	Cload=60pF			150	ns	NCS, SDI, SDO, SCLK
t_{CLK_LEAD}	time passed after NCS H/L edge @ first SCLK edge	Application info	200			ns	NCS, SDI, SDO, SCLK

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	PIN
t_{MOSI_SETUP}	SDI input setup time (time passed after SDI data valid @ sampling SCLK edge)	Application info	50			ns	NCS, SDI, SDO, SCLK
t_{MOSI_HOLD}	SDI input hold time (time passed after propagating SCLK edge @ SDI data “not valid anymore”)	Application info	50			ns	NCS, SDI, SDO, SCLK
t_{CLK_SETUP}	Time passed after CLK -> CPOL @ NCS H/L edge	FCLK_SPI = 2 MHz	200			ns	NCS, SDI, SDO, SCLK
t_{CLK_LAG}	Time passed after CLK -> CPOL @ NCS L/H edge	FCLK_SPI = 2 MHz	200			ns	NCS, SDI, SDO, SCLK
t_{CLK_SETUP}	CLK high after NCS high	FCLK_SPI = 2 MHz	200			ns	NCS, SDI, SDO, SCLK
T_{NO_DATA}	NCS min high time	FCLK_SPI = 2 MHz	8.25			us	NCS, SDI, SDO, SCLK
t_{MISO_DIS}	NCS L/H to SDO @ high impedance	FCLK_SPI = 2 MHz Cload=60pF			100	ns	NCS, SDI, SDO, SCLK
t_{MISO_ACC}	NCS H/L to SDO active	FCLK_SPI = 10 MHz Cload=60pF			100	ns	NCS, SDI, SDO, SCLK
V_{IN_H}	Logic input high voltage		2			V	SCLK, SDI NCS
V_{IN_HYS}	Input hysteresis		0.1		0.5	V	SCLK, SDI NCS
R_{IN_PD}	Input pulldown resistor. Applies to SCLK, SDI		0.4	1	1.6	MΩ	SCLK SDI
R_{IN_PU}	Input pullup resistor. Applies to NCS		0.4	1	1.6	MΩ	NCS

5.13.1.2 *Isolated Vertical Interface (VIF)*

The IC integrates two isolated communication ports (ISOL and ISOH) to interface up to N_{VIF_STACK} devices in daisy chain by isolated cables twisted pair (VIF).

The VIF supports capacitive to capacitive, transformer to transformer, transformer to capacity and vice-versa communication isolation in single access or dual ring daisy-chain for enhanced safety.

The VIF receiver port is always enabled, regardless of the device operating state, and the sensitivity to received commands depends upon the device state as reported in Table 56. VIF receivers and transmitters are, however, disabled, in case under-voltage, or over-voltage faults are detected on V5V output regulator, to protect the communication integrity.

More precisely, each port features two VIF receivers:

- A wakeup receiver, sensing and decoding FAULT/WAKEUP and CYCLIC WAKEUP tones, which are only used to generate FSM transitions but have no effect on the device register configuration
- A main receiver, sensing and decoding functional VIF frames in NORMAL state

Table 56. VIF receiver sensitivity

FSM State	Wakeup RX	Main RX
DEEP SLEEP/STANDBY	Used	Disabled
CYCLIC_WAKEUP	Not used	Used
NORMAL	Not used	Used

For the FAULT/WAKEUP and CYCLIC_WAKEUP tones, refer to Table 64.

The VIF transmitter is enabled according to the GENERAL_REG.ISO<x>_TX_EN configuration bit and to the device state, as listed in Table 57 (by default ISOL_TX_EN=1 and ISOH_TX_EN=1):

Table 57. **ISO Transmitter (TX) Interface enable conditions**

VIF_ID	FSM_STATE	ISO<x>_TX_EN	ISO TX state	Note
0	X	X	Disabled	Addressing procedure required (see Addressing Procedure)
X	DEEP SLEEP STANDBY	X	Disabled	
X	CYCLIC_WAKEUP	X	Enabled	The passthrough between ISOL/ISOH is disabled
≠0	NORMAL	0	Disabled	
≠0	NORMAL	1	Enabled (default at POR_MAIN)	

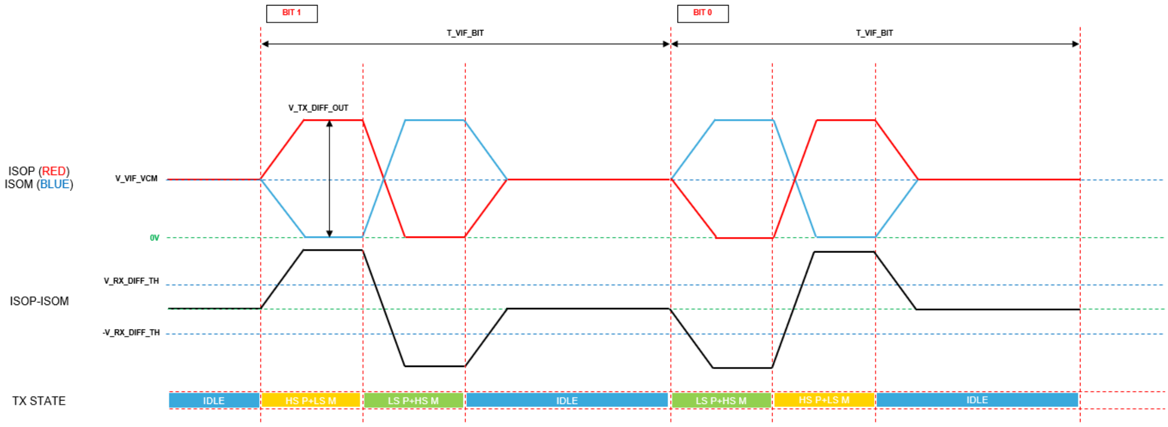
The MCU may selectively enable/disable the ISOL/ISOH transmitters in order to implement dual access commands (refer to Section 5.13.1.2.2).

In a VIF port, both positive and negative terminals are biased to a V_{VIF_CM} common mode voltage, and the information is encoded in the differential signal by a proprietary protocol with the following logic, where each bit lasts T_{VIF_BIT}:

- A negative to positive transition indicates a logic ‘0’
- A positive to negative transition indicates a logic ‘1’.

Signals at the ISO port terminals are normally in the V_{VIF_CM} +/- ($V_{RX\_DIFF\_RANGE}$/2) range, as shown in Figure 20.

Figure 20. **VIF Waveform**



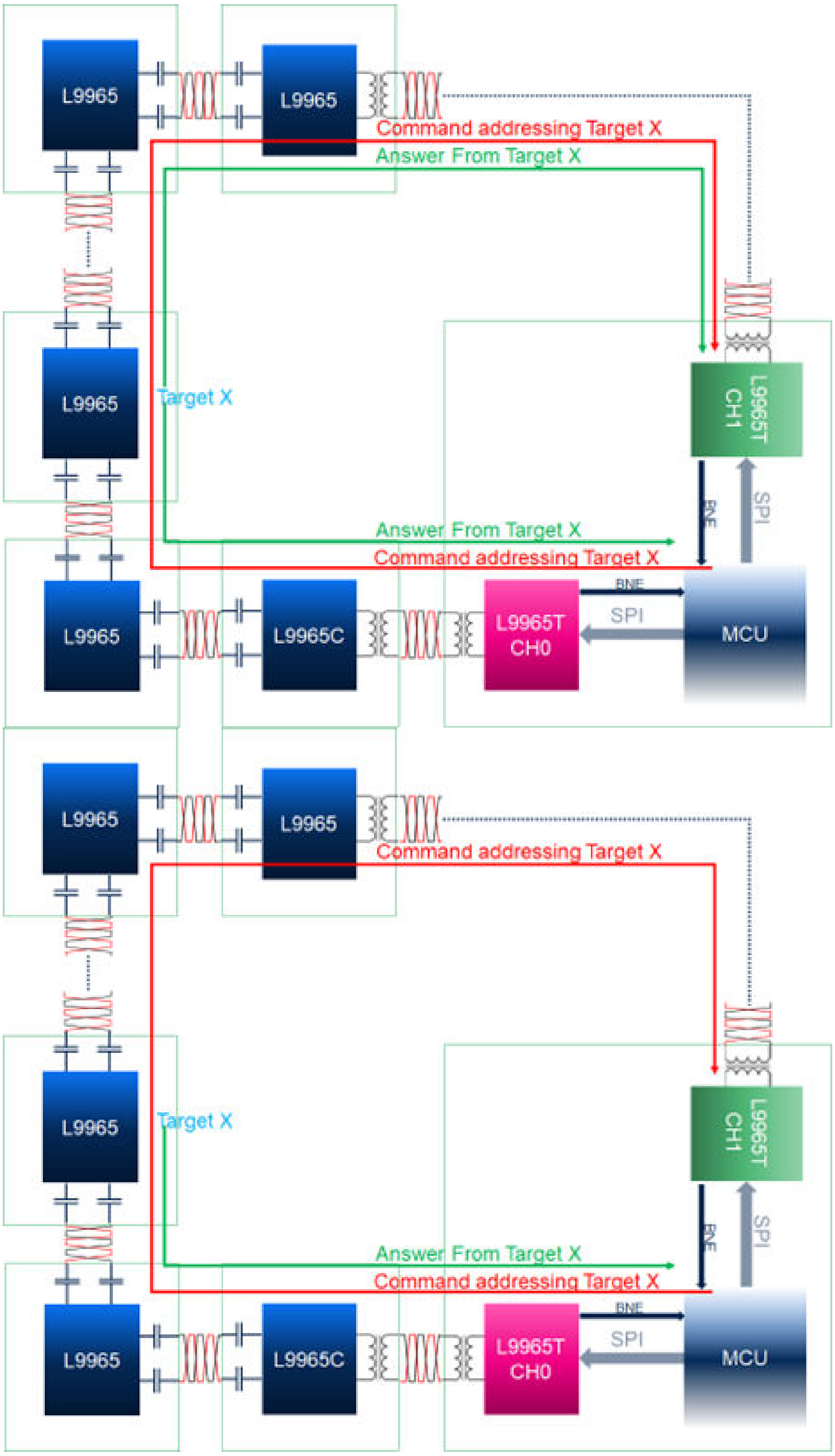
The TX circuit has a $R_{TX\_DIFF\_OUT}$ differential output impedance and shall be terminated using R_{TERM} resistors. Additional external components like DTVS, RVIF_FIL and CVIF_FIL are needed in order to withstand hot plug and pass BCI trials.

5.13.1.2.1 Monodirectional/bidirectional answers

When answering commands, the IC can be configured for generating either mono or bi-directional answers:

- When BIDI_ANSW = 1 (default) the IC generates bi-directional answers on both ISOH and ISOL ports
  - This strategy allows having full redundancy of the information on both channels of the L9965T/ L99BM2T transceiver
  - It is only meaningful when a dual-ring architecture is put in place
- When BIDI_ANSW = 0 the IC answers using the same ISO port that received the command
  - This strategy is recommended to optimize power consumption or when dual ring is not implemented
  - Implementing such strategy is mandatory when doubling the data-rate through simultaneous north/ south access (refer to Section 5.13.1.2.2).
  - To preserve pack balancing it is recommended to swap the dual ring access between consecutive sampling & readout routines.
    - For instance, at the nth thread tick time, the user SW sends a broadcast conversion command from the south side, and performs the data readout procedure accessing the dual ring always from the south side.
    - At the n+1th thread tick time, the user SW sends a broadcast conversion command from the north side, and performs the data readout procedure accessing the dual ring always from the north side.
    - This allows reaching perfect power balancing by equalizing the amount of usage of each target’s transmitters.

Figure 21. **Bidirectional answer (top) and Monodirectional answer (bottom)**



5.13.1.2.2 Single/dual access commands

When the VIF bus is realized through a dual ring, the architecture is designed to allow simultaneous access from the north/south side of the ring, thus enabling double data-rate.

As shown in Figure 22, the ring can be cut into two halves by disabling the transmitters between the X and the X+1th targets. This allows sending commands simultaneously from the south and north sides without creating conflicts.

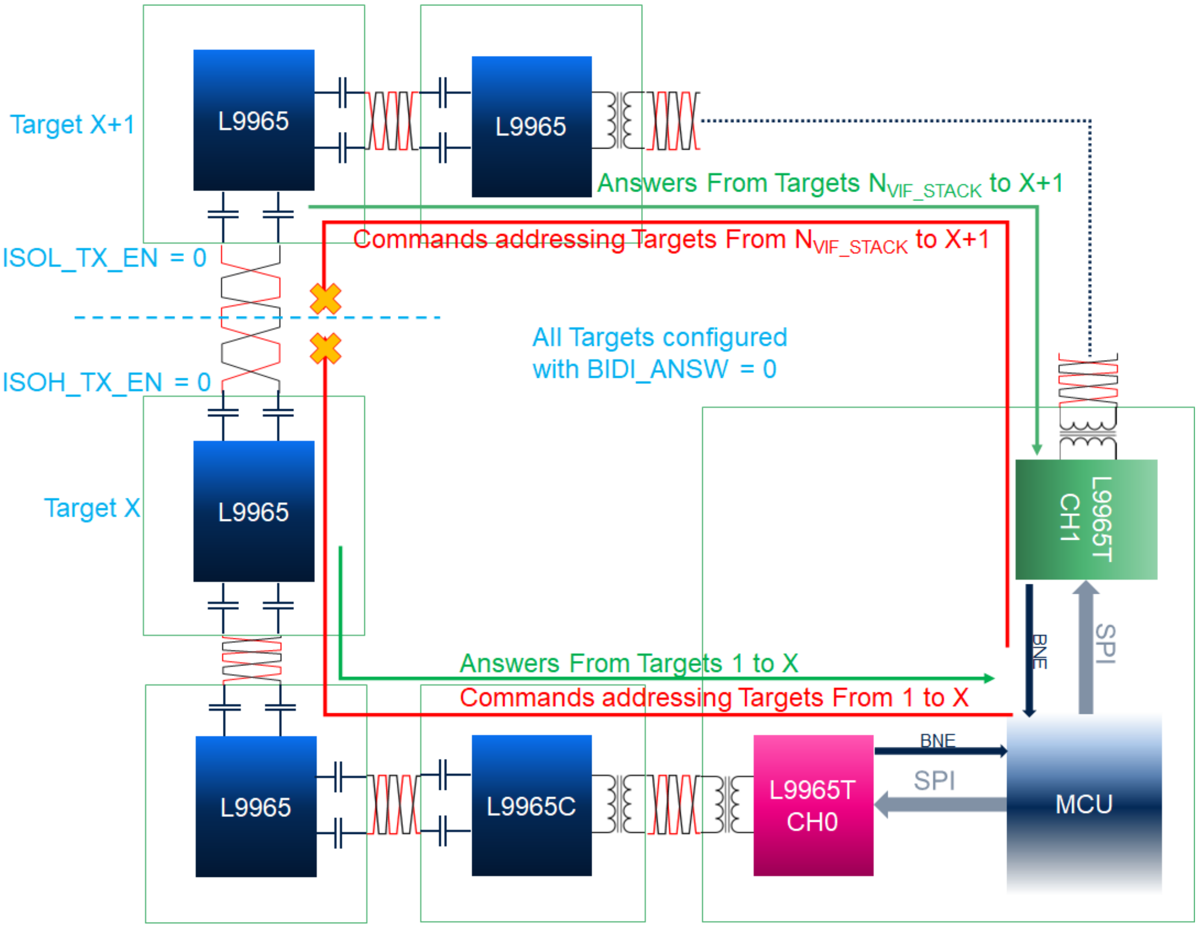
Having also configured the devices for monodirectional answers (BIDI_ANSW = 0, see Section 5.13.1.2.1), the different target answers simultaneously return to both sides of the dual ring and the MCU is able to retrieve the data from the corresponding RX queues of L9965T/L99BM2T.

Such strategy allows doubling the data-rate by maximizing the channel usage, thus enabling running conversion & readout threads with half the tick time.

As a minor drawback, a little unbalancing between packs may arise due to the different utilization of the transmitter between targets. For instance, when Target X answers, all targets below it re-transmit the frame in pass-through mode. However, when the Target X-1 answers, the Target X won’t be propagating the answer since the system works in monodirectional mode. Hence, the TX duty of the Target X is reduced in respect to the TX duty of the Target X-1. Such unbalancing can be effectively recovered through a pack balancing strategy.

Note: *To allow safe fault propagation in bidirectional mode and correct execution of the cyclic wakeup strategy, transmitters are always re-enabled every time the IC transitions to CYCLIC WAKEUP or NORMAL. Hence, once the BMS controller wakes up the system, the daisy-chain needs always to be re-split into two halves before running the threads in dual access mode. Such operation is quick and only requires two additional ISO frames.*

Figure 22. **Double data rate using dual access commands**



5.13.1.2.3 VIF errors and events management

The error and status bits related to VIF communication are reported in Table 58 below.

For the communication protocol please refer to Protocol Layer.

Table 58. **VIF diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
VIF CRC Error	VIF communication wrong CRC error (previous frame received on VIF port has wrong CRC)	• Frame is discarded • COMM_CRC_ERR = 1 in COMM_ERR register • SPI FAULT bit is asserted in NORMAL	Clear on read	COMM_CRC_ERR flag non maskable
VIF Short Frame	VIF communication short frame error (frame received on VIF port is shorter than 40 bit)	• Frame is discarded • SHORT_FRAME = 1 in COMM_ERR register • SPI FAULT is asserted in NORMAL	Clear on read	SHORT_FRAME flag non maskable
VIF Long Frame	VIF communication short frame error (frame received on VIF port is longer than 40 bit)	• Frame is discarded • LONG_FRAME = 1 in COMM_ERR register • SPI FAULT is asserted in NORMAL	Clear on read	LONG_FRAME flag non maskable

5.13.1.2.4 Electrical parameters

Table 59. **VIF electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
N_{VIF_STACK}	Number of addressable devices stacked in a single daisy-chain (including transceiver and AFE ICs)	Application information. There are 64 available addresses, 5 of which are reserved for broadcast commands	1		59	devices	ISOHP, ISOHM, ISOLP, ISOLM
AWG	American wire gauge	Application information		24		-	ISOHP, ISOHM, ISOLP, ISOLM
Z_0	VIP cable characteristic impedance	Application information		120		Ω	ISOHP, ISOHM, ISOLP, ISOLM
L_{VIF_WIRE}	Maximum length of twisted pair cables between two VIF nodes, using the recommended AWG_{VIF_WIRE} size and supporting operation in high frequency	Application information			10	m	ISOHP, ISOHM, ISOLP, ISOLM
V_{VIF_CM}	ISO port positive/negative terminals common mode voltage	V_{VIF_CM} = (V5V - 0.7) / 2	0	V5V/2	V5V	V	ISOHP, ISOHM, ISOLP, ISOLM
$V_{TX\_DIFF\_OUT}$	TX output differential pulse	Using recommended R_{TERM} V5V=5V	0		V5V	V	ISOHP, ISOHM, ISOLP, ISOLM
T_{VIF_BIT}	VIF Bit time		230	250	270	ns	ISOHP, ISOHM, ISOLP, ISOLM
$T_{VIF\_LATENCY}$	VIF Insertion Delay. Latency introduced by the insertion of one IC in the daisy chain		115	125	135	ns	ISOHP, ISOHM, ISOLP, ISOLM

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$T_{VIF\_ANSW\_DELAY}$	VIF Answer Delay. Time interval between the receival of the last command bit and the generation of the 1st answer bit		8.1	8.8	9.5	us	ISOHP, ISOHM, ISOLP, ISOLM
$T_{VIF\_RX\_IDLE\_TIMEOUT}$	VIF RX IDLE condition timeout	Guaranteed by SCAN	1.725	1.875	2.025	us	ISOHP, ISOHM, ISOLP, ISOLM
$V_{RX\_DIFF\_THP}$	RX differential positive threshold		80	200	400	mV	ISOHP, ISOHM, ISOLP, ISOLM
$V_{RX\_DIFF\_THN}$	RX differential negative threshold		-400	-200	-80	mV	ISOHP, ISOHM, ISOLP, ISOLM
$V_{RX\_DIFF\_TH\_SLEEP}$	RX differential threshold - sleeep mode		45	90	135	,V	ISOHP, ISOHM, ISOLP, ISOLM
$R_{RX\_DIFF\_IN}$	RX differential input impedance	Tested in production	5.4	9	12.6	Ω	ISOx

5.13.2 Protocol Layer

This section defines the communication protocol layer. The protocol is 40 bits, out of frame.

Small differences depending on the chosen physical layer (SPI Target or Vertical Interface) are also highlighted in the following sections.

5.13.2.1 *Single Read/Write*

The frame format to send single read/write commands to L9965C/L99BM2C is shown in Table 60. All registers of the IC can be accessed performing single read/write operations.

Table 60. Single Read/Write frame format

<table>
<tr><th></th><th>39</th><th>38</th><th>37</th><th>36</th><th>35</th><th>34</th><th>33</th><th>32</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>MOSI</td><td>PA = 1</td><td>RW</td><td colspan="6">DEV_ID</td><td colspan="7">Address</td><td>RSVD</td><td colspan="18">Data write</td><td colspan="6">CRC</td></tr>
<tr><td>MISO</td><td>PA = 0</td><td>Compressed=0</td><td colspan="6">DEV_ID</td><td colspan="7">Address feedback</td><td>FAULT</td><td colspan="18">Data read</td><td colspan="6">CRC</td></tr>
</table>

The fields of the MOSI/MISO frames are described in Table 61:

Table 61. SPI frame field descriptions

Field	Size [bit]	Description	Value
P.A.	1	Data direction	0 = Answer from device 1 = Command from MCU
R/W	1	Read/Write request	0 = Read 1 = Write

Field	Size [bit]	Description	Value
Compressed	1	Compressed data type	0 = normal frame 1 = decompressed data from a compressed burst
DEV_ID	6	Address of the device object of the communication. Also used for broadcast commands.	[0-63]
Address Address feedback	7	Register address for the Read/Write operation. Also used for burst commands.	[0-127]
RSVD	1	Reserved	0
FAULT	1	Self-detected failure	1= failure in diagnostic routines 0= no failures
DATA WRITE	18	Specifies the register content to be written in Write operations. Don't care in Read operations	Read: X Write: [0 to 2^{18}-1]
DATA READ	18	Returns the register content in both Read/Write operations	[0 to 2^{18}-1]
CRC	6	Checksum	[0-63]

The fault/events bits contributing to the SPI MISO frame FAULT bit are reported in Table 62. Each fault condition is described in detail in the related paragraph.

Table 62. **List of fault flags included in the FAULT bit**

Event	Status bit	SPI FAULT	Mask
Error on I2C transmitter	I2C_MASTER.I2C_TX_ERR	X	
Error on I2C receiver	I2C_MASTER.I2C_RX_ACK_ERR	X	
Fail on the execution of ABIST for VADC	DIAG_STATUS1.VADC_AIN_BIST_FAIL	X	
Overcurrent event during DC-link Precharge	DIAG_STATUS1.DC_LINK_OVC_SAFE	X	DC_LINK_CFG_0.DC_LINK_CFG_OVC_SAFE_MSK
Analog BIST fail	DIAG_STATUS1.ABIST_FAIL	X	
GND Loss fail	DIAG_STATUS1.GND_LOSS_FAIL	X	
Oscillator fail	DIAG_STATUS1.OSC_FAIL	X	
V5V regulator undervoltage	DIAG_STATUS1.V5V_UV	X	
V5V regulator overvoltage	DIAG_STATUS1.V5V_OV	X	
Charge pump undervoltage	DIAG_STATUS1.VCP_UV	X	
Charge pump overvoltage	DIAG_STATUS1.VCP_OV	X	
VANA regulator undervoltage	DIAG_STATUS1.VANA_UV	X	
VANA regulator overvoltage	DIAG_STATUS1.VANA_OV	X	
VTREF regulator undervoltage	DIAG_STATUS1.VTREF_UV	X	
VTREF regulator overvoltage	DIAG_STATUS1.VTREF_OV	X	
VB pin undervoltage	DIAG_STATUS1.VB_UV	X	
Fail on the execution of ABIST on comparator GND loss and open load CSA0 and open load CSA1 (executed only in cyclic wakeup)	DIAG_STATUS2.ABIST_GND_LOSS_OL_FAIL	X	
Fail on the execution of ABIST on comparator CP_UV and CP_OV	DIAG_STATUS2.ABIST_CP_UV_OV_FAIL	X	

Event	Status bit	SPI FAULT	Mask
V5V overcurrent	DIAG_STATUS2.V5V_OC	X	
VANA overcurrent	DIAG_STATUS2.VANA_OC	X	
CRC cyclic on configuration bits	DIAG_STATUS2.CYC_CFG_CRC_FAIL	X	
CRC cyclic on trimming/calib bits	DIAG_STATUS2.CYC_TRIM_CAL_CRC_FAIL	X	
NVM CRC error on at least one trimming/calibration NVM sector.	DIAG_STATUS2.NVM_CRC_TRIM_CAL_FAIL	X	GENERAL_REG. NVM_CRC_FAIL_MSK
NVM CRC error on at least one configuration NVM sector.	DIAG_STATUS2.NVM_CRC_CFG_FAIL	X	GENERAL_REG. NVM_CRC_FAIL_MSK
Fail of cross-check between two temperatures conversions	DIAG_STATUS2.XCHECK_TEMP_FAIL	X	
Fail of clock monitor self test	DIAG_STATUS2.CLOCK_MON_SELFTEST_FAIL	X	
Fail of cross-check between SC0 and SC1 conversions	DIAG_STATUS2.XCHECK_SC_CONV_FAIL	X	
Fail of cross-check CSA self test	DIAG_STATUS2.XCHECK_CSA_SELFTEST_FAIL	X	
Fail of cross-check between CSA0 and CSA1 conversions	DIAG_STATUS2.XCHECK_ADC_INST_CC_FAIL	X	
Timeout for cyclic routine	DIAG_STATUS3.TIMEOUT_FSM_CYCLIC	X	
It is latched when the T_FLTIN_TIMEOUT time expires	DIAG_CSA_SC.FLTIN_TIME_OUT	X	
FLTIN is detected low for longer than T_FLTIN_DEGLITCH	DIAG_CSA_SC.FLTIN_DET	X	
Fail of short circuit in discharge for SC1	DIAG_CSA_SC.SC1_DCHG	X	SC_SET_CFG.SC1_FAULT_MSK (it masks the reaction on FAULT1)
Fail of short circuit in discharge for SC0	DIAG_CSA_SC.SC0_DCHG	X	SC_SET_CFG.SC1_FAULT_MSK (it masks the reaction on FAULT0)
Fail of Open Load on CSA1	DIAG_CSA_SC.CSA1_OPEN	X	
Fail of Open Load on CSA0	DIAG_CSA_SC.CSA0_OPEN	X	
Fail of overcurrent in charge for CSA1	DIAG_CSA_SC.OVC_CHG_1	X	
Fail of overcurrent in discharge for CSA1	DIAG_CSA_SC.OVC_DCHG_1	X	
Fail of overcurrent in charge for CSA0	DIAG_CSA_SC.OVC_CHG_0	X	
Fail of overcurrent in discharge for CSA0	DIAG_CSA_SC.OVC_DCHG_0	X	
Mismatch sample counter between CC and redundant logic	DIAG_STATUS_STBY.XCHECK_CC_DATA_VALID_FAIL	X	
Mismatch accumulation value between CC and redundant logic	DIAG_STATUS_STBY.XCHECK_CC_DATA_FAIL	X	
V5V overcurrent and overtemperature	DIAG_STATUS_STBY.V5V_OC_OT	X	
Mismatch wakeup pulse between CC and redundant logic	DIAG_STATUS_STBY.XCHECK_PLS_WAKEUP_FAIL	X	
Charge/discharge detection wakeup	DIAG_STATUS_STBY.CC_WUP	X	
Error of sample counter saturation	DIAG_STATUS_STBY.CC_SAT	X	

Event	Status bit	SPI FAULT	Mask
Communication wrong VIF ID error (see Section 5.13.1.2 for the list of fault cases handled by this bit)	COMM_ERR.VIF_ID_ERR	X	
Communication wrong CRC error (previous SDI frame was corrupted and it had a wrong CRC)	COMM_ERR.COMM_CRC_ERR	X	
Communication wrong address error (previous SDI frame was specifying an inexistent address)	COMM_ERR.WRONG_ADDR	X	
Communication short frame error (previous SDI frame was shorter than 40 bit)	COMM_ERR.SHORT_FRAME	X	
Communication short frame error (previous SDI frame was longer than 40 bit)	COMM_ERR.LONG_FRAME	X	

5.13.2.2 *Broadcast Write*

Broadcast write commands allow to perform simultaneous write on all devices or a subset.

The MCU can exploit different kinds of broadcast commands by programming the DEV_ID field of the MOSI (refer to Table 60). Every IC is sensitive to the following types of broadcast commands:

- Global broadcast
  - Purpose: for addressing, writing common configurations and executing common tasks for all devices in the stack.
  - DEV_ID = 0x0
- Selective broadcast
  - Purpose: for writing common configurations and executing common tasks for a specific subset of devices in the stack.
  - DEV_ID = 0x3C + BROADCAST_SEL<x>
  - BROADCAST_SEL<x> is a 2-bit field allowing to configure a specific address filter.
  - Two selective broadcast filters have been implemented.

If the DEV_ID field of the frame is equal to a global or selective broadcast filter, the IC accepts the frame and execute the write operation. Otherwise, the frame content is discarded and only used to refresh the Communication Timeout (COMM_TIM).

The IC generates no answer upon receipt of broadcast commands.

Table 63. Broadcast Write frame format

<table>
<tr><th></th><th>39</th><th>38</th><th>37</th><th>36</th><th>35</th><th>34</th><th>33</th><th>32</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>MOSI</td><td>PA = 1</td><td>RW = 1</td><td colspan="6">DEV_ID</td><td colspan="7">Address</td><td>RSVD</td><td colspan="18">Data write</td><td colspan="6">CRC</td></tr>
</table>

Using broadcast commands is only meaningful when the IC is stacked in a daisy chain and accessed via Isolated Vertical Interface (VIF). Nevertheless, to ensure SW portability, broadcast commands are also accepted by the SPI Target.

As reported in Table 63, broadcast commands generate no answer on the Isolated Vertical Interface (VIF).

5.13.2.3 *Special frames*

This section lists the special frames associated with specific events.

FAULT/WAKEUP frame and any functional frame refresh the Communication Timeout (COMM_TIM), if running.

Table 64. **Special frames**

Frame	Description	IC STATE	IC reaction upon frame receipt
0x0 (longer tone)	FAULT/WAKEUP frame. Can be sent by MCU simultaneously on both daisy-chain ends to wakeup the ICs. It is only propagated by the L9965T/ L99BM2T operating in SENDER mode. Can be autonomously sent by an IC that has self-detected a failure in STANDBY or CYCLIC WAKEUP operation. Such frame is not a functional packet and does not encode any meaningful data. It is characterized by a different number of bit and a different frequency	NORMAL	Frame is propagated on the opposite VIF port
		CYCLIC WAKEUP	Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ and frame is propagated on the opposite VIF port. Communication Timeout is restarted. Cyclic wakeup routine still runs in background until the end; if a fault is latched, no further FAULT/ WAKEUP frames are sent.
		STANDBY	Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ and frame is propagated on the opposite VIF port
		DEEP SLEEP	Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ and frame is propagated on the opposite VIF port
0x0 (shorter tone)	CYCLIC WAKEUP frame. Can be autonomously sent by L9965T/L99BM2T transceiver when in CYCLIC WAKEUP state Such frame is not a functional packet and does not encode any meaningful data. It is characterized by a different number of bit and a different frequency.	NORMAL	Frame discarded
		CYCLIC WAKEUP	Frame discarded
		STANDBY	Device moves to CYCLIC WAKEUP within $T_{VIF\_WAKEUP\_TIME}$ (frame propagation depends on the cyclic wakeup routine outcome)
		DEEP SLEEP	Device moves to CYCLIC WAKEUP within $T_{VIF\_WAKEUP\_TIME}$ (frame propagation depends on the cyclic wakeup routine outcome)
0x10	Default frame (only for SPI Target) Since the protocol is out of frame, this is the first answer issued by the IC after a wakeup condition moves it to NORMAL	NORMAL	NA (this is an answer frame)
Functional frame	Functional R/W frame	DEEP SLEEP/ STANDBY/ CYCLIC WAKEUP	Frame content discarded. Wakeup event generated.
		NORMAL	Frame decoded.
SPI ERROR frame. See Table 65	SPI ERROR frame Is issued by the IC when a wrong MOSI has been received on the SPI Target	Such frame will not travel on the Isolated Vertical Interface (VIF), since it is only generated by the SPI Target.	

Table 65. **SPI Error Frames**

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	PA = 0	BURST = 0	DEV_ID = 0x0						Address feedback = 0x7F							FAULT	0x0													WRONG VIF ID	WRONG ADDR	LONG	SHORT	CRC ERROR	CRC					

When the SPI Target is being used, if any of the following errors occur, the corresponding bit is set in the SPI error frame:

- WRONG ADDR: the previous MOSI was specifying a nonexistent Address field.
  - WRONG_ADDR latch set
- WRONG VIF ID: see Table 66 for a list of fault cases handled by this bit
  - VIF_ID_ERR latch set
- LONG: the previous MOSI was longer than 40 bits
  - LONG_FRAME latch set
- SHORT: the previous MOSI was shorter than 40 bits
  - SHORT_FRAME latch set
- CRC ERR: the previous MOSI was corrupted (wrong CRC decoded)
  - COMM_CRC_ERR latch set

Note: *These errors are set by any device on the daisy chain, regardless of its VIF_ID. For any device, communication error log is available in the COMM_ERR register (address 0x41). However, devices configured in VIF mode will not generate any error frame answer. Such frame is only generated when IC is configured in SPI mode, as reported in Table 64.*

5.13.2.4 *Addressing Procedure*

After first powerup every device holds an address (VIF_ID) equal to 0x0 (see Table 60) and starts with the ISOH transmitter disabled (ISOH_TX_EN = 0).

To allow a correct addressing procedure, all the ICs in the daisy chain shall be oriented with the ISOH port connected to the ISOL port of the upper device.

The BMS Master shall access the daisy-chain from the bottom-side and the following Procedure 5: VIF Addressing shall be put in place to perform daisy chain addressing:

Procedure 5: VIF Addressing

For every device on the daisy chain [x=1.. N_{VIF_STACK}]:

1. Send a broadcast command with DEV_ID = 0 to disable the Configuration Integrity Check (CONF_CRC). The command only reaches up to the x-th device of the chain and won't be propagated to upper devices since the x-th device has the ISOH transmitter disabled.
2. Send a broadcast command with DEV_ID = 0 to remove the Configuration Lock;
3. Send a broadcast command with DEV_ID = 0 to program the desired VIF_ID value. Now any command will also reach the x+1th device (which is still holding VIF_ID = 0)
4. (optional, for L9965A BMIC only) Send an addressed write command with DEV_ID = x to program the mailbox BROADCAST_SEL<x> shared by every BMIC device (e.g. BROADCAST_SEL_0 = 0x1)
5. Send an addressed write command with DEV_ID = VIF_ID to program the mailbox BROADCAST_SEL<x> shared by BMIC (L9965A/L99BM218) and CSA (L9965C/L99BM2C) devices (e.g. BROADCAST_SEL_1 = 0x3).

To finalize the addressing, the following steps must be followed:

1. Send a broadcast command with DEV_ID = 0 to push the configuration in the NVM, using a Write command (see NVM Read/Write operations).
2. Send a broadcast command with DEV_ID = 0 to re-apply the Configuration Lock
3. Send a broadcast command with DEV_ID = 0 to re-enable the Configuration Integrity Check.

Once a device has been addressed with a DEV_ID different than the default (0x0), the VIF_ID field is no longer writable using global broadcast commands (DEV_ID = 0x0). This avoids inadvertent change of the VIF_ID while performing the addressing procedure.

Table 66. **Behavior according to DEV_ID**

Device VIF_ID	Received frame DEV_ID	READ CMD behavior	WRITE CMD behavior
SPI MODE			
0	0	Discard cmd and answer with VIF_ID error frame	Perform WRITE operation and answer with updated reg content
0	≠0	Discard cmd and answer with VIF_ID error frame	Discard cmd and answer with VIF_ID error frame
≠0	0	Discard cmd and answer with VIF_ID error frame	Perform WRITE operation and answer with updated reg content
≠0	Device VIF_ID	Perform READ operation and answer with reg content	Perform WRITE operation and answer with updated reg content
≠0	Non-matching device VIF_ID	Discard cmd and answer with VIF_ID error frame	Discard cmd and answer with VIF_ID error frame
≠0	≠0 (matching mailbox)	Discard cmd and answer with VIF_ID error frame	Perform WRITE operation and answer with updated reg content
VIF MODE			
0	0	Discard cmd and no answer (no passthrough since ISOH is disabled)	Perform WRITE operation and no answer (no passthrough since ISOH is disabled)
0	≠0	Discard cmd and no answer (no passthrough since ISOH is disabled)	Discard cmd and no answer (no passthrough since ISOH is disabled)
≠0	0	Discard cmd and no answer (passthrough if ISOH is enabled)	Perform WRITE operation and no answer (passthrough if ISOH is enabled)
≠0	Device VIF_ID	Perform READ operation and answer with reg content (passthrough if ISOH is enabled)	Perform WRITE operation and answer with updated reg content (passthrough if ISOH is enabled)
≠0	Non-matching device VIF_ID	Discard cmd and no answer (passthrough if ISOH is enabled)	Discard cmd and no answer (passthrough if ISOH is enabled)
≠0	≠0 (matching mailbox)	Discard cmd and no answer (passthrough if ISOH is enabled)	Perform WRITE operation and no answer (passthrough if ISOH is enabled)

5.13.2.5 *CRC*

Each frame is equipped with a 6-bit CRC code in order to guarantee information integrity. Whatever physical layer is used for communicating, corrupted commands (identified by P.A = 1, see Table 60) are discarded and won't refresh the Communication Timeout.

Table 67. **CRC Calculation Information**

Parameter	Value
Length	6 bit
Polynomial	$x^6 + x^5 + x^2 + x + 1$
Seed	0x38

The device answer depends on the physical layer:

- Corrupted frames received on the Isolated Vertical Interface (VIF) generate no answer.
- Corrupted frames received on the SPI Target result in the SPI ERROR special frame issued on the next iteration.

5.13.3 Communication Timeout (COMM_TIM)

The IC features a communication watchdog listening to messages incoming on the Isolated Vertical Interface (VIF) or SPI Target.

The watchdog timer is reset at every valid frame detection (correct frame length, no CRC error), regardless of the P.A. bit and VIF_ID (see Table 61).

Any frame recognized as a compressed burst (P.A. = 0 and BURST = 1) resets the communication timeout after the last bit of the sequence has been detected and the line is assessed idle.

If no valid frame is received for an interval longer than T_{COMM_TIM}, the COMM_TIM fault is latched, and the IC moves to a low power state according to the FSM shown in Figure 6.

The communication timeout is enabled by default and can be disabled programming DEV_GEN_CFG_1.COMM_TIM_EN = 0 and the value of the watchdog threshold T_{COMM_TIM} can be selected through DEV_GEN_CFG_1.COMM_TIM_TH.

The communication timeout is disabled when the Cyclic Wakeup routine is in progress.

5.13.3.1 Electrical parameters

Table 68. **Communication timeout electrical characteristics**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	Notes
$T_{COMM\_TIM\_00}$	Communication timeout threshold	COMM_TIM_TH = 00	80	100	130	ms	
$T_{COMM\_TIM\_01}$		COMM_TIM_TH = 01	400	500	600	ms	
$T_{COMM\_TIM\_10}$		COMM_TIM_TH = 10	0.8	1	1.2	s	
$T_{COMM\_TIM\_11}$		COMM_TIM_TH = 11 (default)	1.6	2	2.4	s	

5.13.4 Fault Notification (FAULT)

Self-detected faults are reported by the FAULT bit of the Protocol Layer. The FAULT bit being set to ‘1’ indicates the IC has self-detected a failure.

When in NORMAL state, a device that self-detects a failure does not take over the Isolated Vertical Interface (VIF). The MCU is supposed to poll the device within system FTTI, thus retrieving the fault status.

When in STANDBY or CYCLIC WAKEUP states, a device that self-detects a failure behaves as follows:

- Moves to NORMAL
- Takes over the Isolated Vertical Interface (VIF)
- Sends a FAULT/WAKEUP tone on both VIF ports
- The IC then waits for $T_{VIF\_RX\_IDLE\_TIMEOUT}$ for allowing lower and upper units on the daisy-chain, getting also to the RX IDLE state.
- Enables the VIF passthrough.

5.13.5 Wakeup Functions

The IC can be woken up via communication interfaces. There are three wakeup sources:

- Wakeup via VIF
  - In this scenario, the IC is daisy-chained on the VIF bus along with other companion chips, and can be woken up by Special Frames received on the Isolated Vertical Interface (VIF)
- Wakeup via SPI Target
  - In this scenario, the IC operates in a stand-alone module (e.g. 48V applications) and it is directly connected to the master MCU via SPI Target. Therefore, it can be woken up by dummy frames received on the SPI Target. This wakeup source is only available when the SPI_MODE field is configured as SPI Target.
- Self-Wakeup
  - In this scenario, wakeup trigger is generated internally by the IC low-power logic.

As explained in the Physical Layer section (Physical Layer), the VIF and SPI Target interfaces are considered mutually exclusive in application. In case the SPI Target is selected as the host communication interface, the Isolated Vertical Interface (VIF) pins shall be managed as explained in the Unused Pin section (Unused pins).

Whenever a wakeup source is validated, the wakeup sequence is initiated and shall successfully end within $T_{WAKEUP\_TIMEOUT}$. Otherwise, the IC returns to the previously held low power state.

5.13.5.1 *Electrical parameters*

Table 69. Global wakeup electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$T_{WAKEUP\_TIMEOUT}$	Timeout for completing the wakeup sequence[1]		20		25	ms

1. *Not valid for the first wake-up, since in this case the clock is not yet trimmed*

5.13.5.2 *Self-Wakeup*

When in low power modes (STANDBY) the IC is able to detect failures depending on CC_WUP diagnostic. In case this fault is detected, the IC triggers a self-wakeup in order to perform Fault Notification, (see Fault Notification (FAULT)). Such a wakeup is accomplished within T_{SELF_WAKEUP}.

5.13.5.2.1 Electrical parameters

Table 70. Self-wakeup electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_{SELF_WAKEUP}	Self-wakeup latency	From the assertion of a fault in low-power states to the device ready to communicate			1.8	ms

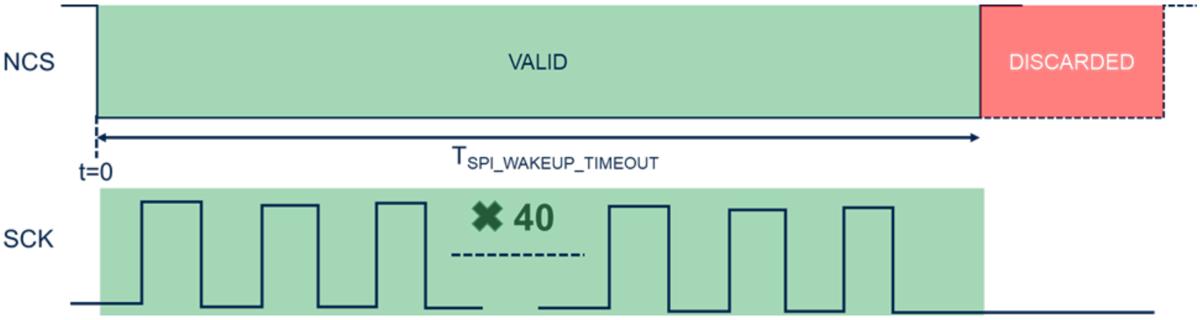
5.13.5.3 *Wakeup via SPI target*

When the SPI target is enabled, the IC can be woken up by any valid SPI frame. A wakeup condition is acknowledged when the following pattern is received:

1. A NCS high to low transition
2. 40 clock pulses
3. A NCS low to high transition

To prevent the logic being stuck in the wakeup detection state upon incomplete patterns, the $T_{SPI\_WAKEUP\_TIMEOUT}$ is started upon every NCS assertion, and the wakeup pattern shall end before timeout expiration, otherwise it is discarded.

Figure 23. Wakeup condition by SPI Target



Wakeup frames are not decoded: their content may be arbitrary. However, it is strongly recommended to send READ commands in order to avoid inadvertent write operations in case the device is already awake.

5.13.5.3.1 Electrical parameters

Table 71. **SPI wakeup parameters**

Symbol	Parameter	Tes condition	Min	Typ	Max	Unit
$T_{SPI\_WAKEUP\_TIMEOUT}$	Timeout for receival of wakeup frame		0.4		2	ms
T_{SPI_WAKEUP}	IC wakeup latency	From the NCS low to high transition to the IC in NORMAL state and ready to communicate			2	ms

5.13.5.4 Wakeup Via VIF

When in low power modes (DEEP SLEEP, STANDBY and CYCLIC WAKEUP) the IC is sensitive to wakeup signals incoming on both VIF ports (refer to Special frames).

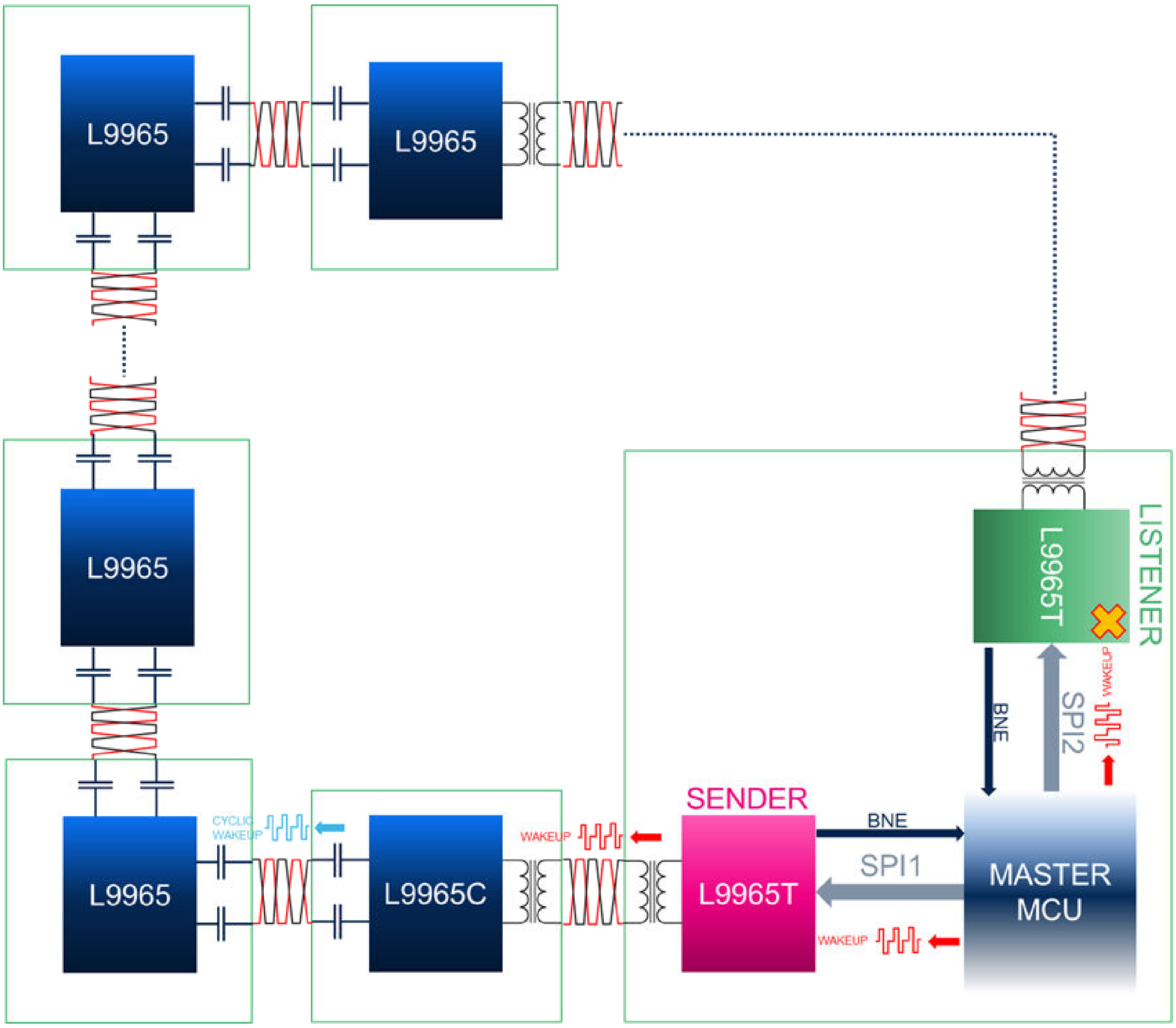
This section explains how the ICs react to wakeup signals in different application conditions. A brief summary of reaction is listed in Table 64.

5.13.5.4.1 Wakeup By MCU

The wakeup by MCU is an asynchronous event in respect to the cyclic wakeup thread managed in background by the L9965T/L99BM2T. As such, it shall be properly managed in order to avoid conflicts that may prevent a correct system wakeup.

Figure 24 shows a typical application scenario where the MCU wakes up the daisy-chain that was previously operating in CYCLIC WAKEUP mode.

Figure 24. Wakeup by MCU



A device generating a CYCLIC WAKEUP tone, while a FAULT/WAKEUP tone is arriving on the opposite port, first completes the transmission of the CYCLIC WAKEUP tone, and then, it will schedule the propagation of the FAULT/WAKEUP tone. This is possible since the VIF passthrough is disabled when in CYCLIC WAKEUP state.

Note: *If the Communication Timeout is enabled, the MCU is supposed to serve it as soon as it receives the wakeup interrupt from L9965T/L99BM2T. Otherwise, the ICs go back to low power state.*

5.13.5.4.2 Wakeup By Fault

The wakeup by fault is an asynchronous event in respect to the cyclic wakeup thread managed in background by the L9965T/L99BM2T. As such, it shall be properly managed in order to avoid conflicts that may prevent a correct system wakeup.

Figure 25 shows a typical application scenario where a BMIC has self-detected a fault and wakes up the daisy-chain sending FAULT/WAKEUP frame on both VIF ports.

Fault Notification (FAULT) has been designed to guarantee that FAULT/WAKEUP frame is correctly propagated at least in one direction, even in the remote case of a conflict with CYCLIC WAKEUP frame.

Depending on the position of the affected BMIC in the daisy chain, the wakeup interrupt reaches the MCU in approximately less than ½*N_{VIF_STACK}*$T_{VIF\_WAKEUP\_TIME}$, but in the worst case it may take up to N_{VIF_STACK}*$T_{VIF\_WAKEUP\_TIME}$ to complete whole daisy-chain wakeup.

When the MCU is woken up by a L9965T/L99BM2T, it is supposed to wait also for the other L9965T/L99BM2T to generate the FLT interrupt to confirm the daisy-chain wakeup. If such event does not occur within the N_{VIF_STACK}*$T_{VIF\_WAKEUP\_TIME}$ timeout, the MCU shall run the Wakeup By MCU procedure.

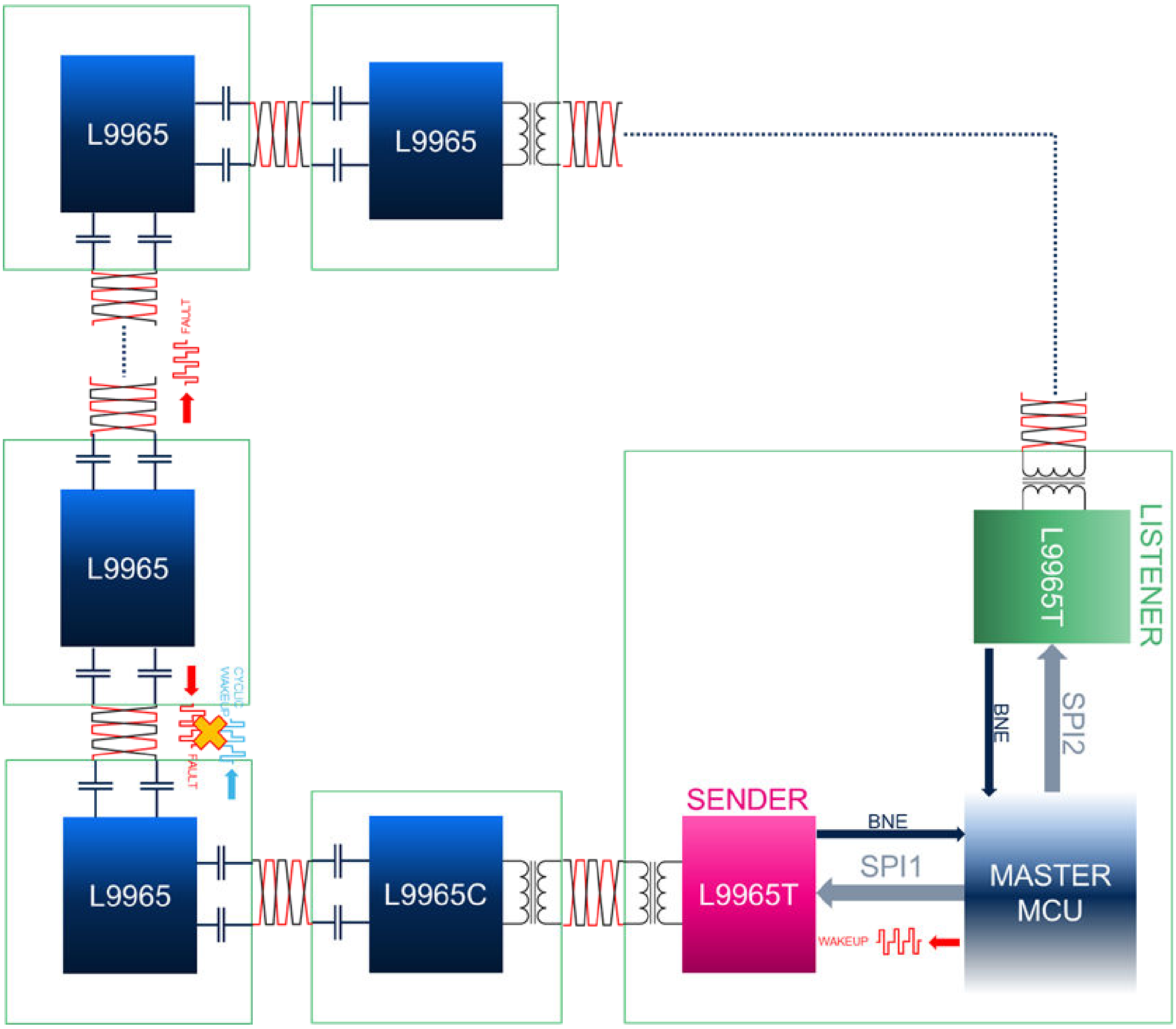


Figure 25. Wakeup by Fault

5.13.5.4.3 Wakeup By Cyclic Wakeup

When in low power modes (DEEP SLEEP or STANDBY) the IC is designed to support standalone operation without MCU intervention. Such operating mode (Cyclic Wakeup) is needed to keep monitoring the battery pack and the integrity of the system even when the system undergoes long periods of inactivity (e.g. vehicle parked and set for holiday mode).

The CYCLIC WAKEUP mode in dual ring configuration has been designed to offer high redundancy, being robust to any single failure point.

To address the cyclic wakeup operation mode, the MCU shall:

- Command all the ICs to DEEP SLEEP/STANDBY via a global broadcast GO2SLP.
- Move the L9965T/L99BM2T transceivers to CYCLIC WAKEUP state simultaneously.

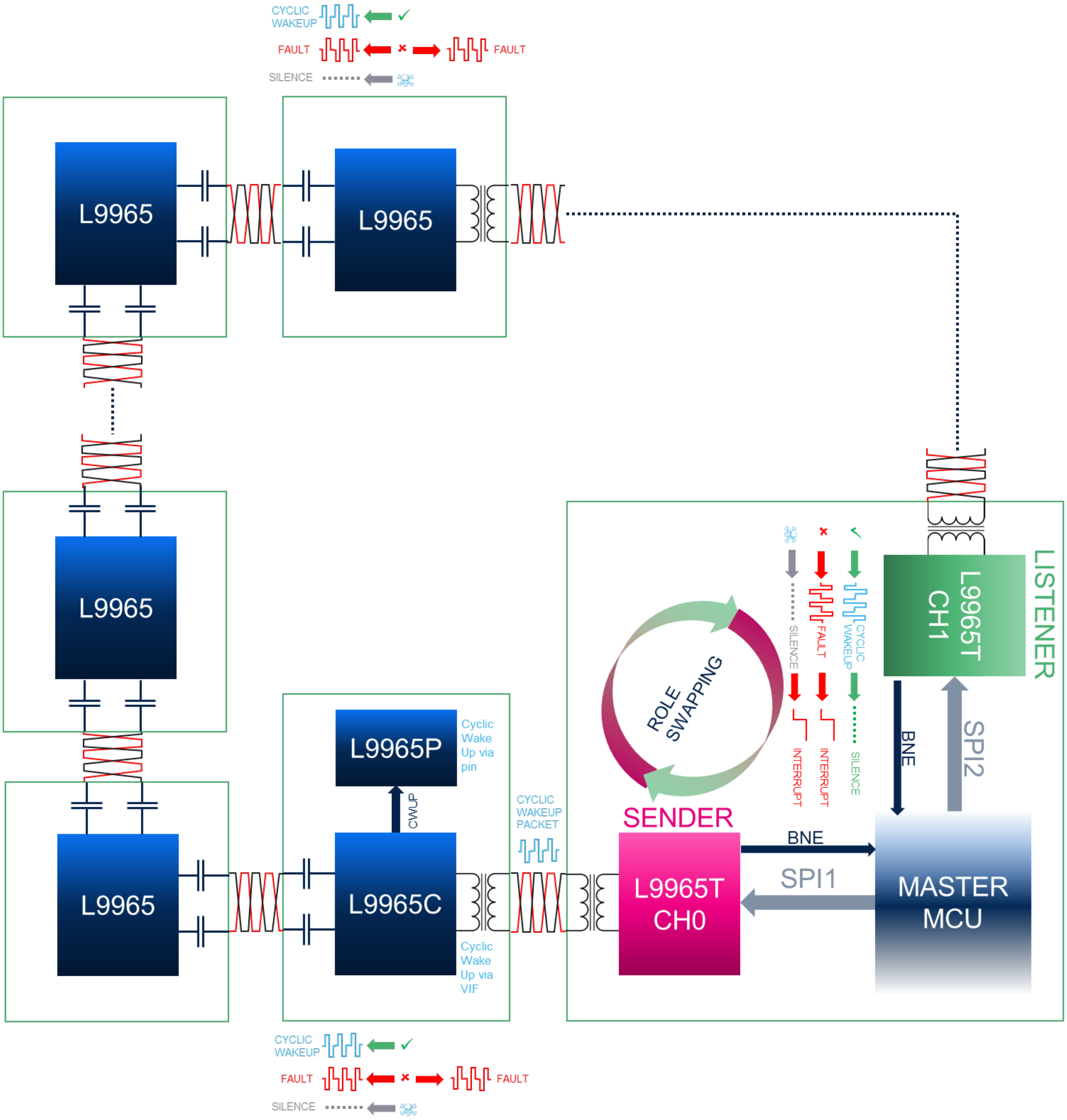
L9965C/L99BM2C CSA operates as follows:

- When the cyclic wakeup frame is received on a VIF port, it moves to CYCLIC WAKEUP and performs the following actions:
  - A routine is started, checking the following diagnostics:
    - Clock Monitor
    - ABIST on the following comparators: V5V_OV and V5V_UV, VTREF_OV and VTREF_UV, VANA_OV and VANA_UV, GND Loss, CSA Open Load
    - CSA Open Load diagnostic
    - GND Loss diagnostic
    - Temperature ADCs X-check
    - CSA ADCs X-check (only if both ADCs are enabled)
    - NVM download integrity check
    - NVM Cyclic CRC Check
    - Linear regulators voltage monitoring (V5V_UV and V5V_OV, VTREF_UV and VTREF_OV, VANA_UV and VANA_OV)
    - VB_UV monitoring
    - Overtemperature monitoring

The routine execution lasts $T_{CYCLIC\_ROUTINE\_DURATION}$, varying from a minimum time to a maximum time, according to the NVM enabling settings (CSA_OL_SET, CUR_INST_EN, CC_EN).

- After that, the outcome of the routine execution is evaluated
  - In case no failure has been detected, the cyclic wakeup frame is propagated on the opposite VIF port. After that, the IC moves back to the previously held low power state (DEEP SLEEP/STANDBY).
  - In case a failure (on one of the diagnostics listed above) has been detected, the flag GSW_CYC is set, the IC propagates on both sides Fault Notification (FAULT), at the end of the routine. The device goes to Normal State.
- If for any problems the routine does not terminate before $T_{CYCLIC\_ROUTINE\_TIMEOUT}$, the flag TIMEOUT_FSM_CYCLIC is asserted.
- During the entire Cyclic Wakeup the Communication Timeout is disabled.
- If during the Cyclic routine the device receives a Fault Wakeup notification, it propagates the Fault notification immediately, enables again the Communication Timeout and the access to the registers, the routine is not interrupted and continues until the end. At this point the device remains in Normal status independently on the routine results.
- It is recommended that the MCU does not write the registers involved in the routine (the configuration registers of the diagnostics described above) until the routine completion is reached (this can be monitored through the flag DIAG_STATUS3.CYC_ROUTINE_BUSY).

Figure 26. Cyclic wakeup operation



5.13.5.4.4 Electrical parameters

Table 72. VIF wakeup parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_{CYCLIC_WAKEUP}	Transceiver cyclic wakeup frame generation period	Sender mode		See L9965T/ L99BM2T DS		
$T_{CYCLIC\_WAKEUP\_TIMEOUT}$	Transceiver cyclic wakeup timeout	Listener mode		See L9965T/ L99BM2T DS		

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$T_{VIF\_WAKEUP\_TIME}$	IC wakeup latency	From the assertion of the VIF wakeup to the generation of the 1st wakeup pulse on the opposite VIF port			2	ms
$T_{CYCLIC\_ROUTINE\_DURATION}$		Guaranteed by design	45		260	ms
$T_{CYCLIC\_ROUTINE\_TIMEOUT}$		Guaranteed by scan	2	2.3	2.6	s

5.14 Communication Interfaces

5.14.1 SPI controller

The IC integrates a SPI Controller peripheral to manage connection to external sensors and NVMs. L9965P/L99BM2P companion chip can also be interfaced with L9965C/L99BM2C through SPI Controller Interface.

The SPI Controller peripheral pins and settings are described in Table 73.

Table 73. **SPI Controller pin description**

PIN	Function	I/O type	Notes	Active states
GPIO0_NCS0	Chip Select	Digital Out	The output buffer is connected to VIO	NORMAL
GPIO2_SDI	Serial Data Input	Digital In	weak pulldown R_{IN_PD}	NORMAL
GPIO3_SDO	Serial Data Output	Digital Out	The output buffer is connected to VIO	NORMAL
GPIO4_SCLK	Serial Clock	Digital Out	The output buffer is connected to VIO	NORMAL

Additionally, GPIO1_NCS1 can be configured as a 2nd chip select programming it as digital output and setting DEV_GEN_CFG_2.GPIO1_NCS1_EN = 1.

Weak pulldown is automatically enabled to address open failures on SDI pin.

The SPI peripheral can communicate with one SPI slave at a time, but if both Chip Selects (GPIO0_NCS0 and GPIO1_NCS1) had been configured as such, to actively drive high the Chip Selects in idle state, it is necessary setting respectively GPIO0_NCS0_ACTIVE_IDLE and GPIO1_NCS1_ACTIVE_IDLE configuration bits (DEV_GEN_CFG_2 register), otherwise pins are left in HiZ.

The SPI peripheral manages transfers using SPI_MISO and SPI_MOSI registers, whose size is 40 bit. In order to adapt to different protocols, the peripheral can be configured to handle frame sizes with multiples of 8 bit. Such configuration can be independently chosen for each of the two supported SPI Slaves. Frame size can be chosen programming SPI_MASTER.SPI_FRAME_SIZE<x> registers.

Table 74. **SPI Controller protocol configuration**

SPI_FRAME_SIZE<x>	Frame size
000	8 bits
001	16 bits
010	24 bits
011	32 bits
100	40 bits
101	40 bits
110	40 bits
111	40 bits

The MCU can trigger a SPI transfer writing SPI_MASTER.SPI_TRANSFER = 1, along with the desired SPI_MASTER.SPI_NCS<x> bit. Writing both SPI_NCS<x> to ‘1’ in the same frame is not allowed: command is discarded, and no transfer takes place. The same happens if a transfer is commanded while another is still ongoing. Only one slave transfer at a time can be managed.

Data on the SPI Controller bus is not decoded, and CRC errors and other safety mechanisms shall be managed by MCU.

The clock phase and polarity can be configured programming DEV_GEN_CFG_2.SPI_MASTER_CPOL<x> and DEV_GEN_CFG2.SPI_MASTER_CPHA<x> bit.

The MCU can verify that the SPI Master transmission has been completed monitoring the flag SPI_MASTER.SPI_MASTER_BUSY.

5.14.1.1 *Electrical Parameters*

Main Oscillator frequency according to operating range of Table 18.

Figure 27. SPI Controller timing diagram (example with CPOL = 0 & CPHA = 1)

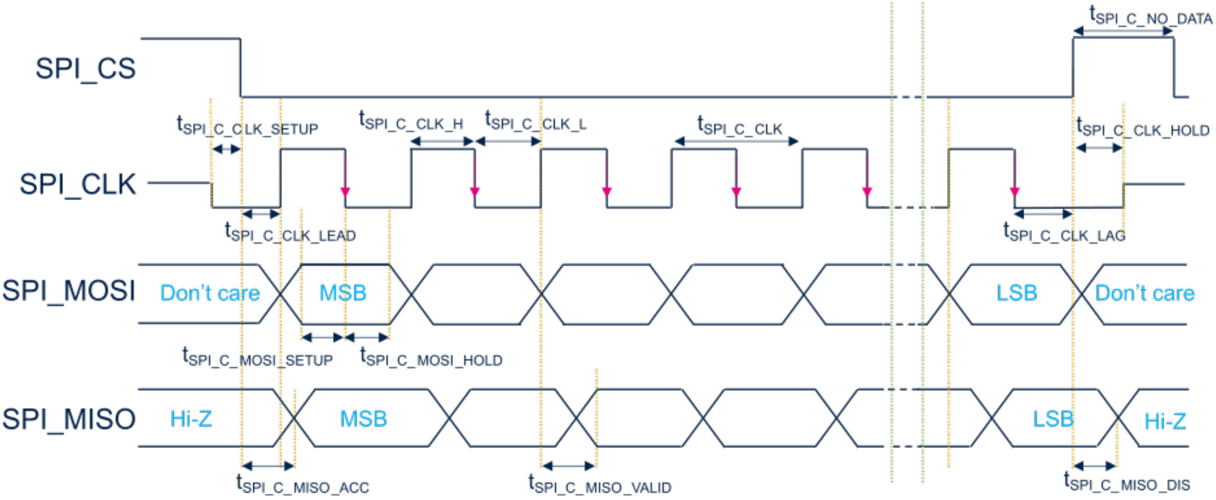


Table 75. SPI Controller electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$f_{SPI\_C\_CLK}$	SPI Controller Clock Frequency, $f_{SPI\_M\_CLK} = 1/t_{SPI\_C\_CLK}$			500		kHz	GPIO4_SCLK
$t_{SPI\_C\_CLK\_SETUP}$	Time passed after CLK -> CPOL @ NCS H/L edge	Cload=60pF	500			ns	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_CLK\_HOLD}$	Time passed after CLK -> CPOL @ NCS L/H edge	Cload=60pF	500			ns	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_CLK\_L}$	Minimum time CLK = LOW		900			ns	GPIO4_SCLK
$t_{SPI\_C\_CLK\_H}$	Minimum time CLK = HIGH		900			ns	GPIO4_SCLK
$t_{SPI\_C\_MISO\_VALID}$	Propagation delay (time passed after propagating SCLK edge @ SDI active)	Application Info			468.7	ns	GPIO2_SDI, GPIO4_SCLK
$t_{SPI\_C\_CLK\_LEAD}$	CLK toggle after NCS = low		4		7.72	us	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_MOSI\_SETUP}$	SDO setup time (time passed after SDO data valid @ sampling SCLK edge)		93.74			ns	GPIO3_SDO, GPIO4_SCLK

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
$t_{SPI\_C\_MOSI\_HOLD}$	SDO hold time (time passed after propagating SCLK edge @ SDO data “not valid anymore”)		93.74			ns	GPIO3_SDO, GPIO4_SCLK
$t_{SPI\_C\_CLK\_LAG}$	CLK toggle before NCS = high		4		7.72	us	GPIO0_NCS0, GPIO1_NCS1, GPIO4_SCLK
$t_{SPI\_C\_NO\_DATA}$	Inter-frame delay: minimum NCS inactive time between two consecutive frames		4			us	GPIO0_NCS0, GPIO1_NCS1
$t_{SPI\_C\_MISO\_DIS}$	NCS L/H to SDI high impedance	Application Info			1	us	GPIO0_NCS0, GPIO1_NCS1, GPIO2_SDI
$t_{SPI\_C\_MISO\_ACC}$	NCS H/L to SDI active	Application Info			3	us	GPIO0_NCS0, GPIO1_NCS1, GPIO2_SDI

The SPI Controller communication can be configured through the following parameters (register DEV_GEN_CFG_2) stored in the NVM Memory:

Procedure 6: SPI Master transmission sequence shows an example of the communication through the SPI Master.

Procedure 6: SPI Master transmission sequence

- Writing of the data to be sent on MOSI
  - SPI_MOSI_39_32: Fifth byte to send;
  - SPI_MOSI_31_24: Fourth byte to send;
  - SPI_MOSI_23_16: Third byte to send;
  - SPI_MOSI_15_8: Second byte to send;
  - SPI_MOSI_7_0: First byte to send.
- Setting of byte number and the NCS to be used:
  - SPI_FRAME_SIZE1: sets the frame size for SPI communication on GPIO1_NCS1 (000 – 8 bits; 001 – 16 bits; 010 – 24 bits; 011 – 32 bits; others – 40 bits);
  - SPI_FRAME_SIZE0: sets the frame size for SPI communication on GPIO0_NCS0. Same codifications as for SPI_FRAME_SIZE1;
  - SPI_NCS1: it selects GPIO1_NCS1 to be used as chip select for SPI Master Communication;
  - SPI_NCS0: it selects GPIO0_NCS0 to be used as chip select for SPI Master Communication;
  - ATTENTION: Setting SPI_NCS0 = 1 and SPI_NCS1 = 1 is not allowed;
- Launching of the signal triggering the start of communication
  - SPI_TRANSFER: it triggers the start of the transmission of SPI Communication. Since the device is the Master, it sends MOSI frame.
- Reading of SPI_MASTER register for checking the communication status. If SPI_MASTER_BUSY = 1, the SPI Master Communication is running.
- Once the communication is finished, MCU can read the MISO message received
  - SPI_MISO_39_32: Fifth byte received;
  - SPI_MISO_31_24: Fourth byte received;
  - SPI_MISO_23_16: Third byte received;
  - SPI_MISO_15_8: Second byte received;
  - SPI_MISO_7_0: First byte received.

5.14.2 I2C Controller

The IC integrates a I2C Controller peripheral to manage connection to external sensors and NVMs.

When enabled, the following pins are configured as I2C Controller:

- GPIO5_SDA_FLTIN → Chip Select (open drain)
- GPIO6_SCL_CWUP → Serial Clock (open drain)

The clock frequency can be configured programming DEV_GEN_CFG_2.I2C_MASTER_CLK bit.

The I2C peripheral manages transfers using I2C_DATA_IN and I2C_DATA_OUT registers, whose size is 32 bit. In order to adapt to different protocols, the peripheral can be configured to handle frame sizes with multiples of 8 bit. Frame size can be chosen programming I2C_FRAME_SIZE register.

MCU can trigger a I2C transfer writing I2C_MASTER.I2C_TRANSFER = 1. A transfer cannot be interrupted: concurrent triggers are discarded.

Data on the I2C bus is not decoded and CRC errors and other safety mechanisms shall be managed by MCU.

Here below, the fields used for setting the parameters, concerning the communication through I2C Controller, are summarized (I2C_MASTER register).

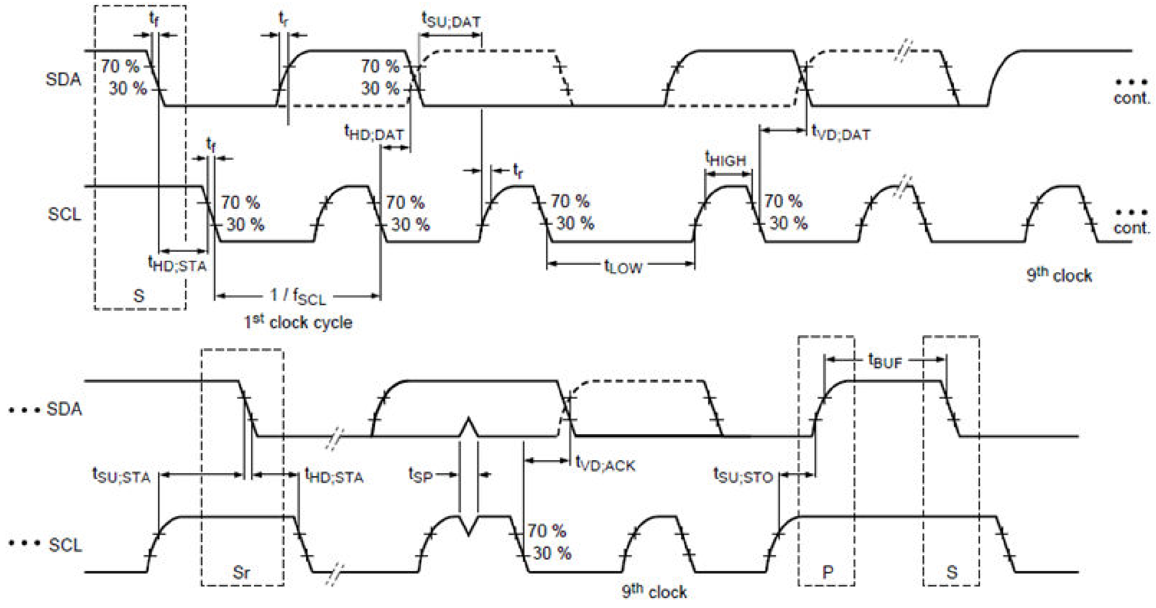
- I2C_STOP_AFTER_NACK: if it is set to 1, it sends a STOP after it has received/sent a NACK;
- I2C_FORCE_NACK: if it is set to 1, it forces a NACK (when the device drives NACK);
- I2C_RD_WRN: it defines which component (controller or target) takes the control of SDA line (0 – writing operation (controller); 1 – reading operation (target));
- I2C_OP_CODE: it codifies the operation required (3 bits field: bit2 – START; bit1 – DATA; bit0 – STOP. Codes 000, 100,101 are reserved);
- I2C_FRAME_SIZE: it sets the frame size for I2C communication (00 – 1 byte; 01 – 2 bytes; 10 – 3 bytes; 11 – 4 bytes. For handling 40-bits frames, bytes must be sent in two times);
- I2C_TRANSFER: if it is set to 1, it triggers the starting of I2C Communication (the device is the controller).

Two bits are available to check if something went wrong during reading/writing operation:

- I2C_MASTER.I2C_TX_ERR: if this flag is asserted, the data has not been sent correctly on SDA line;
- I2C_MASTER.I2C_RX_ACK_ERR: if this flag is asserted, an error on the receiver acknowledgment occurred.

5.14.2.1 Electrical Parameters

Figure 28. **I2C Controller timing**



$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

Table 76. **I2C Controller electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
f_{I2C_CLK0}	I2C Controller Clock Frequency	I2C_MASTER_CLK = 0	40	62.5	100	kHz	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
f_{I2C_CLK1}	I2C Controller Clock Frequency	I2C_MASTER_CLK = 1	200	250	400	kHz	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{LOW_0}	LOW period of the SCL clock	f_{I2C_CLK0} = 100kHz	4.26		12.75	us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{LOW_1}	LOW period of the SCL clock	f_{I2C_CLK1} = 400kHz	1.18		2.75	us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{HIGH_0}	HIGH period of the SCL clock	f_{I2C_CLK0} = 100kHz	4.26		12.75	us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{HIGH_1}	HIGH period of the SCL clock	f_{I2C_CLK1} = 400kHz	1.18		2.75	us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{HD_STA}	SCL hold (High) time, after SDA falling edge has created the START condition, for the START condition to be correctly detected		0.6			us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{SU_STA}	SCL set-up time to High (SDA already High) before SDA falling edge creates the START condition sequence (by falling when SCL is steadily high)		0.6			us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{HD_DAT}	SDA hold time after SCL falling edge		300		-	ns	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{SU_DAT}	SDA set-up time before SCL rising edge		100		-	ns	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_r	Rise time of SDA signal	With 4.7kΩ pullup resistor and 40pF load	0		300	ns	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_f	Fall time of SDA signal	With 4.7kΩ pullup resistor and 40pF load	0		300	ns	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{rf_SCL}	Rise/fall time SCL signal		0		300	ns	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{SU_STO}	SCL set-up time to High (SDA already Low) before SDA rising edge creates the STOP condition sequence (by rising when SCL is steadily high)		0.6			us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{HD_STO}	SCL hold (High) time, after SDA rising edge has created the STOP condition, for the STOP condition to be correctly detected		0.6			us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
t_{BUF}	Bus free time between a STOP and START condition		1.3			us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
C_b	Capacitive load for each bus line				400	pF	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP
$t_{VD\_DAT\_ACK}$	Data (ACK) valid time				0.9	us	GPIO5_SDA_FLTIN, GPIO6_SCL_CWUP

It is possible to set, in NVM memory, the I2C master clock frequency, through the bit DEV_GEN_CFG_2.I2C_MASTER_CLK (0 = 62.5 kHz, 1 = 250 kHz).

Four examples of procedure for communicating through I2C Master are shown, covering the case of reading, writing, in the case of up to 4 bytes and in the case of more than 4 bytes.

Procedure 7: I2C Master Transmission sequence (Write 3-bytes message)

- Writing of the data to be sent
  - I2C_TX_BYTE_0: First byte to send; [write device address of slave + 0 (write command bit)]
  - I2C_TX_BYTE_1: Second byte to send;
  - I2C_TX_BYTE_2: Third byte to send;
- Setting of I2C communication parameters and launching of the signal triggering the start of communication
  - I2C_STOP_AFTER_NACK = 0
  - I2C_FORCE_NACK = 0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 111
  - I2C_FRAME_SIZE = 10
  - I2C_TRANSFER = 1
- Checking of communication. If I2C_TX_ERR flag is asserted, the data has not been sent correctly on SDA.

Procedure 8: I2C Master Transmission sequence (Read of 3-bytes message)

- Writing of the data to be sent in order to set the reading address
  - I2C_TX_BYTE_0: First byte to send; [write device address of slave + 0 (write command bit)]
  - I2C_TX_BYTE_1: Second byte to send. [write register address of slave];
- Launching of the trigger for starting the READ communication
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 110
  - I2C_FRAME_SIZE = 01
  - I2C_TRANSFER = 1
- Writing of device address for preparing the reading: I2C_TX_BYTE_0 must be written with device address of slave + 1 (read command bit)
- Launching of the trigger for indicating device address + read command bit
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 110
  - I2C_FRAME_SIZE = 00
  - I2C_TRANSFER = 1
- Launching of the trigger for starting READ
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 1
  - I2C_OP_CODE = 011
  - I2C_FRAME_SIZE = 10
  - I2C_TRANSFER = 1
- Reading of the received message
  - I2C_RX_BYTE_0: first byte to receive;
  - I2C_RX_BYTE_1: second byte to receive;
  - I2C_RX_BYTE_2: third byte to receive
- Checking of communication.
  - If I2C_TX_ERR flag is asserted, the data has not been sent correctly on SDA;
  - If I2C_RX_ACK_ERR flag is asserted, an error in the receiver acknowledgement occurred.

Procedure 9: I2C Master Transmission sequence (Write 5-bytes message)

- Writing of the data to be sent covering the first four bytes
  - I2C_TX_BYTE_0: First byte to send; [write device address of slave + 0 (write command bit)]
  - I2C_TX_BYTE_1: Second byte to send;
  - I2C_TX_BYTE_2: Third byte to send;
  - I2C_TX_BYTE_3: Fourth byte to send
- Setting of I2C communication parameters and launching of the signal triggering the start of communication for the first 4 bytes
  - I2C_STOP_AFTER_NACK = 0
  - I2C_FORCE_NACK = 0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 110
  - I2C_FRAME_SIZE = 11
  - I2C_TRANSFER = 1
- Writing of the data to be sent for the fifth byte
  - I2C_TX_BYTE_0: Fifth byte to send
- Setting of I2C communication parameters and launching of the signal triggering the start of communication for the fifth byte
  - I2C_STOP_AFTER_NACK = 0
  - I2C_FORCE_NACK = 0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 011
  - I2C_FRAME_SIZE = 00
  - I2C_TRANSFER = 1
- Checking of communication. If I2C_TX_ERR flag is asserted, the data has not been sent correctly on SDA.

Procedure 10: I2C Master Transmission sequence (Read of 5-bytes message)

- Writing of the data to be sent in order to set the reading address
  - I2C_TX_BYTE_0: First byte to send; [write device address of slave + 0 (write command bit)]
  - I2C_TX_BYTE_1: Second byte to send. [write register address of slave];
- Launching of the trigger for starting the READ communication
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 110
  - I2C_FRAME_SIZE = 01
  - I2C_TRANSFER = 1
- Writing of device address for preparing the reading: I2C_TX_BYTE_0 must be written with device address of slave + 1 (read command bit)
- Launching of the trigger for indicating device address + read command bit
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 0
  - I2C_OP_CODE = 110
  - I2C_FRAME_SIZE = 00
  - I2C_TRANSFER = 1
- Launching of the trigger for starting READ (first four bytes)
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 1
  - I2C_OP_CODE = 010
  - I2C_FRAME_SIZE = 11
  - I2C_TRANSFER = 1
- Reading of the received message (first four bytes)
  - I2C_RX_BYTE_0: first byte to receive;
  - I2C_RX_BYTE_1: second byte to receive;
  - I2C_RX_BYTE_2: third byte to receive;
  - I2C_RX_BYTE_3: fourth byte to receive.
- Launching of the trigger for starting READ (fifth byte)
  - I2C_STOP_AFTER_NACK =0
  - I2C_FORCE_NACK =0
  - I2C_RD_WR_N = 1
  - I2C_OP_CODE = 011
  - I2C_FRAME_SIZE = 00
  - I2C_TRANSFER = 1
- Reading of the received message (fifth byte)
  - I2C_RX_BYTE_0: fifth byte to receive
- Checking of communication.
  - If I2C_TX_ERR flag is asserted, the data has not been sent correctly on SDA;
  - If I2C_RX_ACK_ERR flag is asserted, an error in the receiver acknowledgement occurred.

5.15 Configuration lock

To prevent inadvertent modification of Safety Relevant Registers (SRR) and Safety Latent Registers (SLR) (highlighted with the light blue color code in the register map), such register map sectors are protected by a lock field.

By default, SRR/SLR registers are locked. To configure the device, the following Procedure 11: Configuration Lock/Unlock shall be implemented:

Procedure 11: Configuration Lock/Unlock

1. MCU writes 0x55 in the SPECIAL_KEY register, to enter in partial unlock. At this point, the $T_{CFG\_TIMEOUT}$ is started.
2. MCU writes 0x33 in the SPECIAL_KEY register, to confirm the unlock.
3. MCU changes any configuration register within $T_{CFG\_TIMEOUT}$.
4. MCU re-applies the lock writing 0xAA in the SPECIAL_KEY register. At this point the $T_{CFG\_TIMEOUT}$ is reset and stopped. If it expires, the lock is automatically re-applied.

Trying to write a protected register (SRR or SLR) without unlocking it results in data being discarded.

Note: *Writing lock protected registers only alters the current configuration loaded in the SPI registers. To save the configuration and guarantee a correct reload at each powerup, the update has to be pushed into the Non Volatile Memory (NVM) as described in the dedicated section.*

Note: *For temporary modifications to the IC configuration, which do not need to be pushed in the Non Volatile Memory (NVM), it is recommended to disable the Configuration Integrity Check (CONF_CRC).*

5.15.1 Electrical parameters

Table 77. **Configuration timeout**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$T_{CFG\_TIMEOUT}$	Configuration lock timeout			2		s

5.16 Software reset (SW_RST)

It is possible to reset the configuration of the device sending a SW_RST sequence. Once triggered, the software reset procedure manages the flags according to Table 78.

Table 78. **Fault flags management after SW_RST**

CASE 1 (these flags are cleared by SW_RST command)	CASE 2 (two SW_RST commands are required to clear these flags)	CASE 3 (SW_RST command cannot clear these flags)
COMM_TIM(1)	OVC_CHG_1	V5V_UV(2)
POR_MAIN_ASSERTED(1)	OVC_DCHG_1	V5V_OV(2)
POR_SLEEP_ASSERTED(1)	OVC_CHG_0	V5V_OC(2)
FLTIN_TIME_OUT	OVC_DCHG_0	VANA_UV(2)
CC_WUP	GND_LOSS_FAIL	VANA_OV(2)
ABIST_DONE	FLTIN_DET	VANA_OC(2)
V5V_OC_OT		VB_UV(2)
VIF_ID_ERR		VCP_UV(2)
COMM_CRC_ERR		VCP_OV(2)
WRONG_ADDR		VTREF_UV(2)
SHORT_FRAME		VTREF_OV(2)
LONG_FRAME		NVM_CRC_TRIM_CAL_FAIL
VADC_AIN_BIST_DONE		NVM_CRC_CFG_FAIL
ABIST_CP_UV_OV_DONE		XCHECK_TEMP_FAIL

CASE 1 (these flags are cleared by SW_RST command)	CASE 2 (two SW_RST commands are required to clear these flags)	CASE 3 (SW_RST command cannot clear these flags)
DC_LINK_OVC_SAFE		CSA1_OPEN
DC_LINK_END		CSA0_OPEN
DATA_READY_AIN		OSC_FAIL
CLOCK_MON_SELFTEST_FAIL		NVM_VERIFY_ERR
ABIST_GND_LOSS_OL_FAIL		
XCHECK_CSA_SELFTEST_END		
XCHECK_ADC_INST_CC_END		
XCHECK_ADC_INST_CC_FAIL		
DATA_READY_CSA_INST		
XCHECK_PLS_WAKEUP_FAIL		
CYC_CFG_CRC_FAIL		
CYC_TRIM_CAL_CRC_FAIL		
XCHECK_CSA_SELFTEST_FAIL		
I2C_TX_ERR		
I2C_RX_ACK_ERR		
ABIST_FAIL		
VADC_AIN_BIST_FAIL		
ABIST_CP_UV_OV_FAIL		
SC1_DCHG		
SC0_DCHG		
TIMEOUT_FSM_CYCLIC		
XCHECK_SC_CONV_FAIL		
XCHECK_CC_DATA_VALID_FAIL		
XCHECK_CC_DATA_FAIL		

1. *POR_MAIN_ASSERTED=1 and POR_SLEEP_ASSERTED =1 after every SW_RST event, because their default value (HIGH) is restored. For the same reason, Communication Timeout is re-enabled after every SW_RST event (it is enabled by default) and COMM_TIM=1 if the timeout is elapsed with no frames received by the IC.*
2. *For these flags, related to analog comparators, the related diagnostics are continuously running. The status of these flags, after SW_RST, is only depending on the presence, or absence, of the faulty condition.*

To reset the device configuration, the following shall be implemented

Procedure 12: Software reset

1. MCU writes 0xE1 into the SPECIAL_KEY register, to enter partial reset mode;
2. MCU writes 0x1E into the SPECIAL_KEY register, to confirm reset.

Frames must be sent exactly in this sequence, otherwise registers won’t be reset.

User SW can eventually trigger a re-download of the configuration from the Non-Volatile Memory (NVM).

Since the NVM is re-downloaded at each wakeup, the new configuration eventually applied shall be pushed into the memory with a “write” instruction (refer to NVM Read/Write Operations). Otherwise, the old configuration is restored at the next wakeup event.

5.17 Configuration integrity check (CONF_CRC)

In order to guarantee the integrity over time of NVM downloaded trimming/calibration and configuration data, both safety relevant and latent register content (highlighted with the light blue color code in the register map) is automatically and cyclically checked against corruption within NORMAL mode. This is possible because local register data is provided with a CRC signature, that is checked every T_{CONF_CRC}, while no operation on the NVM is being performed (NVM circuit in reset state).

In case of check failure, the following actions are performed:

- In case trimming/calibration data has failed the CRC signature check, DIAG_STATUS2.CYC_TRIM_CAL_CRC_FAIL latch is set (clear-upon-read)
- In case IC configuration data has failed the CRC signature check, DIAG_STATUS2.CYC_CFG_CRC_FAIL latch is set (clear-upon-read)
- No other action is taken; i.e., no interruption/inhibition of IC functionalities

In case of permanent data corruption, failure latch set pulse occurs every T_{CONF_CRC}. Hence, MCU is supposed to confirm permanent corruption performing multiple latch clear attempts with a periodicity larger than T_{CONF_CRC} .

The local register CRC signature is managed in the following way:

- Every time NVM data is downloaded into local registers (either automatically or user-driven), a CRC signature is refreshed as well
- Every time the user changes the local register data, the corresponding CRC signature is not automatically updated, thus a CRC check failure is expected at the next execution cycle. By the way, as the user triggers the NVM upload and refresh operation, after the NVM sector CRC has been automatically updated, the local register CRC signature is updated accordingly, and no further CRC check failure is expected.

The integrity check can be disabled setting GENERAL_REG.CYC_CFG_CRC_DIS = 1. After the diagnostic has been disabled, it is still possible to clear upon read both CYC_TRIM_CAL_CRC_FAIL and CYC_CFG_CRC_FAIL. Disabling such diagnostic can be useful to mask systematic CRC failure detection when updating IC configurations. On the other hand, leaving it enabled while updating register configurations may be used as a fault injection strategy to assess the correct functionality of the diagnostics.

5.17.1 Electrical parameters

Table 79. **Configuration integrity check characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
T_{CONF_CRC}	Configuration integrity check period			49	90	ms

5.18 Non-volatile memory (NVM)

The IC allows saving key configuration parameters in the internal NVM. Refer to the register map file attached. All registers marked with the light blue color code throughout the document identifies configuration registers stored in the NVM.

5.18.1 NVM Read/Write operations

NVM data is automatically downloaded into local registers every time that the IC performs the following FSM transitions:

- DEEP SLEEP to NORMAL
- DEEP SLEEP to CYCLIC WAKEUP
- STANDBY to NORMAL
- STANDBY to CYCLIC WAKEUP

When the IC performs FSM transitions to either DEEP SLEEP or STANDBY states, a selected group of data stored in local registers is retained in order to guarantee IC correct operation, while all other data is lost. Such data are re-downloaded in next transition to NORMAL/CYCLIC WAKEUP.

When the IC performs FSM transitions to OFF state, all data stored in local registers is lost; NVM data are re-downloaded in next transition to NORMAL/CYCLIC WAKEUP.

As the IC reaches NORMAL state, the following commands allow user interaction with the NVM:

- GENERAL_REG.NVM_OP_CMD=0x3 triggers the NVM upload and refresh: this operation fetches the data previously written into configuration registers and writes it to the relative NVM sectors, then it automatically triggers a full NVM re-download in order to guarantee whole data consistency. The operation lasts T_{NVM_UPLOAD} and during such time interval the MCU is not be able to perform R/W operations on configuration registers (any command will be discarded). The other registers remain accessible.
- GENERAL_REG.NVM_OP_CMD=0x5 triggers the NVM refresh, fetching the data from NVM sectors and writing it to the configuration registers. The operation lasts $T_{NVM\_DOWNLOAD}$ and during such time interval the MCU is not be able to perform R/W operations on configuration registers (any command is discarded). The other registers remain accessible.

During NVM upload/download operations, DIAG_STATUS3.NVM_READY flag is reset to ‘0’, indicating that NVM is busy. During such an interval, it is highly recommended to avoid triggering conversions or actuating loads, as the trimming and calibration data is being refreshed. Once the task is complete, the NVM_READY is set high; as no NVM read/write operation is running, the NVM circuit is kept under reset.

In case of error during NVM upload procedure, the flag DIAG_STATUS3.NVM_VERIFY_ERR (clear-upon-read) is asserted, and the correct upload cannot be guaranteed.

L9965C/L99BM2C allows to save 104bit additional values in its NVM. This is possible by writing the content of the data to save in the registers CUSTOMER_DATAx (x= [0..6]). They will be managed by others configuration registers, the upload/download operation can be triggered as described.

In order to guarantee data retention, the NVM write operation number must not exceed $N_{NVM\_WRITE\_CYCLES}$; if such a limit is exceeded, data retention is not guaranteed. Note that the IC continues to accept and perform write operations, even if it is beyond the $N_{NVM\_WRITE\_CYCLES}$ count. Every time a write operation is performed, the IC automatically updates the DEV_GEN_CFG_1.NVM_UPLOADS_COUNT counter field, which is stored in the NVM as well. The counter value is user-accessible, reading NVM_UPLOADS_COUNT bit (read-only): the counter value saturates at $N_{NVM\_WRITE\_CYCLES}$. If a new write operation is done, exceeding the $N_{NVM\_WRITE\_CYCLES}$ limit, counter value is increased at $N_{NVM\_WRITE\_CYCLES}+1$ and will never be updated anymore.

5.18.2 NVM Data Integrity Checks

NVM content can be categorized in two main groups: trimming/calibration data (used to guarantee function accuracy) and configuration data (used to configure IC operation). All this data is organized in sectors, each of them individually protected by CRC. Trimming/calibration data and configuration data do not share the same sectors.

Every time the IC performs an NVM download operation (either automatic or user-driven), an integrity check against the NVM CRC (sector by sector) is performed as well. In case of check failure, the following actions are performed:

- The CRC check failing sector data is not downloaded into the local registers. Such data is replaced by all zeros. It is possible to mask this replacement setting the GENERAL_REG.NVM_CRC_FAIL_MSK bit. Hence, depending on the sector content, either function accuracy is not guaranteed, or IC expected configuration is not applied.
- In case at least one of the trimming/calibration sectors has failed the CRC check, DIAG_STATUS2.NVM_CRC_TRIM_CAL_FAIL latch is set (clear-upon-read). When GENERAL_REG.NVM_CRC_FAIL_MSK is set to 1, this fault can be cleared after a new download is re-triggered.
- In case at least one of the IC configuration sectors has failed the CRC check, DIAG_STATUS2.NVM_CRC_CFG_FAIL latch is set (clear-upon-read). When GENERAL_REG.NVM_CRC_FAIL_MSK is set to 1, this fault can be cleared after a new download is re-triggered.
- No other action is taken, i.e. no interruption/inhibition of IC functionalities.

Every time the user triggers an NVM upload and refresh operation, the corresponding sector CRC is updated as well; this is done by IC automatically.

5.18.3 Electrical parameters

Table 80. NVM electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$N_{NVM\_WRITE\_CYCLES}$	Number of allowed NVM write cycles to guarantee data retention				30	cycles
T_{NVM_UPLOAD}	NVM upload time duration		27.5		34	ms
$T_{NVM\_DOWNLOAD}$	NVM download time duration		0.35		1.1	ms

5.19 Die Temperature Monitor (Tj)

The IC monitors the junction temperature with a sensor placed close to the ADC stage in order to feed the calibration algorithm.

Junction temperature measurement is stored in the DIE_ADC_TEMP_MEAS register and can be computed according to the following procedure:

Procedure 13: Reading of junction temperature

1. User shall read from a dedicated NVM sector the read value at -40 degC (12 bit unsigned) and translate it into decimal value. That is CODE_NVM_TADC0_COLD
    a. CODE_NVM_TADC0_COLD corresponds to CUSTOMER_DATA5[0:11]
2. User shall read from a dedicated NVM sector the read value at 130 degC (12 bit unsigned) and translate it into decimal value. That is CODE_NVM_TADC0_HOT
    a. CODE_NVM_TADC0_HOT corresponds to CUSTOMER_DATA5[12:15]+CUSTOMER_DATA6[0:7]*2^4
3. User shall determine the slope of the characteristic Temperature vs. Code with the following equation:

$$m = \frac{170}{\left(CODE_{NVM_{TADC0_{HOT}}} - CODE_{NVM_{TADC0_{COLD}}}\right)} \quad (5)$$

4. User shall read from DIE_ADC_TEMP_MEAS SPI register the instantaneous temperature value and translate it into decimal value. That is CODE_TADC0.
5. Finally, Tj temperature is obtained with the equation below.

$$Tj = -40 + m\left(CODE_{TADC0} - CODE_{NVM_{TADC0_{COLD}}}\right) \quad (6)$$

The two codes CODE_NVM_TADC0_COLD and CODE_NVM_TADC0_HOT are stored in the NVM and user shall read them only the first time. Once determined, and after evaluating the slope m, steps a-b-c of Procedure 13: Reading of junction temperature can be omitted.

5.19.1 Thermal Shutdown (TSD)

In NORMAL and CYCLIC WAKEUP states the device monitors also V5V Overcurrent and Overtemperature.

For a robust implementation, when both overtemperature and overcurrent are detected, and validated concurrently, the flag DIAG_STATUS_STBY.V5V_OC_OT is latched at 1 (clear-upon-read), V5V regulator is immediately disabled, and IC moves to DEEP SLEEP or STANDBY state. After a new successful power-up, user can read V5V_OC_OT previously latched value, as this bit value is retained in DEEP SLEEP mode.

It is available a DIAG_STATUS2.V5V_OC flag (not retained in DEEP SLEEP) that can be read in Normal Mode in case of Overcurrent event, without Overtemperature.

5.19.2 Temperature ADC X-Check

The 2 ADCs used for temperature calibration are continuously x-checking each other while in NORMAL/CYCLIC WAKEUP to ensure calibration algorithm integrity. In case of mismatch detected, the DIAG_STATUS2.XCHECK_TEMP_FAIL latch is set. It is clearable upon read in case the mismatch disappears, after a maximum time interval of T_{Tj_XCHECK} .

To prevent latent failures affecting the detection, it is possible to perform a fault injection, by programming CMD2.XCHECK_TEMP_FAULT_INJ = 1 and verifying that DIAG_STATUS2.XCHECK_TEMP_FAIL is set after a conversion time of T_{Tj_XCHECK}. After that, the fault injection can be stopped programming CMD2.XCHECK_TEMP_FAULT_INJ = 0 and verifying that XCHECK_TEMP_FAIL is clearable on read.

5.19.3 Electrical Parameters

Table 81. **Die Temperature Monitor electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Note
T_{J_ERR}	Die Temperature Total Conversion Error		-5		+5	°C	
T_{Tj_XCHECK}	Die Temperature x-check period				1	ms	

5.20 Analog BIST (ABIST)

The IC is equipped with analog BIST to prevent latent failures affecting safety relevant comparators:

- Writing CMD2.ABIST = 1, the analog BIST on the following comparators is started
  - VB UV
  - VTREF UV
  - VTREF OV
  - VANA UV
  - VANA OV
  - V5V UV
  - V5V OV

The DIAG_STATUS1.ABIST_DONE = 1 confirms the correct execution of the BIST procedure.

In case of BIST failure, the DIAG_STATUS1.ABIST_FAIL latch is set. It can be reset upon read.

- Writing CMD2.ABIST_CP_UV_OV, the analog BIST on the CP UV / OV comparators is started.

The DIAG_STATUS2.ABIST_CP_UV_OV_DONE = 1 confirms the correct execution of the BIST procedure.

In case of BIST failure, the DIAG_STATUS2.ABIST_CP_UV_OV_FAIL latch is set. It can be reset upon read.

There is also an analog BIST checking the comparators of GND Loss and Open Load; it is available only during Cyclic Wakeup Routine, and a failure on this check can be read through the flag DIAG_STATUS2.ABIST_GND_LOSS_OL_FAIL.

5.20.1 Electrical parameters

Table 82. **ABIST electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
T_{ABIST}	Analog BIST duration	Guaranteed by SCAN			400	μs	-

5.21 Device identification (DEVICE_NAME)

The Isolated Vertical Interface (VIF) allows populating the bus with different devices of the L9965x family. To enable the MCU quickly recognizing the device type and launching the proper initialization, configuration and diagnostic procedures, the CHIPID.NAME_ID field holds a unique code identifying the product type. Specifically, NAME_ID = 0x1C identifies the L9965C/L99BM2C CSA.

In the same register (CHIPID), the following fields are also available: SILICON_ID (3 bit) and METAL_ID (5 bit), identifying the version of the silicon.

These two fields are codified in the way shown on Table 83 and Table 84.

Table 83. **SILICON_ID codification**

Silicon revision	Codification
A	001
B	010
C	011
D	100
E	101
F	110
G	111

Table 84. **METAL_ID codification**

Metal revision	Codification
A	00001
B	00010
C	00011
D	00100
E	00101
F	00110
G	00111
H	01000
I	01001
J	01010
K	01011
L	01100
M	01101
N	01110
O	01111
P	10000
Q	10001
R	10010
S	10011
T	10100
U	10101
V	10110
W	10111
X	11000
Y	11001
Z	11010

5.22 DC-Link precharge controller (PRECHG)

The IC integrates a buck controller designed to allow quick and reliable pre-charge of the DC-Link capacitor using semiconductor-based switches.

Typical EV applications require to pre-charge the DC-Link within 200ms. With the increasing number of loads connected to the HV bus, in order to increase their efficiency, the total capacitance seen by the battery terminals may easily increase up to several mF (e.g. 1.7mF).

To charge such a big capacitor within 200ms would require a low value resistor (in the order of 10-20 Ω). At the beginning of the transient, the whole battery voltage would fall on the limiting resistor, resulting in a huge peak power rating (in the order of many kW).

To perform such function using the standard RC approach might become unaffordable in terms of BOM and PCB space.

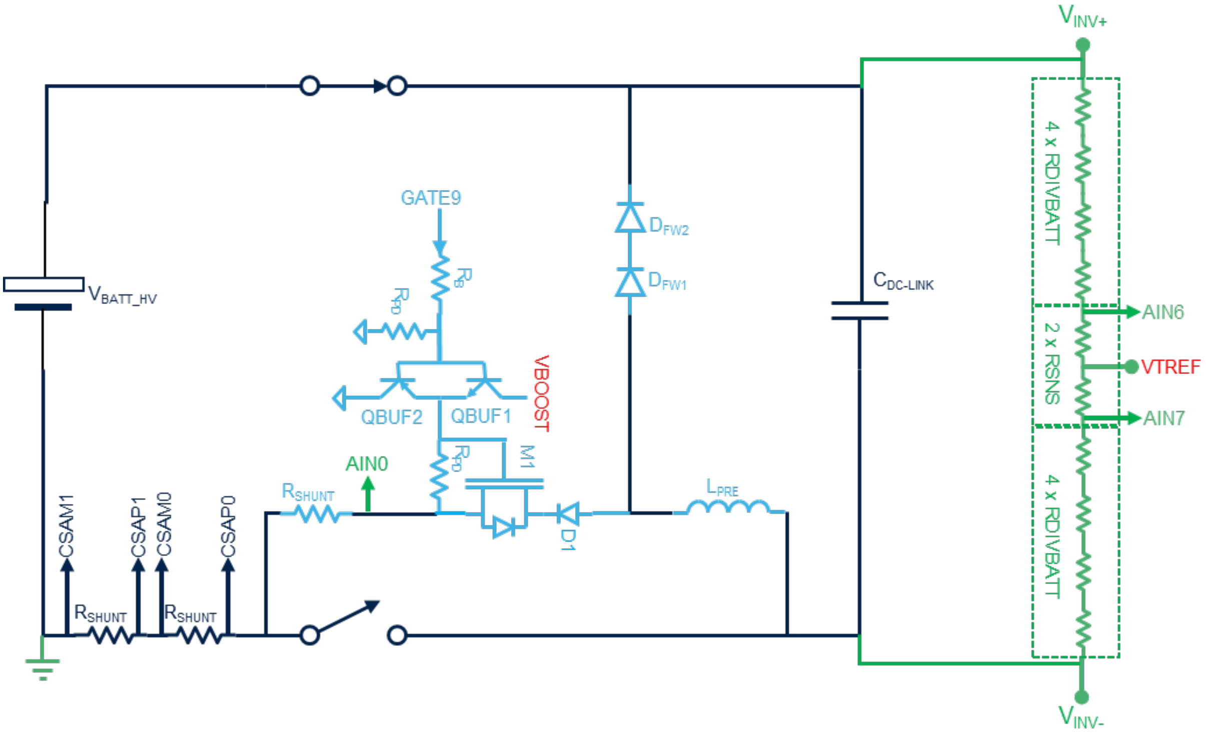
To enable system designers building the DC-Link pre-charge function in a cost-effective and reliable way, the IC implements everything needed to charge the DC-Link controlling the current into a low-side inductor, placed in series to the battery negative terminal.

To preserve Li-ion pack health, the IP is designed for minimizing the AC ripple of the current drawn during the pre-charge interval.

5.22.1 Reference design and BOM

Figure 29 shows the reference design. As explained in Detailed procedure, components and configurations may be adapted to cover a wide range of application scenarios.

Figure 29. DC-Link precharge controller reference design



5.22.2 Functional description

The IP exploits the AIN0/GATE9 pin pair to control the inductor current between a maximum I_{PRE_MAX} and a minimum I_{PRE_MIN} value:

- The turn-off command is comparator-based:
  - When the voltage on AIN0 pin raises above V_{TH_PRECHG} for an interval longer than $T_{PRECHG\_ON\_FIL}$, the GATE9 pre-driver is switched OFF and the T_{HOLD_OFF} timer is started.
  - Having fixed the R_{SHUNT} value, the I_{PRE_MAX} is determined.
- The turn-on command is timer-based
  - The hold-off threshold is dynamically adjusted according to the following equation:

$$T_{HOLD_{OFF}} = \frac{\Delta I * L_{PRE}}{V_{DC-LINK} + 2V_{DFW}} \tag{7}$$

  Where ΔI is the peak-to-peak current ripple, V_{DFW} is the freewheeling diode forward voltage (assumed 1V) and $V_{DC\text{-}LINK}$ is the DC-Link voltage, which is continuously updated by the Analog Input Monitor (AINx).
    - Ror the function to work properly, it is recommended to set TVOLT_FIL = 001 and ABS_RATIO = 1
- Having fixed the L_{PRE} value, the IC calculates the necessary T_{HOLD_OFF} to have a constant ΔI ripple throughout all the cycles. Hence, also $I_{PRE\_MIN} = I_{PRE\_MAX}$ - ΔI is determined.
- The $V_{DC\text{-}LINK}$ update thread is asynchronous in respect to the GATE9 control thread. In case T_{HOLD_OFF} is updated during an OFF interval and the hold-off timer has already overcome the threshold, the recirculation is interrupted and GATE9 is immediately switched ON.
- The Analog Input Monitor (AINx) must have been previously configured for acquiring the DC-Link voltage through any of the possible mux configurations in absolute mode.

As can be seen in Electrical parameters, the algorithm operates with a variable frequency, which is initially small, then reaches its maximum peak in the middle of the transient, and finally tends to zero at the end of the charge.

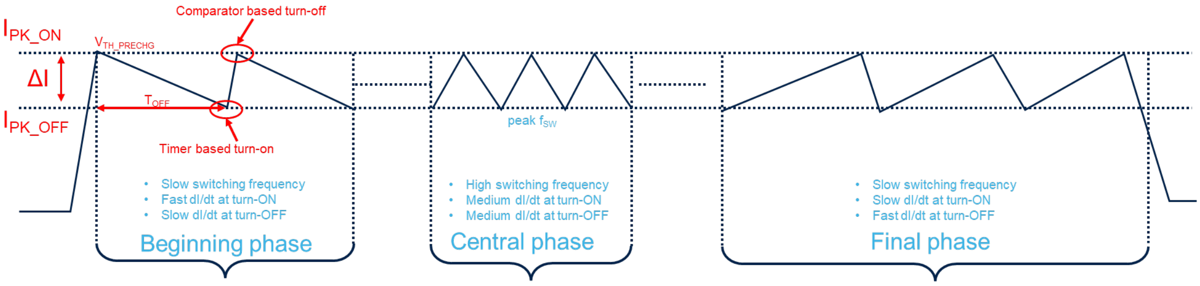
The average precharge current can be estimated as:

$$I_{PRE_{AVG}} = I_{PRE_{MAX}} - \frac{\Delta I}{2} \tag{8}$$

Hence, the time needed to charge the DC-Link can be estimated as follows:

$$T_{PRECHG_{DURATION}} = \frac{C_{DC-LINK} V_{BATT_{HV}}}{I_{PRE_{AVG}}} \tag{9}$$

Figure 30. **Pre-charge current waveform**



To avoid resonance between DC-Link capacitor and pre-charge inductor, the algorithm can detect the end-of-charge condition by comparing the voltage acquired by the Analog Input Monitor (which is the rescaled version of $V_{DC\text{-}LINK}$) with a programmable threshold $V_{DC\text{-}LINK\_OFF\_TH}$. If the converted voltage becomes higher or equal to $V_{DC\text{-}LINK\_OFF\_TH}$, the DC_LINK_CFG_1.DC_LINK_END flag is set and the switching activity is interrupted: GATE9 is then permanently OFF.

5.22.3 Detailed procedure

The function can be run writing DC_LINK_CFG_0.DC_LINK_EN = 1 and can be aborted anytime writing DC_LINK_EN = 0.

The pre-charge controller IP is designed to offer maximum flexibility, adapting the control strategy to application scenarios featuring:

- Different values of $V_{DC\text{-}LINK}$ charge voltage
- Different values of $C_{DC\text{-}LINK}$ capacitance
- Different values of L_{PRE} inductors
- Different values of AC ripple currents

Before running the function, the MCU shall configure the following parameters:

- DC_LINK_GAIN is the parameter specifying how the DC-Link voltage is re-scaled by the external resistive divider down to the Analog Input Monitor (AINx) (refer to Figure 29)

$$DC\_LINK\_GAIN = round\left(\frac{R_{SNS} + 4R_{DIVBATT}}{R_{SNS}}\right) \tag{10}$$

- DC_LINK_CFG_1.DC_LINK_RIPPLE is the product between the current ripple and the pre-charge inductor, expressed in [A*uH]. It is an essential parameter to calculate the hold-off time. Having fixed the external inductor, this parameter determines the current ripple.

$$DC\_LINK\_RIPPLE\left[\frac{A{*}\mu H}{V}\right] = round\left(\frac{\Delta I{*}L_{PRE}{*}630}{DC\_LINK\_GAIN}\right) \tag{11}$$

- DC_LINK_CFG_0.DC_LINK_V_TH field assigns the $V_{DC\text{-}LINK\_OFF\_TH}$ for the detection of the end-of-charge. It is recommended to calculate the final target value using the following equation. Then, a slightly smaller $V_{DC\text{-}LINK\_OFF\_TH}$ can be configured (e.g. c_{GAIN} = 0.97, 3% margin)

$$\begin{cases} DC\_LINK\_V\_TH = round\left(\frac{c_{GAIN}{*}V_{BATT_{HV}}{*}157.5}{DC\_LINK\_GAIN}\right) \\ V_{DC_{LINK_{OFF_{TH}}}} = DC\_LINK\_V\_TH{*}6.3mV \end{cases} \tag{12}$$

- DC_LINK_CFG_0.DC_LINK_DIODE field assigns the recirculation offset $2V_{DWF}$ in Eq. (7), rescaled considering the voltage divider gain and the ADC resolution assigned to these measurements:

$$DC\_LINK\_DIODE = round\left(\frac{2{*}V_{DFW}{*}630}{DC\_LINK\_GAIN}\right) \tag{13}$$

A detailed recommended procedure is described in the dedicated application note.

5.22.4 Diagnostics

Table 85. **Precharge controller diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Overcurrent	During ON phase, if the voltage on AIN0 raises above V_{PRECHG_OC} for longer than $T_{PRECHG\_OC\_FIL}$, the DIAG_STATUS1.DC_LINK_OVC_SAFE fault is acknowledged.	The DC_LINK_OVC_SAFE flag is set The GATE9 driver is switched off	The DC_LINK_OVC_SAFE flag can always be cleared by MCU	Precharge function can be re-engaged upon next DC_LINK_EN rising edge	DC_LINK_EN masks diagnostic execution. When disabled, the DC_LINK_OVC_SAFE flag can always be cleared DC_LINK_OVC_SAFE_MSK masks the detection and the reaction on GATE9 pre-driver

5.22.5 Electrical parameters

Table 86. **DC-Link precharge electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
V_{TH_PRECHG}	Turn-off threshold on AIN0 pin		54	60	66	mV	AIN0

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
$T_{PRECHG\_ON\_FIL}$	Turn-off filter time on AIN0 pin	Voltage rising with dV/dt = 4V/ms on AIN0 pin. From threshold crossing to 10% of GATE9 pulldown current		50	110	ns	AIN0
V_{PRECHG_OC}	Overcurrent threshold on AIN0 pin		64.8	78	92.4	mV	AIN0
$T_{PRECHG\_OC\_FIL}$	Overcurrent filter time on AIN0 pin	Voltage rising with dV/dt = 4V/ms on AIN0 pin. From threshold crossing to 10% of GATE9 pulldown current		25	60	ns	AIN0
DC_LINK_V_TH	DC-Link cut-off voltage (10 bit), $DC\_LINK\_V\_TH = round\left(\frac{V_{BATT_{HV}}*157.5}{DC\_LINK\_GAIN}\right)$		0		2^{10}-1	LSB	AINx
DC_LINK_GAIN	DC-Link conversion gain (8 bit)		0		255	V/V	AINx
DC_LINK_RIPPLE	Inductor current ripple gain (16 bit) $DC\_LINK\_RIPPLE = \frac{\Delta I*L_{PRE}*630}{DC\_LINK\_GAIN}$		0		2^{16}-1	(A*uH)/V	AINx
DC_LINK_DIODE	Recirculation diode gain (6 bit) $DC\_LINK\_DIODE = \frac{2V_{DFW}*630}{DC\_LINK\_GAIN}$		0		2^{6}-1	V/V	AINx

6 Application Information

6.1 Bill of material (BOM)

Referring to Figure 31, this section lists the components to be used in a typical application scenario.

Figure 31. Typical application circuit

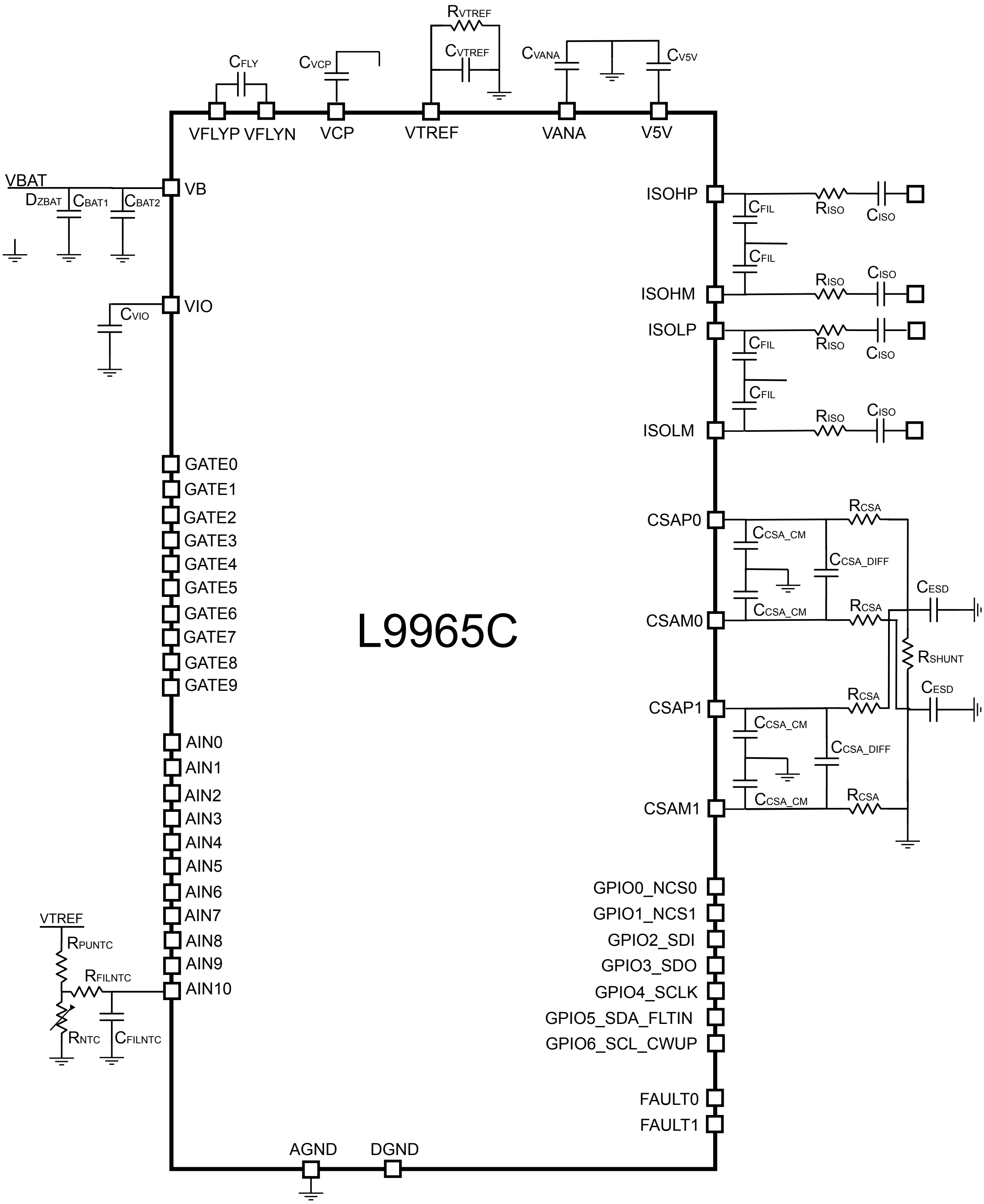


Table 87. **Bill of material**

Symbol	Parameter	Value	Rating	Tolerance	Note
Battery Supply					
D_{ZBAT}	TVS for battery supply line		NA	NA	Optional.
C_{BAT1}	Tank capacitor	2.2µF	50V	10%	Cleans up the input VB from any noise coupled through the DC/DC converter and/or by other shared supply lines
C_{BAT2}	HF bypass capacitor	100nF	50V	10%	Bypasses HF noise and filters out any fast transient due to residual ESD strikes coupled through the DC/DC converter inter-winding capacitance
Charge Pump					
C_{FLY}	Charge pump flying capacitor	47nF	50V	10%	Rated to withstand maximum operating battery voltage.
C_{VCP}	Charge pump tank capacitor	220nF	50V	10%	Rated to withstand maximum operating battery voltage.
Output Regulators					
C_{V5V}	V5V tank capacitor	2.2µF	10V	10%	Electrical parameters guaranteed from 1.6µF to 2.64µF.
C_{VANA}	VANA tank capacitor	2.2µF	10V	10%	Electrical parameters guaranteed from 1.6µF to 2.64µF.
C_{VTREF}	VTREF tank capacitor	2.2µF	10V	10%	Electrical parameters guaranteed from 1.6µF to 2.64µF.
R_{VTREF}	Bias resistor for VTREF regulator	100k	0.125W	10%	
VIF					
R_{ISO}	Series resistor for ISO pins	35Ω to 41Ω 39Ω typical	100mW	1%	Filters common mode and differential noise.Keep tolerance low to maximize differential line balancing.
C_{ISO}	Series capacitor for ISO pins	2.2nF to 6.8nF	100V/1kV	2%	Voltage rating shall be sized according to the maximum isolation voltage to be guaranteed in the application.Keep tolerance low to maximize differential line balancing.
C_{FIL}	Filtering capacitor for ISO termination	100pF	25V	2%	Filters common mode and differential noise.Keep tolerance low to maximize differential line balancing.
R_{TERM}	Termination resistor for unused port	200Ω	0.5W	10%	To be used only on unused VIF port.
Current Sense					
R_{CSA}	CSA differential filtering resistor	47Ω	100mW	1%	Sized to obtain a 3 kHz differential cut-off frequency in conjunction with C_{CSA_DIFF} and C_{CSA_CM}. To guarantee the best performance of SoC and EIS algorithms, such cut-off frequency needs to be matched to the L9965A/L99BM218 companion chip cell voltage differential cut-off frequency.
C_{CSA_DIFF}	CSA differential filtering capacitor	470nF	16V	1%	Sized to obtain a 3 kHz differential cut-off frequency in conjunction with R_{CSA} and C_{CSA_CM}. To guarantee the best performance of SoC and EIS algorithms, such cut-off frequency needs to be matched to the L9965A/L99BM218 companion chip cell voltage differential cut-off frequency.

Symbol	Parameter	Value	Rating	Tolerance	Note
C_{CSA_CM}	CSA common mode filtering capacitor	33nF	16V	1%	Sized to obtain a 100kHz cut-off frequency in conjunction with R_{CSA}. Needed to pass BCI tests. Choose a capacitor showing low impedance up to 400MHz.
NTC Sensing (Optional)					
R_{PUNTC}	NTC pullup biasing resistor	10kΩ	62.5mW/	1%	Pullup resistor chosen to equalize R_{NTC} @25°C. Voltage at AIN pin should be $V_{VTREF}/2$ @25°C.
R_{NTC}	NTC for temperature sensing	10kΩ		1%	NTC chosen to equalize R_{PUNTC} @25°C.
R_{FILNTC}	NTC filtering resistor	1kΩ	62.5mW		Sized to obtain a 1.6kHz cut-off frequency in conjunction with C_{FILNTC}
C_{FILNTC}	NTC filtering capacitor	100nF	16V		Sized to obtain a 1.6kHz cut-off frequency in conjunction with R_{FILNTC}
C_{GPIO_EXT}	GPIO external bypass capacitor	140	pF		
ESD (Optional)					
C_{ESD}	ESD protection capacitor for Current Sense pins	100nF	25V	1%	Optional ESD protection capacitor. Contributes also in filtering BCI. Choose a capacitor showing low impedance up to 400MHz.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 TQFP48L (7x7x1 mm exposed pad down) package information

Figure 32. TQFP48L (7x7x1 mm exposed pad down) package outline - top and bottom

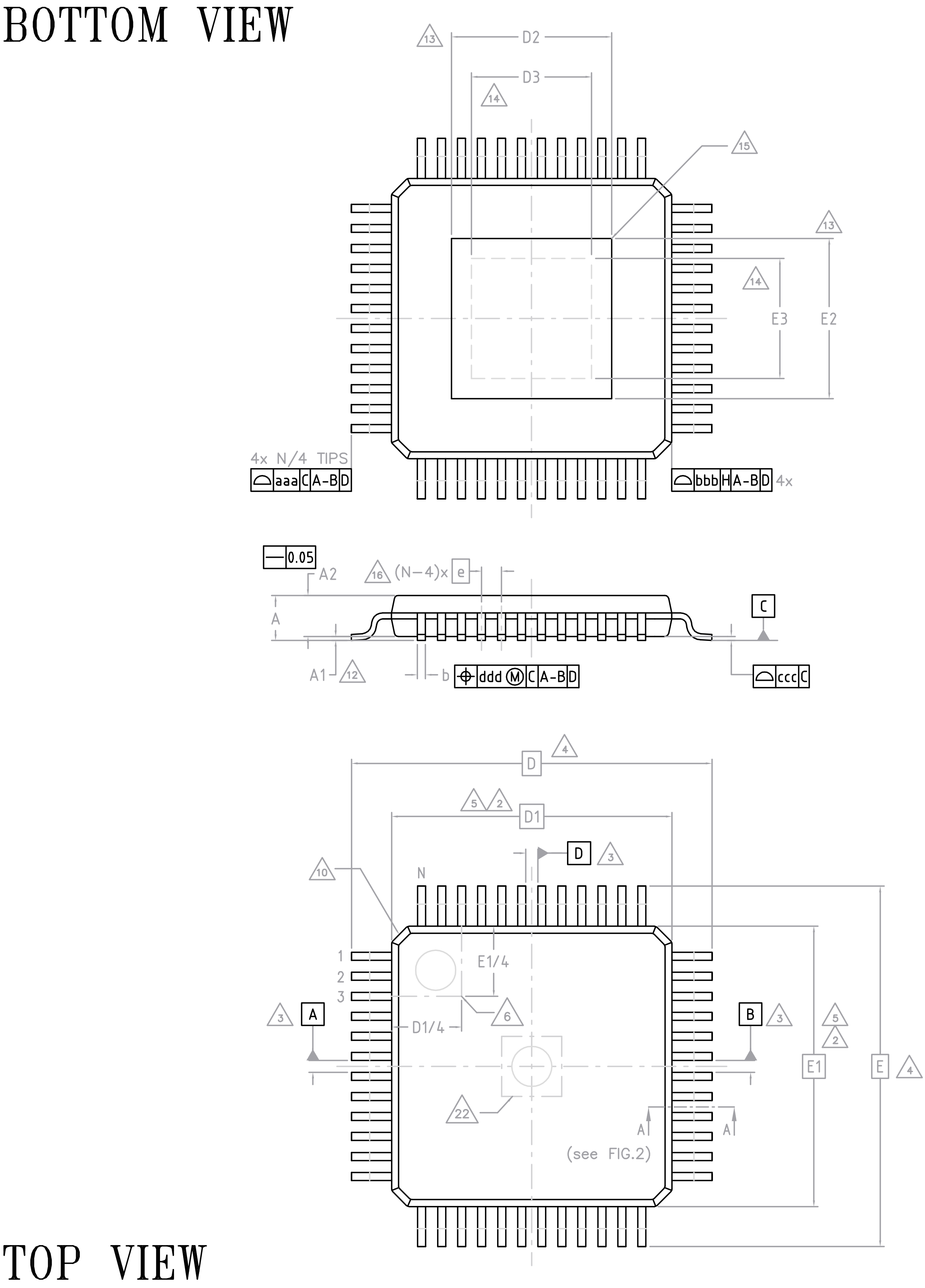


Figure 33. **TQFP48L (7x7x1 mm exposed pad down) package outline - sections**

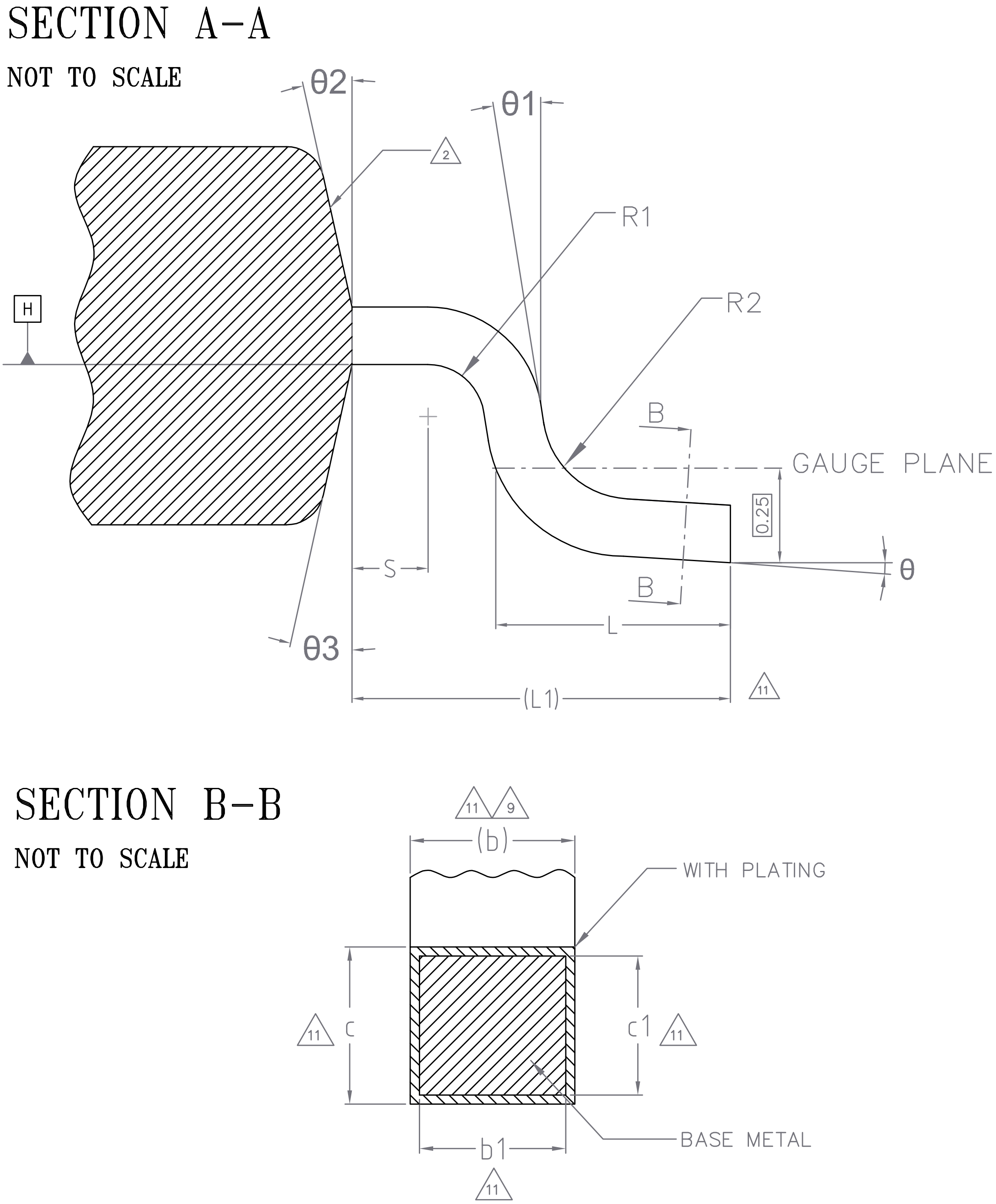


Table 88. **TQFP48L (7x7x1 mm exposed pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
ϴ	0°	3.5°	7°
ϴ1	0°	-	-

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A	-	-	1.2
A1	0.05	-	0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09	-	0.2
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
D2	Variations		
D3	Variations		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
E2	Variations		
E3	Variations		
L	0.45	0.6	0.75
L1	1.00 REF		
N	48		
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
Tolerance of form and position			
aaa	0.2		
bbb	0.2		
ccc	0.08		
ddd	0.08		
Variations 5.0 x5.0			
D2			5.37
E2			5.37
D3	3.4		
E3	3.4		

Revision history

Table 89. **Document revision history**

Date	Version	Changes
04-Mar-2026	1	Initial release.

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