L9965T/L9965TS

Datasheet

Automotive SPI to isolated SPI transceiver

LQFP32L
7x7x1.4 mm

Product status link
L9965T, L9965TS

Product summary		
Order code	Package	Packing
L9965T-TR	LQFP32L	Tape and reel
L9965TS-TR		

Features

- AEC-Q100 qualified
- Temperature grade 1: -40°C to +125°C operating temperature range
- HBM ESD classification level 2
- CDM ESD classification level C4B
- Full ISO26262 compliant, ASIL-D systems ready, documentation available
- Automatic wake-up of BMS/BMU MCU and PMIC from SHUTDOWN/SLEEP in case of fault detected in the chain
- Single or dual channel p/n in the same package for ring connection
- Supports up to 59 devices in chain
- Cable lengths verified up to 10 meters
- 10 MHz 4-wire SPI interface
- 4 Mbps 2-wire vertical interface (VIF)
- Supports both transformer and capacitive isolation
- Compressed burst data read for enhanced communication speed over the whole chain
- Broadcast write command to configure and control all devices in the chain (or a subset)
- Very low EMI susceptibility and emissions
- Compatible with 3.3 V and 5 V logics
- Supply voltage from 6 V to 24 V

Application

- Automotive battery monitoring systems
- Energy storage systems
- UPS

Description

In BMS systems, the L9965T and L9965TS bidirectional SPI transceivers allow communication between isolated devices in different voltage domains through a twisted-pair connection.

The devices belong to the L9965 chipset family for the monitoring and control of high-voltage battery management systems.

1 Overview

In a high voltage battery management system, the master microcontroller accesses the cells monitor and the pack current monitor devices for diagnostics and control purposes. Since the different BMS ICs are located into different voltage domains, it is required isolated communication between each other.

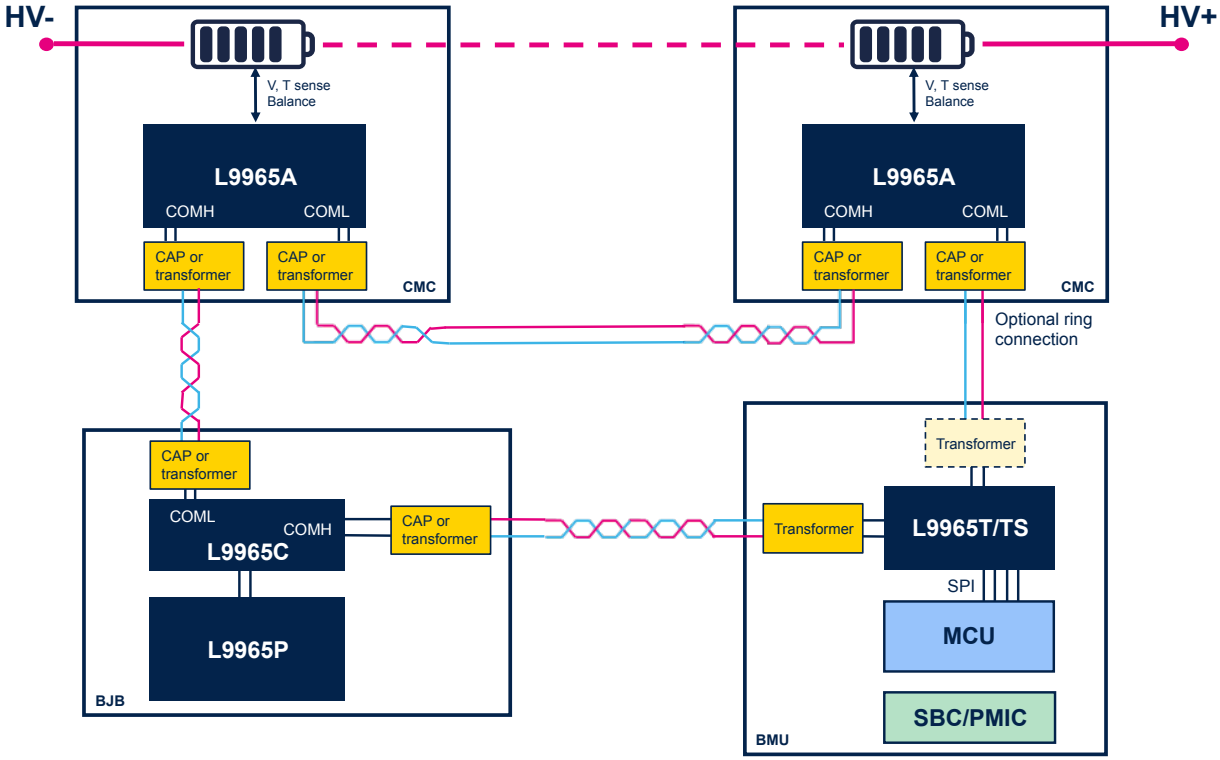
The L9965T/TS allows isolated daisy chain connection through a simple two-wire protocol in L9965x-based HV BMS applications. It converts data from a standard 4-wire SPI protocol to a 2-wire proprietary protocol (and vice versa), supporting the signals isolation by capacitors or transformers.

All the devices in the daisy chain recognize the protocol and can be addressed in read-write mode by a single transceiver. Ring connection can be implemented by the dual channel device L9965T.

L9965T/L9965TS implements two physical communication interfaces.

- SPI Target Interface: this interface is used by the controller MCU to configure and send commands to L9965T/TS and, through it, to all the devices in the chain.
- Isolated Vertical Interface (VIF): this interface is typically used to connect BMS daisy-chained devices L9965A/C to L9965T/TS and to each other on the VIF bus.

Figure 1. L9965T in a L9965x-based BMS system



The L9965T/TS manages periodic wakeup of the devices in the chain for diagnostic purposes and it is sensitive to fault tones from the devices in the chain when in low power mode. It implements a set of commands to optimize the communication over the chain:

- Broadcast command, to write and configure all devices in the chain (or a subset)
- Burst and compressed burst read, to enable high data rate transmission from all devices in the chain with negligible impact on the power consumption
- Go-to-sleep command, to set all the devices in the chain to low power mode
- FAULT/WAKEUP tone, to wake-up the chain for normal operation or faults signaling
- CYCLIC_WAKEUP tone, to trigger periodic diagnostic execution in the chained devices.

These functionalities are implemented using different functional states, to optimize system power consumption:

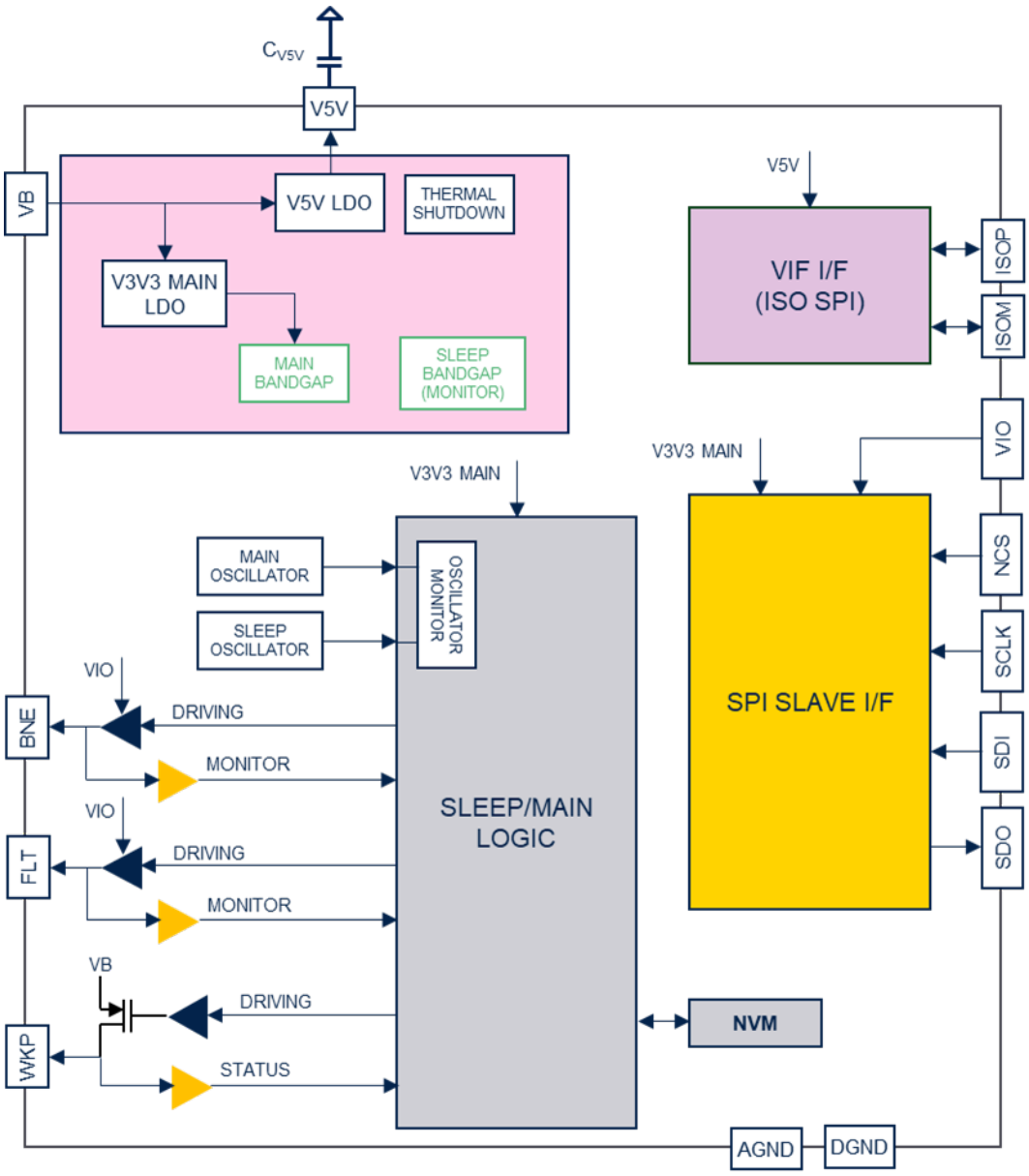
- NORMAL: full operation mode

- CYCLIC_WAKEUP/CYCLIC_COUNT: low power modes to send a periodic tone and trigger cyclic diagnostics in the chained devices during low power operation. In these states the device is sensitive to wakeup tones both from the VIF in case of fault and from the SPI by the MCU
- DEEPSLEEP: Ultralow power state for managing long inactivity periods. In this state the device is sensitive to wakeup tones both from the VIF in case of fault and from the SPI by the MCU.

2 Block diagram and pin description

2.1 Block diagram

Figure 2. **Single die block diagram**



2.2 Pin description

Figure 3. **Pinout L9965T (top view)**

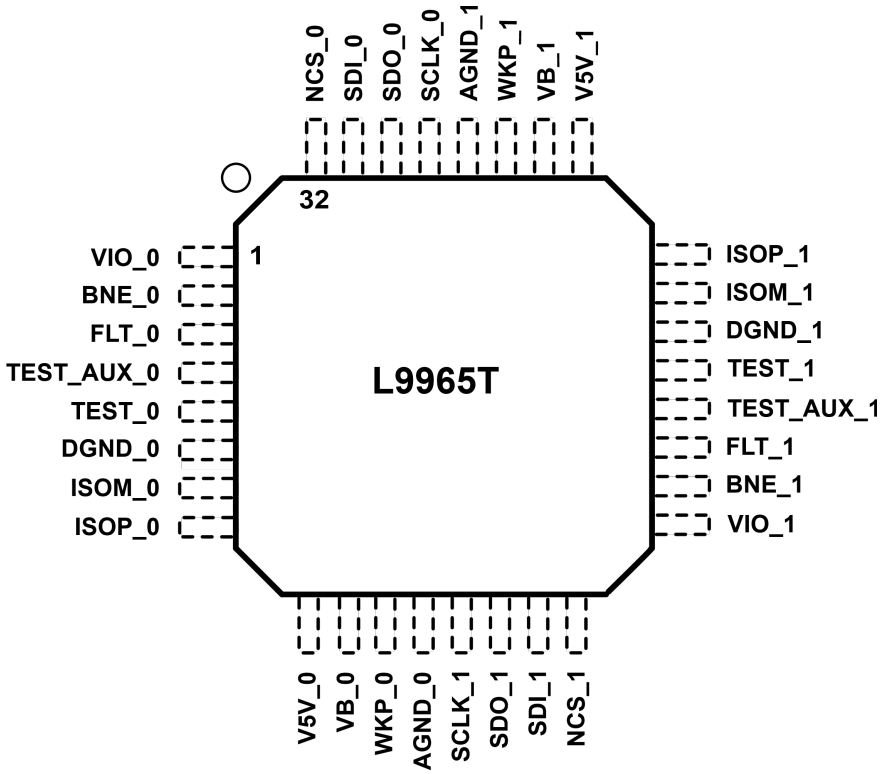


Figure 4. **Pinout L9965T (top view)**

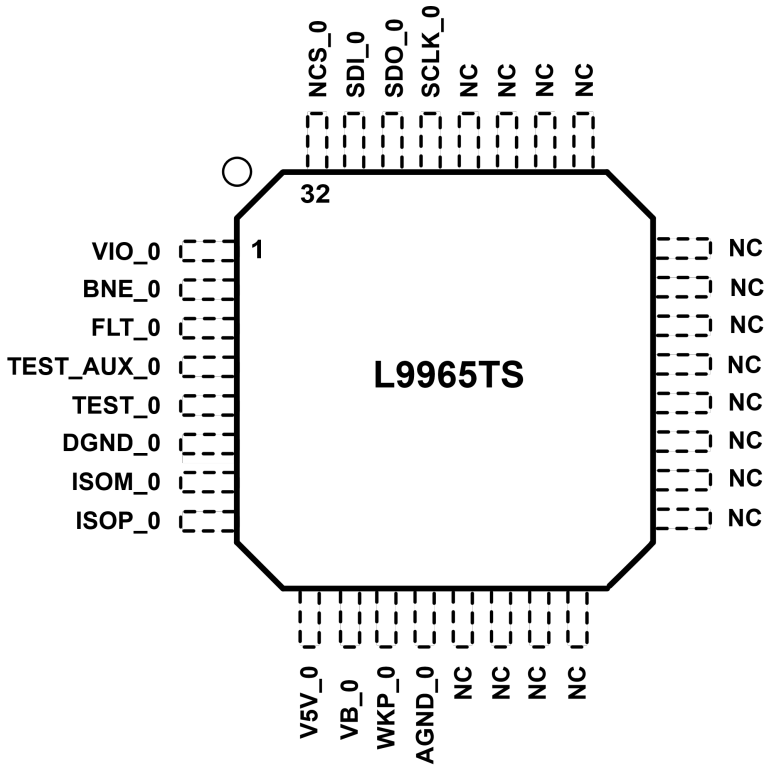


Table 1. L9965T pin function

Pin #	Pin name	Description	Pin type
1	VIO_0	Digital Output Buffer Supply channel 0	Supply
2	BNE_0	Buffer Not Empty flag channel 0	Digital I/O
3	FLT_0	Fault interrupt out channel 0	Digital I/O
4	TEST_AUX_0	Test Mode AUX 0	Reserved(1)
5	TEST_0	Test Mode 0	Reserved(1)
6	DGND_0	Digital Ground channel 0	GND
7	ISOM_0	VIF Port channel 0 (Negative)	Analog I/O
8	ISOP_0	VIF Port channel 0 (Positive)	Analog I/O
9	V5V_0	Internal 5 V supply channel 0	Regulator Out(2)
10	VB_0	Supply input battery compatible channel 0	Supply
11	WKP_0	Wakeup pin channel 0	Analog I/O
12	AGND_0	Analog Ground channel 0	GND
13	SCLK_1	SPI Serial clock channel 1	Digital In
14	SDO_1	SPI Serial Data output channel 1	Digital Out
15	SDI_1	SPI Serial Data Input channel 1	Digital In
16	NCS_1	SPI Chip Select channel 1	Digital In
17	VIO_1	Digital Output Buffer Supply channel 1	Supply
18	BNE_1	Buffer Not Empty flag channel 1	Digital I/O
19	FLT_1	Fault interrupt out channel 1	Digital I/O
20	TEST_AUX_1	Test Mode AUX 1	Reserved(1)
21	TEST_1	Test Mode 1	Reserved(1)
22	DGND_1	Digital Ground channel 1	GND
23	ISOM_1	VIF Port channel 1 (Negative)	Analog I/O
24	ISOP_1	VIF Port channel 1 (Positive)	Analog I/O
25	V5V_1	Internal 5 V supply channel 1	Regulator Out(2)
26	VB_1	Supply input battery compatible channel 1	Supply
27	WKP_1	Wakeup pin channel 1	Analog I/O
28	AGND_1	Analog Ground channel 1	GND
29	SCLK_0	SPI Serial clock channel 0	Digital In
30	SDO_0	SPI Serial Data output channel 0	Digital Out
31	SDI_0	SPI Serial Data Input channel 0	Digital In
32	NCS_0	SPI Chip Select channel 0	Digital In

1. *To be tied to GND*
2. *To be connected to an external filtering capacitor only.*

Table 2. L9965TS pin function

Pin #	Pin name	Description	Pin type
1	VIO_0	Digital Output Buffer Supply channel 0	Supply
2	BNE_0	Buffer Not Empty flag channel 0	Digital I/O
3	FLT_0	Fault interrupt out channel 0	Digital I/O

Pin #	Pin name	Description	Pin type
4	TEST_AUX_0	Test Mode AUX 0	Reserved(1)
5	TEST_0	Test Mode 0	Reserved(1)
6	DGND_0	Digital Ground channel 0	GND
7	ISOM_0	VIF Port channel 0 (Negative)	Analog I/O
8	ISOP_0	VIF Port channel 0 (Positive)	Analog I/O
9	V5V_0	Internal 5 V supply channel 0	Regulator Out(2)
10	VB_0	Supply input battery compatible channel 0	Supply
11	WKP_0	Wakeup pin channel 0	Analog I/O
12	AGND_0	Analog Ground channel 0	GND
13	NC	Not connected	-
14	NC	Not connected	-
15	NC	Not connected	-
16	NC	Not connected	-
17	NC	Not connected	-
18	NC	Not connected	-
19	NC	Not connected	-
20	NC	Not connected	-
21	NC	Not connected	-
22	NC	Not connected	-
23	NC	Not connected	-
24	NC	Not connected	-
25	NC	Not connected	-
26	NC	Not connected	-
27	NC	Not connected	-
28	NC	Not connected	-
29	SCLK_0	SPI Serial clock channel 0	Digital In
30	SDO_0	SPI Serial Data output channel 0	Digital Out
31	SDI_0	SPI Serial Data Input channel 0	Digital In
32	NCS_0	SPI Chip Select channel 0	Digital In

1. *To be tied to GND*
2. *To be connected to an external filtering capacitor only.*

3 Device ratings

3.1 Electrical ratings

The following section describes the different operational ranges.

For each device pin:

- **Operating Range (OR)**: within this range functions operate as specified and without parameter deviations. All the device's electrical parameters are tested and guaranteed in this range and are valid over the whole junction temperature operating range, unless otherwise specified.
- **Absolute Maximum Rating range (AMR)**: within this range functions may not operate properly. However, the IC will not be damaged. Exposure to AMR conditions for extended periods may affect device reliability. Exceeding any AMR may cause permanent damage to the integrated circuit.

Note: Currents are noted with a positive sign when flowing into a pin.

Note: Integrated protections and diagnostics are designed to prevent device destruction under the fault conditions described in the specification. Fault conditions are considered to be out of normal operating range. Protection functions are not designed for continuous repetitive operation.

All device electrical parameters in this document are tested and guaranteed in the operating conditions specified in Table 3 below, unless otherwise noted.

Table 3. Absolute maximum ratings

Param	Description	Test cond	AMR min	OR min	OR typ	OR max	AMR max	Unit	Notes
Power supplies									
V_{VB}	VB_x voltage range	vs. GND	-0.3	6		24	40	V	
V_{VIO}	VIO_x voltage range		3	3		5.5	7	V	
V_{V5V}	V5V: voltage range	vs. GND	-0.3		5		7	V	Regulated supply to be used only for internal use (needed external capacitor) C=1µF + 1µF
Ground									
AGND	Ground		-0.3	-0.1		0.1	0.3	V	
DGND	Ground		-0.3	-0.1		0.1	0.3	V	
VIF									
V_{ISOx} (1)	ISOM_x ISOP_x voltage range	vs. GND	-9	0		V_{V5V}	18	V	AMR account for the maximum voltage that can be withstood during hotplug, BCI, and system level ESD trials
SPI									
V_{NCS}, V_{SDI}, V_{SCK}	NCS, SDI, SCK voltage range		-0.3	0		5.5	7	V	
V_{SDO}	SDO voltage range		-0.3	0		V_{VIO}	V_{VIO} + 0,3	V	fed by VIO (Output)
Digital pins									
BNE	BNE: voltage range		-0.3	0		V_{VIO}	V_{VIO} + 0,3	V	active High, fed by VIO (Output)
FLT	FLT Voltage Range		-0.3	0		V_{VIO}	V_{VIO} + 0,3	V	active High, fed by VIO (Output)
Others									
WKP	WKP Voltage Range		-0.3	0		V_{VB}	V_{VB} + 0.3	V	PMOS open drain

1. *This limit is intended to guarantee DPI EMC, BCI EMC, Hotplug, and ESD 4kV HBM on ISOx pins*

3.2 ESD ratings

Table 4. ESD protection

Test Type	Pin	Value	Unit
HBM(1)	All pins	±2	kV
HBM(1)(2)	ISOPx , ISOMx , VB_x	±4	kV
CDM(3)	All pins	±500	V
CDM(3)	Corner pins	±750	V
Latch-up(4)	All pins	±100	mA

1. *HBM (human body model) test according to AEC-Q100-002*
2. *Each pin is tested versus GND. GND pins connected together*
3. *CDM (Charged Device Model) test according to AEC-Q100-011*
4. *Latch-up test according to AEC-Q100-004 Class-2, Level-A*

3.3 Thermal ratings

All device electrical parameters are tested and guaranteed in the temperature operating conditions reported in Table 5 below, unless otherwise noted.

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating temperature (ECU environment)	-40		125	°C
T_j	Operating junction temperature	-40		150	°C
T_{stg}	Storage temperature	-65		150	°C
$R_{Th\ j\text{-}a}$	Thermal resistance junction-to-ambient(1) (2)		54		°C/W

1. *For each die*
2. *Evaluated according to Jedec JESD51-2, -5, -7 guideline with a 2s2p thermally enhanced PC*

4 Current consumption

L9965T/TS are supplied by VBx pins, which are used to generate all the regulated supplies of related transceiver die.

When used in BEV/PHEV systems, the IC is usually placed in the LV battery junction box, where it is usually supplied by the 12 V battery supply.

Current consumption is reported in different operating modes. Refer to Section 5.1 for functional state definitions.

Table 6. Current consumption for each die

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Pin
I_{VB}(DEEPSLEEP)	Supply Current	DEEPSLEEP -40°C ≤ Tamb ≤ +85°C		4	10	µA	VB
I_{VB}(DEEPSLEEP)	Supply Current	DEEPSLEEP +85°C ≤ Tamb ≤+125°C		10	15	µA	VB
I_{VB}(CYCLIC)	Consumption from VB pin when wakeup timer is active	CYCLIC_COUNT Mode -40°C ≤ Tamb ≤ +85°C		30	37	µA	VB
I_{VB}(CYCLIC)		CYCLIC_COUNT Mode +85°C ≤ Tamb ≤+125°C		40	45	µA	VB
I_{VB}(NORMAL)	Supply Current	NORMAL no current on WKP pin		1.6	2	mA	VB
I_{VIO}(DEEPSLEEP, CYCLIC_COUNT)	VIO Supply Current	DEEPSLEEP CYCLIC_COUNT			1	µA	VIO
I_{VIO}(NORMAL)	VIO Supply Current	NORMAL state, BNE and FLT pins idle		490	600	µA	VIO

5 Functional description

5.1 Device functional states

The following figure shows all possible L9965T and L9965TS states.

Figure 5. L9965T/TS functional state mode (FSM)

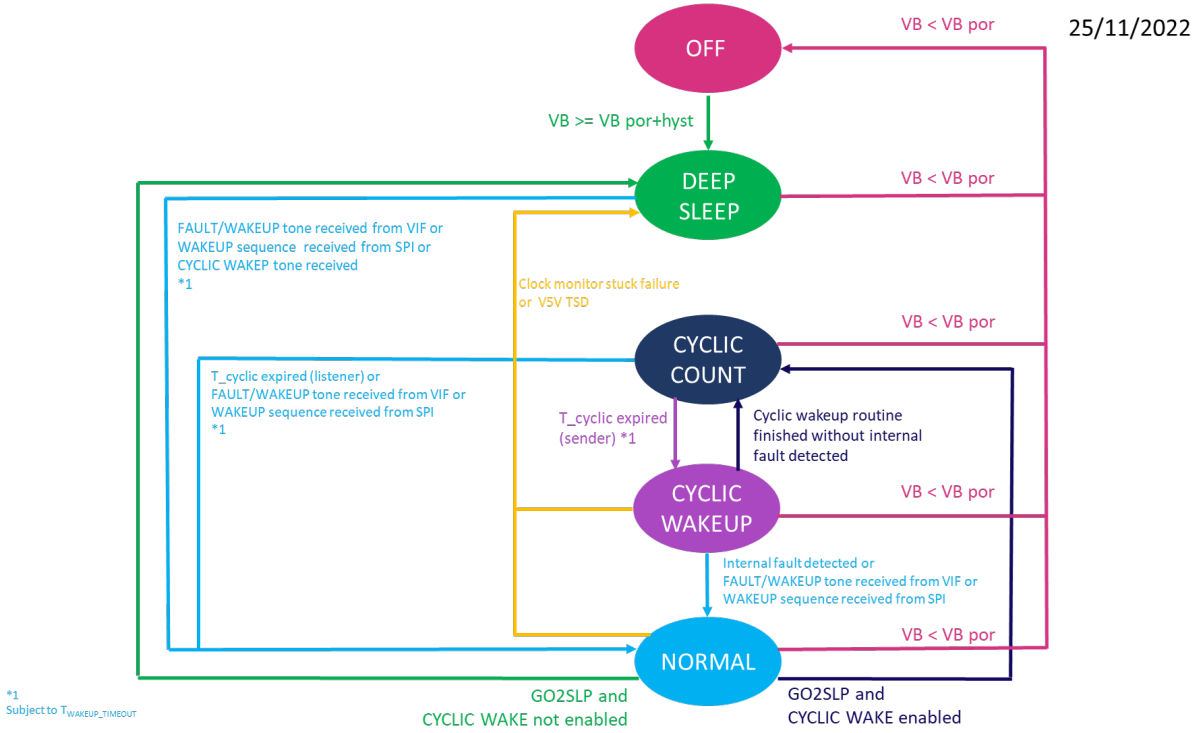


Table 7. Device functional states

State	Purpose	Reached from	Condition	Active resources
OFF	Device OFF	Any state	When VB voltage falls below the POR threshold	None
DEEPSLEEP	Ultra-low power state for managing long inactivity periods	NORMAL	• GO2SLP command received AND no CYCLIC_WAKEUP timer enabled (GEN_CFG5.WAKEUP_CYCLIC_ENB=0) • OSC STUCK detected • V5V_OT detected	Wake up Via VIF Wake up via SPI Target
		CYCLIC_ WAKEUP	• OSC STUCK detected • V5V_OT detected	
		OFF	VB > POR threshold + hysteresis	
CYCLIC_COUNT	Performs count in order to cyclically wake-up the system	CYCLIC_ WAKEUP	CYCLIC_WAKEUP routine finished without internal fault detected	Wake up Via VIF Wake up via SPI Target Cyclic wakeup timer as configured during NORMAL mode
		NORMAL	GO2SLP command validated AND CYCLIC_WAKEUP timer enabled (GEN_CFG5.WAKEUP_CYCLIC_ENB=1)	

State	Purpose	Reached from	Condition	Active resources
CYCLIC_WAKEUP	To perform cyclic diagnostics during low power operation	CYCLIC_ COUNT	CYCLIC_WAKEUP timer expired (in sender mode)	Wake up Via VIF Cyclic wakeup diagnostic routine
NORMAL	Full operation	DEEP SLEEP	• FAULT/WAKEUP tone received from VIF • CYCLIC_WAKEUP tone received from VIF • WAKEUP command received from SPI	All resources fully operative
		CYCLIC_ COUNT	• FAULT/WAKEUP tone received from VIF • WAKEUP command received from SPI • CYCLIC_WAKEUP timeout expired (in listener mode)	
		CYCLIC_ WAKEUP	• Internal fault detected during diagnostic routine • FAULT/WAKEUP tone received from VIF • WAKEUP command received from SPI	

For the special frames VIF FAULT/WAKEUP tone, VIF CYCLIC_WAKEUP tone and SPI WAKEUP sequence, refer to Section 5.8.3.

5.1.1 NORMAL State and wakeup sources

In NORMAL mode all resources are fully available.

5.1.1.1 Wakeup Sources

The L9965T/TS responds to three wakeup sources:

- **Wakeup via VIF**
  - The IC is daisy-chained on the VIF bus along with other companion chips, and can be woken up by VIF special frames (CYCLIC WAKEUP or FAULT/WAKEUP frames) sent from another device (see Section 5.8.3)
- **Wakeup via SPI**
  - The IC can be woken up by any dummy frame received on the SPI
- **Self-Wakeup**
  - A wakeup trigger is internally generated when the device is in CYCLIC_WAKEUP mode (see Section 5.1.2).

The device can reach NORMAL state from low power states by the wakeup via SPI and via VIF sources, described below.

Whenever a wakeup source is validated, the wakeup sequence is initiated and shall successfully end within $T_{WAKEUP\_TIMEOUT}$. Otherwise, the IC returns to DEEPSLEEP state

5.1.1.1.1 Wakeup via VIF

When in DEEPSLEEP, CYCLIC_WAKEUP or CYCLIC_COUNT the IC is sensitive to wakeup signals incoming on VIF port (see Section 5.8.3).

Figure 6 shows a typical application scenario where some L9965x in the chain has self-detected a fault and wakes up the daisy-chain sending the FAULT/WAKEUP tone on both VIF ports.

The wakeup by fault of a VIF daisy chain device is an asynchronous event with respect to the CYCLIC_WAKEUP thread managed in background by the L9965T/TS. Fault notification mechanism guarantees that the FAULT/WAKEUP tone is correctly propagated at least in one direction, even in case of conflict with the CYCLIC_WAKEUP tone.

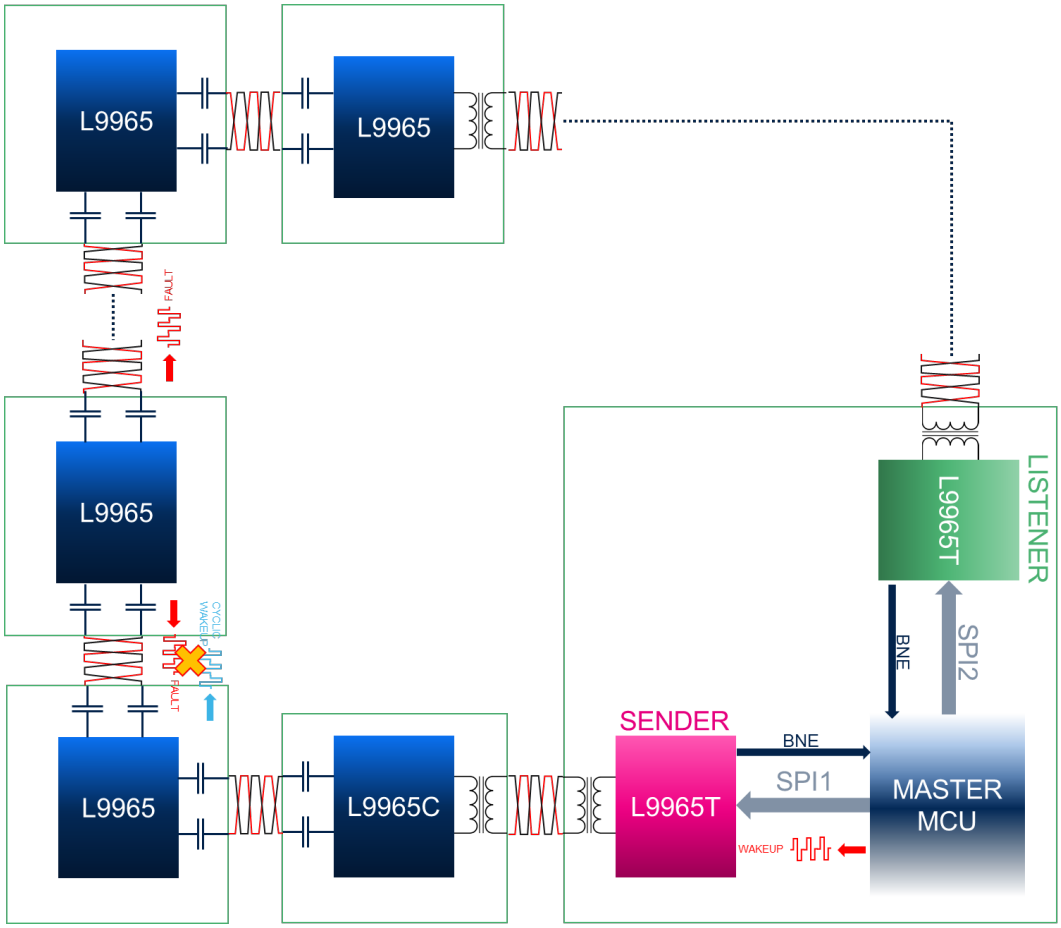
Depending on the position of the sending L9965x in the daisy chain, the wakeup interrupt reaches the MCU in approximately less than:

$½*N_{VIF\_STACK}*T_{VIF\_WAKEUP\_TIME} \leq t \leq N_{VIF\_STACK}*T_{VIF\_WAKEUP\_TIME}$.

In a ring topology, a FLT pin interrupt is generated from both channels of L9965T within N_{VIF_STACK}*$T_{VIF\_WAKEUP\_TIME}$ timeout.

When the MCU is woken up by one channel of L9965T, it is supposed to wait also for the other channel to generate the FLT pin interrupt to confirm the daisy-chain wakeup. If such event does not occur within the N_{VIF_STACK}*$T_{VIF\_WAKEUP\_TIME}$ timeout, the MCU shall run the VIF chain wakeup by MCU procedure.

Figure 6. Wakeup by fault of a daisy chain device



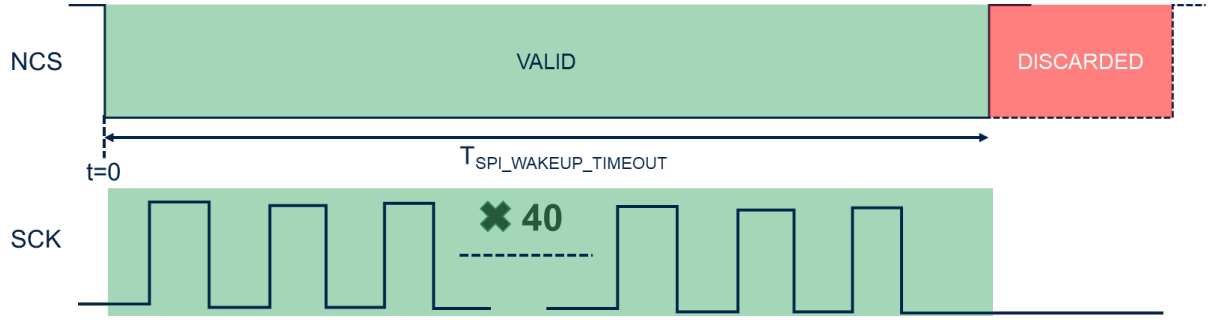
5.1.1.1.2 Wake-up via SPI

L9965T/TS can be woken up in DEEPSLEEP, CYCLIC_COUNT and CYCLIC_WAKEUP state by any valid SPI frame issued by MCU on the SPI Target. A wakeup condition is acknowledged when the following pattern is received:

1. A NCS high to low transition
2. 40 SCK pulses
3. A NCS low to high transition

The $T_{SPI\_WAKEUP\_TIMEOUT}$ is started upon every NCS assertion, and the wakeup pattern shall end before timeout expiration, otherwise it is discarded.

Figure 7. **Wakeup condition by SPI Slave**



Wakeup frames are not decoded: their content may be arbitrary. However, it is strongly recommended to send READ commands to avoid inadvertent write operations in case the device is already awake.

5.1.1.2 *NORMAL State diagnostics*

In this state several diagnostic functions are available:

1. NVM data integrity check
2. Periodic check of registers data integrity, if configured by GENERAL_REG.CYC_CRC_DIS
3. Oscillator fail
4. Oscillator stuck: if detected, logic block is immediately put under reset and the device moves to DEEPSLEEP state (immediate reaction)
5. Oscillators monitor BIST
6. VB undervoltage
7. V3V3 overvoltage
8. V5V overvoltage
9. V5V undervoltage
10. V5V overcurrent
11. GND loss if configured by the GEN_CFG4.EN_GND_LOSS bit
12. Analog comparators BIST if configured by the GEN_CFG5.BIST_ANA_ENB = 1
    a. VB undervoltage comparator analog BIST
    b. V3V3 overvoltage comparator analog BIST
    c. V5V undervoltage comparator analog BIST
    d. V5V overvoltage comparator analog BIST
13. WKP, FLT and BNE pins diagnostics
14. Thermal-shutdown monitoring
15. VIF communication monitoring
16. SPI communication monitoring.

All the fault and events detected by L9965T/TS are latched in a corresponding status bits and can be read by the BMS MCU through SPI communication.

The most relevant faults and events are reported, according to fault detection mask registers, in the internal GSW (Global Status Word). The OR combination of all the bits in the GSW is signaled by the FAULT bit of the SPI MISO frame shown in Table 26 and notified by the FLT pin (HIGH if at least one of the bits in the GSW is set) to trigger an MCU interrupt.

Assert condition and behavior of each fault are described in detail in the related section.

5.1.2 CYCLIC_WAKEUP State

When all the BMS system is in low power mode, the L9965T/TS can be configured to automatically trigger chain monitoring, according to the system topology (single access or ring), alternating CYCLIC_COUNT and CYCLIC_WAKEUP states.

5.1.2.1 *CYCLIC_WAKEUP State operation*

To configure CYCLIC_WAKEUP state the following procedure must be followed.

Procedure 1: Set up of CYCLIC_WAKEUP state

1. Program the proper T_{CYCLIC_WAKEUP} in GEN_CFG5.WAKEUP_CYCLIC_TIMEOUT_SENDER_SEL register
2. Enable the CYCLIC_WAKEUP by setting the GEN_CFG5.WAKEUP_CYCLIC_ENB bit in GEN_CFG5 register
3. Send a global broadcast GO2SLP command (Section 5.8.3.3) to move all the ICs in low power mode
4. L9965T/TS moves to CYCLIC_COUNT state. The value of the cyclic counter during CYCLIC_COUNT state is stored in GEN_STATUS2.WAKEUP_CYCLIC_TRX_COUNTER. The LSB of this register is 4.096e-3 seconds.

Step 1, 2 and 3 of the above procedure must be applied on both channels of the L9965T if configured in ring topology.

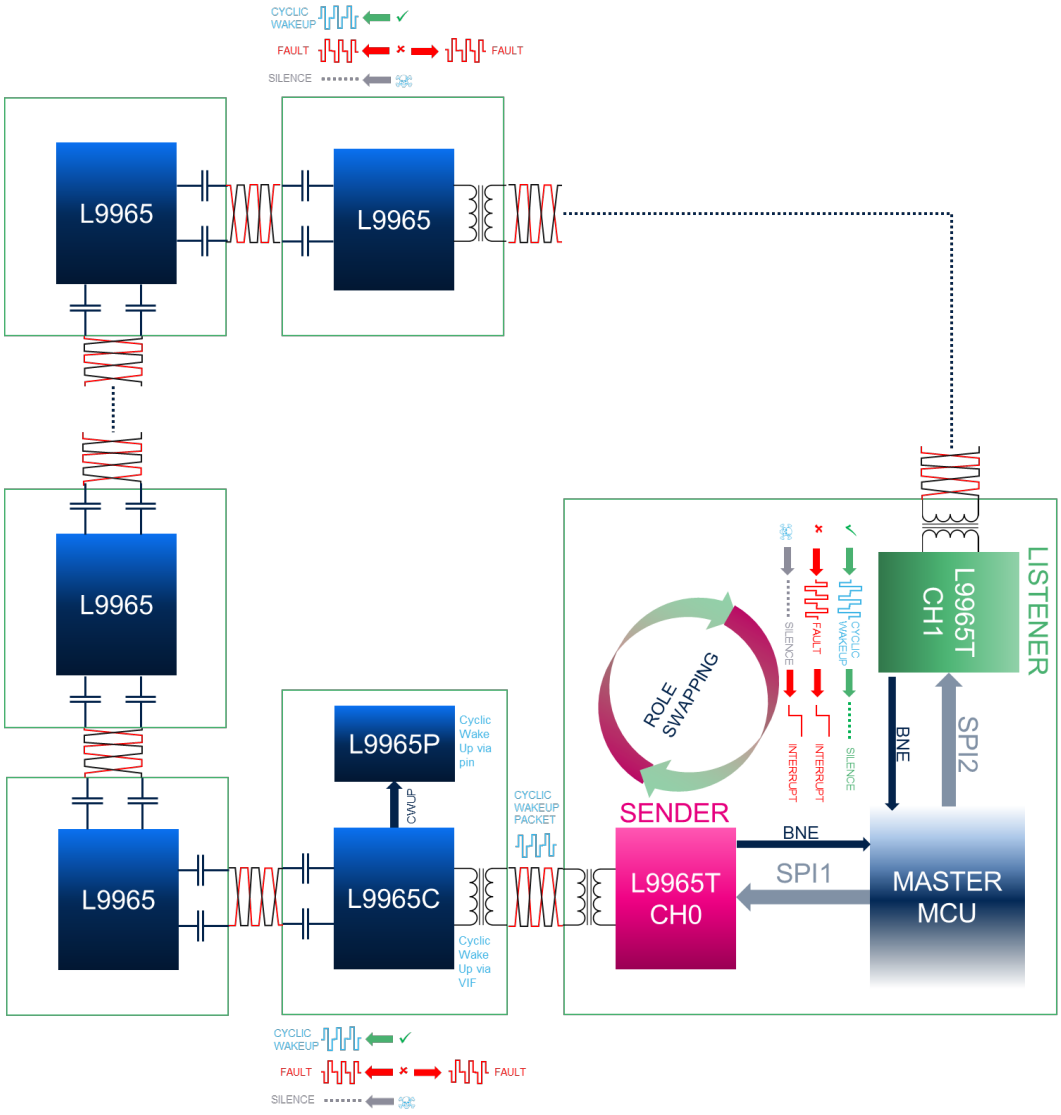
The system operates as shown in Figure 8 according to the daisy-chain topology.

Ring topology:

- **Dual transceiver scenario**: the two L9965T channels should be configured by the MCU in sender (setting GEN_CFG5.WAKEUP_CYCLIC_SENDER bit) and listener (setting CFG5.WAKEUP_CYCLIC_ LISTENER bit) modes.
- **Single transceiver scenario**: If the devices are connected in single access daisy chain, the last L9965A device in the chain can be configured to propagate backward the CYCLIC_WAKEUP tone. In this case the single transceiver channel should be configured by the MCU in sender (setting GEN_CFG5.WAKEUP_CYCLIC_SENDER bit).
- As sender, the transceiver has the VIF RX and VIF TX both enabled. After T_{CYCLIC_WAKEUP} the sender moves from CYCLIC_COUNT to CYCLIC_WAKEUP state, performs the internal diagnosis (see Section 5.1.2.2) and, if no faults are present, it sends a CYCLIC_WAKEUP tone on the VIF to wake up one by one the devices on the daisy chain, then changes his role to listener, set the timer threshold at $T_{CYCLIC\_WAKEUP\_TIMEOUT}$, and moves again to CYCLIC_COUNT state.
- The listener (can be either the The transceiver channel on the opposite end of the ring, or the single transceiver switched from sender in the previous step) has the VIF RX enabled and VIF TX disabled. If the CYCLIC_WAKEUP tone arrives within $T_{CYCLIC\_WAKEUP\_TIMEOUT}$, the “no fault” condition is acknowledged, the listener changes his role to sender, the timer is reset to count until T_{CYCLIC_WAKEUP} and the cycle starts again in the opposite direction.
- If the CYCLIC_WAKEUP tone is not received within $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ when transceiver is listener, it moves to NORMAL state and asserts the WKP and FLT pins (to wake up the MCU) and set GEN_STATUS2.WAKEUP_CYCLIC_TRX_TIMEOUT bit.
- If during the internal diagnosis phase a fault is asserted, the device moves to NORMAL state. According to fault detection mask registers GEN_CFG2 and GEN_CFG3, fault detection is notified by the FLT pin (asserted HIGH) and reported on the FAULT bit of the SPI MISO frame shown in Table 26. Depending on its configuration (see Section 5.9.3) also WKP pin may be asserted HIGH in case of faults. In this case no CYCLIC_WAKEUP tone is generated.

Single access: L9965TS channel moves to CYCLIC_WAKEUP state, performs the diagnostics in Section 5.1.2.2 and generates a CYCLIC_WAKEUP tone every T_{CYCLIC_WAKEUP} period. The transceiver is sensitive to fault wakeup from VIF and wakeup by MCU.

Figure 8. **CYCLIC_WAKEUP operation**



The CYCLIC_WAKEUP state can be divided in three phases:

1. Transition phase from CYCLIC_COUNT to CYCLIC_WAKEUP state.
2. Diagnostic phase
3. CYCLIC_WAKEUP tone generation (see Section 5.8.3.7). CYCLIC_WAKEUP tone is generated only if there aren't fault recorded during diagnostic phase.

During CYCLIC_WAKEUP state every VIF data frame is not recognized by the device, and only FAULT/WAKEUP tones (see Section 5.8.3.8) and SPI wakeup commands (see Section 5.8.3.2) are accepted.

Device reaction to incoming wake-up tones from VIF or from SPI Target are the following:

- During transition phase from CYCLIC_COUNT to CYCLIC_WAKEUP state: IC moves to NORMAL and sets FLT and WKP outputs (depending on the setting of WKP pin, see Section 5.9.3). Device never completes the CYCLIC_WAKEUP phase.
- During diagnostic phase: IC moves to NORMAL state (it becomes again sensitive to VIF communication) and sets FLT and WKP outputs (depending on the setting of WKP pin, see Section 5.9.3); diagnostic routine continues until completion.
- During CYCLIC_WAKEUP tone generation device moves to NORMAL state.

5.1.2.2 *CYCLIC_WAKEUP State diagnostics*

During the CYCLIC_WAKEUP state the following diagnostics are automatically performed:

1. NVM trimming data CRC
2. NVM configuration data CRC
3. Oscillator fail
4. Oscillator stuck: if detected, logic block is immediately put under reset and the device moves to DEEPSLEEP state (immediate reaction)
5. Oscillators Monitor BIST
6. V3V3 overvoltage
7. V5V overvoltage
8. V5V undervoltage
9. V5V overcurrent
10. GND loss (In CYCLIC_WAKEUP this diagnosis is executed automatically independently by the value of GND_LOSS_ENABLE bit)
11. Analog BIST:
    a. V3V3 overvoltage comparator analog BIST
    b. V5V overvoltage comparator analog BIST
    c. V5V undervoltage comparator analog BIST
    d. GND loss comparator BIST
12. Thermal-shutdown monitoring.

If at least one of the above faults is verified, the device moves to NORMAL state and the fault detection is latched in the corresponding bit of the status registers GEN_STATUS1 and GEN_STATUS3. Faults that may happen within VIF tone generation time will not cause a transition to NORMAL state.

According to fault detection mask registers GEN_CFG2 and GEN_CFG3, fault detection is notified by the FLT pin (asserted HIGH) and reported on the FAULT bit of the SPI MISO frame shown in Table 26. Depending on its configuration (see Section 5.9.3), the WKP pin may also be asserted HIGH in case of faults. In this case, no CYCLIC_WAKEUP tone is generated.

Assert condition and behavior of each fault are described in detail in the related section.

In addition to the above faults monitoring, a timeout counter ($T_{CW\_diag\_timeout}$) is running in background during diagnostic phase to monitor its duration.

Table 8. CYCLIC_WAKEUP timeout diagnostic

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
CYCLIC_WAKEUP Duration Timeout	Diagnostic time in CYCLIC_WAKEUP $t > T_{CW\_diag\_timeout}$	• Diagnostic routine is interrupted • Device moves to NORMAL • GEN_CFG5.WAKEUP_CYCLIC_END = 1 • The FLT pin, the WKP pin and the SPI FAULT are asserted	Clear on read	Non maskable
CYCLIC_WAKEUP	Tone not received in $T_{CYCLIC\_WAKEUP\_TIMEOUT}$ when transceiver is listener	• Device moves to NORMAL • GEN_CFG5.WAKEUP_CYCLIC_TRX_TIMEOUT = 1 • The FLT pin, the WKP pin and the SPI FAULT are asserted	Clear on read	Non maskable

5.1.3 Electrical parameters

Table 9. FSM and Wakeup electrical parameters

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{FIRST\_POWERUP}$	Time needed to perform first power-up sequence (to reach DEEP_SLEEP state)				1	ms

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{WAKEUP}	Time from wakeup detection to ISOL-ISOP ready to transmit				3	ms
$T_{VIF\_WAKEUP\_TIME}$	Duration of wakeup from VIF detection				2	ms
$T_{SPI\_WAKEUP\_TIME}$	Duration of wakeup from SPI detection	From the NCS low to high transition to the IC in NORMAL state and ready to communicate			2	ms
T_{SELF_WAKEUP}	Self-wakeup latency	From the assertion of a fault in CYCLIC_WAKEUP to the complete transition in NORMAL			2	ms
$T_{SPI\_WAKEUP\_TIMEOUT}$	Timeout for receipt of wakeup frame		0.4		2	ms
$T_{CW\_diag\_timeout}$	Diagnostics timeout		55		75	ms
$T_{WAKEUP\_TIMEOUT}$	Timeout for completing the wakeup sequence		17	20	33	ms
$T_{CYCLIC\_WAKEUP\_000}$	Transceiver CYCLIC_WAKEUP tone generation period	GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=000	0.96	1.06	1.15	s
$T_{CYCLIC\_WAKEUP\_001}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=001	1.90	2.10	2.30	
$T_{CYCLIC\_WAKEUP\_010}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=010	.90	3.20	3.50	
$T_{CYCLIC\_WAKEUP\_011}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=011	3.80	4.20	4.60	
$T_{CYCLIC\_WAKEUP\_100}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=100	4.802	5.30	5.80	
$T_{CYCLIC\_WAKEUP\_101}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=101	5.80	6.35	6.90	
$T_{CYCLIC\_WAKEUP\_110}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=110	6.70	7.45	8.20	
$T_{CYCLIC\_WAKEUP\_111}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_SENDER_SEL=111	7.70	8.45	9.20	
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_000}$	Transceiver CYCLIC_WAKEUP timeout	GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=000	2.70	3.00	3.30	s
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_001}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=001	4.37	4.86	5.34	
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_010}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=010	6.04	6.71	7.39	
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_011}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=011	7.71	8.57	9.43	
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_100}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=100	9.39	10.43	11.47	
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_101}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=101	11.06	12.29	13.51	
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_110}$		GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=110	12.73	14.14	15.56	

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{CYCLIC\_WAKEUP\_TIMEOUT\_111}$	Transceiver CYCLIC_WAKEUP timeout	GEN_CFG5.WAKEUP_CYCLIC_ TIMEOUT_LISTENER_SEL=111	14.40	16.00	17.60	s
T_{SELF_WAKEUP}	Self-wakeup latency	From the assertion of a fault in CYCLIC_WAKEUP to the complete transition in NORMAL			2	ms
$T_{SPI\_WAKEUP\_TIMEOUT}$	Timeout for receipt of wakeup frame		0.4		2	ms

5.2 Power supply section

The VB pin is the main supply:

- It feeds the 5V LDO (V5V)
- It feeds the 3V3 Internal LDO (V3V3)
- It is directly connected to WKP pin

5.2.1 V_B battery supply

5.2.1.1 Diagnostic functions

Table 10. Power supply diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
VB UV	$V_{VB} < V_{VB\_UV\_TH}$	• VB_UV = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT are asserted in NORMAL if MSK_VB_UV=0 in GEN_CFG3	Clear on read if $V_{VB} > V_{VB\_UV\_TH} + V_{VB\_UV\_HYS}$	• VB_UV status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_VB_UV in GEN_CFG3

5.2.1.2 Electrical parameters

Table 11. Power supply electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V_{VB\_UV\_TH}$	VB Undervoltage Threshold	Tested in production	4.75	5	5.25	V
$V_{VB\_UV\_HYS}$	VB Undervoltage hysteresis	Tested in production	85		185	mV
$T_{VB\_UV\_FIL}$	VB Undervoltage filter time	Tested by SCAN		20		µs

5.2.2 VIO output buffer supply

This supply must be powered externally by a regulated 3.3V or 5V voltage (could be from MCU PMIC).
It powers SDO, FLT, and BNE interface pins.

5.2.3 V3V3 internal LDO

This is the internal 3.3V LDO:

- It is fed by the VB main supply
- It is used for supplying internal circuitry

When in undervoltage, it determines the POR_MAIN assertion.

The bit GEN_CFG5.POR_SLEEP_ASSERTED indicates that a transition to OFF state has occurred or that an oscillator stuck condition has been previously detected. At the first power-up, this bit is normally asserted.

5.2.3.1 Diagnostics functions

Table 12. Power supply diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
V3V3 OV	V_{3V3} > $V3V3_{OV\_TH}$ for t > $T_{V3V3\_OV\_FIL}$	• V3V3_INT_OV=1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_V3V3_INT_OV=0 in GEN_CFG3	Clear on read if V_{3V3} < $V_{V3V3\_OV\_TH}$ + $V_{V3V3\_OV\_HYS}$ for t>$T_{V3V3\_OV\_FIL}$	• V3V3_INT_OV status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_V3V3_INT_OV in GEN_CFG3

5.2.3.2 Electrical parameters

Table 13. Power supply electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$V3V3_{OV\_TH}$	Overvoltage threshold		3.45	3.71	3.97	V
$V3V3_{OV\_HYS}$	Undervoltage hysteresis		10		60	mV
$T_{3V3\_OV\_FIL}$	OV filter time	Tested by SCAN	17		23	µs

5.2.4 5V LDO (V5V)

This is the 5V LDO:

- It is fed by VB main supply
- It feeds the Isolated Vertical Interface (VIF)

5.2.4.1 Diagnostic functions

The undervoltage, overvoltage (caused by external load on V5V pin) and overcurrent (short-to-GND scenario) conditions are covered by dedicated diagnostics.

The V5V pin is protected by a thermal sensor and shut-down comparator. For this diagnostic, refer to Section 5.4.

All V5V monitoring features are available in NORMAL and CYCLIC_WAKEUP states.

Table 14. V5V LDO diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
V5V UV	V_{V5V} < $V_{V5V\_UV\_TH}$ for t > $T_{V5V\_UV\_OV\_FIL}$	• V5V_UV = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_V5V_UV=0 in GEN_CFG3	Clear on read if V_{V5V} > $V_{V5V\_UV\_TH}$ + $V_{V5V\_UV\_HYS}$ for t>$T_{V5V\_UV\_OV\_FIL}$	• V5V_UV status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_V5V_UV in GEN_CFG3
V5V OV	V_{V5V} > $V_{V5V\_OV\_TH}$ for t> $T_{V5V\_UV\_OV\_FIL}$	• V5V_OV = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_V5V_OV=0 in GEN_CFG3	Clear on read if V_{V5V} < $V_{V5V\_OV\_TH}$ - $V_{V5V\_OV\_HYS}$ for t>$T_{V5V\_UV\_OV\_FIL}$	• V5V_OV status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_V5V_OV in GEN_CFG3
V5V OC	I_{V5V} > $I_{TH\_OC\_V5V}$ for t> $t_{FLT\_OC\_V5V}$	• V5V_OC = 1 in GEN_STATUS3	Clear on read if I_{V5V} < $V_{V5V\_OV\_TH}$ - $V_{V5V\_OV\_HYS}$	• V5V_OC status bit non maskable

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
		• The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_V5V_OC=0 in GEN_CFG3	for t>$T_{V5V\_UV\_OV\_FIL}$	• FLT pin and SPI FAULT maskable by bit MSK_V5V_OC in GEN_CFG3

5.2.4.2 *Electrical parameters*

Table 15. V5V electrical parameters

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{V5V}	Regulated voltage	NORMAL, All operating lines and loads	-2%	5	+2%	V
I_{V5V_LIM}	Current limitation	NORMAL, V_{V5V} = 0V Tested in production	-220		-80	mA
C_{V5V}	External LDO capacitance	Application info. Electrical parameters guaranteed from 1.6µF to 2.64µF. Stability down 0.8µF.	0.8	2	2.64	µF
$T_{V5V\_SOFT\_START}$	Soft start timing	From 10% to 90% of $V_{V5V,}$ Guaranteed by design			200	µs
$V_{V5V\_UV\_TH}$	V5V Undervoltage Threshold	Tested in production	4.25		4.75	V
$V_{V5V\_UV\_HYS}$	V5V Undervoltage hysteresis	Tested in production	50		150	mV
$V_{V5V\_OV\_TH}$	V5V Overvoltage Threshold	Tested in production	5.4		6	V
$V_{V5V\_OV\_HYS}$	V5V Overvoltage hysteresis	Tested in production	50		150	mV
$T_{V5V\_UV\_OV\_FIL}$	UV/OV filter time	Tested by SCAN	17		23	µs
$I_{TH\_OC\_V5V}$	V5V overcurrent monitor, threshold current		-185	-145	-85	mA
$t_{FLT\_OC\_V5V}$	V5V overcurrent monitor, detection filter time	Digital filter	17	20	23	µs

5.3 Analog BIST

The IC embeds an analog built-in self-test (BIST) to prevent latent failures affecting safety relevant comparators.

In CYCLIC_WAKEUP state the BIST procedure is executed automatically within the diagnostic routine and it covers the following comparators:

- V3V3 OV
- V5V UV
- V5V OV
- GND LOSS

The BIST procedure can be started in NORMAL state by setting GEN_CFG5.BIST_ANA_ENB = 1 in and covers the following comparators:

- VB UV
- V3V3 OV
- V5V UV
- V5V OV

The bit GEN_STATUS3.BIST_ANA_DONE= 1 confirms the correct execution of the BIST procedure.

5.3.1 Diagnostic functions

Table 16. Analog BIST diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
Analog BIST failure	• VB_UV or • V3V3 OV or • V5V UV or • V5V OV comparator fail in NORMAL. • V3V3 OV or • V5V UV or • V5V OV or • GND LOSS comparator FAIL in CYCLIC_WAKEUP	• BIST_ANA_FAIL = 1 in GEN_STATUS3 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_BIST_ANA_FAIL = 0 in GEN_CFG3	Clear on read	• BIST_ANA_FAIL status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_BIST_ANA_FAIL in GEN_CFG3

5.4 Thermal shutdown

The device embeds a thermal sensor and shut-down comparator to protect, in case of short to GND, the following pins:

- V5V pin (see Section 5.2.4)
- WKP driver circuit (see Section 5.9.3).

Thermal shutdown feature is enabled only after V5V regulator has completed the power-up phase.

5.4.1 Diagnostic functions

When both thermal shutdown and V5V overcurrent are detected concurrently, V5V regulator is immediately disabled and IC moves to DEEPSLEEP state; after a new successful power-up, the V5V_OT flag set is still readable to the user, as this bit only is not cleared in DEEPSLEEP mode.

When thermal shutdown is detected concurrently to WKP_ERR detection (see Section 5.9), a fault is detected and WKP driver is immediately disabled, it can be re-engaged if the fault condition is removed.

Table 17. Thermal shutdown diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to status bit clear	Maskable
TSD	$T_J > T_{TH\_TSD\_V5V}$ for t> $t_{FLT\_TSD\_V5V}$	• TSD = 1 in GEN_STATUS3 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_TSD=0 in GEN_CFG3	Clear on read if $T_J < T_{TH\_TSD\_V5V} - T_{TH\_HYS\_TSD\_V5V}$ for t>$t_{FLT\_TSD\_V5V}$		• TSD status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_TSD in GEN_CFG3
V5V OT	V5V_OC = 1 and TSD = 1	• V5V_OT = 1 in GEN_STATUS1 • V5V regulator is disabled • Transition to DEEP SLEEP state	Clear on read after successful power-up		Non maskable

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to status bit clear	Maskable
WKP_OT	WKP_ERR = 1 and TSD = 1	• WKP driver is disabled • WKP_OT = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_WKP_OT =0 in GEN_CFG3	Clear on read if fault condition is removed	The driver is reengaged	• TSD status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_WKP_OT in GEN_CFG3

5.4.2 Electrical parameters

Table 18. Thermal shutdown electrical parameters

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{TH\_TSD\_V5V}$	V5V thermal shut-down, threshold equivalent temperature	Guaranteed by design		165		deg
$T_{TH\_HYS\_TSD\_V5V}$		Guaranteed by design		10		deg
$t_{FLT\_TSD\_V5V}$	V5V thermal shut-down, detection filter time	Digital filter	17	20	23	µs

5.5 Ground loss monitor

To detect failures in grounding, the IC integrates a ground loss monitor. Such diagnostic is available on-demand in NORMAL state to cover latent failures. Diagnostic execution is enabled programming GEN_CGF_4.EN_GND_LOSS = 1.

5.5.1 Diagnostic functions

Table 19. Ground loss monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
AGND, DGND LOSS	• |AGND – DGND| > $V_{GND\_LOSS\_TH}$ for t > $T_{GND\_LOSS\_FIL}$	• GND_LOSS = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT are asserted in NORMAL if MSK_GND_LOSS = 0 in register GEN_CFG3	Clear on read if |AGND – DGND| < $V_{GND\_LOSS\_TH}$ for t > $T_{GND\_LOSS\_FIL}$	• GND_LOSS status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_GND_LOSS in GEN_CFG3

5.5.2 Electrical parameters

Table 20. Ground loss monitor characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Pin
$V_{GND\_LOSS\_TH}$	Ground loss detection threshold	Tested in production	100	200	300	mV	AGND, DGND
$T_{GND\_LOSS\_FIL}$	Ground loss detection filter time	Tested by SCAN		300		µs	AGND, DGND

5.6 Oscillators

Each transceiver channel embeds two oscillators.

A low frequency oscillator operates at f_{OSCI_SLEEP} in the following states:

- In DEEPSLEEP state it is the time base for wakeup source detection (SPI, VIF)

- In CYCLIC_COUNT it is used to feed the CYCLIC_WAKEUP timer
- In NORMAL it is used for clock monitoring functionality.A high frequency oscillator operates at f_{MAIN_OSC} and it is active in NORMAL and CYCLIC_WAKEUP states

5.6.1 Diagnostic functions

When in NORMAL or in CYCLIC_WAKEUP state, the two oscillators monitor each-other to ensure that the frequency is in the allowed range. If the oscillator frequency is not in the correct operating range, the power up and down transitions and related timing may be affected. Any frequency drift can be detected by the oscillator monitor.

The oscillator monitor is covered, for latent fault detection, by BIST at each transition from low power states to NORMAL and CYCLIC_WAKEUP modes.

Table 21. Oscillator Monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
OSC FAIL	$\lvert f_{OSCI\_SLEEP} - f_{MAIN\_OSC}/32 \rvert > f_{OSC\_MON\_ERR}$	• OSC_FAIL = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_OSC_FAIL =0 in GEN_CFG3	Clear on read	• MSK_OSC_FAIL status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_OSC_FAIL in GEN_CFG3
OSC STUCK	$T_{OSC\_STUCK} > T_{OSCI\_STUCK\_TIMEOUT}$	• The device moves in DEEPSLEEP state • POR_SLEEP_ASSERTED =1 in GEN_CFG5 • Device configurations are restored to default values	-	Non maskable
OSC MON BIST	During transition to NORMAL and CYCLIC_WAKEUP, if oscillator monitor logic check fails	• BIST_OSC_FAIL=1 in GEN_STATUS3 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_BIST_OSC_FAIL=0 in GEN_CFG3	Clear on read(1)	• BIST_OSC_FAIL status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_BIST_OSC_FAIL in GEN_CFG3

1. *This flag must be checked at least 12 ms after the power-up.*

5.6.2 Electrical parameters

Table 22. V5V electrical parameters

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{OSCI_SLEEP}	Stand-by oscillator frequency	Tested in production	-8%	500	+8%	kHz
f_{MAIN_OSC}	Oscillator frequency	Tested in production	-5%	16	+5%	MHz
$f_{OSC\_MON\_ERR}$	Oscillator delta frequency threshold	Guaranteed by SCAN	25		36	%
$T_{OSCI\_STUCK\_TIMEOUT}$	Oscillator stuck detection timeout	Guaranteed by SCAN		2		ms

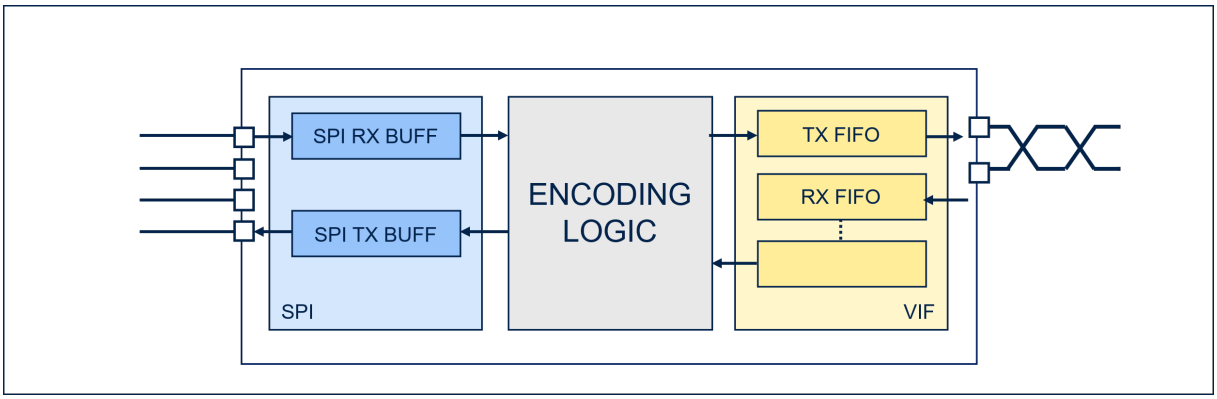
5.7 Communication interfaces

The L9965T/TS implements two communication interfaces allowing BMS microcontroller access to internal registers and interaction with all the L9965x chained devices:

- SPI Target, described in Section 5.7.1: used by the controller MCU to access the L9965T/TS device.
- Isolated Vertical Interface (VIF), described in Section 5.7.2: used by L9965T/TS device to communicate with the L9965x devices connected in daisy chain on the VIF bus.

As shown in Figure 9 below, the SPI frame from MCU is temporarily stored in the VIF port TX FIFO (depth 1) to be transmitted to the chained device, while the incoming frames from VIF are stored in the RX FIFO (depth 32), where they can be read by the MCU. For the communication protocol details, see Section 5.8.

Figure 9. SPI – VIF interface management



5.7.1 SPI target

The registers of both the L9965T/TS and all the L9965x devices connected by VIF on the daisy chain can be accessed by MCU when devices are in NORMAL state, performing read/write operations on the transceiver through SPI.

SPI port is available for communication only in NORMAL functional state. In DEEPSLEEP, CYCLIC_COUNT and CYCLIC_WAKEUP states only NCS and SCLK pins are active to recognize the wake-up sequence.

5.7.1.1 Physical layer

The SPI target peripheral pins and settings are described below.

Table 23. SPI pins description

PIN	Function	I/O type	Notes	Active states
NCS	Chip Select	Digital In	weak pullup R_{IN_PU}	DEEPSLEEP, CYCLIC_COUNT and CYCLIC_WAKEUP (to recognize the wake-up sequence) NORMAL
SDI	Serial Data Input	Digital In	weak pulldown R_{IN_PD}(1)	NORMAL
SDO	Serial Data Output	Digital Out	The output buffer is connected to VIO	NORMAL
SCLK	Serial Clock	Digital In	weak pulldown R_{IN_PD}a	DEEP_SLEEP, CYCLIC_COUNT and CYCLIC_WAKEUP (to recognize the wake-up sequence) NORMAL

1. *Weak pull-down resistors on SDI and SCLK pins and weak pull-up on NCS pin are always enabled to address open failures.*

Table 24. SPI overview

Parameter	Description
Protocol	Out of frame
Single frame length	40 bits
Frame protection	6-bit CRC
Max. Frequency	10 MHz
CPOL	0

Parameter	Description
CPHA	1

5.7.1.2 *SPI frame composition*

The frame format to send read/write commands to L9965T/TS is shown in the table below.

Table 25. Single Read/Write frame format

	39	38	37 36 35 34 33 32	31 30 29 28 27 26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
MOSI	PA = 1	RW	DEV_ID	Address	RSVD	Data write	CRC
MISO	PA = 0	Compressed	DEV_ID	Address feedback	FAULT	Data read	CRC

The fields of the MOSI/MISO frames are described in Table 26:

Table 26. SPI frame fields description

Field	Size [bit]	Description	Value
P.A.	1	Data direction	0 = Answer from device 1 = Command from MCU
R/W	1	Read/Write request	0 = Read 1 = Write
Compressed	1	Compressed data type	0 = normal frame 1 = decompressed data from a compressed burst
DEV_ID	6	Address of the device object of the communication. Also used for broadcast commands.	[0-63]
Address Address feedback	7	Register address for the Read/Write operation. Also used for burst commands.	[0-127]
RSVD	1	Reserved	0
FAULT	1	Self-detected failure	1= failure in diagnostic routines 0= no failures
DATA WRITE	18	Specifies the register content to be written in Write operations. Don't care in Read operations	Read: X Write: [0 to 218-1]
DATA READ	18	Returns the register content in both Read/Write operations	[0 to 218-1]
CRC	6	Checksum	[0-63]

The fault/events bits contributing to the SPI MISO frame FAULT bit and FLT interrupt pin are reported in the below table. Each fault condition is described in detail in the related paragraph.

Table 27. **Status bit outputs to SPI FAULT bit and FLT pin**

Event	Status bit	SPI FAULT	FLT Pin	Mask
FAULT-WAKEUP tone received from VIF	GEN_STATUS2. WAKEUP_FAULT_VIF	X	X	
CYCLIC WAKEUP tone received from VIF, when not in listener mode in CYCLIC_WAKEUP state	GEN_STATUS2. WAKEUP_CYCLIC_VIF	X	X	
CYCLIC_WAKEUP Listener Tone Timeout	GEN_STATUS2. WAKEUP_CYCLIC_TRX_TIMEOUT	X	X	
CYCLIC_WAKEUP diagnosis phase timeout	GEN_CFG5. WAKEUP_CYCLIC_END	X	X	
VB pin undervoltage	GEN_STATUS1.VB_UV	X	X	GEN_CFG3.MSK_VB_UV
V3V3 internal regulator overvoltage	GEN_STATUS1.V3V3_INT_OV	X	X	GEN_CFG3.MSK_V3V3_INT_OV
V5V regulator overvoltage	GEN_STATUS1.V5V_OV	X	X	GEN_CFG3.MSK_V5V_OV
V5V regulator undervoltage	GEN_STATUS1.V5V_UV	X	X	GEN_CFG3.MSK_V5V_UV
V5V regulator overcurrent	GEN_STATUS3.V5V_OC	X	X	GEN_CFG3.MSK_V5V_OC
Thermal shutdown	GEN_STATUS3.TSD	X	X	GEN_CFG3.MSK_TSD
WKP pin overtemperature	GEN_STATUS1.WKP_OT	X	X	GEN_CFG3.MSK_WKP_OT
Ground loss	GEN_STATUS1.GND_LOSS	X	X	GEN_CFG3.MSK_GND_LOSS
NVM trimming data integrity check fail at download	GEN_STATUS3. TRIM_NVM_CRC_FAIL	X	X	GENERAL_REG.NVM_CRC_FAIL_MSK
NVM configuration data integrity check fail at download	GEN_STATUS3. CONF_NVM_CRC_FAIL	X	X	GENERAL_REG.NVM_CRC_FAIL_MSK
NVM trimming data integrity cyclic check fail	GEN_STATUS1. TRIM_CYC_CRC_FAIL	X	X	GENERAL_REG.CYC_CRC_DIS
NVM configuration data integrity cyclic check fail	GEN_STATUS1. CONF_CYC_CRC_FAIL	X	X	GENERAL_REG.CYC_CRC_DIS
Analog BIST fail	GEN_STATUS3.BIST_ANA_FAIL	X	X	GEN_CFG3.MSK_BIST_ANA_FAIL
Oscillator fail	GEN_STATUS1.OSC_FAIL	X	X	GEN_CFG3.MSK_OSC_FAIL
Oscillator monitor fail	GEN_STATUS3. BIST_OSC_FAIL	X	X	GEN_CFG3.MSK_BIST_OSC_FAIL
WKP pin error	GEN_STATUS1.WKP_ERR	X	X	GEN_CFG3.MSK_WKP_ERR
BNE pin error	GEN_STATUS1.BNE_ERR	X	X	GEN_CFG3.MSK_BNE_ERR
VIF frame error	GEN_STATUS1.ISO_ERR	X	X	GEN_CFG2.MSK_ISO_ERR
VIF RX FIFO full	GEN_STATUS1.FIFO_RX_FULL	X	X	GEN_CFG3.MSK_FIFO_RX_FULL
VIF TX FIFO full	GEN_STATUS1.FIFO_TX_FULL	X	X	GEN_CFG3.MSK_FIFO_TX_FULL
FLT pin error	GEN_STATUS1.FLT_ERR	X		GEN_CFG3.MSK_FLT_ERR

5.7.1.3 *CRC*

To guarantee information integrity, each SPI frame embeds a 6-bit CRC code.

Table 28. **SPI Target CRC calculation information**

Parameter	Value
Length	6 bit
Polynomial	x6 + x5 + x2 + x + 1
Seed	0x38

5.7.1.4 *SPI error management*

The SPI communication is covered by several checks, described in Table 29 below. In case the frame received by L9965T/TS on SPI is not correct, it is discarded, the corresponding error bit is asserted in the status register COMM_ERR_SPI and at successive SPI access an SPI ERROR frame is issued with a specific bit set according to the error (see Section 5.8.3.7).

Table 29. **SPI Errors**

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
SPI VIF_ID ERR	Wrong VIF ID in previous received frame	• Frame is discarded • SPI_VIF_ID_ERR = 1 in COMM_ERR_SPI • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI COMM_CRC ERR	Wrong CRC in previous received frame	• Frame is discarded • SPI_COMM_CRC_ERR = 1 in COMM_ERR_SPI • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI WRONG_ADDR	Wrong address in previous received frame	• Frame is discarded • SPI_WRONG_ADDR = 1 in COMM_ERR_SPI • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI SHORT_FRAME	Short frame error (previous frame shorter than 40 bit)	• Frame is discarded • SPI_ SHORT_FRAME = 1 in COMM_ERR_SPI • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No
SPI LONG_FRAME	Long frame error (previous frame longer than 40 bit)	• Frame is discarded • SPI_ LONG_FRAME = 1 in COMM_ERR_SPI • Next SPI MISO frame is the SPI ERROR frame	Clear on read	No

5.7.1.5 *Electrical parameters*

The SPI timings shown in the figure below are reported in Table 30.

Figure 10. **SPI Target timing diagram**

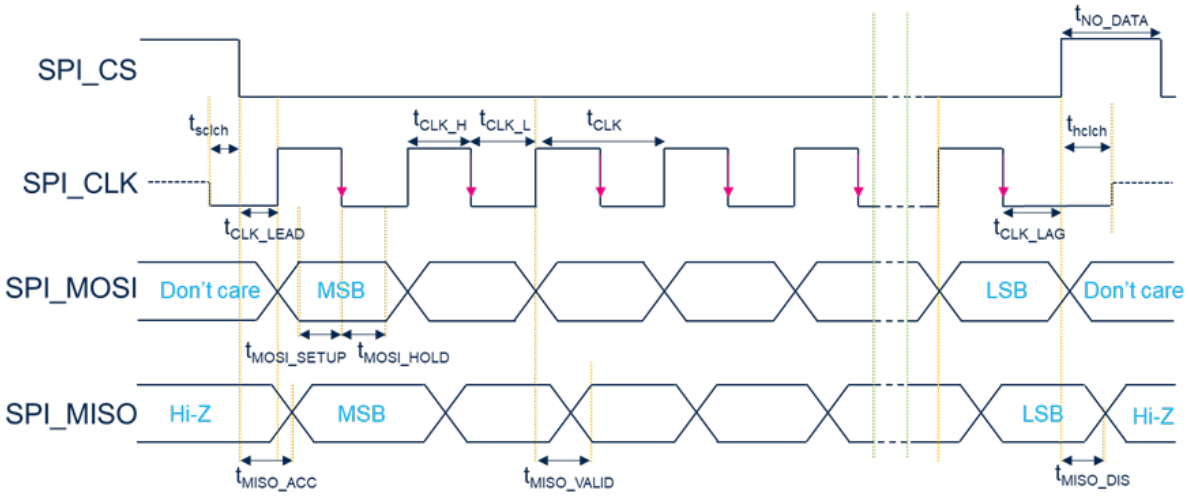


Table 30. **SPI Target electrical parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	PIN
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info			10	MHz	NCS, SDI, SDO, SCLK
T_{CLK_L}	Time interval for CLK = LOW	Application info		50		ns	NCS, SDI, SDO, SCLK
T_{CLK_H}	Time interval for CLK = HIGH	Application info		50		ns	NCS, SDI, SDO, SCLK
T_{MISO_VALID}	Propagation delay (time passed after propagating SCLK edge @ at SDO active)	Guaranteed by design			30	ns	NCS, SDI, SDO, SCLK
T_{CLK_LEAD}	time passed after NCS H/L edge @ first SCLK edge	Application info	110			ns	NCS, SDI, SDO, SCLK
T_{MOSI_SETUP}	SDI input setup time (time passed after SDI data valid @ sampling SCLK edge)	Application info	10			ns	NCS, SDI, SDO, SCLK
T_{MOSI_HOLD}	SDI input hold time (time passed after propagating SCLK edge @ SDI data "not valid anymore")	Application info	10			ns	NCS, SDI, SDO, SCLK
T_{sclch}	Time passed after CLK -> CPOL @ NCS H/L edge	FCLK_SPI = 10 MHz	75			ns	NCS, SDI, SDO, SCLK
T_{CLK_lag}	Time passed after CLK -> CPOL @ NCS L/H edge	FCLK_SPI = 10 MHz	100			ns	NCS, SDI, SDO, SCLK
T_{hclch}	CLK high after NCS high	FCLK_SPI = 10 MHz	100			ns	NCS, SDI, SDO, SCLK
T_{NO_DATA}	NCS min high time	FCLK_SPI = 10 MHz	900			ns	NCS, SDI, SDO, SCLK
t_{MISO_DIS}	NCS L/H to SDO @ high impedance	FCLK_SPI = 10 MHz Cload=60pF			100	ns	NCS, SDI, SDO, SCLK
t_{MISO_ACC}	NCS H/L to SDO active	FCLK_SPI = 10 MHz Cload=60pF			100	ns	NCS, SDI, SDO, SCLK
V_{IN_H}	Logic input high voltage	Tested in production	2			V	SCLK, SDI NCS
V_{IN_HYS}	Input hysteresis	Tested in production	0.1		0.5	V	SCLK, SDI

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	PIN
							NCS
R_{IN_PD}	Input pulldown resistor. Applies to SCK, SDI		0.4	1	1.6	MΩ	SCLK SDI
R_{IN_PU}	Input pullup resistor. Applies to NCS		0.4	1	1.6	MΩ	NCS

5.7.2 Isolated Vertical Interface (VIF)

The IC integrates communication ports to interface up to N_{VIF_STACK} devices in daisy chain by isolated cables twisted pair (VIF).

The VIF supports capacitive to capacitive, transformer to transformer, transformer to capacity and vice-versa communication isolation in single access or dual ring daisy-chain for enhanced safety.

The VIF receiver port is always enabled, regardless of the device operating state, and the sensitivity to received commands depends upon the device state as reported in Table 31 below.

Table 31. VIF receiver sensitivity

FSM State	Received commands	Effect
DEEP SLEEP/CYCLIC COUNT	• FAULT/WAKEUP tone • CYCLIC_WAKEUP tone	FSM transition
CYCLIC_WAKEUP	• FAULT/WAKEUP tone • CYCLIC_WAKEUP tone	FSM transition
NORMAL	VIF frames	Functional operations

For the FAULT/WAKEUP tone, see Section 5.8.3.8 and for the CYCLIC_WAKEUP tone, see Section 5.8.3.7.

The VIF transmitter is enabled according to the GENERAL_REG.ISO_TX_EN configuration bit and to the device state, as listed in the following table:

Table 32. VIF Transmitter (TX) Interface enable conditions

VIF_ID	FSM_STATE	ISO_TX_EN	ISO TX state	Note
0	Any	x	Disabled	Addressing procedure required (see Section 5.8.1)
≠0	DEEPSLEEP CYCLIC_COUNT	x	Disabled	
X	CYCLIC_WAKEUP	x	Enabled	When device is in sender mode to send the CYCLIC_WAKEUP tone
≠0	NORMAL	0	Disabled	
≠0	NORMAL	1	Enabled (default at POR_MAIN)	

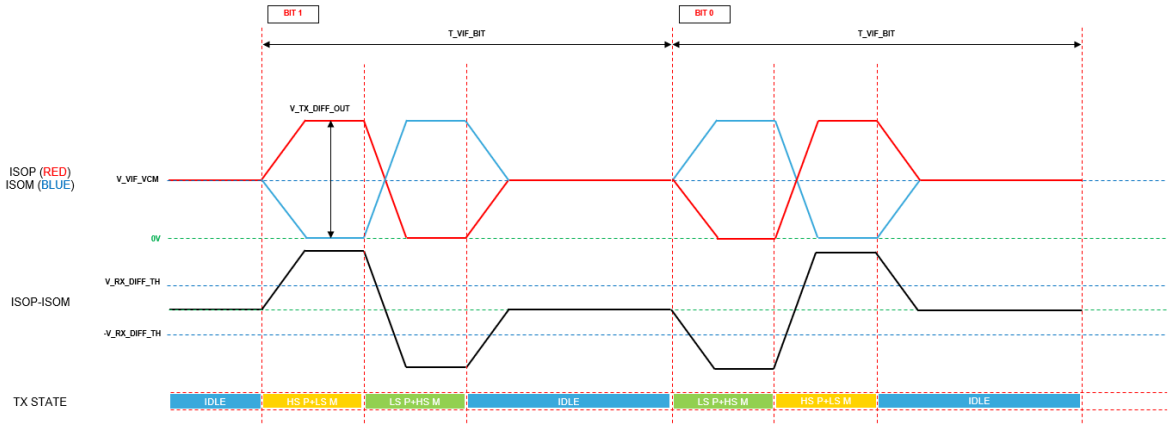
In a VIF port, both positive and negative terminals are biased to a V_{VIF_CM} common mode voltage, and the information is encoded in the differential signal by a proprietary protocol with the following logic, where each bit lasts T_{VIF_BIT}:

- A negative to positive transition indicates a logic ‘0’
- A positive to negative transition indicates a logic ‘1’

A VIF frame is normally composed of 40 bits. If it is a compressed frame (Compressed = 1) it may be longer than 40 bits, in this case the device decompress it and fill the RX FIFO with the corresponding 40-bit decompressed frames.

Signals at the ISO port terminals are normally in the V_{VIF_CM} ± (V5V/2) range, as shown in Figure 11 below.

Figure 11. **VIF waveform**



5.7.2.1 *VIF errors and events management*

The error and status bits related to VIF communication are reported in Table 33 below.
For the communication protocol, see Section 5.8.

Table 33. **VIF diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
VIF CRC Error	VIF communication wrong CRC error (previous frame received on VIF port has wrong CRC)	• Frame is discarded • ISO_COMM_CRC_ERR = 1 in COMM_ERR_ISO • ISO_ERR = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_ISO_ERR = 0 in GEN_CFG2	Clear on read	• ISO_COMM_CRC_ERR status bit non maskable • ISO _ERR status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_ISO_ERR in GEN_CFG2
VIF Short Frame	VIF communication short frame error (frame received on VIF port is shorter than 40 bits)	• Frame is discarded • ISO_SHORT_FRAME = 1 in COMM_ERR_ISO • ISO_ERR = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_ISO_ERR = 0 in GEN_CFG2	Clear on read	• ISO_SHORT_FRAME status bit non maskable • ISO _ERR status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_ISO_ERR in GEN_CFG2
VIF Long Frame	VIF communication long frame error (frame received on VIF port – with exception of compressed frames(1) – is longer than 40 bits)	• Frame is discarded • ISO_LONG_FRAME = 1 in COMM_ERR_ISO • ISO_ERR = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_ISO_ERR = 0 in GEN_CFG2	Clear on read	• ISO_LONG_FRAME status bit non maskable • ISO _ERR status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_ISO_ERR in GEN_CFG2
FIFO TX FULL	Overwriting of last TX frame with a new frame to be sent through VIF	• Ongoing transmission continues • FIFO_TX frame is overwritten • FIFO_TX_FULL = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_FIFO_TX_FULL = 0 in GEN_CFG3	Clear on read	• FIFO_TX_FULL status bit non maskable • FLT pin and the SPI FAULT maskable by bit MSK_FIFO_TX_FULL in GEN_CFG3

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
FIFO RX FULL	Write request of received VIF frame to full FIFO RX	• FIFO_RX_FULL = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_FIFO_RX_FULL = 0 in GEN_CFG3	Clear on read	• FIFO_RX_FULL status bit non maskable • FLT pin and the SPI FAULT maskable by bit MSK_FIFO_RX_F • ULL in GEN_CFG3
FIFO RX EMPTY	Read request to empty FIFO RX	• FIFO_RX_EMPTY = 1 in GEN_STATUS1 • Next SPI MISO frame is RX FIFO EMPTY (see Section 5.8.4)	Clear on read	• FIFO_RX_EMPTY status bit non maskable

1. *For burst read, see Section 5.8.2.2*

5.7.2.2 *Electrical parameters*

Table 34. VIF electrical parameters

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Pin
N_{VIF_STACK}	Number of addressable devices stacked in a single daisy-chain (including L9965T, L9965C)	Application information. There are 64 available addresses, 5 of which are reserved for broadcast commands	1		59	devices	ISOP_0, ISOM_0, ISOP_1, ISOM_1
L_{VIF_WIRE}	Maximum length of twisted pair cables between two VIF nodes, using the recommended AWGVIF_WIRE size and supporting operation in high frequency	Application information			10	m	ISOP_0, ISOM_0, ISOP_1, ISOM_1
V_{VIF_VCM}	ISO port positive/negative terminals common mode voltage	Tested in production	0	V5V/2	V5V	V	ISOP_0, ISOM_0, ISOP_1, ISOM_1
$V_{TX\_DIFF\_OUT}$	TX output differential pulse	Tested in production using recommended R_{TERM}	0		V5V	V	ISOP_0, ISOM_0, ISOP_1, ISOM_1
T_{VIF_START}	Delay between NCS pin rising and start of VIF transmission	Guaranteed by SCAN		1.3		µs	ISOP_0, ISOM_0, ISOP_1, ISOM_1
T_{VIF_BIT}	VIF Bit time	Guaranteed by SCAN	230	250	270	ns	ISOP_0, ISOM_0, ISOP_1, ISOM_1
$T_{VIF\_LATENCY}$	VIF Insertion Delay. Latency introduced by the insertion of one IC in the daisy chain	Guaranteed by SCAN	115	125	135	ns	ISOP_0, ISOM_0, ISOP_1, ISOM_1
VRX_DIFF_TH_POS	RX differential threshold positive	Tested in production	80	200	400	mV	ISOP_0, ISOM_0, ISOP_1, ISOM_1
VRX_DIFF_TH_NEG	RX differential threshold negative	Tested in production	-400	-200	-80	mV	ISOP_0, ISOM_0, ISOP_1, ISOM_1

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Pin
WAIT_RX_BEGIN	Maximum waiting time for an answer from VIF	Tested in SCAN	53		67	µs	
WAIT_RX_END	Maximum waiting time between two successive frames received on VIF	Tested in SCAN	6.6		8.4	µs	

5.8 Communication protocol

5.8.1 Addressing procedure

At first power-up the L9965T/TS holds an address (VIF_ID_CFG.VIF_ID) equal to 0x0 and its VIF transmitter is disabled. To communicate it is necessary to implement the addressing procedure below.

Procedure 2: L9965T/TS addressing

1. Send a SPI frame with DEV_ID = 0 to disable the configuration integrity check by writing GENERAL_REG.CYC_CRC_DIS = 1.
   The command only reaches the first device in the chain not initialized and won't be propagated until this device is addressed and has the VIF transmitter enabled.
2. Send SPI frames with DEV_ID = 0 to remove the configuration lock:
   a. Write 0x55 in the SPECIAL_REG.SPECIAL_KEY register to enter in partial unlock
   b. Write 0x33 in the SPECIAL_REG.SPECIAL_KEY register to confirm the unlock
3. Send a SPI frame with DEV_ID = 0 to program the desired VIF_ID value in the VIF_ID_CFG.VIF_ID register
4. Send a SPI frame with DEV_ID = VIF_ID_CFG.VIF_ID to enable VIF transmitter setting GENERAL_REG.ISOH_TX_EN = 1
   The steps above can be repeated for all devices in the chain that in this way are initialized one by one.
5. To enable selective broadcast (see Section 5.8.2.3), send a SPI frames with DEV_ID = VIF_ID_CFG.VIF_ID to write the GEN_CFG1.BROADCAST_SEL<x> registers with values matching those programmed in the IC in the chain that will be addressed by broadcast communication.
6. Send SPI commands with DEV_ID = 0 to apply the configuration lock to all devices in the chain:
   a. Write 0xAA in the SPECIAL_REG.SPECIAL_KEY to apply the lock.
7. Send a SPI command with DEV_ID = 0 to enable the configuration integrity check by writing GENERAL_REG.CYC_CRC_DIS = 0.

The device response to commands from the BMS MCU is summarized in the table below and explained in details in following paragraphs.

Table 35. Device response according to VIF_ID

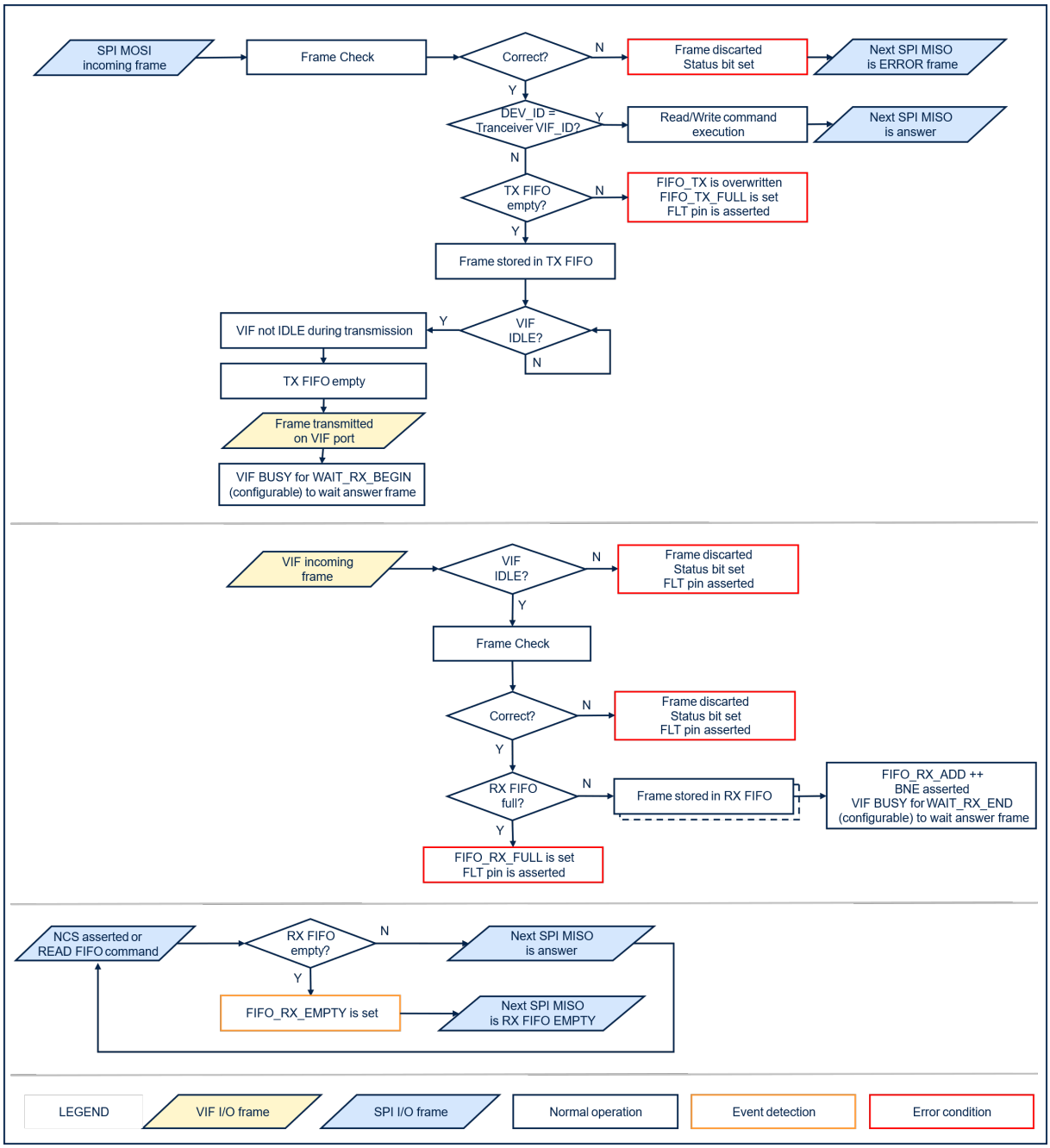
Device VIF_ID	SPI MOSI DEV_ID	READ CMD Behavior	WRITE CMD Behavior
0	0	Discard cmd and load MISO with SPI ERROR FRAME with WRONG_VIF_ID=1 Set COMM_ERR_SPI.SPI_VIF_ID_ERR	Perform WRITE operation and load MISO with updated reg content
0	!=0	Discard cmd and load MISO with SPI ERROR FRAME with WRONG_VIF_ID=1 Set COMM_ERR_SPI.SPI_VIF_ID_ERR	Discard cmd and load MISO with SPI ERROR FRAME with WRONG_VIF_ID=1
!=0	0 (Broadcast)	Discard cmd and load MISO with SPI ERROR FRAME with WRONG_VIF_ID=1 Set COMM_ERR_SPI.SPI_VIF_ID_ERR	Perform WRITE operation and load MISO with updated reg content. Propagate cmd on VIF
!=0	!=0 (matching VIF_ID)	Perform READ operation and load MISO with reg content. No propagation on VIF	Perform WRITE operation and load MISO with reg content. No propagation on VIF
!=0	!=0 (non matching)	Propagate cmd on VIF transmitter and load MISO with FIFO_RX content	Propagate cmd on VIF and load MISO with FIFO RX content

Device VIF_ID	SPI MOSI DEV_ID	READ CMD Behavior	WRITE CMD Behavior
!=0	!=0 (matching BROADCAST_SEL_<x>)	Discard cmd and load MISO with SPI ERROR FRAME with WRONG_VIF_ID=1 Set COMM_ERR_SPI.SPI_VIF_ID_ERR	Perform WRITE operation and load MISO with updated reg content. Propagate cmd on VIF

5.8.2 Communication with L9965T/TS and L9965x

The BMS MCU can access the L9965T/TS transceiver or any BMS device in the chain with proper SPI frames. The flow chart of the process is shown in Figure 12 and explained in detail in the paragraphs below.

Figure 12. Single read/write frame protocol



5.8.2.1 *Single read/write*

When in NORMAL mode the device is available for SPI and VIF communication.

If the DEV_ID field in the SPI frame corresponds to the transceiver VIF_ID_CFG.VIF_ID register value, the frame is checked (for CRC, length, register address) and, if correct, the internal register of L9965T, pointed by the Address field, is accessed with out-of-frame approach.

If the DEV_ID field in the SPI frame does not correspond to the transceiver VIF_ID programmed value, the SPI frame is checked (for CRC, length) and if correct, the frame is put in the TX_FIFO (depth 1).

The frame in TX FIFO is sent when the VIF interface is in IDLE state (readable in GEN_STATUS3.ISO_IDLE =1), which means it is not already busy in a previous transmission task. When the transmission starts the TX FIFO is cleared.

During transmission the VIF peripheral remains busy for a time that depends on the GEN_CFG5. ISO_RX_TIMEOUT_ENB configuration bit value; the bit default value is zero and, in this case, the VIF returns IDLE when transmission is completed; if the bit is set, the VIF remains busy to wait for an answer for an additional time equal to WAIT_RX_BEGIN; when this timeout expires the VIF returns in IDLE state and is ready for a new transmission.

In case of concurrent access from both SPI and VIF, the arbitration mechanism waits until VIF RX port is in IDLE mode, then present the data to the VIF TX port to be transmitted.

If a new SPI frame is received to be transmitted on the VIF when TX FIFO is not empty, ongoing transmission continues without interruption, but the previous frame in the TX FIFO is overwritten and the GEN_STATUS1.FIFO_TX_FULL bit is set.

When a frame is received from the VIF the CRC and length are checked and, if correct, the frame is stored in the first empty location of the VIF RX FIFO (depth 32) and the BNE pin is asserted. The VIF remains BUSY for a time equal to WAIT_RX_END, then returns to IDLE state in case other frames must be received (i.e. Burst frame). This timeout is disabled by default and can be enabled by bit GEN_CFG4. ISO_RX_TIMEOUT_ENB.

A FIFO_RX counter register (GEN_STATUS3.FIFO_RX_ADD) is incremented for each frame received and decremented for each frame read. An SPI flush command is also available (writing 0xDC in CMD_REG) to clear the entire RX FIFO.

When the microprocessor asserts the SPI NCS, L9965T/TS starts sending out on SDO the VIF RX FIFO content with a FIFO approach. Each bit is sent synchronously with SCK provided by the microprocessor itself. The timings of SDO with respect to SCK and NCS must follow the electrical characteristics listed in Table 30.

The first answer issued by the IC when, after a wakeup condition, it moves to NORMAL from DEEP SLEEP, CYCLIC COUNT or CYCLIC_WAKEUP state is the default frame 0x0000000010 (see Section 5.8.3.4).

To enable interrupt-based communication with the BMS MCU, the BNE pin remains set until the VIF RX queue is not empty (it contains at least an unread frame).

5.8.2.2 *Burst read*

To enable quick data retrieval from a specific chained L9965x AFEs, the IC implements a flexible burst read mode available only on the VIF port. Burst packets can be requested performing a read access to L9965x specific registers.

Two types of burst read can be requested:

- Standard burst
  - L9965T/TS receives on the VIF a flexible number of registers, depending on L9965A setup (refer to L9965A datasheet). This strategy can be used to quickly retrieve diagnostic and configuration data.
- Compressed burst
  - L9965T/TS receives on the VIF a compressed packet according to L9965A setup (refer to L9965A datasheet). This strategy is recommended to achieve high data rate with negligible impact on the power consumption. It enables very fast conversion and readout threads, while keeping low power consumption due to the reduced VIF transmitter duty-cycle.

Broadcast burst reads are not supported.

L9965T/TS features the decompressor for compressed burst frame, thus freeing MCU from implementing complex routines to recover original cell/temperature/pack/busbar data.

As for all the received VIF frames, the packet CRC is checked and if correct, the information is formatted as in Table 25 and stored in the VIF RX FIFO. The BNE pin is asserted.

When a compressed burst from L9965A is decompressed in the L9965T/TS RX FIFO, the FIFO contains variable number of frames depending on the specific configuration of the addressed L9965A.

The SPI frame sent to MCU (see Table 25) contains:

- Bit 38: Compressed = 1
- The DEV_ID of the particular L9965A addressed in the burst request
- The Address feedback field:
  - 0x38 to 0x49 (VCELLx_MEAS) depending on the enabled cells in L9965A. If a particular cell is not enabled or it is configured as busbar (according to VCELL<x>_BB) the corresponding VCELLx_MEAS register is not present in the FIFO
  - 0x4A (BB_MEAS) if the Bus Bar measurement is enabled. If not enabled, the BB_MEAS register is not present in the FIFO
  - 0x4B (VBS_MEAS) if the VBS measurement is enabled. If not enabled, the VBS_MEAS register is not present in the FIFO
  - 0x4D to 0x56 (NTC_GPIO_MEAS_x) depending on the GPIO setting in L9965A. If a particular GPIO is not enabled or it is masked the corresponding register is not present in the FIFO
- The FAULT bit is set according to the GSW of the addressed L9965A
- The DATA READ is composed according to the register structure (for more information, see the L9965A datasheet)
- The CRC of the frame.

In case of standard burst, single packet sent with an interframe time is received on VIF RX and is stored in FIFO RX with the same approach of a single read.

5.8.2.3 *Broadcast write*

A broadcast write command allows simultaneous writing of the same data on all devices in a chain, or on a subset.

The MCU can exploit different broadcast commands by programming the DEV_ID field of the SPI MOSI frame (see Table 25). There are two types of broadcast commands, configured as described in table below:

Table 36. Broadcast commands

Type	DEV_ID	Purpose	Notes
Global broadcast	0x0	• Chain device addressing, for all devices in the stack • Writing common configurations to all devices in the stack • Executing common tasks for all devices in the stack	• Transceivers can only be addressed via SPI target
Selective broadcast	0x3C + BROADCAST_SEL_<x>	• Writing common configurations to a specific subset of devices in the stack • Executing common tasks to a specific subset of devices in the stack	

BROADCAST_SEL_<x> is a 2-bit field allowing sending commands to a subset of chained devices. The command is accepted if the BROADCAST_SEL_<x> is equal to the BROADCAST_SEL_1 or BROADCAST_SEL_2 in GEN_CFG1 register.

If the DEV_ID field of the frame is equal to a global or selective broadcast filter, the IC sends it to the VIF if the SPI frame is correct (in terms of length, CRC).

The devices addressed are those programmed with matching BROADCAST_SEL_<x> value.

In both cases the next MISO frame is an echo of the SPI command (DEV_ID and Address).

The ICs on the VIF chain don't generate answer upon receipt of broadcast commands.

The registers that can be addressed by broadcast write are reported in the registers map.

5.8.2.4 *Read VIF received frames*

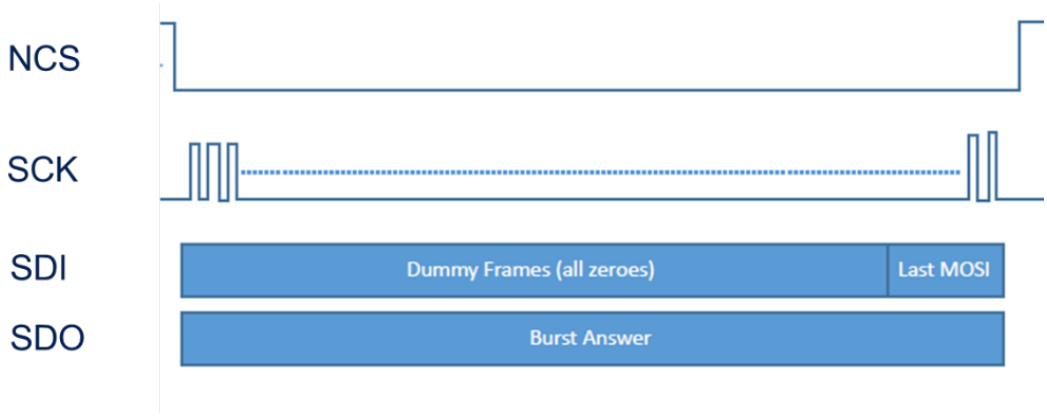
All the frames received from VIF, already decompressed if necessary, are stored in the VIF RX FIFO.

The MCU accesses the frames in the RX FIFO:

1. With a single read/write frame (see Section 5.8.2.1).

2. Setting the CMD_TRX field in CMD_REG equal to 0xB5. This is a dedicated read command that must be sent for all the FIFO locations to read. The command doesn't transfer any data on the VIF interface.
3. With an SPI burst access approach to reduce the time needed to readout long data series from a single unit. This access is achieved by MCU asserting the NCS and sending N*40 clock cycles on SCK, where N is the number of frames to be read from FIFO. If a wrong number of clock cycle is sent by MCU, the last frame is not reliable and the pointed FIFO location is lost. At the next access to the SPI slave, an SPI ERROR frame is sent, and an error bit (SPI_SHORT_FRAME or SPI_LONG_FRAME) is asserted in the status register COMM_ERR_SPI.

Figure 13. SPI burst read



5.8.2.5 *RX VIF FIFO handling*

The device includes two types of memory: the internal register memory, which configures the device functionalities, and the VIF RX FIFO, which stores all frames received from the Vertical Interface. Access to these memories is managed using a hardware pointer. This pointer changes based on the SPI request received and points to the register whose value will be shifted out on the next MISO.

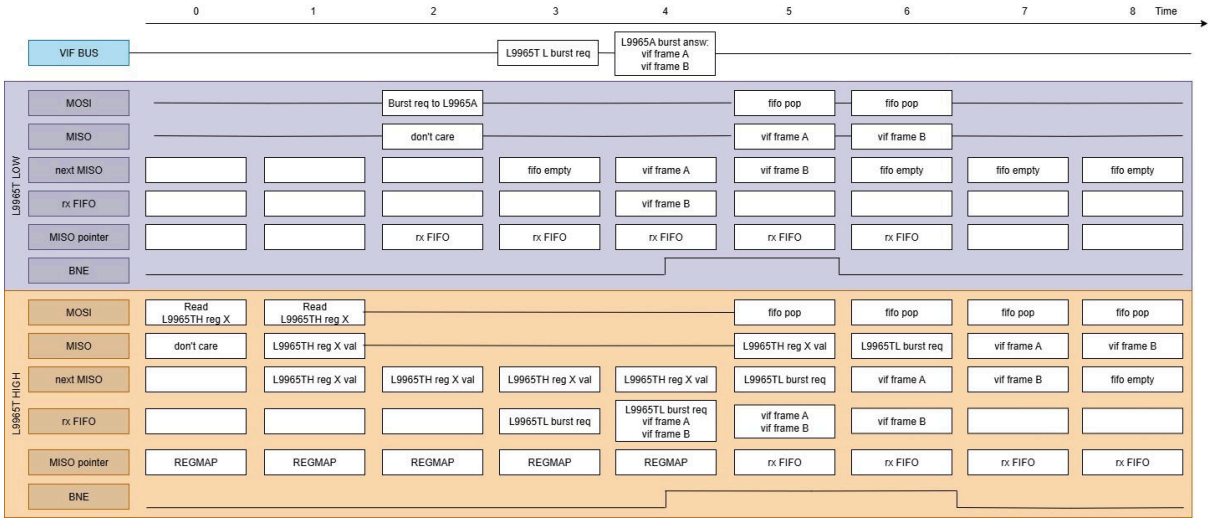
- When the MCU sends an SPI read/write command addressing the IC's own registers, the pointer switches to the internal register map at the end of the SPI frame.
- When the MCU sends an SPI read/write command to pop a VIF frame from the FIFO, the pointer switches to the FIFO at the end of the SPI frame.
- When the MCU sends an SPI read/write command addressing an external device on the VIF bus, the pointer switches to the FIFO at the end of the SPI frame.

The pointer's behavior is transparent when the MCU retrieves VIF data from the same transceiver used to send the VIF request. However, it becomes visible when the MCU sends a VIF request from one transceiver and retrieves the response from the opposite transceiver.

Referring to Figure 14, in a dual-ring topology with the bidirectional answer enabled for all devices, the MCU reads an internal register of the high transceiver during time interval [t0-t1]. Then it sends a standard burst command to a device along the chain from the low transceiver during time interval [t2-t3-t4].

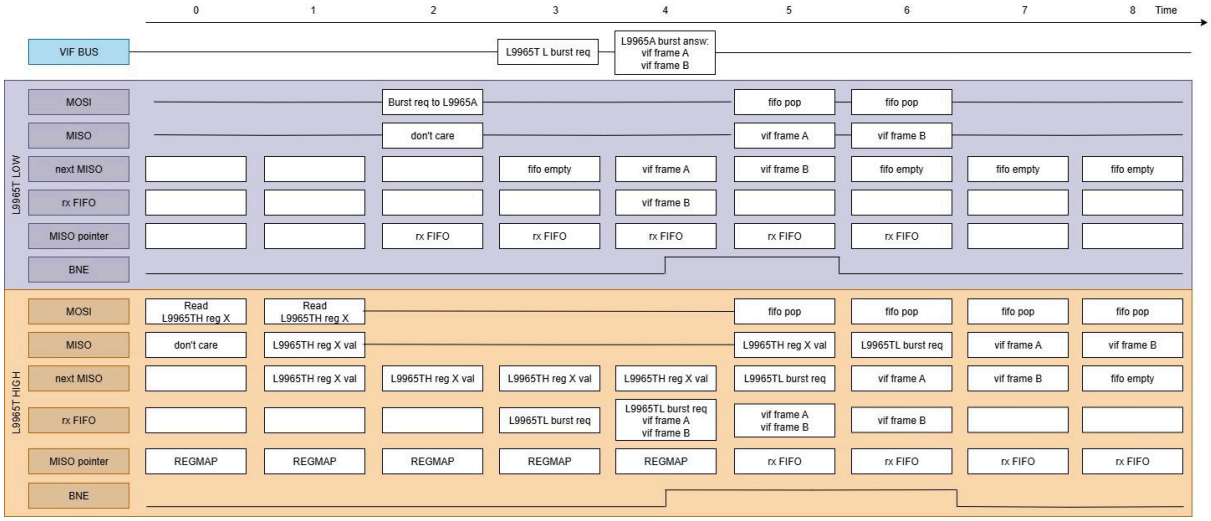
To read the response frames from the same transceiver side, the MCU must send N FIFO POP commands during time interval [t5-t6-…], where N is the number of burst response frames. If the MCU needs to read the responses using the high transceiver, it must send N+2 FIFO POP commands. The first retrieves the internal register data (requested initially) and updates the pointer to the first FIFO location [t5]. The second retrieves the burst request (sent by the low transceiver) [t6], and the remaining N FIFO POP commands retrieve the burst answers during time interval [t7-t8-…].

Figure 14. Accessing the FIFO from the same side of the ring



The long frame access allows the MCU to send a single long SPI frame of 40*N bits, where N is the number of burst responses. In the scenarios described before, if the MCU needs to retrieve the data from the high transceiver using the long SPI frame, it must send at least one FIFO POP command to update the MISO pointer from local memory to the FIFO during time interval [t5]. Then, it can generate the long frame of (N+1)*40 bits. The long frame retrieves the burst request (sent by the low transceiver) during time interval [t6] and the N burst responses during time interval [t7-t8-…].

Figure 15. Accessing the FIFO from the opposite side of the ring



In a typical application scenario, to perform a burst read on a target device on the VIF bus, the following procedures must be performed:

Procedure 1: Burst request and response from the same transceiver

1. Send an SPI burst request to the target device along the chain through the transceiver (see Section 5.8.2.2).
2. Wait to receive the N response frames to the burst.
3. Send N SPI commands to pop responses from the FIFO.

Procedure 2: Burst request from transceiver A and response from transceiver B, when the pointer of transceiver B already points to the RX FIFO

1. Send an SPI burst request to the target device along the chain through one of the two transceivers in the chain (see Section 5.8.2.2).
2. Wait to receive the N response frames to the burst.
3. From transceiver B, send one frame to pop from the FIFO the burst request sent by transceiver A.
4. From transceiver B, send N frames to pop from the FIFO the related N responses of burst.

Procedure 3: Burst request from transceiver A and response from transceiver B, when the pointer of transceiver B points to its internal register

1. Send an SPI burst request to the target device along the chain through one of the two transceivers in the chain (see Section 5.8.2.2).
2. Wait to receive the N response frames to the burst.
3. From transceiver B, send a FIFO pop frame to point to the FIFO memory (the MISO will contain the data of the internal register read before).
4. From transceiver B, send one SPI frame to pop from the FIFO the burst request sent by transceiver.
5. From transceiver B, send N SPI frames to pop from the FIFO the related N responses of burst.

5.8.2.6 *Chained devices wakeup requested by MCU*

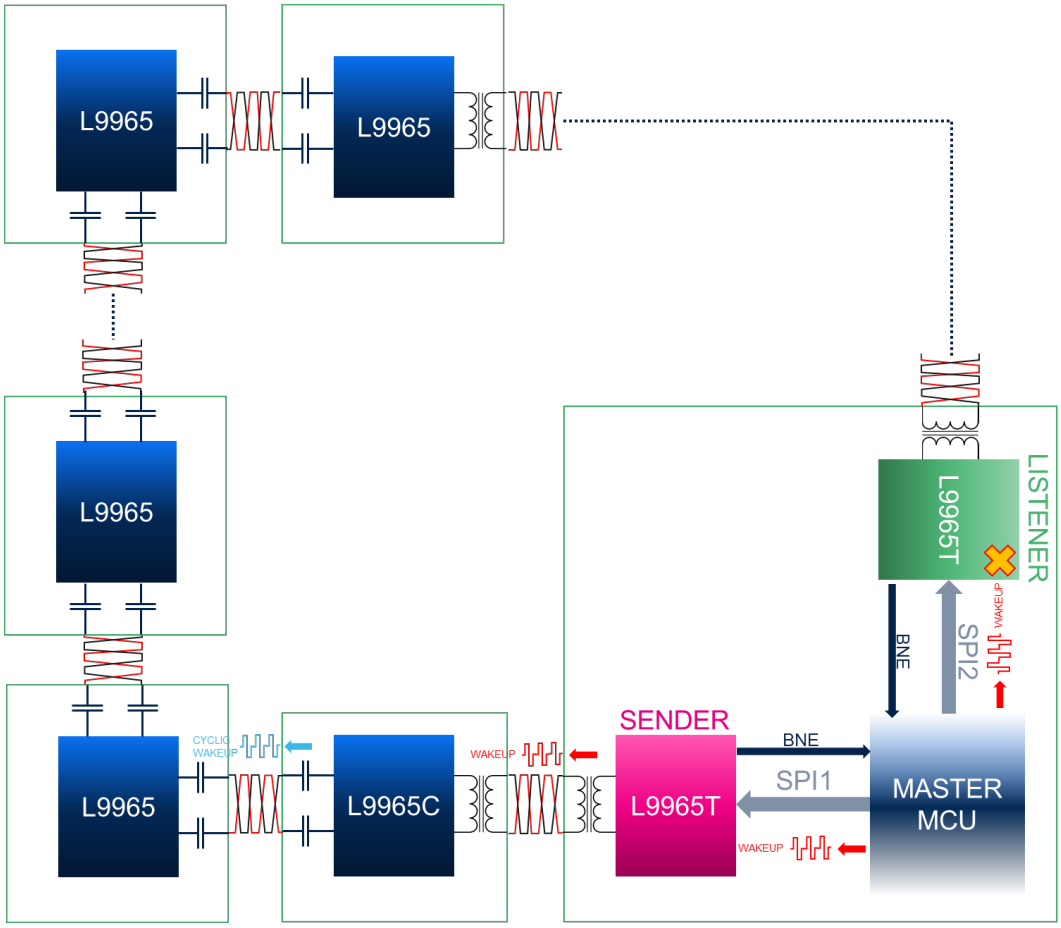
The wakeup of the devices on the VIF bus requested by MCU is an asynchronous event with respect to the CYCLIC_WAKEUP thread managed in background by the L9965T/TS.

Figure 16 shows a typical application scenario where the MCU wakes up the daisy-chain that was previously operating in CYCLIC_WAKEUP mode.

To wake up the daisy-chain:

1. The MCU moves both L9965T channels to NORMAL state
2. The MCU waits for the L9965T wakeup period (T_{WAKEUP})
3. The MCU checks the internal status bit of both L9956T channels (WAKEUP_CYCLIC_TRX_SENDER, WAKEUP_CYCLIC_TRX_LISTENER in register GEN_STATUS2) to determine which one is operating in SENDER mode, and sends it a SPI FAULT/WAKEUP command (see par 5.8.3.1) to be propagated on the VIF. This guarantees that CYCLIC_WAKEUP and FAULT/WAKEUP tones travel in the same direction to avoid conflicts.
4. The listener channel of the transceiver, receiving the FAULT/WAKEUP tone from the VIF, assert the FLT pin.
5. Waking up the whole daisy chain will take approximately N_{VIF_STACK}*$T_{VIF\_WAKEUP\_TIME}$, and is confirmed by the FLT interrupt generated by the listener L9965T channel, once it receives the FAULT/WAKEUP tone
   a. The MCU is supposed to check the L9965T status register to verify that the FLT/WAKEUP source flag is asserted. As shown in Figure 12, it is possible that a CYCLIC_WAKEUP tone reaches the LISTENER transceiver before the FAULT/WAKEUP tone arrives. In such case, the MCU shall anyway wait for the FAULT/WAKEUP tone to consider the daisy-chain fully woken up.

Figure 16. **Wakeup by MCU**



5.8.3 Special Frames

This section lists the special frames associated to specific events.

5.8.3.1 SPI FAULT/WAKEUP command

This command can be sent by MCU SPI writing the data 0xAE in CMD_REG to request L9965T/TS the transmission of FAULT/WAKEUP tone to VIF chain.

Table 37. **IC reaction to FAULT/WAKEUP frame**

IC STATE	IC reaction upon frame receipt
NORMAL	• FAULT/WAKEUP tone transmitted on the VIF to wake up all the devices on the chain
CYCLIC_WAKEUP CYCLIC_COUNT	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • The sender/listener states of the L9965T is latched in the WAKEUP_CYCLIC_TRX_SENDER • Or WAKEUP_CYCLIC_TRX_LISTENER bits in register GEN_STATUS2 • GEN_STATUS2.WAKEUP_FAULT_SPI = 1 • The frame is not decoded
DEEPSLEEP	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • GEN_STATUS2.WAKEUP_FAULT_SPI = 1 • The frame is not decoded

5.8.3.2 SPI WAKEUP command

Whatever frame sent by MCU SPI on both daisy-chain ends wakes up the L9965T/TS from a low power state (see Section 5.1.1.1.2).

Note: After a wakeup frame, an interframe time of at least 20 µs should be considered before sending any other frames.

Table 38. IC reaction to WAKEUP frame

IC STATE	IC reaction upon frame receipt
NORMAL	• L9965T/TS answers to SPI frame as described in Section 5.8.2.1, Section 5.8.2.2, or Section 5.8.2.3
CYCLIC_WAKEUP CYCLIC_COUNT	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • The sender/listener states of the L9965T is latched in the WAKEUP_CYCLIC_TRX_SENDER • Or WAKEUP_CYCLIC_TRX_LISTENER bits in register GEN_STATUS2 • GEN_STATUS2.WAKEUP_FAULT_SPI = 1 • The frame is not decoded
DEEPSLEEP	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • GEN_STATUS2.WAKEUP_FAULT_SPI = 1 • The frame is not decoded

5.8.3.3 *SPI GO2SLEEP command*

This command can be sent by MCU SPI writing the data 0xCC in SPECIAL_REG to put the L9965T/TS in SLEEP state. If the address of the frame is for broadcast write, the device sends a proper tone on daisy-chain to put the whole chain in SLEEP state and then it moves to SLEEP state.

Note: After GOTOSLEEP frame an interframe time of at least 20 µs should be considered before sending any other frame.

Table 39. IC reaction to GO2SLEEP Frame

IC STATE	IC reaction upon frame receipt
NORMAL	• If sent only to Transceiver DEV_ID, L9965T will move to DEEP SLEEP state if the CYCLIC_WAKEUP is not enabled. In case the CYCLIC_WAKEUP is enabled will move to CYCLIC COUNT state. • If sent as broadcast frame, the L9965T will propagate the GO2SLEEP tone on the VIF and then moves to SLEEP state
CYCLIC_WAKEUP CYCLIC_COUNT	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$. • The sender/listener states of the L9965T is latched in the WAKEUP_CYCLIC_TRX_SENDER • Or WAKEUP_CYCLIC_TRX_LISTENER bits in register GEN_STATUS2 • GEN_STATUS2. WAKEUP_FAULT_SPI = 1 • The frame is not decoded
DEEPSLEEP	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$. • GEN_STATUS2. WAKEUP_FAULT_SPI = 1 • The frame is not decoded

5.8.3.4 *SPI Default frame*

Since the protocol is out of frame, the first answer issued by the IC when, after a wakeup condition, it moves to NORMAL from DEEP SLEEP, CYCLIC COUNT or CYCLIC_WAKEUP state is the frame 0x0000000010.

Table 40. SPI Default frame

	39	38	37 36 35 34 33 32	31 30 29 28 27 26 25	24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6	5 4 3 2 1 0
MISO	PA = 0	Compressed = 0	DEV_ID 0x00	Address feedback 0x00	FAULT	DATA read 0x00	CRC 0x10

5.8.3.5 *SPI ERROR frame*

It is the IC answer when a wrong MOSI frame has been received.

Table 41. SPI Error frame

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	PA = 0	Compressed = 0	DEV_ID 0x00						Address feedback 0x7F							FAULT	0x00													WRONG VIF ID	WRONG ADDRESS LONG		SHORT	CRC ERR	CRC						

5.8.3.6 *RX FIFO EMPTY frame*

It is the IC answer when the MCU request a read from the RX FIFO and it is empty.

Table 42. RX FIFO empty special frame

	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	PA = 0	Compressed = 0	DEV_ID Transceiver						Address feedback 0x1C							FAULT	Data read 0xEEEE																				CRC					

5.8.3.7 *VIF SHORT TONE – CYCLIC WAKEUP TONE*

It is a 0x0 frame that represents a CYCLIC_WAKEUP tone. It is sent autonomously by L9965T/TS transceiver when in CYCLIC_WAKEUP state. It is characterized by a specific number of bit and frequency.

Table 43. IC reaction to VIF Short tone

IC STATE	IC reaction upon frame receipt
NORMAL	• FLT pin is asserted • GEN_STATUS2. WAKEUP_CYCLIC_VIF = 1
CYCLIC_WAKEUP	• Tone is discarded
CYCLIC_COUNT	• If L9965T/TS is in sender mode, tone is discarded. • If L9965T/TS is in listener mode and the cyclic wake up timeout is not expired, the status becomes sender and the cyclic wake up timer is restarted.
DEEPSLEEP	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • FLT pin is asserted • GEN_STATUS2. WAKEUP_CYCLIC_VIF = 1

5.8.3.8 *VIF LONG TONE – FAULT/WAKEUP tone*

It is a 0x0 VIF frame that represents a FAULT/WAKEUP tone from/to the chain. It is characterized by a specific number of bit and frequency.

Table 44. IC reaction to VIF LONG tone

IC STATE	IC reaction upon frame receipt
NORMAL	• FLT pin is asserted • GEN_STATUS2.WAKEUP_FAULT_VIF = 1
CYCLIC_WAKEUP CYCLIC_COUNT	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • WKUP and FLT pins are asserted • The sender/listener states of the L9965T is latched in the WAKEUP_CYCLIC_TRX_SENDER • Or WAKEUP_CYCLIC_TRX_LISTENER bits in register GEN_STATUS2

IC STATE	IC reaction upon frame receipt
	• GEN_STATUS2.WAKEUP_FAULT_VIF = 1
DEEPSLEEP	• Device moves to NORMAL within $T_{VIF\_WAKEUP\_TIME}$ • FLT pin is asserted • GEN_STATUS2.WAKEUP_FAULT_VIF = 1

5.8.4 Device identification (DEVICE_NAME)

The Isolated Vertical Interface (VIF) allows populating the bus with different devices of the L9965x family. To enable the MCU quickly recognizing the device type and launching the proper initialization, configuration and diagnostic procedures, the CHIP_ID.NAME_ID register holds a unique code identifying the product type. Specifically, NAME_ID = 0x17 identifies the L9965T.

In the same register are also available the following fields: CHIP_ID.SILICON_ID and CHIP_ID.METAL_ID identifying the version of the silicon.

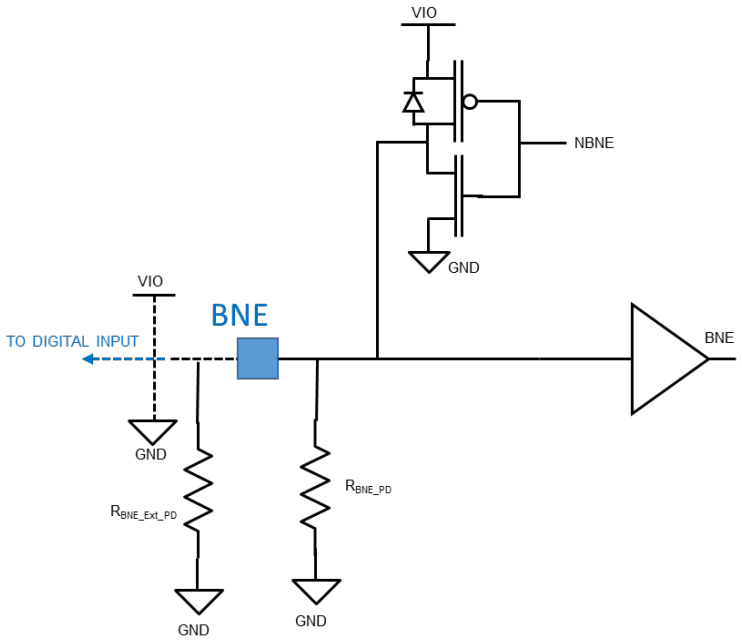
5.9 Output pins

5.9.1 BNE

BNE is a push-pull output pin, it's functional in NORMAL state and Hi-Z in all other states. in NORMAL state this pin output the information on Buffer Not Empty to implement interrupt-based communication with the MCU. When high, it means that the RX FIFO stores at least one frame. The default value is LOW.

BNE value can be read in the bit GEN_STATUS3.BNE.

Figure 17. BNE pin structure



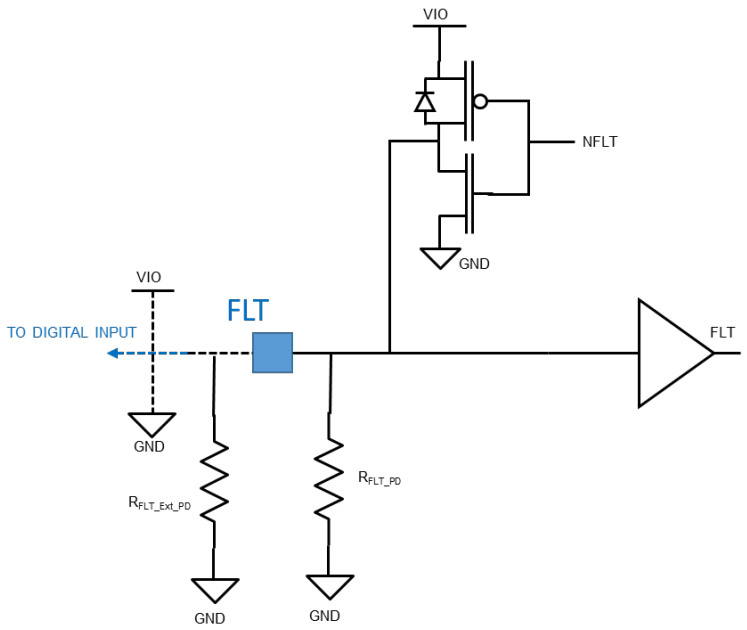
5.9.2 FLT

FLT is a push-pull output pin, it's functional in NORMAL state and Hi-Z in all other states.

Its purpose is to implement interrupt-based communication with the MCU. The default value is LOW.

When FLT pin and SPI FAULT are HIGH, it means that a fault tone has been received on VIF or an internal L9965T fault, according to mask register GEN_CFG3 configuration, has been detected. The default value is LOW.

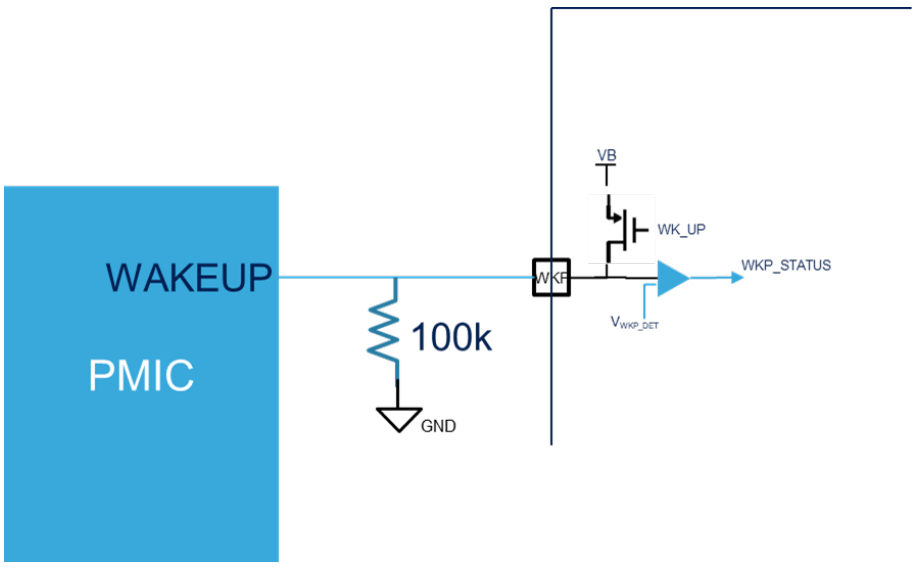
Figure 18. **FLT pin structure**



5.9.3 WKP

The WKP pin is a high voltage output pin that provides a voltage VB - V_{WKP_DROP} to enable external regulators (SBC, PMIC) used to power the microprocessor and VIO pin as shown in figure below.

Figure 19. **WKP pin application circuit**



When WKP PMOS pullup is not activated, WKP pin is in high impedance, and the external circuitry defines the pin voltage (in the typ. application circuit, 100 kΩ resistor to GND is used).

WKP PMOS pullup is triggered:

- When a FAULT/WAKEUP tone is received on VIF in DEEP_SLEEP, CYCLIC_WAKEUP and CYCLIC_COUNT. In this case the device moves to NORMAL state and WKP pin is asserted
- In NORMAL mode, WKP can be asserted by setting bit WKP_SET =1 (in GEN_CFG4 register).

WKP function can be disabled configuring WKP_DIS=1 (in GEN_CFG4 register); the default value is WKP_DIS=0. In NORMAL mode, the WKP pin operates accordingly to the following table:

Table 45. **WKP pin truth table**

WKP_DIS	WKP_SET	WKP pin status
0	X	1
1	0	0
1	1	1

WKP pin should be used to drive the wake-up terminal of the system's power management device. It should not be used as a switch for power management supply itself. This terminal is not reverse battery protected and thus should not be connected outside of the system module.

5.9.4 Diagnostic functions

In NORMAL mode a short to GND/VIO detection is implemented to protect the pins output buffer through a coherency check between the driving signal and the pin value.

In case of short to GND, the WKP pin is protected with thermal shutdown, see Section 5.4 for further details.

Table 46. **Interrupt pins diagnostic functions**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to release	Maskable
BNE short to GND or VIO	BNE pin ≠ GEN_STATUS3.BNE in NORMAL	• BNE_ERR = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_BNE_ERR=0 in GEN_CFG3 • The output buffer is put in HiZ	Clear on read	• The driver is reengaged	• BNE_ERR = 1 in status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_BNE_ERR in GEN_CFG3
FLT short to GND or VIO	FLT pin ≠ SPI MISO frame bit 24	• FLT_ERR = 1 in GEN_STATUS1 • The SPI FAULT is asserted in NORMAL if MSK_FLT_ERR=0 in GEN_CFG3 • The output buffer is put in HiZ	Clear on read	• The driver is reengaged	• FLT_ERR = 1 in status bit non maskable • SPI FAULT maskable by bit MSK_FLT_ERR in GEN_CFG3
WKP short to GND or VIO	WKP pin ≠ GEN_STATUS3. WKP_STATUS in NORMAL	• WKP_ERR = 1 in GEN_STATUS1 • The FLT pin and the SPI FAULT is asserted in NORMAL if MSK_WKP_ERR =0 in GEN_CFG3 • The output buffer is put in HiZ	Clear on read	• The driver is reengaged	• WKP_ERR = 1 in status bit non maskable • FLT pin and SPI FAULT maskable by bit MSK_WKP_ERR in GEN_CFG3

5.9.5 Electrical parameters

Table 47. **Output buffer electrical characteristics**

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	PIN
V_{OUT_L}	Low output level	I=2mA			0.4	V	BNE FLT
V_{OUT_H}	High output level	I=-2mA	VIO-0.4			V	BNE FLT
T_{OUT_trans}	Digital output Rise and Fall time.	Cload=100pF 20-80% on rising edge, OUT 80-20% on falling edge	5		400	ns	BNE FLT

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	PIN
R_{BNE_PD}	BNE weak pulldown resistor to GND		0.4	1	1.6	MΩ	BNE
R_{FLT_PD}	FLT weak pulldown resistor to GND		0.4	1	1.6	MΩ	FLT
I_{WKP}	WKP output current			2	4	mA	WKP
V_{WKP_DROP}	Voltage drop from VB to WKP	I_{WKP} = -0.5mA		0.5	1	V	WKP
V_{WKP_DET}	Threshold to set WKP_STATUS to '1'	WKP_SET =1		1.5		V	WKP

5.10 Configuration lock (UNLOCK_KEY)

To prevent inadvertent modification of Safety Relevant Registers (SRR) and Safety Latent Registers (SLR) (indicated in the register map) such register map sectors are protected by a lock field.

By default, SRR/SLR registers are locked. To configure the device, the following procedure shall be implemented:

Procedure 3: Configuration Lock/Unlock

1. Write 0x55 in the SPECIAL_REG.SPECIAL_KEY register to enter in partial unlock
2. Write 0x33 in the SPECIAL_REG.SPECIAL_KEY register to confirm the unlock
3. Any configuration register must be written within $T_{CFG\_TIMEOUT}$
   a. If the TCFG_TIMEOUT expires, the lock is automatically re-applied
4. Write 0xAA in the SPECIAL_REG.SPECIAL_KEY to re-apply the lock.

Trying to write a protected register (SRR or SLR) without unlocking it before results in command being ignored.

Writing lock protected registers only changes the current configuration loaded in the SPI registers. To save the configuration and guarantee a correct reload at each powerup, the update has to be pushed into the Non-Volatile Memory (NVM) as described in Section 5.12.

Note: For temporary modifications to the IC configuration, which do not need to be pushed in the Non-Volatile Memory (NVM), it is recommended to disable the Configuration Register Data Integrity Check (CONF_CRC).

Note:

5.10.1 Electrical parameters

Table 48. Configuration lock electrical parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$T_{CFG\_TIMEOUT}$	Configuration lock timeout	Tested in SCAN		2		s

5.11 Software reset (SW_RST)

It is possible to reset the device configuration sending a SW_RST sequence.

Once triggered, the software reset procedure resets all SPI registers to their default values, including the lock protected ones.

The software reset procedure also acts on SPI registers clear on read flags depending on their diagnosis source:

- Runtime diagnosis: VB_UV, V3V3_INT_OV, V5V_OV, V5V_UV, V5V_OT, WKP_OT, GND_LOSS, TRIM_CYC_CRC_FAIL, CONF_CYC_CRC_FAIL, OSC_FAIL, FLT_ERR, WKP_ERR, BNE_ERR, V5V_OC, TSD). These status bits are cleared by sw reset only if faults are no more detected.
- One time diagnosis without results retention (analog comparators BIST and oscillator monitor BIST): POR_SLEEP_ASSERTED, WAKEUP_CYCLIC_END, WAKEUP_CYCLIC_TRX_TIMEOUT, BIST_ANA_DONE, BIST_ANA_FAIL, BIST_OSC_DONE, BIST_OSC_FAIL. In this case the status bits are always cleared by sw reset.
- One time diagnosis with results retention: TRIM_NVM_CRC_FAIL, CONF_NVM_CRC_FAIL, NVM_VERIFY_ERR. These status bits are cleared by sw reset only if diagnosis ends with no fault detected.

- Diagnosis related to SPI or VIF communication events: ISO_ERR, FIFO_RX_EMPTY, FIFO_RX_FULL, FIFO_TX_FULL, WAKEUP_FAULT_VIF, SPI_VIF_ID_ERR, SPI_COMM_CRC_ERR, SPI_WRONG_ADDR, SPI_SHORT_FRAME, SPI_LONG_FRAM, ISO_COMM_CRC_ERR, ISO_SHORT_FRAME, ISO_LONG_FRAME. In this case the status bits are always cleared by sw reset.

To reset the device configuration, the following procedure shall be implemented.

Procedure 4: Software reset

1. Write 0xE1 in the SPECIAL_REG register to enter in partial reset mode
2. Write 0x1E in the SPECIAL_REG register to confirm the reset
3. If required from the application, download the configuration from the NVM.

Since the NVM is re-downloaded at each wakeup, any new configuration should be pushed into the memory with a “write” instruction (see Section 5.12.1). Otherwise, the previous configuration will be restored at the next wakeup event.

5.12 Non-Volatile Memory (NVM)

Key device Device key configuration parameters can be stored in the internal NVM. For the registers that can be saved to the NVM please refer to the device register map.

5.12.1 NVM Read/Write Operations

NVM data is automatically downloaded into local registers every time that the IC performs the following FSM transitions:

- DEEP SLEEP to NORMAL
- CYCLIC_COUNT to CYCLIC_WAKEUP
- CYCLIC_COUNT to NORMAL

When the IC performs FSM transitions to DEEPSLEEP or CYCLIC_COUNT state, a selected group of data stored in local registers is retained to guarantee IC correct operation (VIF_ID_CFG, GEN_CFG1, GEN_CFG2, GEN_CFG3), while all other data is lost. Such data will be re-downloaded in next transition to NORMAL.

When the IC performs FSM transitions to OFF state, all data stored in local registers is lost; NVM data will be re-downloaded in next transition to NORMAL.

As the IC reaches NORMAL state, the following commands allow user interaction with the NVM:

- GENERAL_REG.VM_OP_CMD=0x3 triggers the NVM upload and refresh: this operation fetches the data previously written into configuration registers and writes it to the relative NVM sectors, then it automatically triggers a full NVM re-download to guarantee whole data consistency. The operation lasts T_{NVM_UPLOAD} and during such time interval the MCU will not be able to perform R/W operations (any command will be discarded)
- GENERAL_REG.NVM_OP_CMD=0x5 triggers the NVM refresh, fetching the data from NVM sectors and writing it to the configuration registers. The operation lasts $T_{NVM\_DOWNLOAD}$ and during such time interval the MCU will not be able to perform R/W operations (any command will be discarded)

During NVM upload/download operations, GENERAL_REG.NVM_READY bit is reset to ‘0’, indicating that NVM is busy. Once the task is complete, the GENERAL_REG.NVM_READY is set; as no NVM read/write operation is running, the NVM circuit is kept under reset.

To guarantee data retention, NVM write operation number must not exceed $N_{NVM\_WRITE\_CYCLES}$; if such a limit is exceeded, data retention is not guaranteed. The IC continues to accept and perform every write operation, even if it is beyond $N_{NVM\_WRITE\_CYCLES}$ count. Every time a write operation is performed, the IC automatically updates the GEN_CFG1.NVM_UPLOAD_COUNT counter field, stored in the NVM as well. The counter value saturates at $N_{NVM\_WRITE\_CYCLES}$: if a new write operation is done above the $N_{NVM\_WRITE\_CYCLES}$ limit, counter value is increased at $N_{NVM\_WRITE\_CYCLES}+1$ and will never be updated anymore.

5.12.2 NVM data integrity checks

Device trimming data and configuration data (used to configure IC operation) in VIF_ID_CFG, GEN_CFG1, GEN_CFG2, GEN_CFG3 registers are stored in different sectors, each protected by its own CRC.

Every time the IC performs an NVM download operation (either automatic or user-driven), an integrity check of the NVM CRC (sector by sector) is performed.

Every time the user triggers an NVM upload and refresh operation, the corresponding sector CRC is updated as well; this is done by IC automatically.

5.12.2.1 *Diagnostic functions*

Table 49. NVM integrity check diagnostic functions

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
NVM Trimming Integrity check fail	At least one of the trimming sectors has failed the CRC check	• The CRC check failing sector data is not downloaded into the local registers. Register data is replaced by all zeros. • TRIM_NVM_CRC_FAIL = 1 in GEN_STATUS3 • The FLT pin and the SPI FAULT is asserted in NORMAL if NVM_CRC_FAIL_MSK =0 in GENERAL_REG	Clear on read	• It is possible to mask all zeros replacement setting the NVM_CRC_FAIL_MSK bit before a download • FLT pin and SPI FAULT maskable by bit NVM_CRC_FAIL_MSK in GENERAL_REG
NVM Configuration Integrity check fail	At least one of the configuration sectors has failed the CRC check	• The CRC check failing sector data is not downloaded into the local registers. Register data is replaced by all zeros. • CONF_NVM_CRC_FAIL = 1 in GEN_STATUS3 • The FLT pin and the SPI FAULT is asserted in NORMAL if NVM_CRC_FAIL_MSK =0 in GENERAL_REG	Clear on read	• It is possible to mask all zeros replacement setting the NVM_CRC_FAIL_MSK bit before a download • FLT pin and SPI FAULT maskable by bit NVM_CRC_FAIL_MSK in GENERAL_REG
NVM Upload fail	Failure in the upload phase of the NVM registers	• NVM_VERIFY_ERR = 1 in GENERAL_REG	Clear on read	

5.12.2.2 *Electrical parameters*

Table 50. NVM electrical parameters

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$N_{NVM\_WRITE\_CYCLES}$	Number of allowed NVM write cycles to guarantee data retention	Guaranteed by SCAN			1000	cycles
T_{NVM_UPLOAD}	NVM user sector upload time duration	Guaranteed by SCAN			12	ms
$T_{NVM\_DOWNLOAD}$	NVM full download time duration	Guaranteed by SCAN			400	µs

5.12.3 Configuration Register data integrity check (CONF_CRC)

In order to guarantee the integrity over time of key trimming and configuration data downloaded from NVM, safety relevant registers content (VIF_ID_CFG, GEN_CFG1, GEN_CFG2, GEN_CFG3) is automatically and cyclically checked against corruption within NORMAL mode: this is possible because local register data is provided with a CRC signature, that can be checked periodically (with period t_{CONF_CRC}) when no operation on the NVM is performed, i.e. NVM circuit is in reset state.

The local register CRC signature is managed in the following way:

- Every time NVM data is downloaded into local registers (either automatic or user-driven), a CRC signature is refreshed as well
- Every time the user changes the local register data, the corresponding CRC signature is not automatically updated, thus a CRC check failure is expected at the next execution cycle; as the user requests an NVM upload and refresh operation the local register CRC signature is updated accordingly, and no further CRC check failure is expected. To mask this systematic CRC check failure the user can set the GENERAL_REG.CYC_CRC_DIS bit.

5.12.3.1 Diagnostic functions

Table 51. NVM cyclic check diagnostic functions

Fault type	Assertion condition	IC reaction to assertion	Release condition	Maskable
NVM Trimming Cyclic check fail	At least one of the trimming sectors has failed the cyclic CRC check	• TRIM_CYC_CRC_FAIL = 1 in GEN_STATUS1	Clear on read	• Check disabled by GENERAL_REG.CYC_CRC_DIS = 1
NVM Configuration Cyclic check fail	At least one of the configuration sectors has failed the cyclic CRC check	• CONF_CYC_CRC_FAIL = 1 in GEN_STATUS1	Clear on read	• Check disabled by GENERAL_REG.CYC_CRC_DIS = 1

5.12.3.2 Electrical parameters

Table 52. Configuration integrity check characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{CONF_CRC}	Configuration integrity check period	Tested by SCAN		25	30	ms

6 Application Information

6.1 Application circuit

Figure 20. **Application circuit – capacitive isolation**

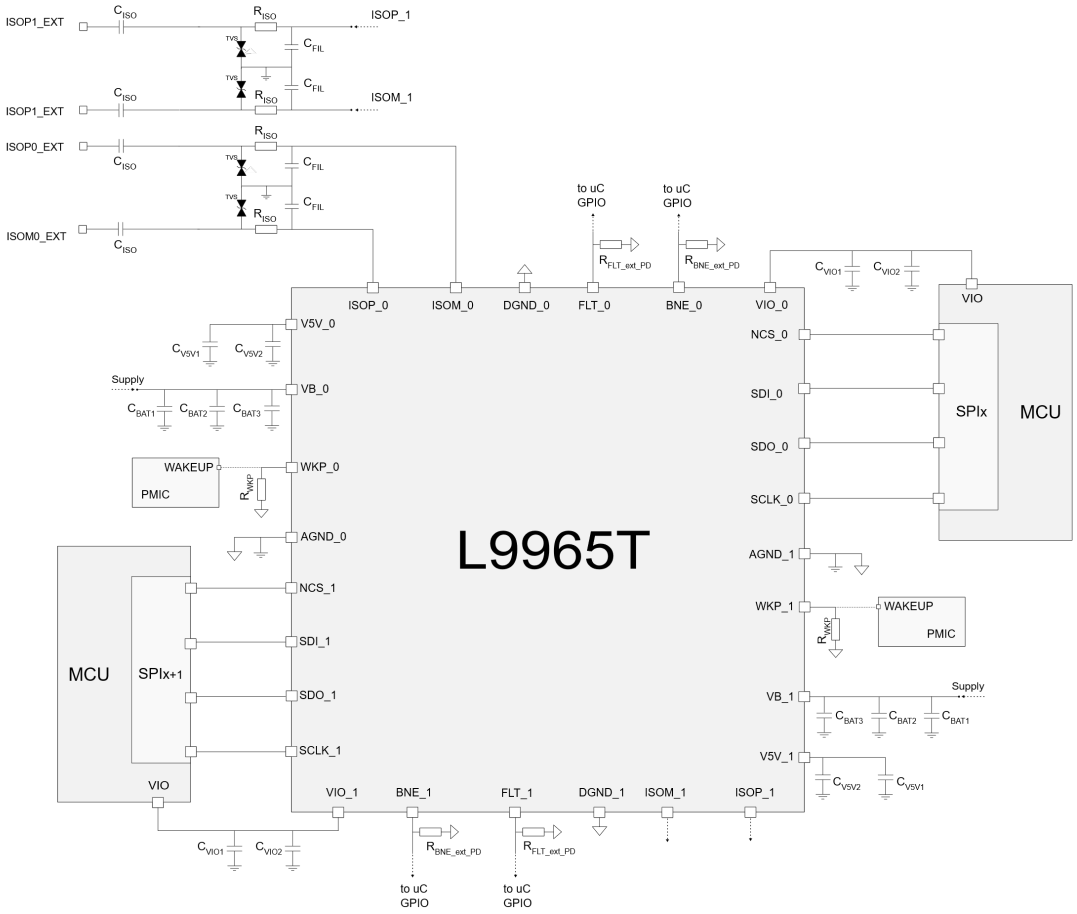
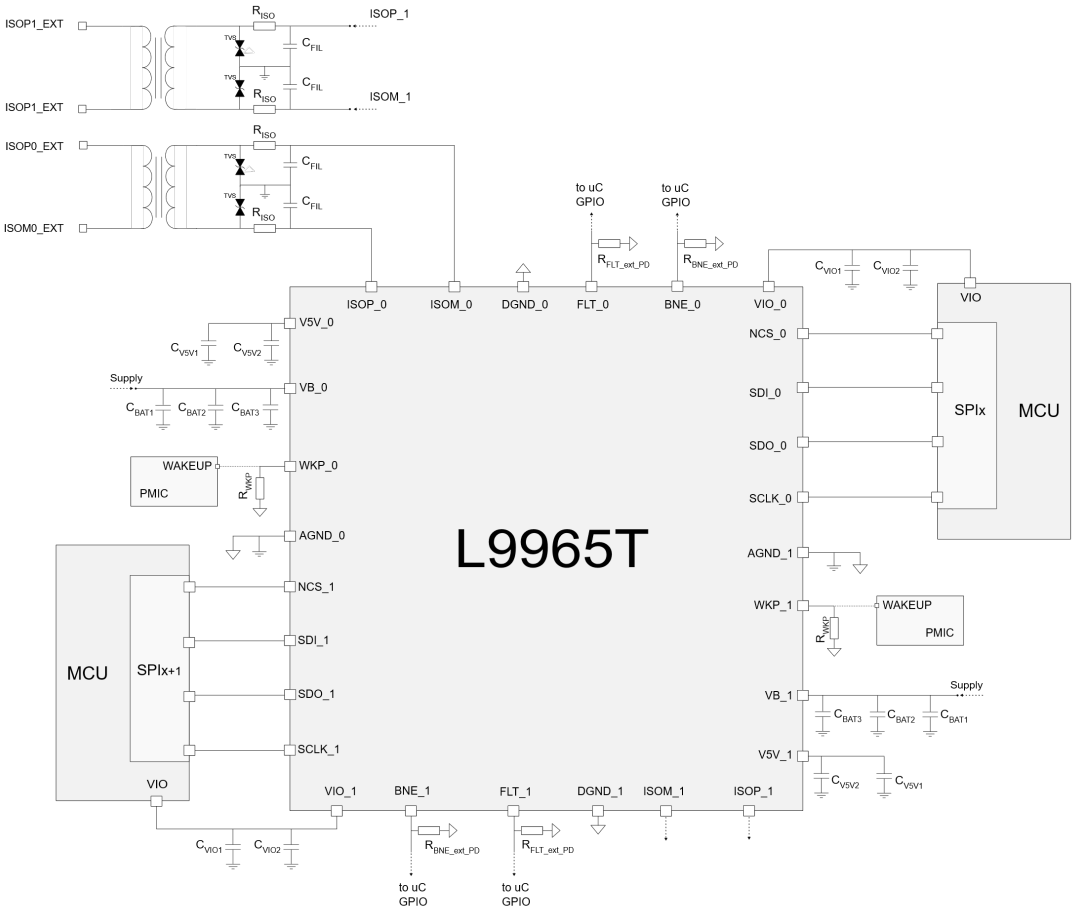


Figure 21. **Application circuit – transformer isolation**



6.1.1 Bill of materials

Table 53. Bill of materials

Symbol	Parameter	Value	Rating	Tolerance	Note
C_{BAT1}	Capacitor on VB	2.2 µF	50V		
C_{BAT2}	Capacitor on VB	100 nF	50V		Filtering capacitor
C_{BAT3}	Capacitor on VB	10 nF	50V		Filtering capacitor
C_{VIO1}	Capacitor on VIO	2.2 µF	16V		
C_{VIO2}	Capacitor on VIO	100 nF	16V		Filtering capacitor
C_{V5V1}	Capacitor on V5V	2.2 µF	16V		
C_{V5V2}	Capacitor on V5V	100 nF	16V		
C_{ISO}	Series capacitor for ISO pins	2.2nF to 6.8nF	100V/1kV	2%	Voltage rating shall be sized according to the maximum isolation voltage to be guaranteed in the application. Keep tolerance low to maximize differential line balancing.
C_{FIL}	Filtering capacitor for ISO termination	100pF	25V	2%	Filters common mode and differential noise. Keep tolerance low to maximize differential line balancing.
R_{TERM}	Termination resistor for unused port	200Ω	0.5W	10%	To be used only on unused VIF port.
R_{WKP}	Pull-down resistor on WKP pin	Typical: 100kΩ			
$R_{FLT\_ext\_PD}$	Pull-down resistor on FLT pin	Typical: 1MΩ			To be mounted if pin is not used.
$R_{BNE\_ext\_PD}$	Pull-down resistor on BNE pin	Typical: 1MΩ			To be mounted if pin is not used.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 LQFP32L (7x7x1.4 mm 5V FULL PLASTIC) package information

Figure 22. LQFP32L (7x7x1.4 mm 5V FULL PLASTIC) package outline

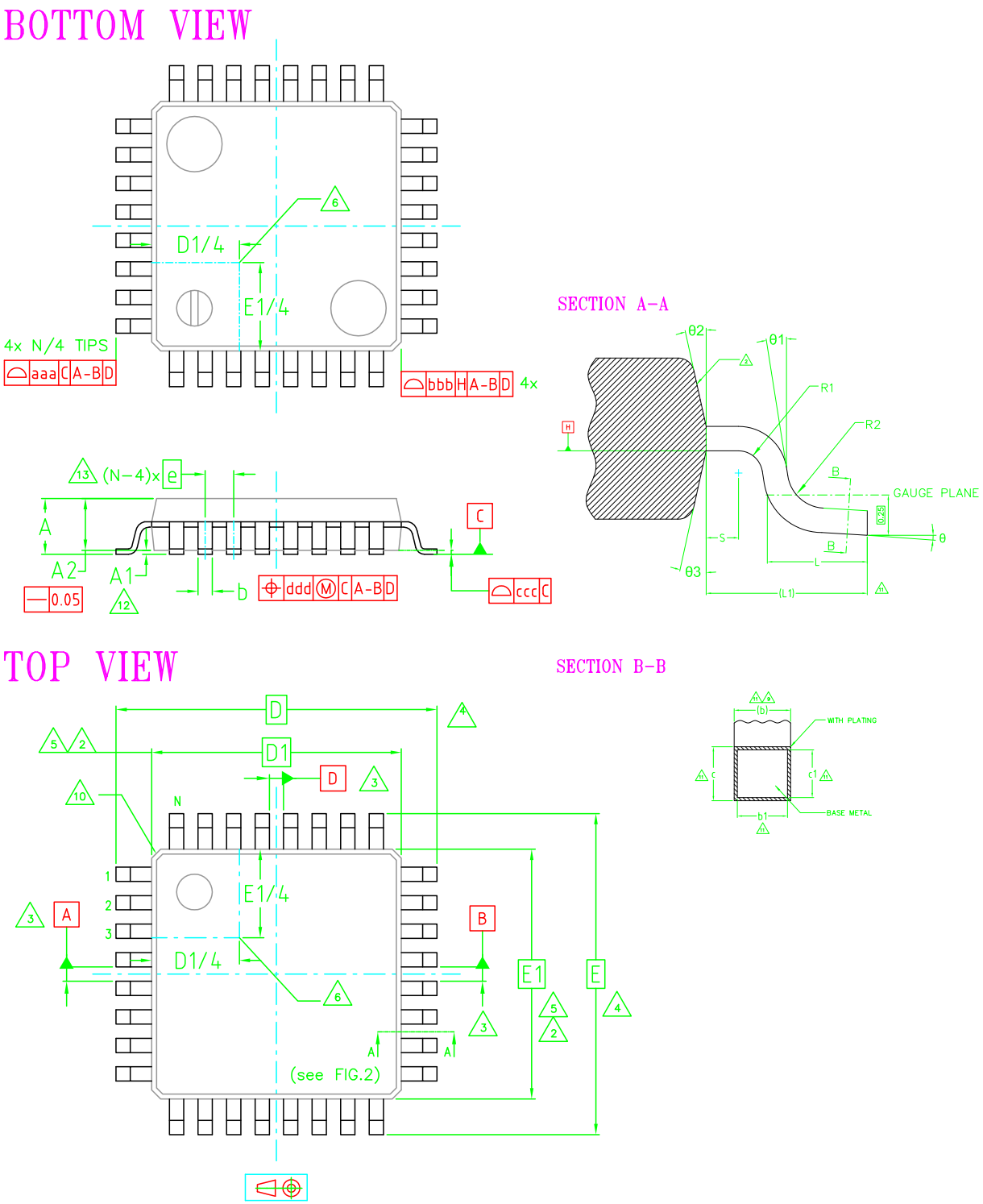


Table 54. **LQFP32L (7x7x1.4 mm 5V FULL PLASTIC) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	10°	12°	14°
θ3	10°	12°	14°
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
c	0.09	-	0.20
c1	0.09	-	0.16
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 BSC		
N	32		
R1	0.08	-	-
R1	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		

Revision history

Table 55. **Document revision history**

Date	Version	Changes
09-Sep-2025	1	Initial release.

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