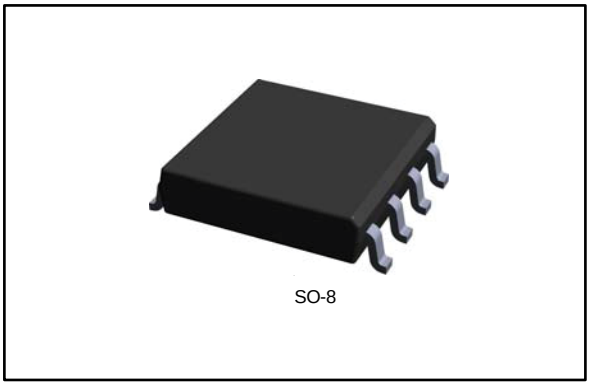
# LCP1521S

## Programmable transient voltage suppressor for SLIC protection

Datasheet - production data



SO-8

## Features

- Programmable transient suppressor
- Wide negative firing voltage range: $V_{Gn}$ = -175 V max.
- Low dynamic switching voltages: $V_{FP}$ and $V_{DGL}$
- Low gate triggering current: $I_{GT}$ = 5 mA max.
- Peak pulse current: $I_{PP}$ = 40 A (5/310 µs)
- Holding current: $I_H$ = 150 mA min.

## Benefits

- A Trisil™ is not subject to ageing and provides a fail-safe mode in short circuit for a better protection.
- Trisils are used to help equipment to meet various standards such as UL60950, IEC 60950 / CSA C22.2, UL1459 and TIA-968-A (formerly FCC part 68)
- Trisils have UL94 V0 resin approved (Trisils are UL497B approved - file: E136224)

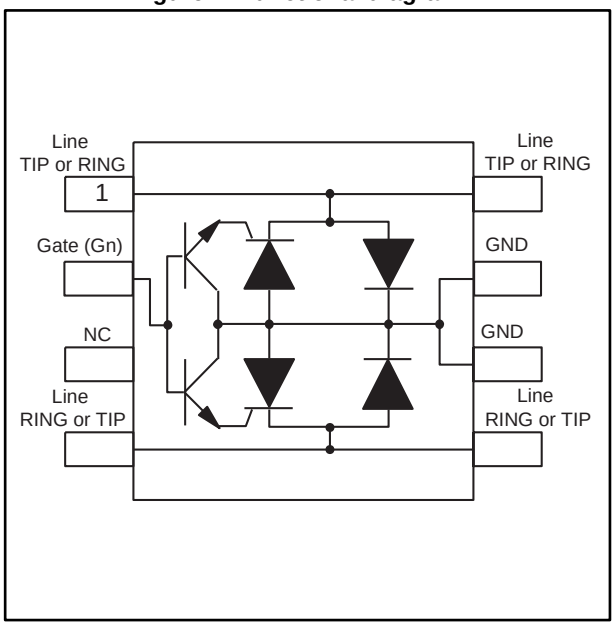
## Description

These devices have been especially designed to protect new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to -$V_{BAT}$ through the gate.

These components present a very low gate triggering current (IGT) in order to reduce the current consumption on printed circuit board during the firing phase.

**Figure 1: Functional diagram**



# 1 Characteristics

**Table 1: Standards compliance**

| Standard | Peak surge voltage (V) | Voltage waveform | Required peak current (A) | Current waveform | Minimum serial resistor to meet standard ( Ω ) |
|---|---|---|---|---|---|
| GR-1089 Core First level | 2500<br>1000 | 2/10 µs<br>10/1000 µs | 500<br>100 | 2/10 µs<br>10/1000 µs | 12<br>24 |
| GR-1089 Core Second level | 5000 | 2/10 µs | 500 | 2/10 µs | 24 |
| GR-1089 Core Intra-building | 1500 | 2/10 µs | 100 | 2/10 µs | 0 |
| ITU-T-K20/K21 | 6000<br>1500 | 10/700 µs | 150<br>37.5 | 5/310 µs | 110<br>0 |
| ITU-T-K20 (IEC 61000-4-2) | 8000<br>15000 | 1/60 ns | ESD contact discharge<br>ESD air discharge | | 0<br>0 |
| IEC 61000-4-5 | 4000<br>4000 | 10/700 µs<br>1.2/50 µs | 100<br>100 | 5/310 µs<br>8/20 µs | 60<br>0 |
| TIA-968-A, lightning surge type A | 1500<br>800 | 10/160 µs<br>10/560 µs | 200<br>100 | 10/160 µs<br>10/560 µs | 22.5<br>15 |
| TIA-968-A, lightning surge type B | 1000 | 9/720 µs | 25 | 5/320 µs | 0 |

**Table 2: Thermal resistances**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(j-a)}$ | Junction to ambient | 120 | °C/W |

**Table 3: Absolute ratings ($T_j$ = 25 °C, unless otherwise specified)**

| Symbol | Parameter | | | Value | Unit |
|---|---|---|---|---|---|
| $I_{pp}$ | Peak pulse current[(1)] | Telcordia GR-1089-CORE Issue 6, May 2011, section 4 | 10/1000 µs | 30 | A |
| | | TIA-968-A, lightning surge type A | 10/560 µs | 35 | |
| | | ITU-T K20/21/44/45, (10/700 µs open circuit voltage waveshape) | 5/310 µs | 40 | |
| | | TIA-968-A, lightning surge type A | 10/160 µs | 50 | |
| | | IEC 61000-4-5, (1.2/50 µs open circuit waveshape) with 10 Ω | 4/30 µs | 110 | |
| | | ITU-T K20/21/44/45, (1.2/50 µs open circuit voltage waveshape) | 8/20 µs | 120 | |
| | | Telcordia GR-1089-CORE Issue 6, (2/10 µs open circuit waveshape) | 2/10 µs | 150 | |
| $I_{TSM}$ | Non repetitive surge peak on-state current (50 Hz sinusoidal) | | t = 20 ms<br>t = 200 ms<br>t = 1 s | 18<br>10<br>7 | A |
| $V_{GN}$ | Negative battery voltage range | -40 °C < $T_{amb}$ < +85 °C | | -175 | V |
| $T_{stg}$ | Storage junction temperature range | | | -55 to + 150 | °C |
| $T_j$ | Operating junction temperature range | | | | |
| $T_L$ | Maximum temperature for soldering during 10 s | | | 260 | °C |

**Notes:**

(1)The rated current values may be applied either to the Ring to GND or to the Tip to GND terminal pairs. Additionally, the four terminal pairs may have their rated current values applied simultaneously (in this case the GND terminal current will be four times the rated current value of an individual terminal pair). Both GND pins must be connected to GND.

**Figure 2: Electrical characteristics (definitions)**

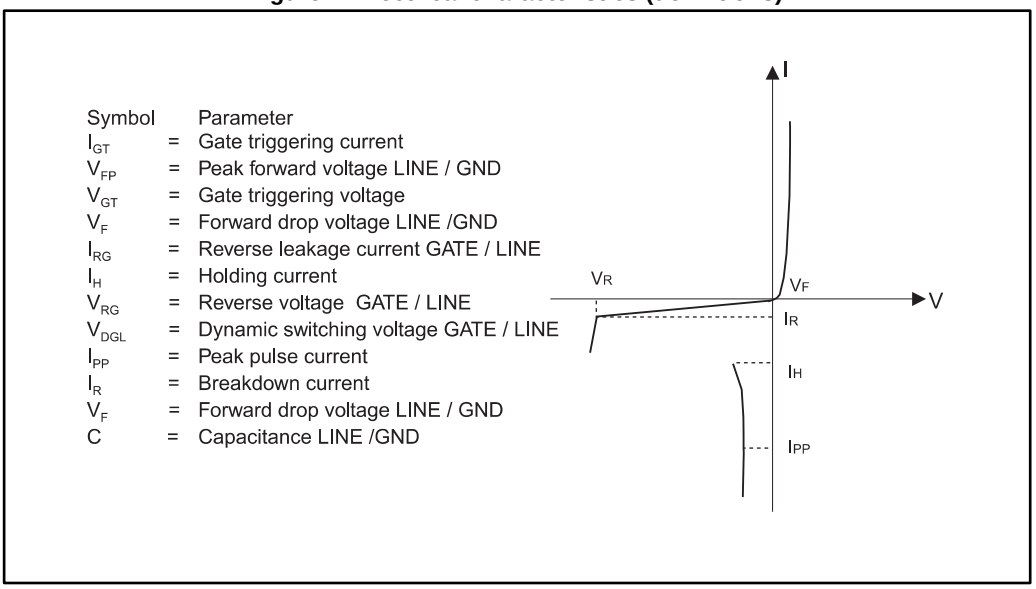



**Figure 3: Pulse waveform**

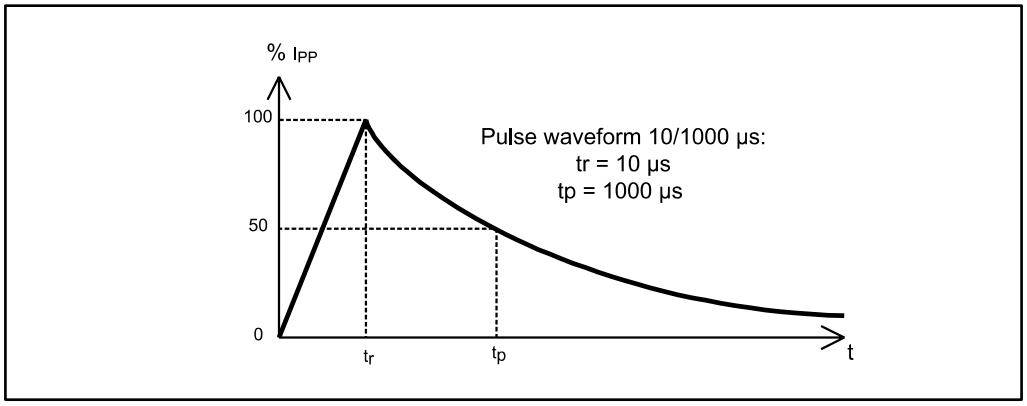


**Table 4: Parameters ($T_j$ = 25 °C, unless otherwise specified)**

| Symbol | Test conditions | | | | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $I_{GT}$ | $V_{LINE}$ = -48 V | | | | | 0.1 | | 5 | mA |
| $I_H$ | $V_{Gn}$ = -48 V | | | | | 150 | | | mA |
| $V_{GT}$ | at $I_{GT}$ | | | | | | | 2.5 | V |
| $I_{RG}$ | $V_{RG}$ = -175 V<br>$V_{RG}$ = -175 V | | | | $T_j$ = 25 °C<br>$T_j$ = 85 °C | | | 5<br>50 | µA |
| $V_{DGL}$ (1) | $V_{Gn}$ = -48 V | 10/700 µs | 1.5 kV | $R_S$ = 10 Ω | $I_{PP}$ = 30 A | | | 7 | V |
| | | 1.2/50 µs | 1.5 kV | $R_S$ = 10 Ω | $I_{PP}$ = 30 A | | | 10 | |
| | | 2/10 µs | 2.5 kV | $R_S$ = 62 Ω | $I_{PP}$ = 38 A | | | 25 | |
| $V_F$ | $I_F$ = 1 A | | t = 500 µs | | | | | 3 | V |
| $V_{FP}$ | 10/700 µs | | | 1.5 kV | $R_S$ = 10 Ω | | | 5 | V |
| | 1.2/50 µs | | | 1.5 kV | $R_S$ = 10 Ω | | | 9 | |
| | 2/10 µs | | | 2.5 kV | $R_S$ = 62 Ω | | | 30 | |
| $I_R$ | $V_{Gn / LINE}$ = -1 V, $V_{LINE}$ = -175 V<br>$V_{Gn / LINE}$ = -1 V, $V_{LINE}$ = -175 V | | | | $T_j$ = 25 °C<br>$T_j$ = 85 °C | | | 5<br>50 | µA |
| C | $V_{LINE}$ = -50 V, $V_{RMS}$ = 1 V, f = 1 MHz<br>$V_{LINE}$ = -2 V, $V_{RMS}$ = 1 V, f = 1 MHz | | | | | | 15<br>35 | | pF |

**Notes:**

(1)The oscillations with a time duration lower than 50 ns are not taken into account.

**Table 5: Recommended gate capacitance**

| Symbol | Component | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_G$ | Gate decoupling capacitance | 100 | 220 | | nF |

# 2 Technical information

**Figure 4: LCP concept behavior**

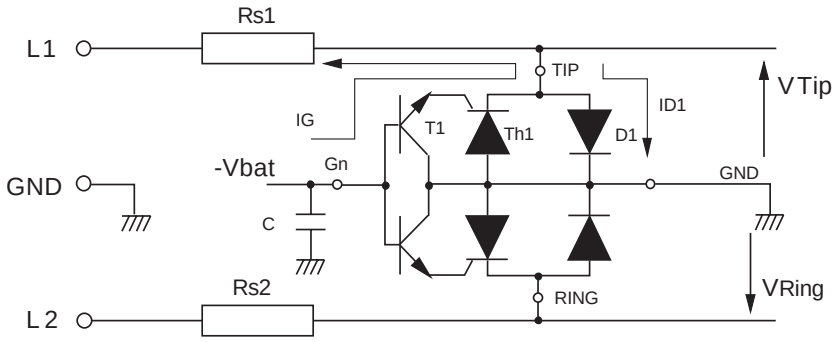



*Figure 4: "LCP concept behavior"* shows the classical protection circuit using the LCP crowbar concept. This topology has been developed to protect the new high voltage SLICs. It allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current IG flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current IH, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

**Figure 5: Example of PCB layout based on LCP1521S protection**

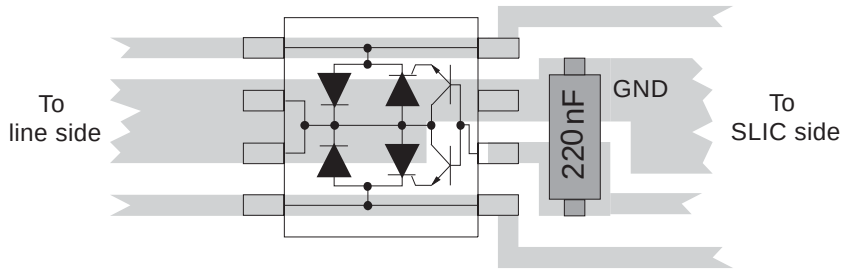



*Figure 5: "Example of PCB layout based on LCP1521S protection"* shows the classical PCB layout used to optimize line protection.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This allows minimization of the dynamic breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - $V_{bat}$ pin.

So to be efficient it has to be as close as possible from the LCP Gate pin and from the reference ground track (or plan) (see *Figure 5: "Example of PCB layout based on LCP1521S protection"*). The optimized value for C is 220 nF.

The series resistors Rs1 and Rs2 designed in *Figure 4: "LCP concept behavior"* represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests imposed by the various country standards. Taking into account this fact the actual lightning surge current flowing through the LCP is equal to:

- I surge = V surge / ($R_g$ + $R_s$) with:
  - V surge = peak surge voltage imposed by the standard.
  - $R_g$ = series resistor of the surge generator
  - $R_s$ = series resistor of the line card (e.g. PTC)

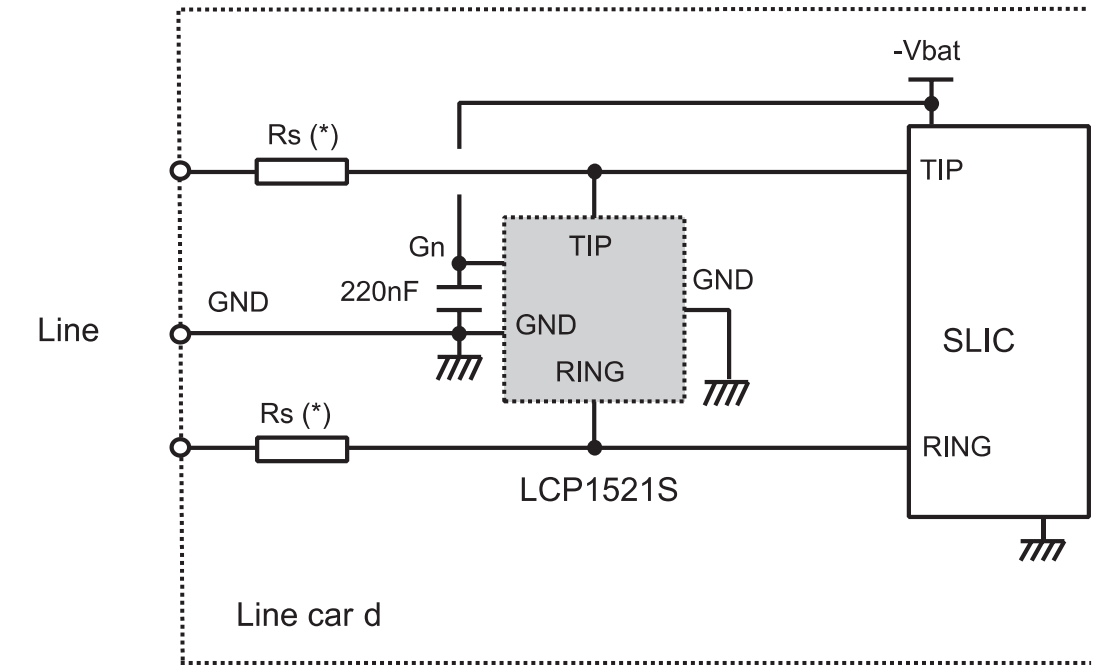
E.g. For a line card with 30 Ω of series resistors which has to be qualified under GR1089 core 1000V 10/1000 µs surge, the actual current through the LCP is equal to:

- I surge = 1000 / (10 + 30) = 25 A

The LCP is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable.

The schematics of *Figure 6: "Protection of high voltage SLIC"* give the most frequent topology used for these applications.

**Figure 6: Protection of high voltage SLIC**




Rs (*) = PTC or fuse resistor

**Figure 7: Surge peak current versus duration**

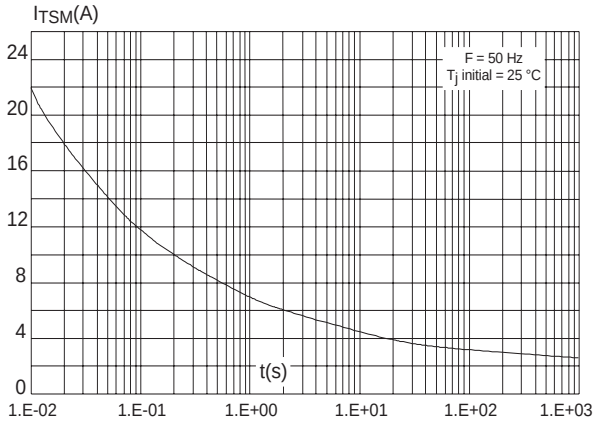
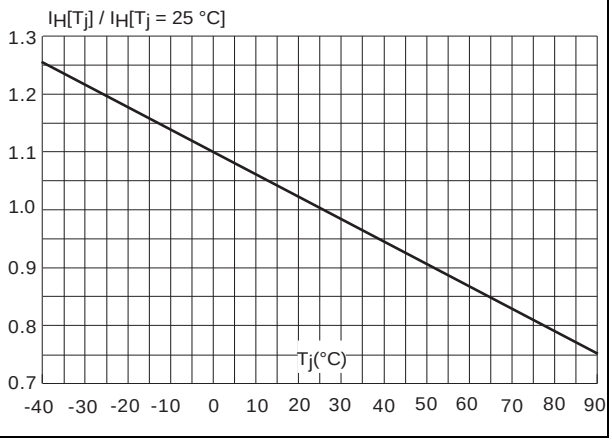



**Figure 8: Relative variation of holding current versus junction temperature**



# 3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 3.1 SO-8 package information

**Figure 9: SO-8 package outline**

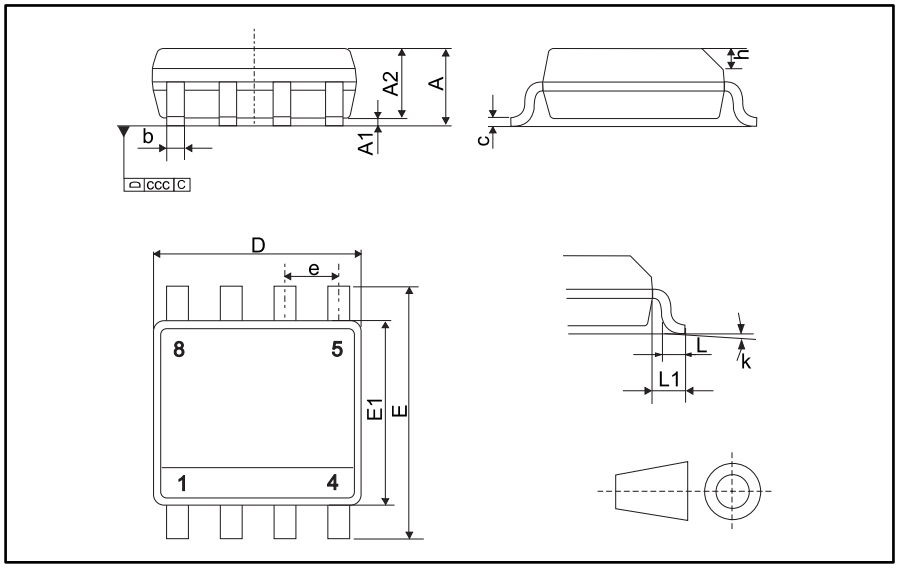



**Table 6: SO-8 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.069 |
| A1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.25 | | | 0.049 | | |
| b | 0.31 | | 0.51 | 0.012 | | 0.020 |
| c | 0.10 | | 0.25 | 0.004 | | 0.010 |
| D | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| E | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| E1 | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| e | | 1.27 | | | 0.050 | |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.05 |
| L1 | | 1.04 | | | 0.041 | |
| k° | 0 | | 8 | 0 | | 8 |
| ccc | | | 0.10 | | | 0.004 |

**Figure 10: Footprint recommendations, dimensions in mm (inches)**

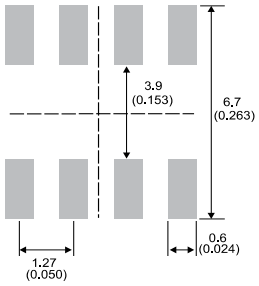



**Figure 11: Marking layout (refer to ordering information table for marking)**

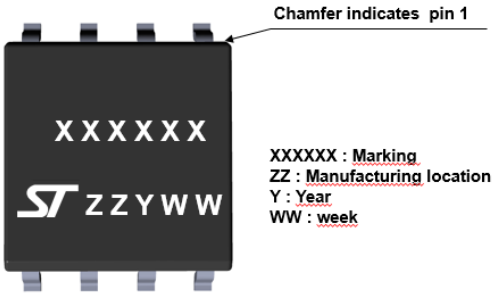
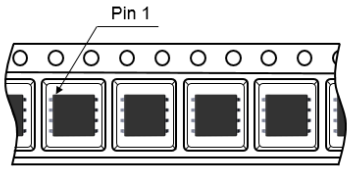



**Figure 12: Package orientation in reel**




Taped according to EIA-481
Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

**Figure 13: Tape and reel orientation**

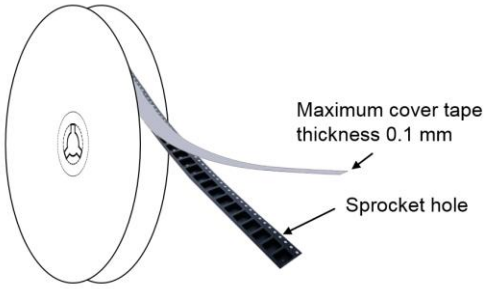



**Figure 14: Reel dimensions (mm)**

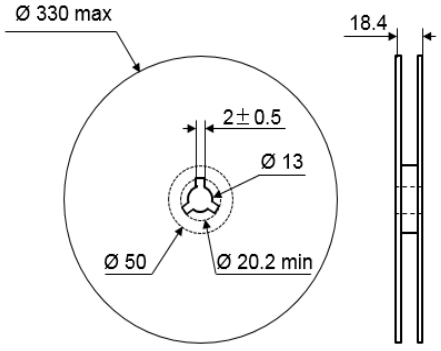



**Figure 15: Inner box dimensions (mm)**

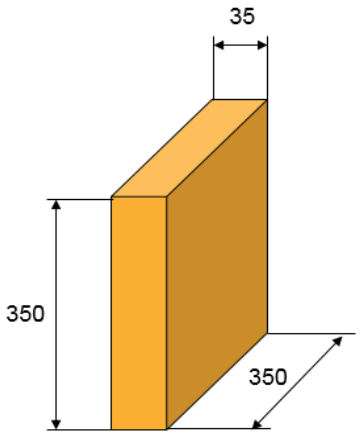


**Figure 16: Tape and reel outline**

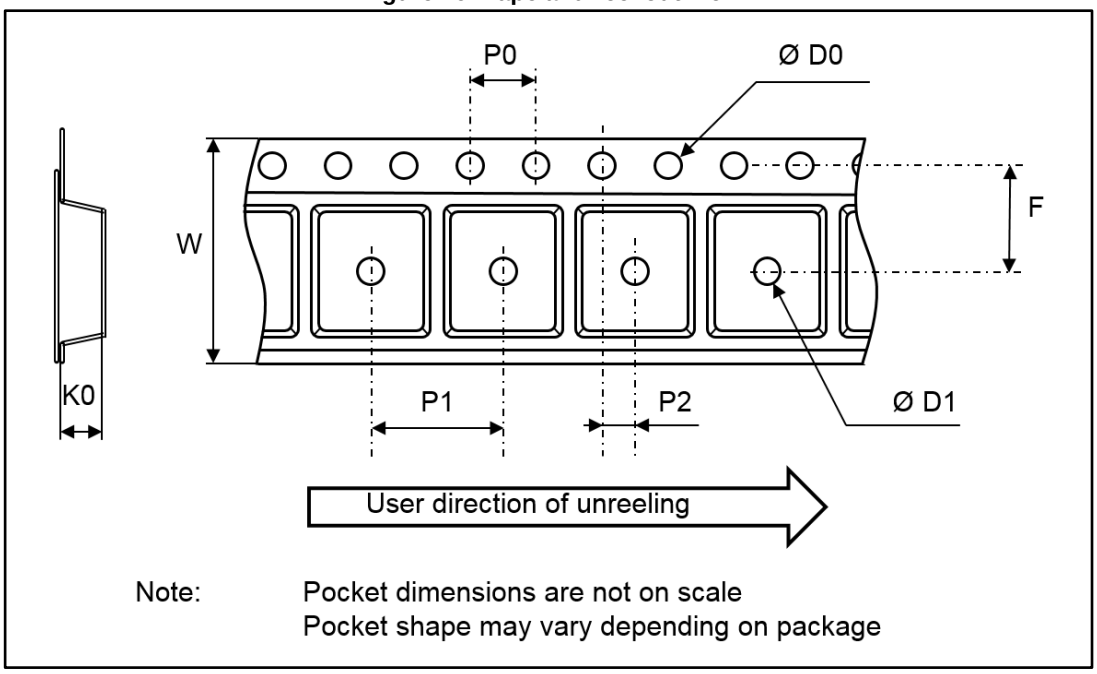
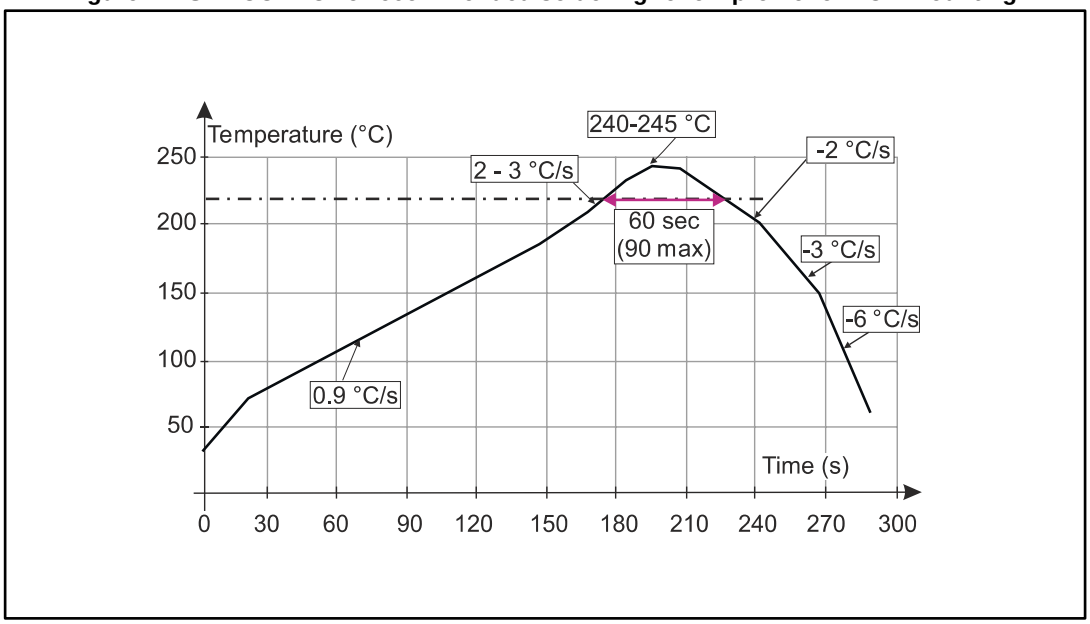



**Table 7: Tape and reel mechanical data**

| Ref. | Dimensions | | |
|---|---|---|---|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| P0 | 3.9 | 4 | 4.1 |
| P1 | 7.9 | 8 | 8.1 |
| P2 | 1.95 | 2 | 2.05 |
| ØD0 | 1.45 | 1.5 | 1.6 |
| ØD1 | 1.6 | | |
| F | 5.45 | 5.5 | 5.55 |
| K0 | 2.5 | 2.6 | 2.7 |
| W | 11.7 | 12 | 12.3 |

**Figure 17: ST ECOPACK® recommended soldering reflow profile for PCB mounting**




Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

# 4 Ordering information

**Table 8: Ordering information**

| Order code | Marking | Package | Weight | Base qty. | Delivery mode |
|---|---|---|---|---|---|
| LCP1521SRL | CP152S | SO-8 | 0.08 g | 2500 | Tape and reel |

# 5 Revision history

**Table 9: Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 20-Nov-2009 | 1 | First issue. |
| 23-Feb-2012 | 2 | Standardized nomenclature for Gn. |
| 15-Nov-2013 | 3 | Updated Figure 9. |
| 10-Apr-2015 | 4 | Updated Figure 1, Figure 10 and package view. Added Figure 11. Updated Table 3 and Table 7. |
| 02-Jul-2015 | 5 | Updated package information. |
| 08-Jul-2015 | 6 | Updated Figure 9. |
| 12-Dec-2017 | 7 | Updated *Table 3: "Absolute ratings ($T_j$ = 25 °C, unless otherwise specified)"* and *Section 3: "Package information"*. |

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