

## Rad-hard plastic Quad two-input AND gate

TSSOP-20



Maturity status link

LEOAC08

### Features

- AND gate
- 1.65 V to 6 V operating supply
- 7 V max. rating
- 8.5 ns propagation delay
- Nickel/Palladium/Gold-lead-finished (NiPdAu), whisker-free
- Gold-wires
- RML < 1% and CVCM < 0.1% guaranteed outgassing
- 50 krad (Si) Total Ionizing Dose
- SEL-free up to 62.5 MeV.cm<sup>2</sup>/mg
- Mass: 80 mg
- Compliant with ST-LEO-specification

### Applications

- Low earth orbit (LEO) applications

### Description

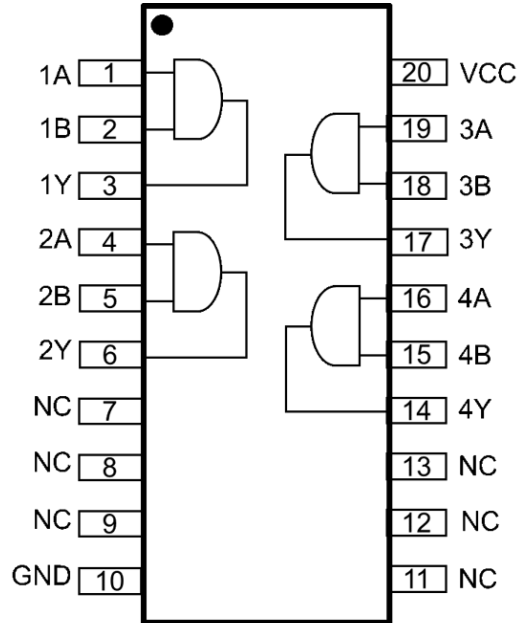
The **LEOAC08** is a CMOS low power quad 2-input AND gate qualified for use in aerospace environments. It operates from 1.65 V to 6 V power supply (7 V absolute maximum rating).

The **LEOAC08** can operate over a large temperature range of -40 °C to +125 °C and it is housed in plastic TSSOP-20, Thin-Shrink Small Outline Package, 20 leads, using golden bonding and Nickel/Palladium/Golden-lead-finishing to prevent whiskers.

The **LEOAC08** is compliant with ST-LEO-specification, dedicated specification for space-ready rad-hard plastic products. This AEC-Q100-based specification offers a specific trade-off between footprint size savings, cost of ownership and quality assurance together with radiation hardness and large quantity capability.

# 1 Functional description

Figure 1. Pin connections (top view)



NC: not internally connected.

The pin can be externally connected to any potential.

Table 1. Truth table

Each gate		
INPUT (A)	INPUT (B)	OUTPUT (Y)
L	L	L
L	H	L
H	L	L
H	H	H

with: L = low level, H = high Level.

For all inputs,  $V_{IN} = V_{IH}$  minimum or  $V_{IL}$  maximum, verify output  $V_{OUT}$ .

## 2 Maximum ratings and operating conditions

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}^{(1)}$	Maximum power supply between $V_{CC}$ and GND	-0.5 to 7	V
$V_{IN}$	DC input voltage range	-0.5 to $V_{CC} + 0.5$ (and 7 V max.)	V
$V_{OUT}$	DC output voltage range	-0.5 to $V_{CC} + 0.5$ (and 7 V max.)	V
$I_K$	I/O clamp diode current	+/-20	mA
$T_{stg}$	Maximum temperature storage	-65 to +150	°C
$T_j^{(2)}$	Maximum junction temperature	+150	°C
$R_{th}^{(3)}$	Junction to ambient thermal resistance ( $\Theta_{ja}$ )	80	°C/W
	Junction to case thermal resistance ( $\Theta_{jc}$ )	17	°C/W
ESD	HBM (human body model)	2k	V
	CDM (charged device model)	1k	V

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal .
2. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions as per the method 5004 of MIL-STD-883.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

**Table 3. Operating conditions**

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Analog supply voltage	1.65	6	V
$V_{IN}$	Input voltage range	0	$V_{CC}$	V
$V_{OUT}$	Output voltage range	0	$V_{CC}$	V
$T_a$	Ambient temperature range	-40	+125	°C

*Note:* All unused inputs must be held at  $V_{CC}$  or GND to ensure proper device operation.

### 3 Electrical characteristics

$V_{CC} = 3\text{ V}$  to  $5.5\text{ V}$ , typical values are at ambient  $T_a = +25\text{ }^\circ\text{C}$ , min. and max. values are at  $T_a = -40\text{ }^\circ\text{C}$  and  $+125\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test condition	VCC (V)	Min.	Typ.	Max.	Unit
$V_{OH}^{(1)}$	High level output voltage	For all inputs affecting output under test, $V_{IN} = V_{IH}$ minimum or $V_{IL}$ maximum. For all other inputs, $V_{IN} = V_{CC}$ or GND, $I_{OH} = -50\text{ }\mu\text{A}$	3	2.9			V
			4.5	4.4			
			5.5	5.4			
		For all inputs affecting output under test, $V_{IN} = V_{IH}$ minimum or $V_{IL}$ maximum. For all other inputs, $V_{IN} = V_{CC}$ or GND, $I_{OH} = -12\text{ mA}$	3	2.4			
			4.5	3.7			
			5.5	4.7			
$V_{OL}^{(1)}$	Low level output voltage	For all inputs affecting output under test, $V_{IN} = V_{IH}$ minimum or $V_{IL}$ maximum. For all other inputs, $V_{IN} = V_{CC}$ or GND, $I_{OL} = +50\text{ }\mu\text{A}$	3		0.1		V
			4.5		0.1		
			5.5		0.1		
		For all inputs affecting output under test, $V_{IN} = V_{IH}$ minimum or $V_{IL}$ maximum. For all other inputs, $V_{IN} = V_{CC}$ or GND, $I_{OL} = +12\text{ mA}$	3		0.5		
			4.5		0.5		
			5.5		0.5		
$I_{OH}$	High level output current		3	-12			mA
			4.5	-24			
			5.5	-24			
			3			12	
$I_{OL}$	Low level output current		4.5			24	
			5.5			24	
			3			0.9	
$V_{IH}^{(2)}$	High level input voltage		4.5	3.15			mA
			5.5	3.85			
			3			0.9	
$V_{IL}^{(2)}$	Low level input voltage		4.5			1.35	V
			5.5			1.65	
			3			0.9	
$V_{IC+}$	Positive input clamp voltage	For input under test, $I_{IN} = -1.0\text{ mA}$	0	0.4		1.5	V

Symbol	Parameter	Test condition	VCC (V)	Min.	Typ.	Max.	Unit
V <sub>IC-</sub>	Negative input clamp voltage	For input under test, I <sub>IN</sub> = -1.0 mA	Open	0.4		1.5	V
I <sub>IH</sub>	Input current high	For input under test, V <sub>IN</sub> = V <sub>CC</sub> For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1	μA
I <sub>IL</sub>	Input current low	For input under test, V <sub>IN</sub> = GND For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND	5			-1	μA
I <sub>CCH</sub>	Quiescent supply current, output high	For all inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 A	5.5			40	μA
I <sub>CCL</sub>	Quiescent supply current, output low	For all inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 A	5.5			40	μA
C <sub>IN</sub> <sup>(3)</sup>	Input capacitance	Ta = +25 °C	5			10	pF
C <sub>PD</sub> <sup>(4)</sup> <sup>(3)</sup>	Power dissipation capacitance	Ta = +25 °C, F = 1 MHz	5			88	pF
T <sub>r</sub> , T <sub>f</sub>	Output rise time and fall time	C <sub>L</sub> = 2 pF, R <sub>L</sub> = 500 ohm (see Figure 2)	3		3.3		ns
			4.5		2.7		
		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 ohm (see Figure 2)	3		4.6		
			4.5		3.3		
T <sub>PHL</sub> <sup>(5)</sup>	Propagation delay time An to Yn, high to low	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 ohm (see Figure 2)	3	1		11.5	ns
			4.5	1		8.5	
T <sub>PLH</sub> <sup>(5)</sup>	Propagation delay time An to Yn, low to high	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 ohm (see Figure 2)	3	1		12.5	
			4.5	1		9	

1. The V<sub>OH</sub> and V<sub>OL</sub> tests shall be tested at V<sub>CC</sub> = 3.0 V and 4.5 V. The V<sub>OH</sub> and V<sub>OL</sub> tests are guaranteed, if not tested, for other values of V<sub>CC</sub>. Limits shown apply to operation at V<sub>CC</sub> = 3.3 V, ±0.3 V and V<sub>CC</sub> = 5.0 V ±0.5 V. Tests with input current at +50 mA and -50 mA are performed on only one input at a time with duration not to exceed 10 ms. Transmission driving tests may be performed using V<sub>IN</sub> = V<sub>CC</sub> or GND. When V<sub>IN</sub> = V<sub>CC</sub> or GND is used, the test is guaranteed for V<sub>IN</sub> = V<sub>IH</sub> minimum and V<sub>IL</sub> maximum.
2. The V<sub>IH</sub> and V<sub>IL</sub> tests are not required if applied as forcing functions for V<sub>OH</sub> and V<sub>OL</sub> tests.
3. C<sub>IN</sub> and C<sub>PD</sub> shall be measured only for initial qualification and after process or design changes which may affect capacitance. C<sub>IN</sub> shall be measured between the designated terminal and GND at a frequency of 1 MHz. C<sub>PD</sub> shall be tested in accordance with the latest revision of JEDEC Standard JESD20 and table IA herein. For C<sub>IN</sub> and C<sub>PD</sub>, test all applicable pins on five devices with zero failures.
4. Power dissipation capacitance (C<sub>PD</sub>) determines both the power consumption (P<sub>D</sub>) and dynamic current consumption (IS). Where: P<sub>D</sub> = (C<sub>PD</sub> + C<sub>L</sub>) (V<sub>CC</sub> × V<sub>CC</sub>) f + (I<sub>CC</sub> × V<sub>CC</sub>) and IS = (C<sub>PD</sub> + C<sub>L</sub>) V<sub>CC</sub> × f + I<sub>CC</sub>, and f is the frequency of the input signal and C<sub>L</sub> is the external output load capacitance.
5. For propagation delay tests, all paths are tested. The AC limits at V<sub>CC</sub> = 5.5 V are equal to the limits at V<sub>CC</sub> = 4.5 V and guaranteed by testing at V<sub>CC</sub> = 4.5 V. The AC limits at V<sub>CC</sub> = 3.6 V are equal to the limits at V<sub>CC</sub> = 3.0 V and guaranteed by testing at V<sub>CC</sub> = 3.0 V. Minimum AC limits for V<sub>CC</sub> = 5.5 V and V<sub>CC</sub> = 3.6 V are 1.0 ns and guaranteed by guard banding the V<sub>CC</sub> = 4.5 V and V<sub>CC</sub> = 3.0 V minimum limits, respectively, to 1.5 ns. For propagation delay tests, all paths must be tested.

## 4 Waveform and test circuit

Figure 2. Waveform

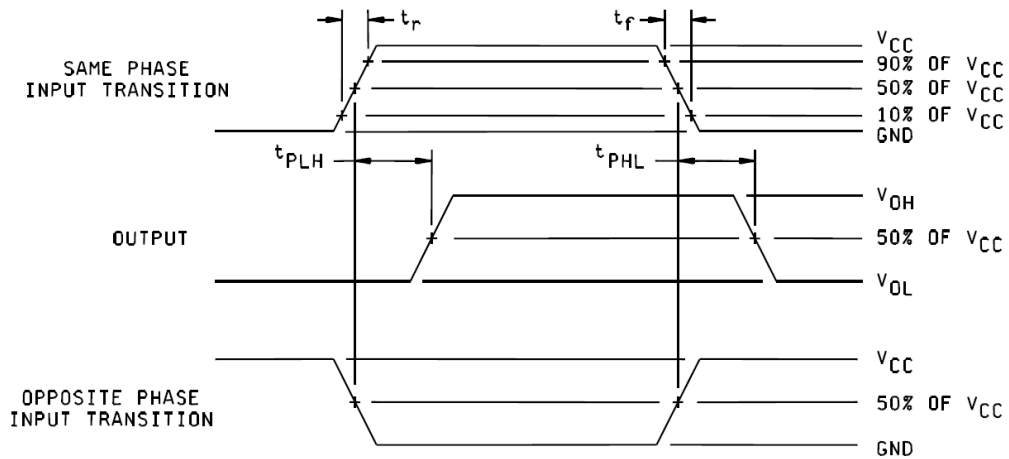
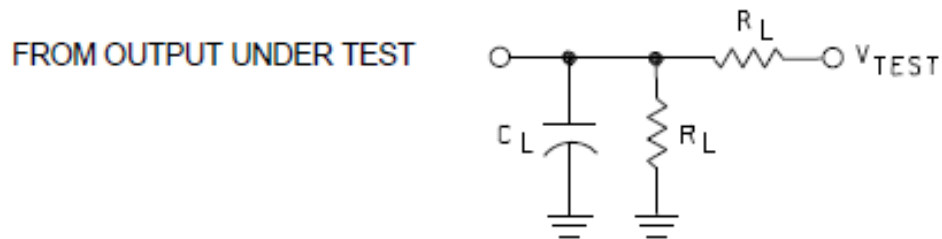


Figure 3. Test circuit



Note:

- $V_{TEST}$  = open for  $t_{PLH}$  and  $t_{PHL}$ .
- $C_L$  = 50 pF or equivalent (includes probe and jig capacitance).
- $R_L$  = 500-ohm or equivalent.
- Input signal from pulse generator:  $V_{IN} = 0.0$  V to  $V_{CC}$ ;  $P_{RR} < 1$  MHz;  $Z_0 = 50$ -ohm;  $t_r < 3.0$  ns;  $t_f < 3.0$  ns;  $t_r$  and  $t_f$  shall be measured from 10% of  $V_{CC}$  to 90% of  $V_{CC}$  and from 90% of  $V_{CC}$  to 10% of  $V_{CC}$ , respectively; duty cycle = 50 percent.
- Timing parameters shall be tested at a minimum input frequency of 1 MHz.
- The outputs are measured one at a time with one transition per measurement.

## 5 Radiations

### Total ionizing dose (TID):

For the qualification, the product is characterized in TID as per MIL-STD-883 TM 1019 up to 50 krad (Si) on 5 biased parts at high dose rate, such a rate being the worst condition for a pure CMOS technology.

All parameters provided in Table 1 apply to both pre- and post-irradiation.

Each new production lot is tested at high dose rate as per MIL-STD-883 TM 1019 on 5 parts.

### Heavy-ions:

Single Event Latchup (SEL) is characterized at 125 °C at a LET of 62.5 MeV.cm<sup>2</sup>/mg. The test shows the product is immune to heavy ions at this LET. Heavy-ion trials are performed on qualification lots only.

The results in radiation are summarized in Table 5 as follows.

**Table 5. Radiations**

Type	Conditions	Results
TID <sup>(1)</sup>	<ul style="list-style-type: none"> <li>High-dose rate (40 krad (Si) / h)</li> <li>Temperature: 25 °C</li> <li>Performed on 5 biased parts</li> </ul>	Within Table 1 up to 50 krad(Si)
SEL <sup>(2)</sup>	<ul style="list-style-type: none"> <li>LET: 62.5 MeV.cm<sup>2</sup>/mg (Xenon ions)</li> <li>Temperature: 125 °C</li> <li>Fluence: 1 x 10<sup>7</sup> ions/cm<sup>2</sup> (10 Million of particles per cm<sup>2</sup>)</li> <li>Normal incidence</li> </ul>	Immune to SEL up to 62.5 MeV.cm <sup>2</sup> /mg (extracted from the LEOAC00, by similarity of architecture)

1. A total ionizing dose (TID) of 50 krad(Si) is equivalent to 500 Gy(Si), (1 gray = 100 rad).

2. SEL: single event latch-up

## 6 Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML) <sup>(1)</sup>	0.06	%
Collected volatile condensable material (CVCM) <sup>(2)</sup>	0.00	%

1. RML < 1%

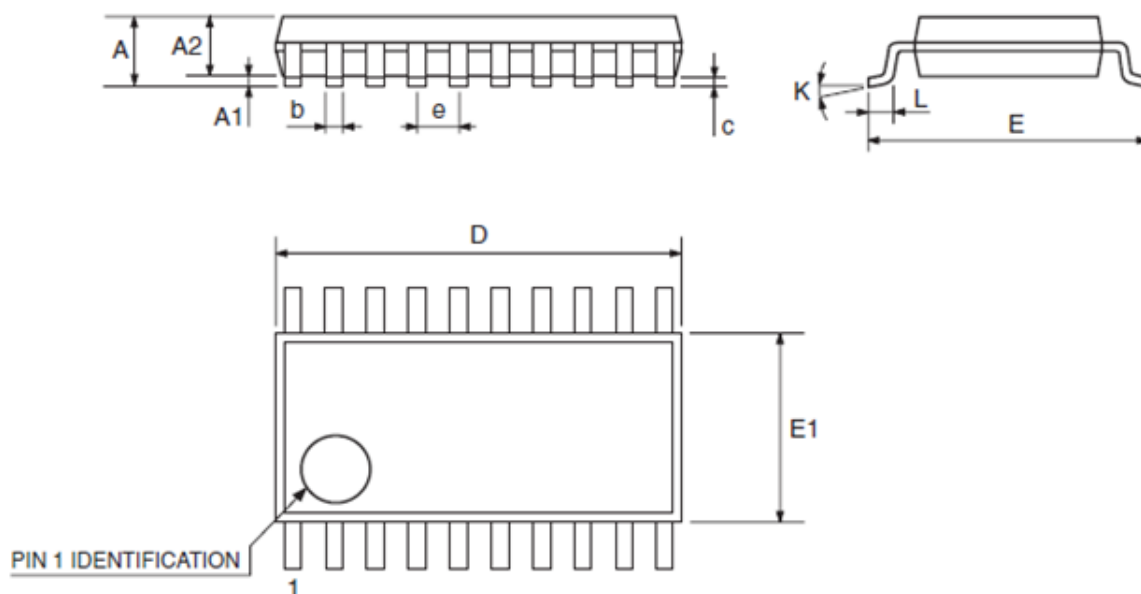
2. CVCM < 0.1%

## 7 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 7.1 TSSOP-20 package information

**Figure 4. TSSOP-20 package outline**



**Table 6. TSSOP-20 package mechanical data**

Symbol	Millimeters			Inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		
c	0.09		0.20	0.004		
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Note:** TSSOP: Thin-Shrink Small Outline Package, using golden bonding and Nickel/Palladium/Golden-lead-finishing.

## 7.2 TSSOP-20 packing information

Figure 5. TSSOP-20 Carrier tape (dimensions in mm) outline

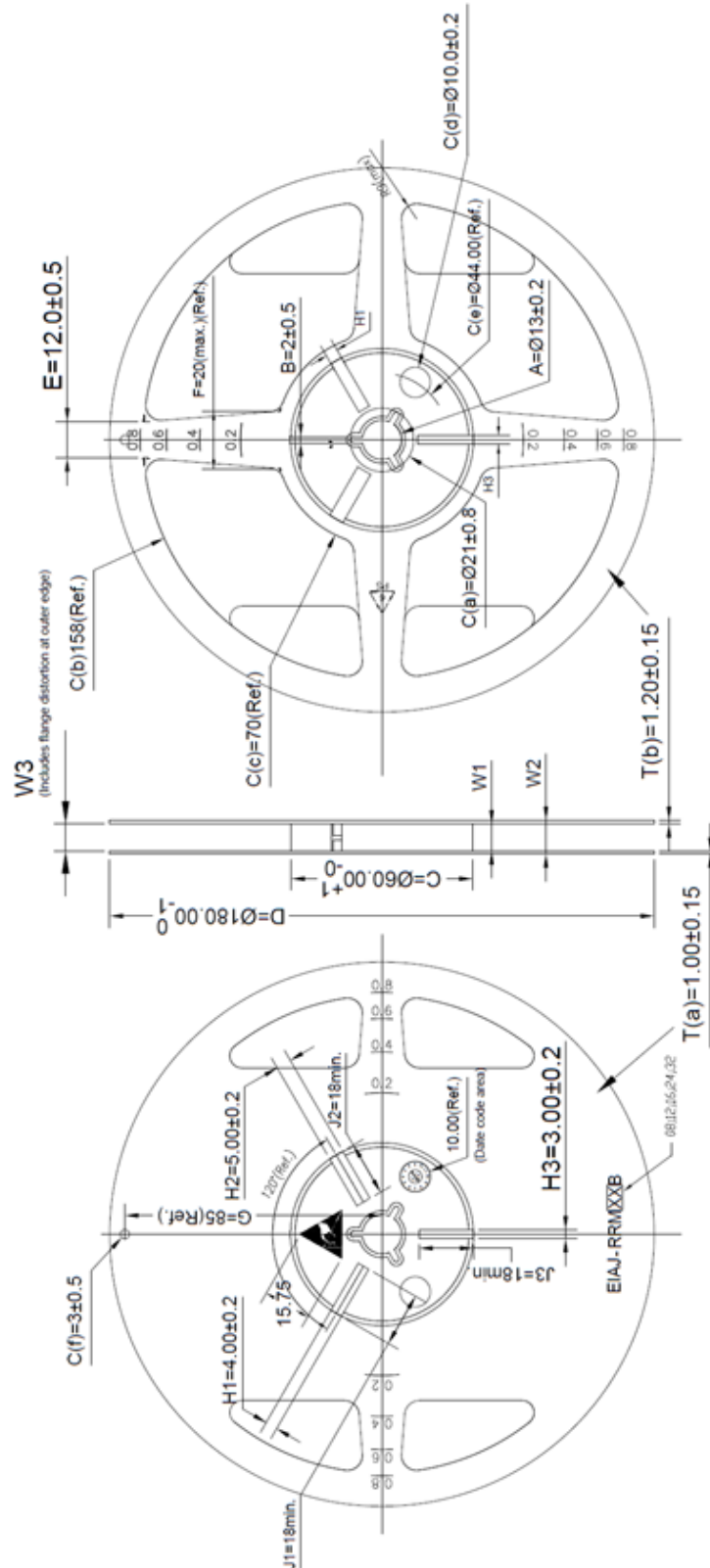
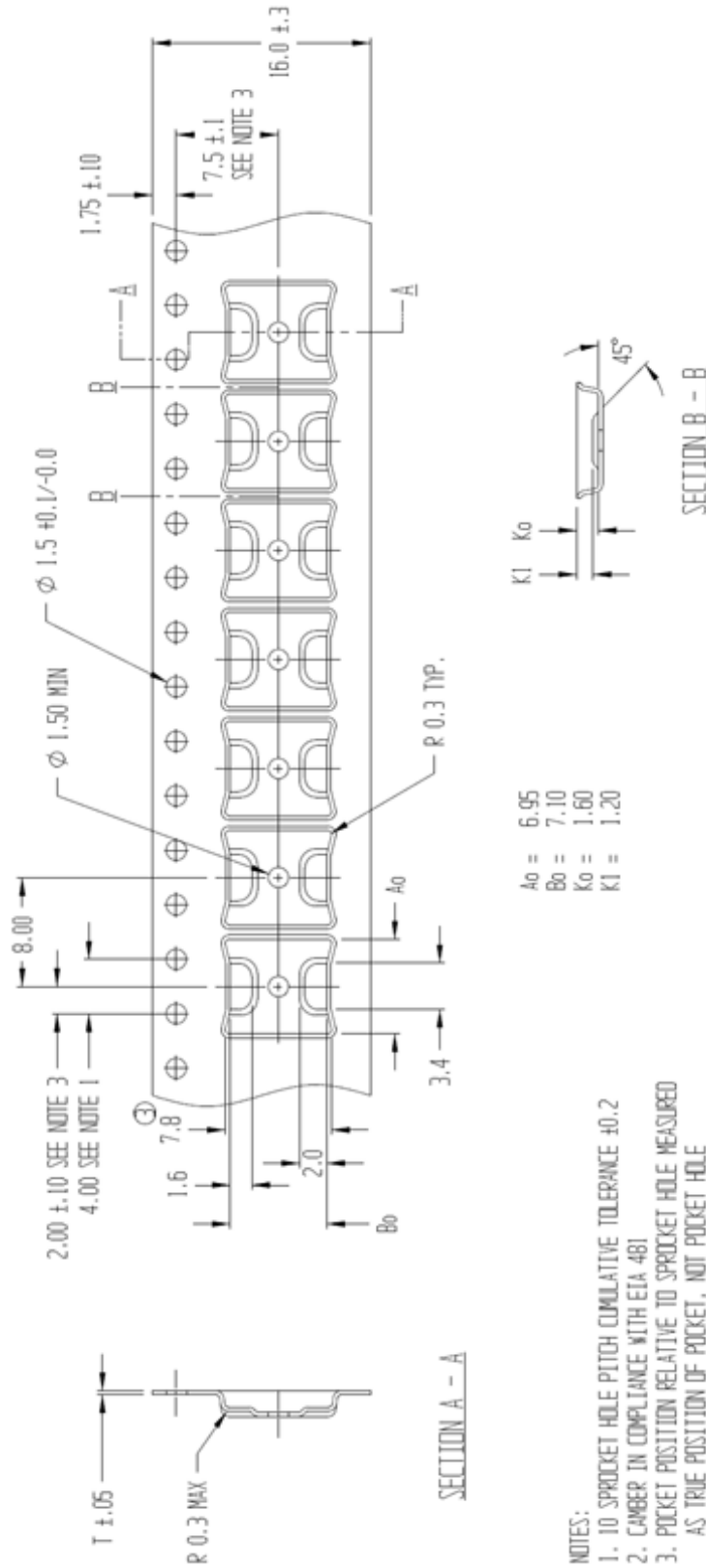


Figure 6. TSSOP-20 tape (dimensions in mm) outline



## 8 Ordering information

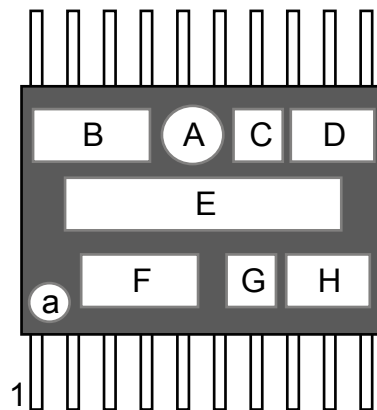
**Table 7. Ordering information**

Order code	Quality level	Package	Lead-finish	Marking	Packing
LEOAC08PT	Flight model	TSSOP-20	NiPdAu	LEOAC08	Tape and reel

**Table 8. Order code**

LEO	AC08	P	T
LEO qualification	Name	TSSOP-20 package	Tape and reel

**Figure 7. TSSOP-20 marking**



- a: pin-1 reference
- A : Second Level of interconnexion (type of lead-finishing)
- B: ST logo
- C: Assy plant
- D: Lot code
- E: Marking area
- F: Country of origin
- G: Assy year
- H: Assy week

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
10-Jan-2022	1	First release.
01-Feb-2022	2	Removed footnote in Table 7. Ordering information.
04-Oct-2024	3	Updated minimum operating power supply from 2 V to 1.65 V.
16-Mar-2026	4	Updated <a href="#">Table 7</a> .

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