

## Rad-hard plastic Hex inverter with Schmitt trigger input

TSSOP-20

[Product status link](#)

LEOAC14

### Features

- Schmitt trigger input
- 6 V max. operating
- 7 V max. rating
- Nickel/palladium/gold-lead-finished (NiPdAu), whisker-free
- Gold-wires
- RML <1% and CVCM <0.1% guaranteed outgassing
- 50 krad (Si) total ionizing dose
- SEL-free up to 62.5 MeV.cm<sup>2</sup>/mg
- Mass: 80 mg
- Compliant with ST-LEO-specification

### Application

- Low earth orbit (LEO) applications

### Description

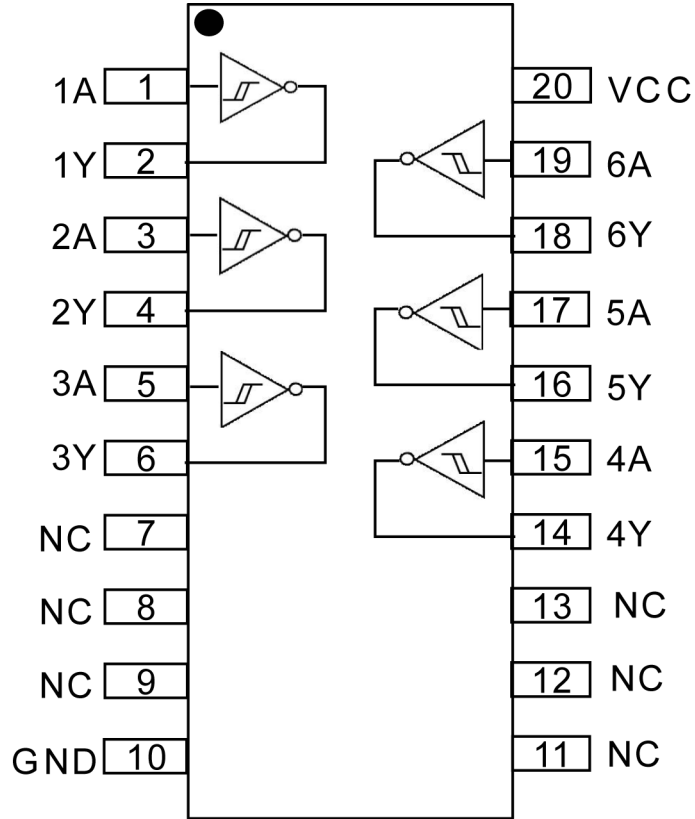
The **LEOAC14** is a CMOS low power hex inverter qualified for use in aerospace environments. It operates from 2 V to 6 V power supply (7 V absolute maximum ratings). Each operator features a Schmitt trigger input that is capable of transforming slowly changing input signals into sharp output signals.

The **LEOAC14** can operate over a large temperature range of -40 °C to +125 °C and it is housed in a plastic TSSOP-20, thin-shrink small outline package, 20 leads, using gold-wires and nickel/palladium/golden-lead-finishing to prevent whiskers.

The **LEOAC14** is compliant with ST-LEO-specification, dedicated specification for space-ready rad-hard plastic products. This AEC-Q100-based specification offers a specific trade-off between footprint size savings, cost of ownership and quality assurance together with radiation hardness and large quantity capability.

# 1 Functional description

Figure 1. Pin connections (top view)



Note: NC: not internally connected. The pin can be externally connected to any potential.

Table 1. Input and output gate

Each gate	
INPUT (A)	OUTPUT (Y)
H	L
L	H

with: L = low level, H = high level.

For all inputs,  $V_{IN} = V_{IH}$  minimum or  $V_{IL}$  maximum, verify output  $V_{OUT}$ .

## 2 Maximum ratings and operating conditions

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
VCC <sup>(1)</sup>	Maximum power supply between VCC and GND	-0.5 to 7	V
VIN	DC input voltage range	-0.5 to VCC+0.5 (and 7 V max.)	V
VOUT	DC output voltage range	-0.5 to VCC+0.5 (and 7 V max.)	V
IK	I/O clamp diode current	+/-20	mA
T <sub>stg</sub>	Maximum temperature storage	-65 to 150	°C
T <sub>j</sub> <sup>(2)</sup>	Maximum junction temperature	+150	°C
R <sub>th</sub> <sup>(3)</sup>	Junction-to-ambient thermal resistance (Θ <sub>ja</sub> )	80	°C/W
	Junction-to-case thermal resistance (Θ <sub>jc</sub> )	17	°C/W
ESD	HBM (human body model)	2 k	V
	CDM (charged device model)	1 k	

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.
2. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions as per the method 5004 of MIL-STD-883.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

**Note:** Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

**Table 3. Operating conditions**

Symbol	Parameter	Min.	Max.	Unit
VCC	Analog supply voltage	2	6	V
VIN	Input voltage range	0	VCC	V
VOUT	Output voltage range	0	VCC	V
T <sub>a</sub>	Ambient temperature range	-40	+125	°C

**Note:** All unused inputs must be held at VCC or GND to ensure proper device operation.

### 3 Electrical characteristics

VCC = 3 V to 5.5 V, typical values are at ambient  $T_a = +25\text{ }^\circ\text{C}$ , minimum and maximum values are at  $T_a = -40\text{ }^\circ\text{C}$  and  $+125\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test conditions	VCC	Min.	Typ.	Max.	Unit
VOH <sup>(1)</sup>	High level output voltage	For all inputs affecting output under test, VIN = VIH minimum or VIL maximum For all other inputs, VIN = VCC or GND, IOH = -50 $\mu\text{A}$	3 V	2.9			V
			4.5 V	4.4			
			5.5 V	5.4			
		For all inputs affecting output under test, VIN = VIH minimum or VIL maximum. For all other inputs, VIN = VCC or GND, IOH = -12 mA	3 V	2.4			
			4.5 V	3.7			
			5.5 V	4.7			
VOL <sup>(1)</sup>	Low level output voltage	For all inputs affecting output under test, VIN = VIH minimum or VIL maximum. For all other inputs, VIN = VCC or GND, IOL = +50 $\mu\text{A}$	3 V			0.1	V
			4.5 V			0.1	
			5.5 V			0.1	
		For all inputs affecting output under test, VIN = VIH minimum or VIL maximum. For all other inputs, VIN = VCC or GND, IOL = +12 mA	3 V			0.5	
			4.5 V			0.5	
			5.5 V			0.5	
IOH	High level output current		3 V	-12			mA
			4.5 V	-24			
			5.5 V	-24			
IOL	Low level output current		3 V			12	mA
			4.5 V			24	
			5.5 V			24	
VIH	High level input voltage		3 V	2.1			V
			4.5 V	3.15			
			5.5 V	3.85			
VIL	Low level input voltage		3 V			0.9	V
			4.5 V			1.35	
			5.5 V			1.65	

Symbol	Parameter	Test conditions	VCC	Min.	Typ.	Max.	Unit
VT+	Positive-going threshold voltage		3 V			2.2	V
			4.5 V			3.2	
			5.5 V			3.9	
VT-	Negative-going threshold voltage		3 V	0.5			V
			4.5 V	0.9			
			5.5 V	1.1			
VHYS	Hysteresis voltage		3 V	0.3		1.2	V
			4.5 V	0.4		1.4	
			5.5 V	0.5		1.6	
VIC+	Positive input clamp voltage	For input under test, IIN = 1 mA	0 V	0.4		1.5	V
VIC-	Negative input clamp voltage	For input under test, IIN = -1.0 mA	Open	-0.4		-1.5	V
I <sub>IH</sub>	Input current high	For input under test, VIN = VCC For all other inputs, VIN = VCC or GND	5.5 V			1	μA
I <sub>IL</sub>	Input current low	For input under test, VIN = GND For all other inputs, VIN = VCC or GND	5.5 V			-1	μA
IC <sub>CH</sub>	Quiescent supply current, output high	For all inputs, VIN = VCC or GND IO <sub>UT</sub> = 0 A	5.5 V			40	μA
IC <sub>CL</sub>	Quiescent supply current, output low	For all inputs, VIN = VCC or GND IO <sub>UT</sub> = 0 A	5.5 V			40	μA
C <sub>IN</sub> <sup>(2)</sup>	Input capacitance	Ta=+25 °C	5 V			8	pF
CPD <sup>(2)(3)</sup>	Power dissipation capacitance	Ta=+25 °C, F=1 MHz	5 V			50	pF
T <sub>r</sub> , T <sub>f</sub>	Output rise time and fall time	CL = 2 pF, RL = 500 ohm, see Figure 2. Waveform	3 V		3.3		ns
			4.5 V		2.7		
			3 V		4.6		
			4.5 V		3.3		
t <sub>PHL</sub> <sup>(4)</sup>	Propagation delay time An to Yn, high to low	CL = 50 pF, RL = 500 ohm See Figure 2. Waveform	3 V	1		14	ns
			4.5 V	1		10	
t <sub>PLH</sub> <sup>(4)</sup>	Propagation delay time An to Yn, low to high	CL = 50 pF, RL = 500 ohm See Figure 2. Waveform	3 V	1		16	ns
			4.5 V	1		12	

1. The VOH and VOL tests are performed at VCC = 3.0 V and 4.5 V. The VOH and VOL tests are guaranteed, if not tested, for other values of VCC. The limits shown apply to operation at VCC = 3.3 V ± 0.3 V and VCC = 5.0 V ± 0.5 V. Tests with input current at +50 mA and -50 mA are performed on only one input at a time with duration not to exceed 10 ms. Transmission driving tests may be performed using VIN = VCC or GND. When VIN = VCC or GND is used, the test is guaranteed for VIN = VIH minimum and VIL maximum.
2. CIN and CPD shall be measured only for initial qualification and after process or design changes which may affect capacitance. CIN shall be measured between the designated terminal and GND at a frequency of 1 MHz. CPD shall be tested in accordance with the latest revision of JEDEC standard JESD20 and table IA herein. For CIN and CPD, test all applicable pins on five devices with zero failures.
3. Power dissipation capacitance (CPD) determines both the power consumption (PD) and dynamic current consumption (IS). Where:  $PD = (CPD + CL) (VCC \times VCC) f + (ICC \times VCC)$  and  $IS = (CPD + CL) VCC \times f + ICC$ , and f is the frequency of the input signal and CL is the external output load capacitance.

- The AC limits at  $V_{CC} = 5.5\text{ V}$  are equal to the limits at  $V_{CC} = 4.5\text{ V}$  and guaranteed by testing at  $V_{CC} = 4.5\text{ V}$ . The AC limits at  $V_{CC} = 3.6\text{ V}$  are equal to the limits at  $V_{CC} = 3.0\text{ V}$  and guaranteed by testing at  $V_{CC} = 3.0\text{ V}$ . Minimum AC limits for  $V_{CC} = 5.5\text{ V}$  and  $V_{CC} = 3.6\text{ V}$  are  $1.0\text{ ns}$  and guaranteed by guard banding the  $V_{CC} = 4.5\text{ V}$  and  $V_{CC} = 3.0\text{ V}$  minimum limits, respectively, to  $1.5\text{ ns}$ . For propagation delay tests, all paths must be tested.*

## 4 Waveform and test circuit

Figure 2. Waveform

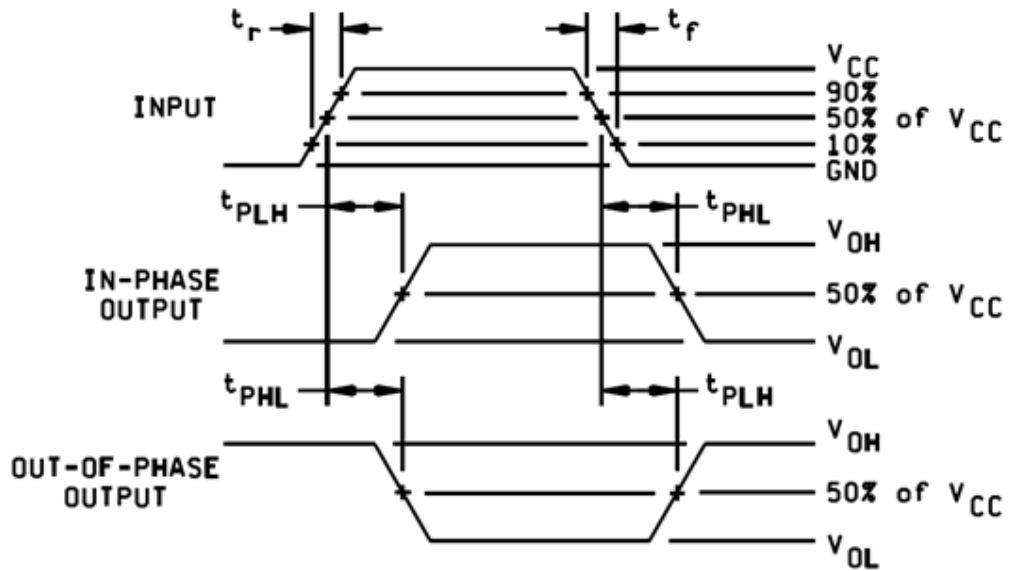
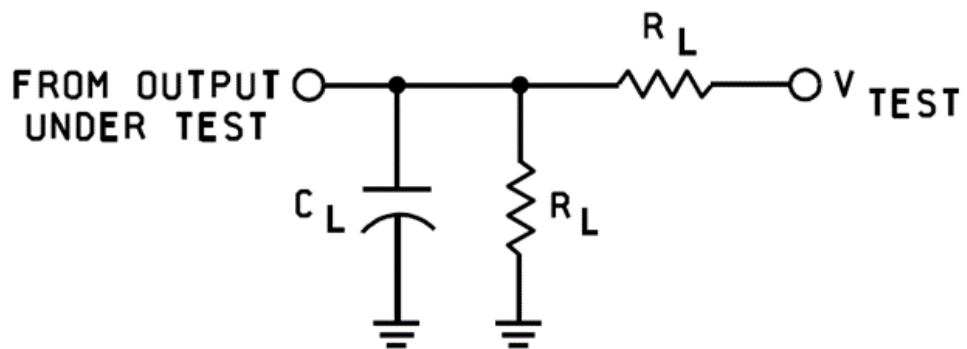


Figure 3. Test circuit



Note:

- When measuring  $t_{PHL}$  or  $t_{PLH}$ :  $V_{TEST} = \text{open}$ .
- $C_L = 50 \text{ pF}$  minimum or equivalent (includes probe and jig capacitance).
- $R_L = 500 \Omega$  or equivalent.
- Input signal from pulse generator:  $V_{IN} = 0.0 \text{ V to } V_{CC}$ ;  $PRR \leq 1 \text{ MHz}$ ;  $Z_O = 50 \Omega$ ;  $t_r \leq 3.0 \text{ ns}$ ;  $t_f \leq 3.0 \text{ ns}$ ;  $t_r$  and  $t_f$  is measured from 10% of  $V_{CC}$  to 90% of  $V_{CC}$  and from 90% of  $V_{CC}$  to 10% of  $V_{CC}$ , respectively; duty cycle = 50 percent.
- Timing parameters are tested at a minimum input frequency of 1 MHz.
- The outputs are measured one at a time with one transition per measurement.

## 5 Radiations

### Total ionizing dose (TID):

For the qualification, the product is characterized in TID as per MIL-STD-883 TM 1019 up to 50 krad(Si) on 5 biased parts at high dose rate; such a rate being the worst condition for a pure CMOS technology.

All parameters provided in [Table 4. Electrical characteristics](#) apply to both pre- and post-irradiation.

Each new production lot is tested at high dose rate as per MIL-STD-883 TM 1019 on 5 parts.

### Heavy-ions:

Single event latchup (SEL) is characterized at 125 °C at a LET of 62.5 MeV.cm<sup>2</sup>/mg. The test shows the product is immune to heavy ions at this LET. Heavy-ion trials are performed on qualification lots only.

The results in radiation are summarized in [Table 5. Radiations](#) as follows:

**Table 5. Radiations**

Symbol	Characteristics	Value
TID <sup>(1)</sup>	<ul style="list-style-type: none"> <li>High-dose rate (40 rad (Si) / h)</li> <li>Temperature: 25 °C</li> <li>Performed on 5 biased parts</li> </ul>	Within <a href="#">Table 4. Electrical characteristics</a> up to 50 krad(Si)
SEL <sup>(2)</sup>	<ul style="list-style-type: none"> <li>LET: 62.5 MeV.cm<sup>2</sup>/mg (Xenon ions)</li> <li>Temperature: 125 °C</li> <li>Fluence: 1 x 10<sup>7</sup> ions/cm<sup>2</sup> (10 Million of particles per cm<sup>2</sup>)</li> <li>Normal incidence</li> </ul>	Immune to SEL up to 62.5 MeV.cm <sup>2</sup> /mg

1. A total ionizing dose (TID) of 50 krad(Si) is equivalent to 500 Gy(Si), (1 gray = 100 rad).

2. SEL: single event latchup.



## 6 Outgassing

Specification (tested per ASTM E 595)	Value	Unit
Recovered mass loss (RML) <sup>(1)</sup>	0.06	%
Collected volatile condensable material (CVCM) <sup>(2)</sup>	0.00	%

1. RML < 1%.
2. CVCM < 0.1%.

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 7.1 TSSOP-20 package information

Figure 4. TSSOP-20 package outline

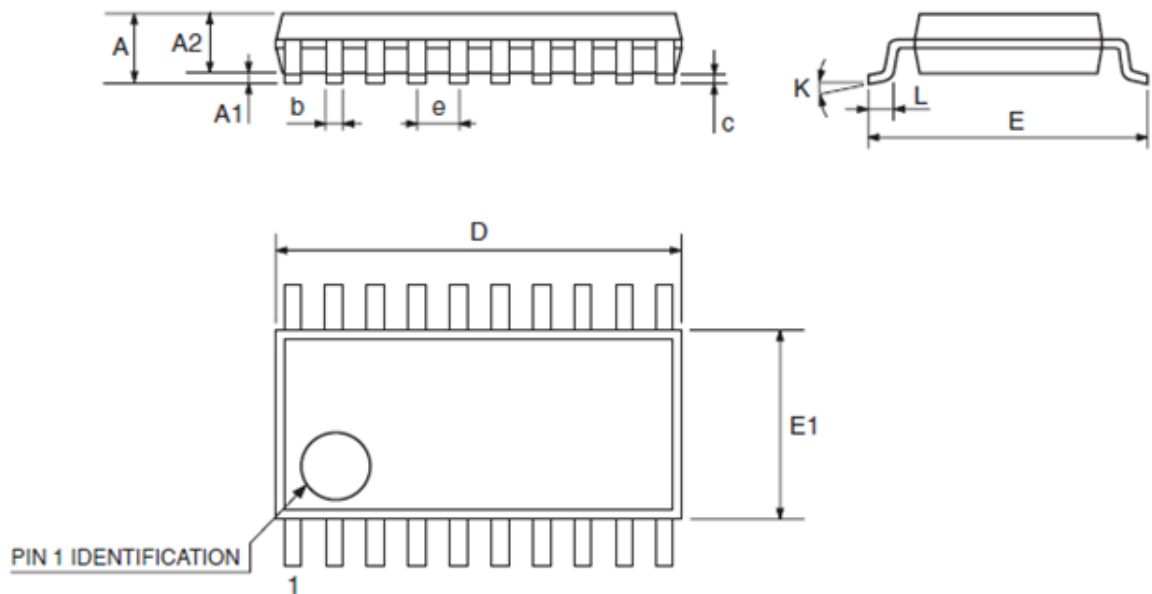


Table 6. TSSOP-20 package mechanical data

Symbol	Millimeters			Inches <sup>(1)</sup>		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		
c	0.09		0.20	0.004		
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 7.2 TSSOP-20 packing information

Figure 5. TSSOP-20 Carrier tape (dimensions in mm) outline

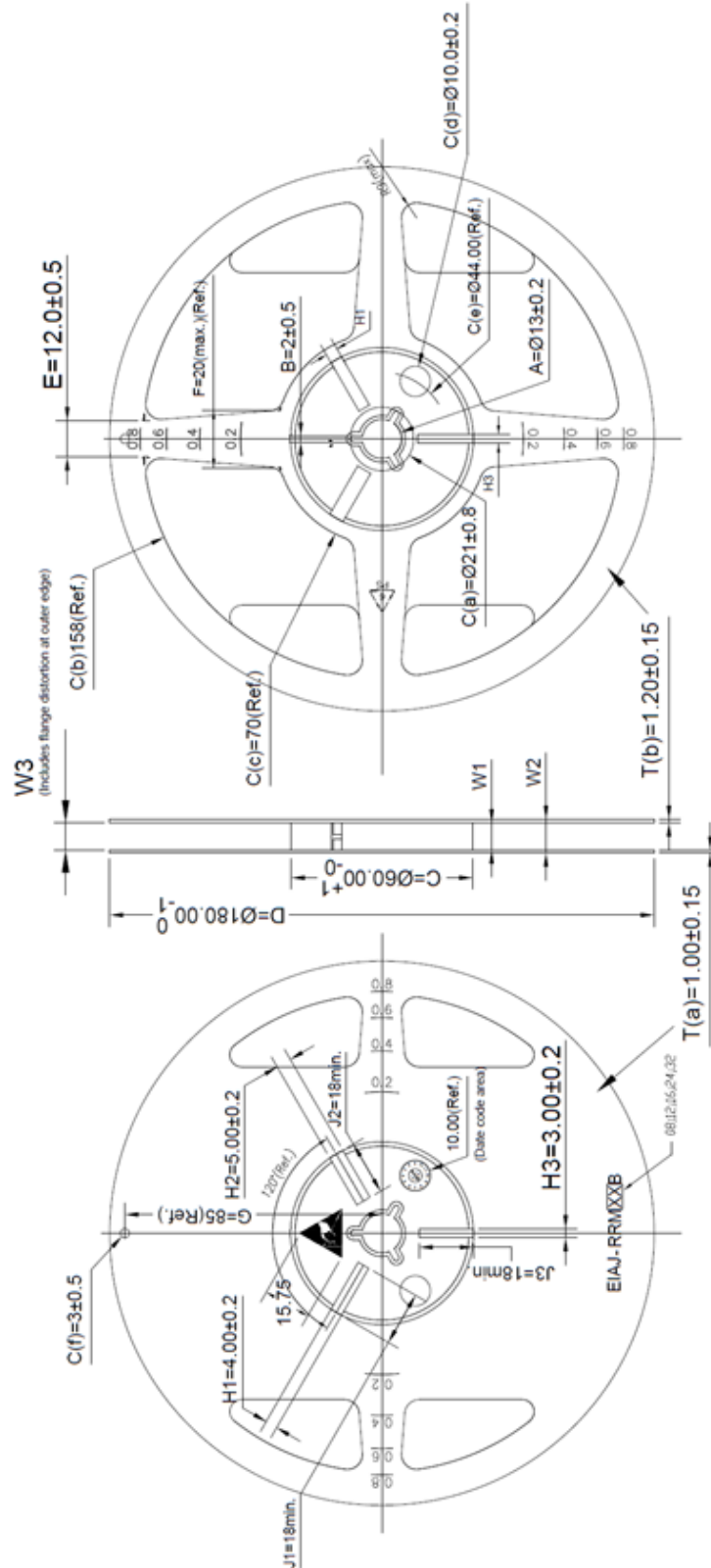
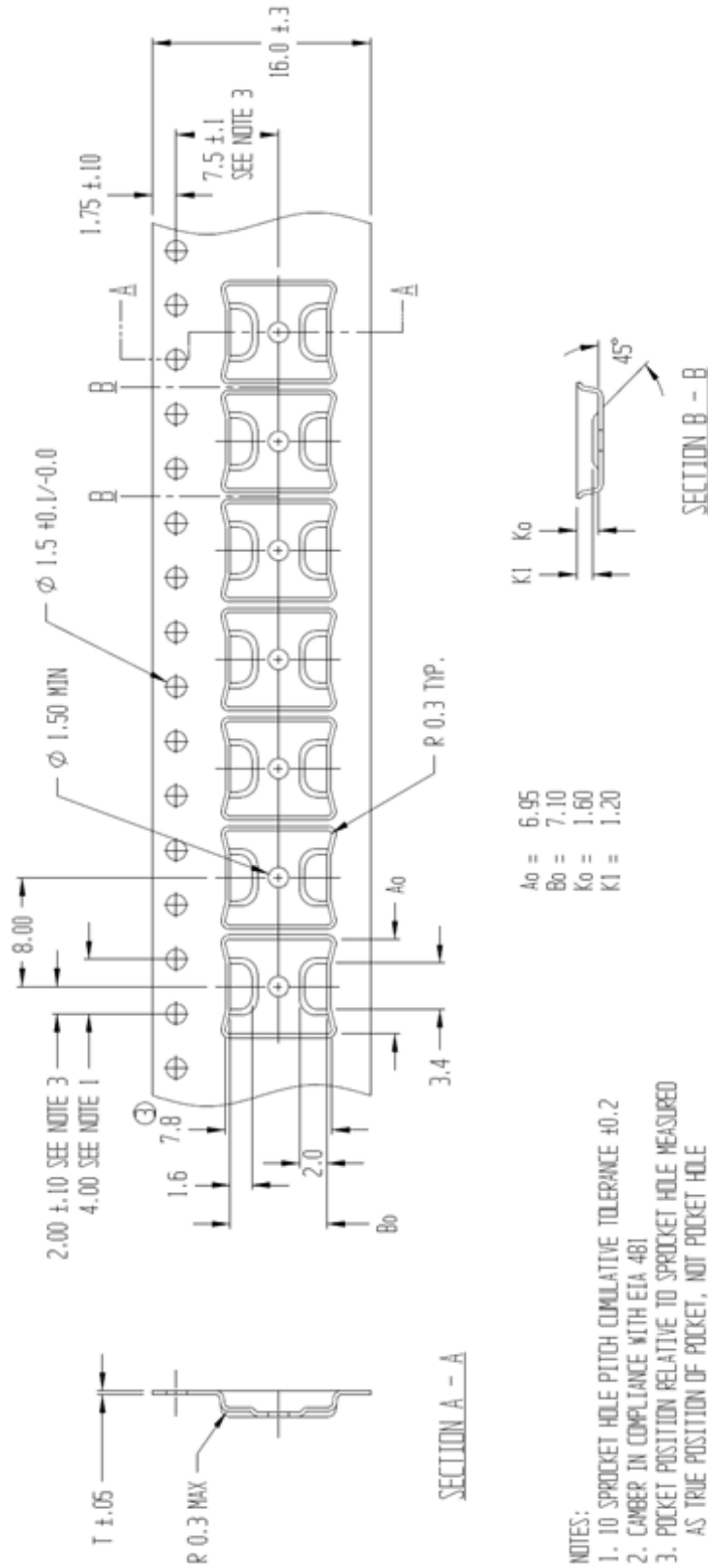


Figure 6. TSSOP-20 tape (dimensions in mm) outline



## 8 Ordering information

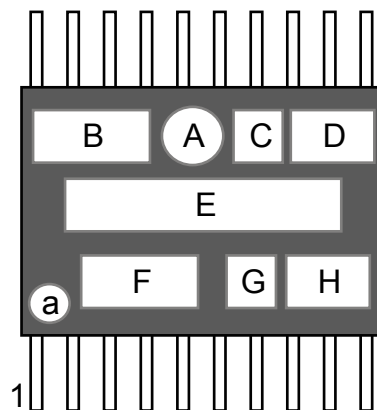
**Table 7. Ordering information**

Order code	Quality level	Package	Lead-finish	Marking	Packing
LEOAC14PT-D	Development sample	TSSOP-20	NiPdAu	DLEOAC14	Tape and reel
LEOAC14PT	Flight model	TSSOP-20	NiPdAu	LEOAC14	Tape and reel

**Table 8. Order code**

LEO	AC14	P	T
LEO qualification	Name	TSSOP-20 package	Tape and reel

**Figure 7. TSSOP-20 marking**



- a: pin-1 reference
- A : Second Level of interconnexion (type of lead-finishing)
- B: ST logo
- C: Assy plant
- D: Lot code
- E: Marking area
- F: Country of origin
- G: Assy year
- H: Assy week

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
10-Feb-2021	1	Initial release.
29-Mar-2021	2	Updated Section 8 Ordering information. Removed "Product documentation" section.
08-Jun-2021	3	Updated $T_{stg}$ value in Table 2 and TID characteristics in Table 5.
30-Aug-2021	4	Updated Section 5 Radiations.
10-Jan-2022	5	Removed ICCT parameter in Table 4.

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## Contents

<b>1</b>	<b>Functional description</b> .....	<b>2</b>
<b>2</b>	<b>Maximum ratings and operating conditions</b> .....	<b>3</b>
<b>3</b>	<b>Electrical characteristics</b> .....	<b>4</b>
<b>4</b>	<b>Waveform and test circuit</b> .....	<b>7</b>
<b>5</b>	<b>Radiations</b> .....	<b>8</b>
<b>6</b>	<b>Outgassing</b> .....	<b>9</b>
<b>7</b>	<b>Package information</b> .....	<b>10</b>
<b>7.1</b>	<b>TSSOP-20 package information</b> .....	<b>10</b>
<b>7.2</b>	<b>TSSOP-20 packing information</b> .....	<b>11</b>
<b>8</b>	<b>Ordering information</b> .....	<b>13</b>
	<b>Revision history</b> .....	<b>14</b>

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## List of tables

<b>Table 1.</b>	Input and output gate . . . . .	2
<b>Table 2.</b>	Absolute maximum ratings . . . . .	3
<b>Table 3.</b>	Operating conditions . . . . .	3
<b>Table 4.</b>	Electrical characteristics . . . . .	4
<b>Table 5.</b>	Radiations . . . . .	8
<b>Table 6.</b>	TSSOP-20 package mechanical data . . . . .	10
<b>Table 7.</b>	Ordering information. . . . .	13
<b>Table 8.</b>	Order code . . . . .	13
<b>Table 9.</b>	Document revision history . . . . .	14



## List of figures

<b>Figure 1.</b>	Pin connections (top view) . . . . .	2
<b>Figure 2.</b>	Waveform . . . . .	7
<b>Figure 3.</b>	Test circuit . . . . .	7
<b>Figure 4.</b>	TSSOP-20 package outline . . . . .	10
<b>Figure 5.</b>	TSSOP-20 Carrier tape (dimensions in mm) outline. . . . .	11
<b>Figure 6.</b>	TSSOP-20 tape (dimensions in mm) outline . . . . .	12
<b>Figure 7.</b>	TSSOP-20 marking. . . . .	13

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