LPS22HH

High-performance MEMS nano pressure sensor:
260-1260 hPa absolute digital output barometer

Datasheet - production data

Properties
- 260 to 1260 hPa absolute pressure range
- Current consumption down to 4 μA
- Absolute pressure accuracy: 0.5 hPa
- Low pressure sensor noise: 0.65 Pa
- High-performance TCO: 0.65 Pa/°C
- Embedded temperature compensation
- 24-bit pressure data output
- ODR from 1 Hz to 200 Hz
- SPI, I2C or MIPI I3C interfaces
- Embedded FIFO
- Interrupt functions: Data-Ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 22,000 g
- Small and thin package
- ECOPACK® lead-free compliant

Applications
- Altimeters and barometers for portable devices
- GPS applications
- Weather station equipment
- Sport watches
- e-cigarettes
- Drones
- Gas metering

Description
The LPS22HH is an ultra-compact piezoresistive absolute pressure sensor which functions as a digital output barometer. The device comprises a sensing element and a IC interface which communicates through I2C, MIPI I3C or SPI from the sensing element to the application.

The sensing element, which detects absolute pressure, consists of a suspended membrane manufactured using a dedicated process developed by ST.

The LPS22HH is available in a full-mold, holed LGA package (HLGA). It is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

Table 1. Device summary

<table>
<thead>
<tr>
<th>Order code</th>
<th>Temperature range [°C]</th>
<th>Package</th>
<th>Packing</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPS22HHTR</td>
<td>-40 to +85°C</td>
<td>HLGA-10L</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

February 2019
DocID030890 Rev 2
1/59

This is information on a product in full production.

www.st.com
Contents

1 Block diagrams ......................................................... 7
2 Pin description .......................................................... 8
3 Mechanical and electrical specifications ......................... 9
   3.1 Mechanical characteristics ........................................ 9
   3.2 Electrical characteristics .......................................... 10
   3.3 Communication interface characteristics ..................... 11
      3.3.1 SPI - serial peripheral interface .......................... 11
      3.3.2 I²C - inter-IC control interface ......................... 12
   3.4 Absolute maximum ratings ......................................... 13
4 Functionality ............................................................... 14
   4.1 Sensing element .................................................... 14
   4.2 IC interface ........................................................ 14
   4.3 Factory calibration ............................................... 14
   4.4 Interpreting pressure readings ................................... 15
   4.5 Interpreting temperature readings .............................. 16
5 FIFO ....................................................................... 17
   5.1 Bypass mode ....................................................... 18
   5.2 FIFO mode ........................................................ 19
   5.3 Continuous (Dynamic-Stream) mode ............................. 20
   5.4 Bypass-to-FIFO mode ............................................. 21
   5.5 Bypass-to-Continuous (Dynamic-Stream) mode ................. 22
   5.6 Continuous (Dynamic-Stream)-to-FIFO mode .................. 23
   5.7 Retrieving data from FIFO ...................................... 23
6 Application hints .......................................................... 24
   6.1 Soldering information ............................................ 25
7 Digital interfaces ......................................................... 26
   7.1 Serial interfaces .................................................. 26
7.2  I²C serial interface (CS = high) ................................................. 26
    7.2.1  I²C operation .............................................................. 27
7.3  SPI bus interface (CS = low) .................................................. 29
    7.3.1  SPI read ................................................................. 30
    7.3.2  SPI write ............................................................... 31
    7.3.3  SPI read in 3-wire mode .............................................. 32
7.4  MIPI I3C<sup>SM</sup> slave interface .......................................... 33
    7.4.1  MIPI I3C<sup>SM</sup> CCC supported commands ......................... 33
7.5  I²C/MIPI I3C<sup>SM</sup> coexistence in LPS22HH ............................... 35
8  Register mapping ................................................................. 37
9  Register description ............................................................. 39
    9.1  INTERRUPT_CFG (0Bh) .................................................... 39
    9.2  THS_P_L (0Ch) ............................................................ 41
    9.3  THS_P_H (0Dh) ............................................................ 41
    9.4  IF_CTRL (0Eh) ............................................................ 42
    9.5  WHO_AM_I (0Fh) .......................................................... 42
    9.6  CTRL_REG1 (10h) ......................................................... 43
    9.7  CTRL_REG2 (11h) ......................................................... 45
    9.8  CTRL_REG3 (12h) ......................................................... 47
    9.9  FIFO_CTRL (13h) ......................................................... 48
    9.10 FIFO_WTM (14h) .......................................................... 49
    9.11 REF_P_L (15h) ............................................................ 49
    9.12 REF_P_H (16h) ............................................................ 49
    9.13 RPDS_L (18h) ............................................................. 50
    9.14 RPDS_H (19h) ............................................................. 50
    9.15 INT_SOURCE (24h) ....................................................... 50
    9.16 FIFO_STATUS1 (25h) .................................................... 51
    9.17 FIFO_STATUS2 (26h) .................................................... 51
    9.18 STATUS (27h) ............................................................. 51
    9.19 PRESS_OUT_XL (28h) ................................................... 52
    9.20 PRESS_OUT_L (29h) ..................................................... 52
    9.21 PRESS_OUT_H (2Ah) ..................................................... 52
9.22 TEMP_OUT_L (2Bh) ................................................. 53
9.23 TEMP_OUT_H (2Ch) ............................................. 53
9.24 FIFO_DATA_OUT_PRESS_XL (78h) ............................. 53
9.25 FIFO_DATA_OUT_PRESS_L (79h) ............................... 53
9.26 FIFO_DATA_OUT_PRESS_H (7Ah) .............................. 54
9.27 FIFO_DATA_OUT_TEMP_L (7Bh) ................................. 54
9.28 FIFO_DATA_OUT_TEMP_H (7Ch) ................................. 54

10  Package information ..................................................... 55
10.1 HLGA-10L package information ................................. 55
10.2 HLGA-10L packing information ................................. 56

11  Revision history ......................................................... 58
List of tables

Table 1. Device summary ................................................................. 1
Table 2. Pin description ................................................................. 8
Table 3. Pressure and temperature sensor characteristics ......................... 9
Table 4. Electrical characteristics .................................................. 10
Table 5. DC characteristics ............................................................ 10
Table 6. SPI slave timing values ..................................................... 11
Table 7. I²C slave timing values ...................................................... 12
Table 8. Absolute maximum ratings .................................................. 13
Table 9. Serial interface pin description ........................................... 26
Table 10. I²C terminology ............................................................... 26
Table 11. SAD+Read/Write patterns .................................................. 27
Table 12. Transfer when master is writing one byte to slave ....................... 27
Table 13. Transfer when master is writing multiple bytes to slave ................ 28
Table 14. Transfer when master is receiving (reading) one byte of data from slave 28
Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave 28
Table 16. MIPI I3C™ CCC commands ............................................... 33
Table 17. Registers address map ...................................................... 37
Table 18. Output data rate bit configurations ..................................... 43
Table 19. Low-pass filter configurations ........................................... 44
Table 20. RMS noise and power consumption ..................................... 46
Table 21. Interrupt configurations ................................................... 47
Table 22. FIFO mode selection ......................................................... 48
Table 23. Reel dimensions for carrier tape of HLGA-10L package ................ 57
Table 24. Document revision history ................................................ 58
## List of figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1.</td>
<td>Device architecture block diagram</td>
<td>7</td>
</tr>
<tr>
<td>Figure 2.</td>
<td>Digital logic</td>
<td>7</td>
</tr>
<tr>
<td>Figure 3.</td>
<td>Pin connections (bottom view)</td>
<td>8</td>
</tr>
<tr>
<td>Figure 4.</td>
<td>SPI slave timing diagram</td>
<td>11</td>
</tr>
<tr>
<td>Figure 5.</td>
<td>I²C slave timing diagram</td>
<td>12</td>
</tr>
<tr>
<td>Figure 6.</td>
<td>Pressure readings</td>
<td>15</td>
</tr>
<tr>
<td>Figure 7.</td>
<td>Temperature readings</td>
<td>16</td>
</tr>
<tr>
<td>Figure 8.</td>
<td>Bypass mode</td>
<td>18</td>
</tr>
<tr>
<td>Figure 9.</td>
<td>FIFO mode</td>
<td>19</td>
</tr>
<tr>
<td>Figure 10.</td>
<td>Continuous (Dynamic-Stream) mode</td>
<td>20</td>
</tr>
<tr>
<td>Figure 11.</td>
<td>Bypass-to-FIFO mode</td>
<td>21</td>
</tr>
<tr>
<td>Figure 12.</td>
<td>Bypass-to-Continuous (Dynamic-Stream) mode</td>
<td>22</td>
</tr>
<tr>
<td>Figure 13.</td>
<td>Continuous (Dynamic-Stream)-to-FIFO mode</td>
<td>23</td>
</tr>
<tr>
<td>Figure 14.</td>
<td>LPS22HH electrical connections (top view)</td>
<td>24</td>
</tr>
<tr>
<td>Figure 15.</td>
<td>LPS22HH power-off sequence</td>
<td>25</td>
</tr>
<tr>
<td>Figure 16.</td>
<td>Read and write protocol</td>
<td>29</td>
</tr>
<tr>
<td>Figure 17.</td>
<td>SPI read protocol</td>
<td>30</td>
</tr>
<tr>
<td>Figure 18.</td>
<td>Multiple byte SPI read protocol (2-byte example)</td>
<td>30</td>
</tr>
<tr>
<td>Figure 19.</td>
<td>SPI write protocol</td>
<td>31</td>
</tr>
<tr>
<td>Figure 20.</td>
<td>Multiple byte SPI write protocol (2-byte example)</td>
<td>31</td>
</tr>
<tr>
<td>Figure 21.</td>
<td>SPI read protocol in 3-wire mode</td>
<td>32</td>
</tr>
<tr>
<td>Figure 22.</td>
<td>I²C and MIPI I3C\textsuperscript{SM} both active (INT_DRDY pin not connected)</td>
<td>35</td>
</tr>
<tr>
<td>Figure 23.</td>
<td>Only MIPI I3C\textsuperscript{SM} active (INT_DRDY pin connected to VDD_IO)</td>
<td>36</td>
</tr>
<tr>
<td>Figure 24.</td>
<td>“Threshold-based” interrupt event</td>
<td>40</td>
</tr>
<tr>
<td>Figure 25.</td>
<td>Interrupt events on INT_DRDY pin</td>
<td>47</td>
</tr>
<tr>
<td>Figure 26.</td>
<td>HLGA-10L (2.0 x 2.0 x 0.73 mm typ.) package outline and mechanical dimensions</td>
<td>55</td>
</tr>
<tr>
<td>Figure 27.</td>
<td>Carrier tape information for HLGA-10L package</td>
<td>56</td>
</tr>
<tr>
<td>Figure 28.</td>
<td>HLGA-10L package orientation in carrier tape</td>
<td>56</td>
</tr>
<tr>
<td>Figure 29.</td>
<td>Reel information for carrier tape of HLGA-10L package</td>
<td>57</td>
</tr>
</tbody>
</table>
# Block diagrams

**Figure 1. Device architecture block diagram**

**Figure 2. Digital logic**
2 Pin description

Figure 3. Pin connections (bottom view)

Table 2. Pin description

<table>
<thead>
<tr>
<th>Pin number</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vdd_IO</td>
<td>Power supply for I/O pins</td>
</tr>
<tr>
<td>2</td>
<td>SCL</td>
<td>I²C / MIPI I3C℠ serial clock (SCL)</td>
</tr>
<tr>
<td></td>
<td>SPC</td>
<td>SPI serial port clock (SPC)</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>Connect to GND</td>
</tr>
<tr>
<td>4</td>
<td>SDA</td>
<td>I²C / MIPI I3C℠ serial data (SDA)</td>
</tr>
<tr>
<td></td>
<td>SDI</td>
<td>4-wire SPI serial data input (SDI)</td>
</tr>
<tr>
<td></td>
<td>SDI/SDO</td>
<td>3-wire serial data input/output (SDI/SDO)</td>
</tr>
<tr>
<td>5</td>
<td>SDO</td>
<td>4-wire SPI serial data output (SDO)</td>
</tr>
<tr>
<td></td>
<td>SA0</td>
<td>I²C least significant bit of the device address (SA0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MIPI I3C℠ least significant bit of the static address (SA0)</td>
</tr>
<tr>
<td>6</td>
<td>CS</td>
<td>SPI enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I²C and MIPI I3C℠ / SPI mode selection (1: SPI idle mode / I²C and MIPI I3C℠ communication enabled; 0: SPI communication mode / I²C and MIPI I3C℠ disabled)</td>
</tr>
<tr>
<td>7</td>
<td>INT_DRDY</td>
<td>Interrupt or Data-Ready</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>0 V supply</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>0 V supply</td>
</tr>
<tr>
<td>10</td>
<td>VDD</td>
<td>Power supply</td>
</tr>
</tbody>
</table>
3  Mechanical and electrical specifications

3.1  Mechanical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ. (1)</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTop</td>
<td>Operating temperature range</td>
<td></td>
<td>-40</td>
<td>+85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>P_top</td>
<td>Operating pressure range</td>
<td></td>
<td>260</td>
<td>1260</td>
<td></td>
<td>hPa</td>
</tr>
<tr>
<td>P_bits</td>
<td>Pressure output data</td>
<td></td>
<td>24</td>
<td></td>
<td></td>
<td>bits</td>
</tr>
<tr>
<td>Psens</td>
<td>Pressure sensitivity</td>
<td></td>
<td>4096</td>
<td></td>
<td></td>
<td>LSB/ hPa</td>
</tr>
<tr>
<td>P_AccRel</td>
<td>Relative accuracy over pressure (2)</td>
<td>P = 800 - 1100 hPa</td>
<td>±0.025</td>
<td></td>
<td></td>
<td>hPa</td>
</tr>
<tr>
<td>P_AccT</td>
<td>Absolute accuracy over temperature</td>
<td>P_op, T = -20 to 80°C</td>
<td>±0.5</td>
<td></td>
<td></td>
<td>hPa</td>
</tr>
<tr>
<td>P_noise</td>
<td>RMS pressure sensing noise (3)</td>
<td>with embedded filter and at T = 25 °C</td>
<td>0.0065</td>
<td></td>
<td></td>
<td>hPa RMS</td>
</tr>
<tr>
<td>ODR_Pres</td>
<td>Pressure output data rate (4)</td>
<td></td>
<td>1</td>
<td>10</td>
<td>100</td>
<td>Hz</td>
</tr>
<tr>
<td>TCO</td>
<td>Temperature coefficient offset</td>
<td>P = 660 ~ 1160 hPa, T = -20 ~ +65 °C</td>
<td>±0.65</td>
<td></td>
<td></td>
<td>Pa/°C</td>
</tr>
<tr>
<td>P_longterm</td>
<td>Pressure accuracy, long-term stability (5)</td>
<td></td>
<td>±0.33</td>
<td></td>
<td></td>
<td>hPa/year</td>
</tr>
<tr>
<td>P_drift</td>
<td>Soldering drift</td>
<td></td>
<td>±0.5</td>
<td></td>
<td></td>
<td>hPa</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ. (1)</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_top</td>
<td>Operating temperature range</td>
<td>-40</td>
<td>+85</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>T_sens</td>
<td>Temperature sensitivity</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>LSB/°C</td>
</tr>
<tr>
<td>T_acc</td>
<td>Temperature absolute accuracy</td>
<td>T = 0 to 80°C</td>
<td>±1.5</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>ODR_T</td>
<td>Output temperature data rate</td>
<td></td>
<td>1</td>
<td>10</td>
<td>100</td>
<td>Hz</td>
</tr>
</tbody>
</table>

Table 3. Pressure and temperature sensor characteristics
3.2 Electrical characteristics

VDD = 1.8 V, T = 25 °C, unless otherwise noted.

Table 4. Electrical characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ. (1)</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply voltage</td>
<td></td>
<td>1.7</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Vdd_IO</td>
<td>IO supply voltage</td>
<td></td>
<td>1.7</td>
<td>Vdd+0.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Idd</td>
<td>Supply current</td>
<td>@ ODR 1 Hz</td>
<td>4</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOW_NOISE_EN = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>@ ODR 1 Hz</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LOW_NOISE_EN = 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IddPdn</td>
<td>Supply current in</td>
<td></td>
<td>0.9</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>power-down mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Typical specifications are not guaranteed.

Table 5. DC characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC input characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vil</td>
<td>Low-level input voltage</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(Schmitt buffer)</td>
<td></td>
<td></td>
<td></td>
<td>Vdd_IO</td>
<td></td>
</tr>
<tr>
<td>Vih</td>
<td>High-level input voltage</td>
<td>-</td>
<td>0.8</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(Schmitt buffer)</td>
<td></td>
<td>Vdd_IO</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC output characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vol</td>
<td>Low-level output voltage</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>Voh</td>
<td>High-level output voltage</td>
<td>Vdd_IO - 0.2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>
3.3 Communication interface characteristics

3.3.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value(^{(1)})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{C}(SPC)</td>
<td>SPI clock cycle</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>f_{C}(SPC)</td>
<td>SPI clock frequency</td>
<td>10(^{(2)}) MHz</td>
<td></td>
</tr>
<tr>
<td>t_{SU}(CS)</td>
<td>CS setup time</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>t_{H}(CS)</td>
<td>CS hold time</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>t_{SU}(SI)</td>
<td>SDI input setup time</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>t_{H}(SI)</td>
<td>SDI input hold time</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>t_{V}(SO)</td>
<td>SDO valid output time</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>t_{H}(SO)</td>
<td>SDO output hold time</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>t_{DIS}(SO)</td>
<td>SDO output disable time</td>
<td>50</td>
<td></td>
</tr>
</tbody>
</table>

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

2. Recommended to set max SPI clock 8 MHz to ≤50 Hz ODR.

Figure 4. SPI slave timing diagram

Note: Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both ports.
3.3.2  I²C - inter-IC control interface

Subject to general operating conditions for Vdd and $T_{OP}$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter (1)</th>
<th>I²C standard mode(1)</th>
<th>I²C fast mode(1)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{(SCL)}$</td>
<td>SCL clock frequency</td>
<td>0</td>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td>$t_{w(SCLL)}$</td>
<td>SCL clock low time</td>
<td>0.0047</td>
<td>1.3</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{w(SCLH)}$</td>
<td>SCL clock high time</td>
<td>0.040</td>
<td>0.6</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{su(SDA)}$</td>
<td>SDA setup time</td>
<td>0.0250</td>
<td>0.0345</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{h(SDA)}$</td>
<td>SDA data hold time</td>
<td>0.0045</td>
<td>0.009</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{h(ST)}$</td>
<td>START condition hold time</td>
<td>0.004</td>
<td>0.006</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{su(SR)}$</td>
<td>Repeated START condition setup time</td>
<td>0.0047</td>
<td>0.006</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{su(SP)}$</td>
<td>STOP condition setup time</td>
<td>0.004</td>
<td>0.006</td>
<td>μs</td>
</tr>
<tr>
<td>$t_{w(SP-SR)}$</td>
<td>Bus free time between STOP and START condition</td>
<td>0.0047</td>
<td>0.013</td>
<td></td>
</tr>
</tbody>
</table>

1. Data based on standard I²C protocol requirement, not tested in production.

**Figure 5. I²C slave timing diagram**

**Note:** Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.
3.4 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Ratings</th>
<th>Maximum value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>Supply voltage</td>
<td>-0.3 to 4.8</td>
<td>V</td>
</tr>
<tr>
<td>Vdd_IO</td>
<td>I/O pins supply voltage</td>
<td>-0.3 to 4.8</td>
<td>V</td>
</tr>
<tr>
<td>Vin</td>
<td>Input voltage on any control pin</td>
<td>-0.3 to Vdd_IO +0.3</td>
<td>V</td>
</tr>
<tr>
<td>P</td>
<td>Overpressure</td>
<td>2</td>
<td>MPa</td>
</tr>
<tr>
<td>T_{STG}</td>
<td>Storage temperature range</td>
<td>-40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic discharge protection</td>
<td>2.5 (HBM)</td>
<td>kV</td>
</tr>
</tbody>
</table>

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.
4 Functionality

The LPS22HH is a high-resolution, digital output pressure sensor packaged in an HLGA full-mold package. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach, and an IC interface which communicates a digital signal from the sensing element to the application.

4.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

4.2 IC interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/MIPI I3C℠/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS22HH features a Data-Ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

4.3 Factory calibration

The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation which allows the device to be used without requiring any further calibration.
4.4 Interpreting pressure readings

The pressure data are stored in 3 registers: PRESS_OUT_H (2Ah), PRESS_OUT_L (29h), and PRESS_OUT_XL (28h). The value is expressed as a 24-bit signed number (in 2's complement).

To obtain the pressure in hPa, take the complete 24-bit word and then divide by the sensitivity 4096 LSB/hPa. This same interpretation is applied to pressure readings when FIFO is enabled and the pressure data are stored in 3 registers: FIFO_DATA_OUT_PRESS_XL (78h), FIFO_DATA_OUT_PRESS_L (79h), and FIFO_DATA_OUT_PRESS_H (7Ah).

![Figure 6. Pressure readings](image)

Equation 1

Pressure Value (LSB) = PRESS_OUT_H (2Ah) & PRESS_OUT_L (29h) & PRESS_OUT_XL (28h)

= 3FF58Dh = 4191629 LSB (signed decimal)

Equation 2

Pressure (hPa) = \frac{\text{Pressure Value (LSB)}}{4096 \text{ LSB/hPa}} = 1023.3 \text{ hPa}
4.5 Interpreting temperature readings

The temperature data are stored in 2 registers: `TEMP_OUT_H (2Ch)` and `TEMP_OUT_L (2Bh)`.

The value is expressed as 2's complement. To obtain the temperature in °C, take the two’s complement of the complete 16-bit word and then divide by the sensitivity 100 LSB/°C. This same interpretation is applied to temperature readings when FIFO is enabled and the temperature data are stored in 2 registers: `FIFO_DATA_OUT_TEMP_H (7Ch)` and `FIFO_DATA_OUT_TEMP_L (7Bh)`.

![Figure 7. Temperature readings](image)

Temperature Value (LSB) = `TEMP_OUT_H (2Ch) & TEMP_OUT_L (2Bh)`

\[
= 09C4 = 2500 \text{ LSB (decimal signed)}
\]

Temperature (°C) = \[
\frac{\text{Temperature Value (LSB)}}{\text{Sensitivity}} = \frac{2500 \text{ LSB}}{100 \text{ LSB/°C}} = 25.00°C
\]
The LPS22HH embeds 128 slots of 40-bit data FIFO to store the pressure and temperature output values. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to six different modes:

- Bypass mode
- FIFO mode
- Continuous (Dynamic-Stream) mode
- Continuous (Dynamic-Stream)-to-FIFO mode
- Bypass-to-Continuous (Dynamic-Stream)
- Bypass-to-FIFO mode

The FIFO buffer is enabled when a configuration different from all bits '0' are written in \( \text{FIFO\_CTRL (13h)} \) and each mode is selected by the TRIG\_MODES bit and F\_MODE[1:0] bits in \( \text{FIFO\_CTRL (13h)} \). Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the \( \text{FIFO\_STATUS1 (25h)} \) and \( \text{FIFO\_STATUS2 (26h)} \) registers and can be set to generate dedicated interrupts on the INT\_DRDY pad using the \( \text{CTRL\_REG3 (12h)} \) register.

\( \text{FIFO\_STATUS2 (26h)} \) (FIFO\_WTM\_IA) goes to '1' when the number of unread samples (\( \text{FIFO\_STATUS1 (25h)} \)(FSS[7:0])) is greater than or equal to WTM[6:0] in \( \text{FIFO\_WTM (14h)} \). If \( \text{FIFO\_WTM (14h)} \)(WTM[6:0]) is equal to 0, \( \text{FIFO\_STATUS2 (26h)} \) (FIFO\_WTM\_IA) stays at '0'.

\( \text{FIFO\_STATUS2 (26h)} \) (FIFO\_OVR\_IA) is equal to '1' if a FIFO slot is overwritten.

\( \text{FIFO\_STATUS1 (25h)} \)(FSS[7:0]) contains stored data levels of unread samples; when FSS[7:0] is equal to '00000000', FIFO is empty; when FSS[7:0] is equal to '10000000', FIFO is full and the unread samples are 128.
5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (13h)* (TRIG_MODES and F_MODE[1:0] = ‘000’ or ‘100’)), the FIFO is not operational and it remains empty.

Switching to Bypass mode is also used to reset the FIFO. Passing through Bypass mode is mandatory when switching between different FIFO buffer operating modes.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

**Figure 8. Bypass mode**
5.2 FIFO mode

In FIFO mode \(\text{FIFO_CTRL (13h)(TRIG_MODES and F_MODE[1:0] = '001')}\) data from the output \text{PRESS_OUT_XL (28h)}, \text{PRESS_OUT_L (29h)}, \text{PRESS_OUT_H (2Ah)}, \text{TEMP_OUT_L (2Bh)}, \text{and TEMP_OUT_H (2Ch)}\) are stored in the FIFO until it is full.

To reset FIFO content, in order to select Bypass mode the value '000' must be written in \text{FIFO_CTRL (13h)(TRIG_MODE & F_MODE[1:0])}. After this reset command it is possible to restart FIFO mode by writing the value '001' in \text{FIFO_CTRL (13h)(TRIG_MODE & F_MODE[1:0])}.

The FIFO buffer memorizes 128 levels of data, but the depth of the FIFO can be resized/reduced by setting the \text{FIFO_CTRL (13h)(STOP_ON_WTM)} bit. If the \text{STOP_ON_WTM} bit is set to '1', FIFO depth is limited to \text{FIFO_WTM (14h)(WTM[6:0])} data.

![Figure 9. FIFO mode](image-url)
5.3 Continuous (Dynamic-Stream) mode

In Continuous (Dynamic-Stream) mode (`FIFO_CTRL (13h)` (TRIG_MODES and F_MODE[1:0] = ‘01’) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way, the number of new data available in FIFO does not depend on the previous read.

In Continuous (Dynamic-Stream) mode `FIFO_STATUS1 (25h)` (FSS[7:0]) is the number of new pressure and temperature samples available in the FIFO buffer.

Continuous (Dynamic-Stream) is intended to be used to read `FIFO_STATUS1 (25h)` (FSS[7:0]) samples when it is not possible to guarantee reading data within 1/OVRD time period.

Also, a FIFO threshold interrupt on the INT_DRDY pad through `CTRL_REG3 (12h)` (INT_F_WTM) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 10. Continuous (Dynamic-Stream) mode
5.4 **Bypass-to-FIFO mode**

In Bypass-to-FIFO mode *(FIFO_CTRL (13h))(TRIG_MODES and F_MODE[1:0] = ‘101’)*, FIFO behavior switches when the *INT_SOURCE (24h)(IA)* bit rises for the first time. When the *INT_SOURCE (24h)(IA)* bit is equal to ‘0’, FIFO behaves like in Bypass mode. Once the *INT_SOURCE (24h)(IA)* bit rises to ‘1’, FIFO behavior switches and keeps behaving like in FIFO mode.

An interrupt generator has to be set to the desired configuration through *INTERRUPT_CFG*(0Bh).

![Figure 11. Bypass-to-FIFO mode](image_url)
5.5 Bypass-to-Continuous (Dynamic-Stream) mode

In Bypass-to-Continuous (Dynamic-Stream) mode \((FIFO\_CTRL\ (13h)\text{(TRIG\_MODES and F\_MODE[1:0] = ‘110’)})\), FIFO operates in Bypass mode until it switches to Continuous (Dynamic-Stream) mode behavior when \(INT\_SOURCE\ (24h)\text{(IA)}\) rises to ‘1’, then FIFO behavior keeps behaving like in Continuous (Dynamic-Stream) mode.

An interrupt generator has to be set to the desired configuration through \(INTERRUPT\_CFG\ (0Bh)\).

Figure 12. Bypass-to-Continuous (Dynamic-Stream) mode
5.6 Continuous (Dynamic-Stream)-to-FIFO mode

In Continuous (Dynamic-Stream)-to-FIFO mode (FIFO_CTRL (13h)(TRIG_MODES and F_MODE[1:0] = ‘111’), data are stored in FIFO and FIFO operates in Continuous (Dynamic-Stream) mode behavior until it switches to FIFO mode behavior when INT_SOURCE (24h)(IA) rises to ‘1’.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

![Figure 13. Continuous (Dynamic-Stream)-to-FIFO mode](image)

5.7 Retrieving data from FIFO

FIFO data is read through FIFO_DATA_OUT_PRESS (78h, 79h and 7Ah) and FIFO_DATA_OUT_TEMP (7Bh, 7Ch).

The read address is automatically updated by the device and it rolls back to 78h when register 7Ch is reached. In order to read all FIFO levels in a multiple byte read, 640 bytes (5 output registers by 128 levels) must be read.
6 Application hints

Figure 14. LPS22HH electrical connections (top view)

The device power supply must be provided through the VDD line; a power supply decoupling capacitor C1 (100 nF) must be placed as near as possible to the supply pads of the device. The C1 capacitor can be tied to VDD and VDDIO, but it is recommended to use 2 capacitors, one on each VDD and VDDIO line, in case VDD are VDDIO are separate. Depending on the application, an additional capacitor of 4.7 μF could be placed on VDD line.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C, MIPI I3C℠, SPI interface. When using the I²C and MIPI I3C℠, CS must be tied to Vdd_IO.

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to Figure 14). It is possible to remove VDD while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

Note: To guarantee proper power-off of the device, it is recommended to maintain the duration of the VDD line to GND for at least 10 ms.
6.1 Soldering information

The HLGA package is compliant with the ECOPACK® standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.
7 Digital interfaces

7.1 Serial interfaces

The registers embedded in the LPS22HH may be accessed through either the I²C, MIPI I3C℠ or SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I²C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

### Table 9. Serial interface pin description

<table>
<thead>
<tr>
<th>Pin name</th>
<th>Pin description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CS</td>
<td>SPI enable</td>
</tr>
<tr>
<td></td>
<td>I²C/SPI mode selection</td>
</tr>
<tr>
<td></td>
<td>(1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)</td>
</tr>
<tr>
<td>SCL/SPC</td>
<td>I²C serial clock (SCL)</td>
</tr>
<tr>
<td></td>
<td>SPI serial port clock (SPC)</td>
</tr>
<tr>
<td>SDA</td>
<td>I²C serial data (SDA)</td>
</tr>
<tr>
<td>SDI</td>
<td>4-wire SPI serial data input (SDI)</td>
</tr>
<tr>
<td>SDI/SDO</td>
<td>3-wire serial data input/output (SDI/SDO)</td>
</tr>
<tr>
<td>SDO</td>
<td>4-wire SPI serial data output (SDO)</td>
</tr>
<tr>
<td>SAO</td>
<td>I²C less significant bit of the device address (SA0)</td>
</tr>
</tbody>
</table>

7.2 I²C serial interface (CS = high)

The LPS22HH I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in Table 10.

### Table 10. I²C terminology

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter</td>
<td>The device which sends data to the bus</td>
</tr>
<tr>
<td>Receiver</td>
<td>The device which receives data from the bus</td>
</tr>
<tr>
<td>Master</td>
<td>The device which initiates a transfer, generates clock signals and terminates a transfer</td>
</tr>
<tr>
<td>Slave</td>
<td>The device addressed by the master</td>
</tr>
</tbody>
</table>

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines have to be connected to Vdd_IO through pull-up resistors.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.
7.2.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the master has transmitted this, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The 7-bit slave address (SAD) associated to the LPS22HH is 101110xb. The SDO/SA0 pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to voltage supply, LSb is ‘1’ (7-bit address 1011101b=5Dh), otherwise if the SA0 pad is connected to ground, the LSb value is ‘0’ (7-bit address 1011100b=5Ch). This solution permits connecting and addressing two different LPS22HH devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge has been returned (SAK), an 8-bit sub-address will be transmitted (SUB): the 7 LSB represent the actual register address while the MSB has no meaning. The IF_ADD_INC bit in CTRL_REG2 (11h) enables sub-address auto increment (IF_ADD_INC is ’1’ by default), so if IF_ADD_INC = ’1’ the SUB (sub-address) will be automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. Table 11 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

<table>
<thead>
<tr>
<th>Command</th>
<th>SAD[6:1]</th>
<th>SAD[0] = SA0</th>
<th>R/W</th>
<th>SAD+R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>101110</td>
<td>0</td>
<td>1</td>
<td>10111001 (B9h)</td>
</tr>
<tr>
<td>Write</td>
<td>101110</td>
<td>0</td>
<td>0</td>
<td>10111000 (B8h)</td>
</tr>
<tr>
<td>Read</td>
<td>101110</td>
<td>1</td>
<td>1</td>
<td>10111011 (BBh)</td>
</tr>
<tr>
<td>Write</td>
<td>101110</td>
<td>1</td>
<td>0</td>
<td>10111010 (BAh)</td>
</tr>
</tbody>
</table>

Table 12. Transfer when master is writing one byte to slave

<table>
<thead>
<tr>
<th>Master</th>
<th>ST</th>
<th>SAD + W</th>
<th>SUB</th>
<th>DATA</th>
<th>SP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slave</td>
<td></td>
<td>SAK</td>
<td>SAK</td>
<td>SAK</td>
<td></td>
</tr>
</tbody>
</table>
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other functions, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function), the data line must be kept HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

<table>
<thead>
<tr>
<th>Table 13. Transfer when master is writing multiple bytes to slave</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master</td>
</tr>
<tr>
<td>Slave</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 14. Transfer when master is receiving (reading) one byte of data from slave</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master</td>
</tr>
<tr>
<td>Slave</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master</td>
</tr>
<tr>
<td>Slave</td>
</tr>
</tbody>
</table>
7.3 SPI bus interface (CS = low)

The LPS22HH SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 4 wires: CS, SPC, SDI and SDO.

**Figure 16. Read and write protocol**

CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. SPC is the serial port clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the serial port data input and output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the read register and write register commands are completed in 16 clock pulses or multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of CS.

**bit 0:** RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive SDO at the start of bit 8.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the IF_ADD_INC bit is 0, the address used to read/write data remains the same for every block. When the IF_ADD_INC bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of SDI and SDO remain unchanged.
7.3.1 SPI read

The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0**: READ bit. The value is 1.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

**bit 16-**: data DO(...-8). Further data in multiple byte reads.

---

**Figure 17. SPI read protocol**

CS
SPC
SDI
SDO

**Figure 18. Multiple byte SPI read protocol (2-byte example)**

CS
SPC
SDI
SDO
7.3.2 SPI write

The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0**: WRITE bit. The value is 0.

**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

**bit 16-...**: data DI(...-8). Further data in multiple byte writes.

---

**Figure 19. SPI write protocol**

---

**Figure 20. Multiple byte SPI write protocol (2-byte example)**
7.3.3  SPI read in 3-wire mode

A 3-wire mode is entered by setting bit SIM to ‘1’ (SPI serial interface mode selection) in \textit{CTRL\_REG1 (10h)}.

![Figure 21. SPI read protocol in 3-wire mode](image)

The SPI read command is performed with 16 clock pulses:

\textit{bit 0}: READ bit. The value is 1.

\textit{bit 1-7}: address AD(6:0). This is the address field of the indexed register.

\textit{bit 8-15}: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.
7.4 MIPI I3C<sup>SM</sup> slave interface

The LPS22HH interface includes a MIPI I3C<sup>SM</sup> SDR only slave interface with MIPI I3C<sup>SM</sup> SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt and hot-join requests

7.4.1 MIPI I3C<sup>SM</sup> CCC supported commands

The list of MIPI I3C<sup>SM</sup> CCC commands supported by the device is detailed in the following table.

<table>
<thead>
<tr>
<th>Command</th>
<th>Command code</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENEC</td>
<td>0x80 / 0x00</td>
<td>0x00 / 0x08</td>
<td>Slave activity control (direct and broadcast)</td>
</tr>
<tr>
<td>RSTDAA</td>
<td>0x86 / 0x06</td>
<td>0x00 / 0x08</td>
<td>Reset the assigned dynamic address (direct and broadcast)</td>
</tr>
<tr>
<td>DISEC</td>
<td>0x81 / 0x01</td>
<td>0x00 / 0x08</td>
<td>Slave activity control (direct and broadcast)</td>
</tr>
<tr>
<td>ENTAS0</td>
<td>0x82 / 0x02</td>
<td>0x00 / 0x08</td>
<td>Enter activity state (direct and broadcast)</td>
</tr>
<tr>
<td>ENTAS1</td>
<td>0x83 / 0x03</td>
<td>0x00 / 0x08</td>
<td>Enter activity state (direct and broadcast)</td>
</tr>
<tr>
<td>ENTAS2</td>
<td>0x84 / 0x04</td>
<td>0x00 / 0x08</td>
<td>Enter activity state (direct and broadcast)</td>
</tr>
<tr>
<td>ENTAS3</td>
<td>0x85 / 0x05</td>
<td>0x00 / 0x08</td>
<td>Enter activity state (direct and broadcast)</td>
</tr>
<tr>
<td>SETMWL</td>
<td>0x89 / 0x08</td>
<td>0x00 / 0x08</td>
<td>Define maximum write length during private write (direct and broadcast)</td>
</tr>
<tr>
<td>SETMRL</td>
<td>0x8A / 0x09</td>
<td>0x00 / 0x10 / 0x04</td>
<td>Define maximum read length during private read (direct and broadcast)</td>
</tr>
<tr>
<td>SETDASA</td>
<td>0x87</td>
<td></td>
<td>Assign dynamic address using static address (0x5C / 0x5D depending on the SDO level)</td>
</tr>
<tr>
<td>SETNEWDA</td>
<td>0x88</td>
<td></td>
<td>Change dynamic address</td>
</tr>
<tr>
<td>GETMWL</td>
<td>0x8B</td>
<td>0x00 / 0x08</td>
<td>Get maximum write length during private write</td>
</tr>
<tr>
<td>GETMRL</td>
<td>0x8C</td>
<td>0x00 / 0x10 / 0x04</td>
<td>Get maximum read length during private read</td>
</tr>
</tbody>
</table>
Table 16. MIPI I3C℠ CCC commands (continued)

<table>
<thead>
<tr>
<th>Command</th>
<th>Command code</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GETPID</td>
<td>0x8D</td>
<td>0x02&lt;br&gt;0x08&lt;br&gt;0x00&lt;br&gt;0xB3&lt;br&gt;0x00&lt;br&gt;0x00</td>
<td>Device ID register</td>
</tr>
<tr>
<td>GETBCR</td>
<td>0x8E</td>
<td>0x07</td>
<td>Bus characteristics register</td>
</tr>
<tr>
<td>GETDCR</td>
<td>0x8F</td>
<td>0x62</td>
<td>DCR</td>
</tr>
<tr>
<td>GETSTATUS</td>
<td>0x90</td>
<td>0x00&lt;br&gt;0x20</td>
<td>Status register</td>
</tr>
<tr>
<td>GETMXDS</td>
<td>0x94</td>
<td>0x00</td>
<td>Return max data speed</td>
</tr>
<tr>
<td>GETXTIME</td>
<td>0x99</td>
<td>0x07&lt;br&gt;0x04&lt;br&gt;0x0A&lt;br&gt;0x64</td>
<td>Get exchange time information</td>
</tr>
</tbody>
</table>
7.5 **I²C/MIPI I3C\textsuperscript{SM} coexistence in LPS22HH**

In the LPS22HH, the SDA and SCL lines are common to both I²C and MIPI I3C\textsuperscript{SM}. The I²C bus requires anti-spike filters on the SDA and SCL pins that are not compatible with MIPI I3C\textsuperscript{SM} timing.

The device can be connected to both I²C and MIPI I3C\textsuperscript{SM} or only to the MIPI I3C\textsuperscript{SM} bus depending on the connection of the INT1 pin when the device is powered up:

- **INT\_DRDY pin floating (internal pull-down):** I²C/MIPI I3C\textsuperscript{SM} both active, see **Figure 22**
  - I²C case: INT\_DRDY pin is by default an input with pull-down. If I²C is used, INT\_DRDY must be left unconnected or eventually pulled down during device initialization. After power-on, during device configuration, the INT\_DRDY pin can be programmed as an interrupt output pin and it is recommended to set bit I3C\_disable to ‘1’.
  - I3C case: INT\_DRDY pin is by default an input with pull-down. If I3C is used and the INT\_DRDY pin is unconnected, dynamic address assignment must be performed using I²C Fast Mode Plus Timing (max 1 MHz clock). After dynamic address assignment, I3C can be used in full speed mode.

- **INT\_DRDY pin connected to VDD\_IO:** only MIPI I3C\textsuperscript{SM} active, see **Figure 23**
  - Only I3C: INT\_DRDY pin is by default an input with pull-down. If INT\_DRDY is set to Vdd\_IO, I3C slave is selected and device can be initialized at full speed through the SETDASA command. If the I3C bus is available for more than 10 msec and the device is not yet addressed, a hot join request is performed (SDA line kept to ground from slave) and the master must manage the request. After device address assignment, a private write can be performed to disconnect the INT\_DRDY pull-down.

**Figure 22. I²C and MIPI I3C\textsuperscript{SM} both active (INT\_DRDY pin not connected)**

---

1. Address assignment (SETDASA) must be performed with I²C Fast Mode Plus Timing. When the slave is addressed, the I²C slave is disabled and the timing is compatible with MIPI I3C\textsuperscript{SM} specifications.
Figure 23. Only MIPI I3C\textsuperscript{SM} active (INT\_DRDY pin connected to VDD\_IO)

1. When the slave is MIPI I3C\textsuperscript{SM} only, the I²C slave is always disabled. The address can be assigned using MIPI I3C\textsuperscript{SM} SDR timing.
### Table 17. Registers address map

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Register address</th>
<th>Default</th>
<th>Function and comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td></td>
<td>00 – 0A</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>INTERRUPT_CFG</td>
<td>R/W</td>
<td>0B</td>
<td>0000000000</td>
<td>Interrupt register</td>
</tr>
<tr>
<td>THS_P_L</td>
<td>R/W</td>
<td>0C</td>
<td>0000000000</td>
<td>Pressure threshold registers</td>
</tr>
<tr>
<td>THS_P_H</td>
<td>R/W</td>
<td>0D</td>
<td>0000000000</td>
<td>Pressure threshold registers</td>
</tr>
<tr>
<td>IF_CTRL</td>
<td>R/W</td>
<td>0E</td>
<td>0000000000</td>
<td>Interface control register</td>
</tr>
<tr>
<td>WHO_AM_I</td>
<td>R</td>
<td>0F</td>
<td>10110011</td>
<td>Who am I</td>
</tr>
<tr>
<td>CTRL_REG1</td>
<td>R/W</td>
<td>10</td>
<td>0000000000</td>
<td>Control registers</td>
</tr>
<tr>
<td>CTRL_REG2</td>
<td>R/W</td>
<td>11</td>
<td>0001000000</td>
<td>Control registers</td>
</tr>
<tr>
<td>CTRL_REG3</td>
<td>R/W</td>
<td>12</td>
<td>0000000000</td>
<td>Control registers</td>
</tr>
<tr>
<td>FIFO_CTRL</td>
<td>R/W</td>
<td>13</td>
<td>0000000000</td>
<td>FIFO configuration register</td>
</tr>
<tr>
<td>FIFO_WTM</td>
<td>R/W</td>
<td>14</td>
<td>0000000000</td>
<td>FIFO configuration register</td>
</tr>
<tr>
<td>REF_P_L</td>
<td>R</td>
<td>15</td>
<td>0000000000</td>
<td>Reference pressure registers</td>
</tr>
<tr>
<td>REF_P_H</td>
<td>R</td>
<td>16</td>
<td>0000000000</td>
<td>Reference pressure registers</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>17</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>RPDS_L</td>
<td>R/W</td>
<td>18</td>
<td>0000000000</td>
<td>Pressure offset registers</td>
</tr>
<tr>
<td>RPDS_H</td>
<td>R/W</td>
<td>19</td>
<td>0000000000</td>
<td>Pressure offset registers</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>1A-23</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>INT_SOURCE</td>
<td>R</td>
<td>24</td>
<td>Output</td>
<td>Interrupt register</td>
</tr>
<tr>
<td>FIFO_STATUS1</td>
<td>R</td>
<td>25</td>
<td>Output</td>
<td>FIFO status registers</td>
</tr>
<tr>
<td>FIFO_STATUS2</td>
<td>R</td>
<td>26</td>
<td>Output</td>
<td>FIFO status registers</td>
</tr>
<tr>
<td>STATUS</td>
<td>R</td>
<td>27</td>
<td>Output</td>
<td>Status register</td>
</tr>
<tr>
<td>PRESSURE_OUT_XL</td>
<td>R</td>
<td>28</td>
<td>Output</td>
<td>Pressure output registers</td>
</tr>
<tr>
<td>PRESSURE_OUT_L</td>
<td>R</td>
<td>29</td>
<td>Output</td>
<td>Pressure output registers</td>
</tr>
<tr>
<td>PRESSURE_OUT_H</td>
<td>R</td>
<td>2A</td>
<td>Output</td>
<td>Pressure output registers</td>
</tr>
<tr>
<td>TEMP_OUT_L</td>
<td>R</td>
<td>2B</td>
<td>Output</td>
<td>Temperature output registers</td>
</tr>
<tr>
<td>TEMP_OUT_H</td>
<td>R</td>
<td>2C</td>
<td>Output</td>
<td>Temperature output registers</td>
</tr>
<tr>
<td>Reserved</td>
<td></td>
<td>2D - 77</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>FIFO_DATA_OUT_PRESS_XL</td>
<td>R</td>
<td>78</td>
<td>Output</td>
<td>FIFO pressure output registers</td>
</tr>
<tr>
<td>FIFO_DATA_OUT_PRESS_L</td>
<td>R</td>
<td>79</td>
<td>Output</td>
<td>FIFO pressure output registers</td>
</tr>
<tr>
<td>FIFO_DATA_OUT_PRESS_H</td>
<td>R</td>
<td>7A</td>
<td>Output</td>
<td>FIFO pressure output registers</td>
</tr>
</tbody>
</table>
Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

### Table 17. Registers address map (continued)

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Register address</th>
<th>Default</th>
<th>Function and comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_DATA_OUT_TEMP_L</td>
<td>R</td>
<td>7B</td>
<td>Output</td>
<td>FIFO temperature output registers</td>
</tr>
<tr>
<td>FIFO_DATA_OUT_TEMP_H</td>
<td>R</td>
<td>7C</td>
<td>Output</td>
<td></td>
</tr>
</tbody>
</table>
9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

9.1 INTERRUPT_CFG (0Bh)

Interrupt mode for pressure acquisition configuration (R/W)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUTOREFP</td>
<td>RESET_ARP</td>
<td>AUTOZERO</td>
<td>RESET AZ</td>
<td>DIFF EN</td>
<td>LIR</td>
<td>PLE</td>
<td>PHE</td>
</tr>
</tbody>
</table>

- **AUTOREFP**: Enable AUTOREFP function. Default value: 0 (0: normal mode; 1: AUTOREFP enabled)
- **RESET_ARP**: Reset AUTOREFP function. Default value: 0 (0: normal mode; 1: reset AUTOREFP function)
- **AUTOZERO**: Enable AUTOZERO function. Default value: 0 (0: normal mode; 1: AUTOZERO enabled)
- **RESET AZ**: Reset AUTOZERO function. Default value: 0 (0: normal mode; 1: reset AUTOZERO function)
- **DIFF EN**: Enable interrupt generation. Default value: 0 (0: interrupt generation disabled; 1: interrupt generation enabled)
- **LIR**: Latch interrupt request to the INT_SOURCE (24h) register. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
- **PLE**: Enable interrupt generation on pressure low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on pressure value lower than preset threshold)
- **PHE**: Enable interrupt generation on pressure high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on pressure value higher than preset threshold)

Referring to Figure 24: "Threshold-based" interrupt event, the LPS22HH can be set by the user to support the interrupt function when P_DIFF_IN (defined below) is higher or lower than the threshold value stored in THS_P_L (0Ch) and THS_P_H (0Dh).

It is enabled when the DIFF EN bit in INTERRUPT_CFG (0Bh) register is set to '1' and either PHE bit or PLE bit (or both bits) = '1'. Then, the differential pressure can be compared to a user-defined threshold stored in the 15-bit THS_P (0Ch and 0Dh) registers.

The threshold pressure value defined by the user is a 15-bit unsigned value in a 16-bit register composed of THS_P_L (0Ch) and THS_P_H (0Dh). The value is:

THS_P (15-bit unsigned) = Desired Interrupt threshold (hPa) x 16

The PHE and PLE bits in INTERRUPT_CFG (0Bh) enable the differential pressure interrupt generation on the positive or negative event respectively.

The differential interrupt must be used with AUTOREFP or AUTOZERO mode. Please refer to the application note (ANS209: Section 8. Interrupt modes) for further details.
Figure 24. “Threshold-based” interrupt event

To enable the AUTOZERO mode, the AUTOZERO bit must be set to ‘1’ and then the measured pressure value is used as the reference and stored in the register REF_P (REF_P_L (15h), REF_P_H (16h)). From this point on, the output pressure value (PRESS_OUT_XL (28h), PRESS_OUT_L (29h), PRESS_OUT_H (2Ah)) is updated with the difference between the measured pressure and REF_P.

- P_DIFF_IN = measured pressure - REF_P
- PRESS_OUT = measured pressure - REF_P

After the first conversion, the AUTOZERO bit is automatically set back to ‘0’. In order to return back to normal mode, the RESET_AZ bit in the INTERRUPT_CFG (0Bh) register has to be set to ‘1’. This also resets the content of the REF_P registers to 0.

AUTOREFP mode allows using the pressure differential for the generation of the interrupt keeping the output pressure registers PRESS_OUT (PRESS_OUT_XL (28h), PRESS_OUT_L (29h), PRESS_OUT_H (2Ah)) without comparing REF_P. If the AUTOREFP bit is set to ‘1’, the measured output pressure is used as the reference in the register REF_P (REF_P_L (15h), REF_P_H (16h)) for interrupt generation with following:

- P_DIFF_IN = measured pressure - REF_P

The output registers PRESS_OUT (28h, 29h and 2Ah) are not changed by REF_P and shows as follows.

- PRESS_OUT = measured pressure

After the first conversion, the AUTOREFP bit is automatically set to ‘0’. In order to return back to normal mode, the RESET_ARP bit has to be set to ‘1’.
9.2 **THS_P_L (0Ch)**

User-defined threshold value for pressure interrupt event (Least significant bits) (R/W)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>THS7</td>
<td>THS6</td>
<td>THS5</td>
<td>THS4</td>
<td>THS3</td>
<td>THS2</td>
<td>THS1</td>
<td>THS0</td>
</tr>
</tbody>
</table>

THS[7:0] This register contains the low part of threshold value for pressure interrupt generation. Default value: 00h

The threshold value for pressure interrupt generation is a 15-bit unsigned right-justified value composed of **THS_P_H (0Dh)** and **THS_P_L (0Ch)**. The value is expressed as:

\[
\text{THS}_P (15\text{-bit unsigned}) = \text{Desired interrupt threshold (hPa)} \times 16
\]

To enable the interrupt event based on this user-defined threshold, the DIFF_EN bit in **INTERRUPT_CFG (0Bh)** must be set to ‘1’, the PHE bit or PLE bit (or both bits) in **INTERRUPT_CFG (0Bh)** has to be enabled.

9.3 **THS_P_H (0Dh)**

User-defined threshold value for pressure interrupt event (Most significant bits) (R/W)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>THS14</td>
<td>THS13</td>
<td>THS12</td>
<td>THS11</td>
<td>THS10</td>
<td>THS9</td>
<td>THS8</td>
</tr>
</tbody>
</table>

THS[14:8] This register contains the high part of threshold value for pressure interrupt generation. Refer to **THS_P_L (0Ch)**. Default value: 00h
### 9.4 IF_CTRL (0Eh)

Interface control register (R/W)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>INT_EN_I3C: Enable INT1 pad with MIPI I3C. If the INT_EN_I3C bit is set, the INT1 pad is polarized as OUT. Default value: 0</td>
</tr>
<tr>
<td>6</td>
<td>SDA_PU_EN: Enable pull-up on the SDA pin. Default value: 0</td>
</tr>
<tr>
<td>5</td>
<td>SDO_PU_EN: Enable pull-up on the SDO pin. Default value: 0</td>
</tr>
<tr>
<td>4</td>
<td>PD_DIS_INT1: Disable pull down on the INT1 pin. Default value: 0</td>
</tr>
<tr>
<td>3</td>
<td>I3C_DISABLE: Disable MIPI I3C interface. Default value: 0</td>
</tr>
<tr>
<td>2</td>
<td>I2C_DISABLE: Disable I²C interface. Default value: 0</td>
</tr>
</tbody>
</table>

1. I3C_DISABLE bit disables the MIPI I3C communication protocol.
2. I2C_DISABLE bit disables the I²C interface, by default both SPI and I²C interfaces are enabled.

### 9.5 WHO_AM_I (0Fh)

Device Who am I

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
9.6 **CTRL_REG1 (10h)**

Control register 1 (R/W)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ODR2</td>
<td>ODR1</td>
<td>ODR0</td>
<td>EN_LPFP</td>
<td>LPFP_CFG</td>
<td>BDU</td>
<td>SIM</td>
</tr>
</tbody>
</table>

| ODR[2:0] | Output data rate selection. Default value: 000
| Refer to [Table 18](#) |
| EN_LPFP | Enable low-pass filter on pressure data when Continuous mode is used.
| Default value: 0
| (0: Low-pass filter disabled; 1: Low-pass filter enabled) |
| LPFP_CFG | LPFP_CFG: Low-pass configuration register. Default value: 0
| Refer to [Table 19](#) |
| BDU(1) | Block data update. Default value: 0
| (0: continuous update;
| 1: output registers not updated until MSB and LSB have been read) |
| SIM | SPI Serial Interface Mode selection. Default value: 0
| (0: 4-wire interface; 1: 3-wire interface) |

1. To guarantee the correct behavior of BDU feature, **PRESS_OUT_H (2Ah)** must be the last address read.

### Table 18. Output data rate bit configurations

<table>
<thead>
<tr>
<th>ODR[2:0]</th>
<th>Temperature, Pressure</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>One-shot</td>
</tr>
<tr>
<td>001</td>
<td>1 Hz</td>
</tr>
<tr>
<td>010</td>
<td>10 Hz</td>
</tr>
<tr>
<td>011</td>
<td>25 Hz</td>
</tr>
<tr>
<td>100</td>
<td>50 Hz</td>
</tr>
<tr>
<td>101</td>
<td>75 Hz</td>
</tr>
<tr>
<td>110(1)</td>
<td>100 Hz</td>
</tr>
<tr>
<td>111(1)</td>
<td>200 Hz</td>
</tr>
</tbody>
</table>

1. This option disables the low-noise mode automatically.

When the ODR bits are set to '000', the device is in **Power-down mode**. When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. The I²C interface is still active to allow communication with the device. The content of the configuration registers is preserved and output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

If the ONE_SHOT bit in **CTRL_REG2 (11h)** is set to '1', **One-shot mode** is triggered and a new acquisition starts when it is required. Enabling this mode is possible only if the device was previously in power-down mode (ODR bits set to '000'). Once the acquisition is completed and the output registers updated, the device automatically enters in power-down mode. ONE_SHOT bit self-clears itself.
When the ODR bits are set to a value different than '000', the device is in **Continuous mode** and automatically acquires a set of data (pressure and temperature) at the frequency selected through the ODR[2:0] bits.

Once the additional low-pass filter has been enabled through the EN_LPFP bit, it is possible to configure the device bandwidth acting on the LPFP_CFG bit. See **Table 19** for low-pass filter configurations.

### Table 19. Low-pass filter configurations

<table>
<thead>
<tr>
<th>EN_LPFP</th>
<th>LPFP_CFG</th>
<th>Additional low-pass filter status</th>
<th>Device bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>Disabled</td>
<td>ODR/2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Enabled</td>
<td>ODR/9</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Enabled</td>
<td>ODR/20</td>
</tr>
</tbody>
</table>

The BDU bit is used to inhibit the update of the output registers until both upper and lower (and XLOW) register parts are read. In default mode (BDU = ‘0’) the output register values are updated continuously. If for any reason it is not sure to read faster than the output data rate, it is recommended to set the BDU bit to ‘1’. In this way, the content of the output registers is not updated until MSB, LSB and XLSB have been read which avoids reading values related to different sample times.
## 9.7 CTRL_REG2 (11h)

Control register 2 (R/W)

<p>| | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BOOT</td>
<td>INT_H_L</td>
<td>PP_OD</td>
<td>IF_ADD_INC</td>
<td>0</td>
<td>SWRESET</td>
<td>LOW_NOISE_EN</td>
<td>ONE_SHOT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **BOOT**
  - Reboots memory content. Default value: 0
  - (0: normal mode; 1: reboot memory content)

- **INT_H_L**
  - Interrupt active-high, active-low. Default value: 0
  - (0: active high; 1: active low)

- **PP_OD**
  - Push-pull/open-drain selection on interrupt pad. Default value: 0
  - (0: push-pull; 1: open-drain)

- **IF_ADD_INC**
  - Register address automatically incremented during a multiple byte access with a serial interface (I²C or SPI). Default value: 1
  - (0: disable; 1: enable)

- **SWRESET**
  - Software reset. Default value: 0
  - (0: normal mode; 1: software reset)
  - The bit is self-cleared when the reset is completed.

- **LOW_NOISE_EN**
  - Enables low noise (used only if ODR is lower than 100 Hz). Default value: 0
  - (0: low-current mode; 1: low-noise mode)

- **ONE_SHOT**
  - Enables one-shot. Default value: 0
  - (0: idle mode; 1: a new dataset is acquired)

The BOOT bit is used to refresh the content of the internal registers stored in the Flash memory block. At device power-up, the content of the Flash memory block is transferred to the internal registers related to the trimming functions to allow correct behavior of the device itself. If for any reason the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to ‘1’, the content of the internal Flash is copied into the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They allow the correct behavior of the device and normally they should not be changed. At the end of the boot process, the BOOT bit is set again to ‘0’ by hardware. The BOOT bit takes effect immediately after it is set to 1.

INT_H_L selects an interrupt active-high/low value.

PP_OD selects push-pull/open-drain on the interrupt pad.

The IF_ADD_INC bit enables the address to be automatically incremented during a multiple byte access with a serial interface (SPI or I²C).

The SWRESET bit resets the volatile registers to default value ‘0’. It returns to ‘0’ by hardware.
LOW_NOISE_EN is disabled by default and must be changed when the device is in power-down mode. It enables low-noise mode but can be used when the ODR is lower than 100 Hz. If ODR = 100 Hz or ODR = 200 Hz, this option is automatically switched off and the value of the low-noise enable bit is ignored.

LOW_NOISE_EN mode is enabled to have less RMS noise and the best performance is achieved with LOW_NOISE_EN set to 1 and filter at ODR/20. Depending on the application, the LOW_NOISE_EN bit can be enabled (low-noise mode) or disabled (low-current mode) to have less RMS noise or less power consumption (refer to the following table).

<table>
<thead>
<tr>
<th>Mode</th>
<th>Additional low-pass filter status</th>
<th>Device bandwidth</th>
<th>RMS noise [Pa]</th>
<th>Supply current @ ODR = 1 Hz [μA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low noise</td>
<td>Disabled</td>
<td></td>
<td>1.7</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>Enabled</td>
<td>ODR/9</td>
<td>0.9</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>Enabled</td>
<td>ODR/20</td>
<td>0.65</td>
<td>12</td>
</tr>
<tr>
<td>Low current</td>
<td>Disabled</td>
<td></td>
<td>4.5</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>Enabled</td>
<td>ODR/9</td>
<td>2.6</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>Enabled</td>
<td>ODR/20</td>
<td>1.7</td>
<td>4</td>
</tr>
</tbody>
</table>

The ONE_SHOT bit is used to start a new conversion when the ODR[2:0] bits in \texttt{CTRL\_REG1 (10h)} are set to '000'. Writing a '1' in ONE_SHOT triggers a single measurement of pressure and temperature. Once the measurement is done, the ONE_SHOT bit will self-clear, the new data are available in the output registers, and the \texttt{STATUS (27h)} bits are updated.
## 9.8 CTRL_REG3 (12h)

Control register 3 - INT_DRDY pin control register (R/W)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>INT_F_FULL, FIFO full flag on INT_DRDY pin. Default value: 0 (0: empty; 1: full - 128 unread samples)</td>
</tr>
<tr>
<td>6</td>
<td>INT_F_WTM, FIFO threshold (watermark) status on INT_DRDY pin. Default value: 0 (0: lower than FTH level; 1: equal to or higher than FTH level)</td>
</tr>
<tr>
<td>5</td>
<td>INT_F_OVR, FIFO overrun status on INT_DRDY pin. Default value: 0 (0: not overwritten; 1: at least one sample in the FIFO has been overwritten)</td>
</tr>
<tr>
<td>4</td>
<td>DRDY, Data-ready signal on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)</td>
</tr>
<tr>
<td>3</td>
<td>INT_S[1:0], Data signal on INT_DRDY pin control bits. Default value: 00 Refer to Table 21.</td>
</tr>
</tbody>
</table>

### Table 21. Interrupt configurations

<table>
<thead>
<tr>
<th>INT_S1</th>
<th>INT_S0</th>
<th>INT_DRDY pin configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Data signal (in order of priority: DRDY or INT_F_WTM or INT_F_OVR or INT_F_FULL)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Pressure high (P_high)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Pressure low (P_low)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Pressure low OR high</td>
</tr>
</tbody>
</table>

### Figure 25. Interrupt events on INT_DRDY pin

- New data set is available
- FIFO Threshold (Watermark)
- FIFO Overrun
- FIFO Full
- Pressure higher than threshold
- Pressure lower than threshold

**Legend:**
- CTRL_REG3 (@12h)
- DRDY
- INT_F_WTM
- INT_F_OVR
- INT_F_FULL
- INT_S[1:0]

**INT_DRDY pin**

- 00
- 01
- 10
- 11
9.9 FIFO_CTRL (13h)

FIFO control register (R/W)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>STOP_ON_WTM</td>
<td>TRIG_MODES</td>
<td>F_MODE1</td>
<td>F_MODE0</td>
<td></td>
</tr>
</tbody>
</table>

STOP_ON_WTM: Stop-on-FIFO watermark. Enables FIFO watermark level use. Default value: 0 (0: disable; 1: enable)

TRIG_MODES: Enables triggered FIFO modes. Default value: 0

F_MODE[1:0]: Selects triggered FIFO modes. Default value: 00

Refer to **Table 22**.

Table 22. FIFO mode selection

<table>
<thead>
<tr>
<th>TRIG_MODES</th>
<th>F_MODE[1:]</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>00</td>
<td>Bypass</td>
</tr>
<tr>
<td>0</td>
<td>01</td>
<td>FIFO mode</td>
</tr>
<tr>
<td>0</td>
<td>1x</td>
<td>Continuous (Dynamic-Stream)</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>Bypass-to-FIFO</td>
</tr>
<tr>
<td>1</td>
<td>10</td>
<td>Bypass-to-Continuous (Dynamic-Stream)</td>
</tr>
<tr>
<td>1</td>
<td>11</td>
<td>Continuous (Dynamic-Stream)-to-FIFO</td>
</tr>
</tbody>
</table>

The STOP_ON_WTM bit enables the use of the FIFO watermark level: when the number of samples in FIFO is equal to the watermark level (set using the WTM[4:0] bits in FIFO_WTM (14h)) then FIFO is full.

The TRIG_MODES bit enables the triggered FIFO modes.

The F_MODE[1:0] bits select one of the FIFO modes, as described in **Table 22**.

Output data (pressure and temperature) are read through FIFO_DATA_OUT_PRESS_XL (78h), FIFO_DATA_OUT_PRESS_L (79h), FIFO_DATA_OUT_PRESS_H (7Ah), FIFO_DATA_OUT_TEMP_L (7Bh) and FIFO_DATA_OUT_TEMP_H (7Ch); both single read and multiple read operations can be used.
## 9.10 FIFO_WTM (14h)

FIFO threshold setting register (R/W)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>WTM6</td>
<td>WTM5</td>
<td>WTM4</td>
<td>WTM3</td>
<td>WTM2</td>
<td>WTM1</td>
<td>WTM0</td>
</tr>
</tbody>
</table>

WTM[6:0] FIFO threshold. Watermark level setting. Default value: 0000000

## 9.11 REF_P_L (15h)

Reference pressure LSB data (R)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFL7</td>
<td>REFL6</td>
<td>REFL5</td>
<td>REFL4</td>
<td>REFL3</td>
<td>REFL2</td>
<td>REFL1</td>
<td>REFL0</td>
</tr>
</tbody>
</table>

REFL[7:0] This register contains the low part of the reference pressure value. Default value: 00000000

The Reference pressure value is 16-bit data and it is composed of REF_P_H (16h) and REF_P_L (15h). The value is expressed as 2's complement.

The reference pressure value is stored and used when the AUTOZERO or AUTOREFP function is enabled. Please refer to the INTERRUPT_CFG (0Bh) register description.

## 9.12 REF_P_H (16h)

Reference pressure MSB data (R)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>REFL15</td>
<td>REFL14</td>
<td>REFL13</td>
<td>REFL12</td>
<td>REFL11</td>
<td>REFL10</td>
<td>REFL9</td>
<td>REFL8</td>
</tr>
</tbody>
</table>

REFL[15:8] This register contains the high part of the reference pressure value. Default value: 00000000
9.13 **RPDS_L (18h)**

Pressure offset (LSB data)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPDS7</td>
<td>RPDS6</td>
<td>RPDS5</td>
<td>RPDS4</td>
<td>RPDS3</td>
<td>RPDS2</td>
<td>RPDS1</td>
<td>RPDS0</td>
</tr>
</tbody>
</table>

RPDS[7:0]  This register contains the low part of the pressure offset value.
Default value: 00000000

The pressure offset value is 16-bit data that can be used to implement one-point calibration (OPC) after soldering. This value is composed of **RPDS_H (19h)** and **RPDS_L (18h)**. The value is expressed as 2’s complement.

9.14 **RPDS_H (19h)**

Pressure offset (MSB data)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPDS15</td>
<td>RPDS14</td>
<td>RPDS13</td>
<td>RPDS12</td>
<td>RPDS11</td>
<td>RPDS10</td>
<td>RPDS9</td>
<td>RPDS8</td>
</tr>
</tbody>
</table>

RPDS[15:8]  This register contains the high part of the pressure offset value.
Refer to **RPDS_L (18h)**. Default value: 00000000

9.15 **INT_SOURCE (24h)**

Interrupt source (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOT_ON</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>IA</td>
<td>PL</td>
<td>PH</td>
</tr>
</tbody>
</table>

BOOT_ON  Indication of Boot phase.
(0: Boot phase has ended;
1: Boot phase is running).

IA  Interrupt active.
(0: no interrupt has been generated;
1: one or more interrupt events have been generated).

PL  Differential pressure Low.
(0: no interrupt has been generated;
1: low differential pressure event has occurred).

PH  Differential pressure High.
(0: no interrupt has been generated;
1: high differential pressure event has occurred).
9.16 FIFO_STATUS1 (25h)
FIFO status register (read only)

FSS[7:0] FIFO stored data level, number of unread samples stored in FIFO.
(00000000: FIFO empty; 10000000: FIFO full, 128 unread samples)

9.17 FIFO_STATUS2 (26h)
FIFO status register (read only)

FIFO_WTM_IA FIFO threshold (watermark) status. Default value: 0
(0: FIFO filling is lower than treshold level;
1: FIFO filling is equal or higher than treshold level).

FIFO_OVR_IA FIFO overrun status. Default value: 0
(0: FIFO is not completely full;
1: FIFO is full and at least one sample in the FIFO has been overwritten).

FIFO_FULL_IA FIFO full status. Default value: 0
(0: FIFO is not completely filled;
1: FIFO is completely filled, no samples overwritten)

9.18 STATUS (27h)
Status register (read only)

T_OR Temperature data overrun.
(0: no overrun has occurred;
1: a new data for temperature has overwritten the previous data)

P_OR Pressure data overrun.
(0: no overrun has occurred;
1: new data for pressure has overwritten the previous data)

T_DA Temperature data available.
(0: new data for temperature is not yet available;
1: a new temperature data is generated)

P_DA Pressure data available.
(0: new data for pressure is not yet available;
1: a new pressure data is generated)

This register is updated every ODR cycle.
9.19 PRESS_OUT_XL (28h)

Pressure output value LSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>POUT7</td>
<td>POUT6</td>
<td>POUT5</td>
<td>POUT4</td>
<td>POUT3</td>
<td>POUT2</td>
<td>POUT1</td>
<td>POUT0</td>
</tr>
</tbody>
</table>

POUT[7:0] This register contains the low part of the pressure output value.

The pressure output value is a 24-bit data that contains the measured pressure. It is composed of PRESS_OUT_H (2Ah), PRESS_OUT_L (29h) and PRESS_OUT_XL (28h). The value is expressed as 2’s complement.

The output pressure register PRESS_OUT is provided as the difference between the measured pressure and the content of the register RPDS (18h, 19h)*.

Please refer to Section 4.4: Interpreting pressure readings for additional info.

*DIFF_EN = '0', AUTOZERO = '0', AUTOREFP = '0'

9.20 PRESS_OUT_L (29h)

Pressure output value middle data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>POUT15</td>
<td>POUT14</td>
<td>POUT13</td>
<td>POUT12</td>
<td>POUT11</td>
<td>POUT10</td>
<td>POUT9</td>
<td>POUT8</td>
</tr>
</tbody>
</table>

POUT[15:8] This register contains the mid part of the pressure output value.

Refer to PRESS_OUT_XL (28h)

9.21 PRESS_OUT_H (2Ah)

Pressure output value MSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>POUT23</td>
<td>POUT22</td>
<td>POUT21</td>
<td>POUT20</td>
<td>POUT19</td>
<td>POUT18</td>
<td>POUT17</td>
<td>POUT16</td>
</tr>
</tbody>
</table>

POUT[23:16] This register contains the high part of the pressure output value.

Refer to PRESS_OUT_XL (28h)
### 9.22 TEMP_OUT_L (2Bh)

Temperature output value LSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOUT7</td>
<td>TOUT6</td>
<td>TOUT5</td>
<td>TOUT4</td>
<td>TOUT3</td>
<td>TOUT2</td>
<td>TOUT1</td>
<td>TOUT0</td>
</tr>
</tbody>
</table>

**TOUT[7:0]** This register contains the low part of the temperature output value.

The temperature output value is 16-bit data that contains the measured temperature. It is composed of TEMP_OUT_H (2Ch), and TEMP_OUT_L (2Bh). The value is expressed as 2’s complement.

### 9.23 TEMP_OUT_H (2Ch)

Temperature output value MSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOUT15</td>
<td>TOUT14</td>
<td>TOUT13</td>
<td>TOUT12</td>
<td>TOUT11</td>
<td>TOUT10</td>
<td>TOUT9</td>
<td>TOUT8</td>
</tr>
</tbody>
</table>

**TOUT[15:8]** This register contains the high part of the temperature output value.

### 9.24 FIFO_DATA_OUT_PRESS_XL (78h)

FIFO pressure output LSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_P7</td>
<td>FIFO_P6</td>
<td>FIFO_P5</td>
<td>FIFO_P4</td>
<td>FIFO_P3</td>
<td>FIFO_P2</td>
<td>FIFO_P1</td>
<td>FIFO_P0</td>
</tr>
</tbody>
</table>

**FIFO_P[7:0]** Pressure LSB data in FIFO buffer

### 9.25 FIFO_DATA_OUT_PRESS_L (79h)

FIFO pressure output middle data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_P15</td>
<td>FIFO_P14</td>
<td>FIFO_P13</td>
<td>FIFO_P12</td>
<td>FIFO_P11</td>
<td>FIFO_P10</td>
<td>FIFO_P9</td>
<td>FIFO_P8</td>
</tr>
</tbody>
</table>

**FIFO_P[15:8]** Pressure middle data in FIFO buffer
### FIFO_DATA_OUT_PRESS_H (7Ah)
FIFO pressure output MSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_P23</td>
<td>FIFO_P22</td>
<td>FIFO_P21</td>
<td>FIFO_P20</td>
<td>FIFO_P19</td>
<td>FIFO_P18</td>
<td>FIFO_P17</td>
<td>FIFO_P16</td>
</tr>
</tbody>
</table>

FIFO_P[23:16] Pressure middle data in FIFO buffer

### FIFO_DATA_OUT_TEMP_L (7Bh)
FIFO temperature output LSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_T7</td>
<td>FIFO_T6</td>
<td>FIFO_T5</td>
<td>FIFO_T4</td>
<td>FIFO_T3</td>
<td>FIFO_T2</td>
<td>FIFO_T1</td>
<td>FIFO_T0</td>
</tr>
</tbody>
</table>

FIFO_T[7:0] Temperature LSB data in FIFO buffer

### FIFO_DATA_OUT_TEMP_H (7Ch)
FIFO temperature output MSB data (read only)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFO_T15</td>
<td>FIFO_T14</td>
<td>FIFO_T13</td>
<td>FIFO_T12</td>
<td>FIFO_T11</td>
<td>FIFO_T10</td>
<td>FIFO_T9</td>
<td>FIFO_T8</td>
</tr>
</tbody>
</table>

FIFO_T[15:8] Temperature MSB data in FIFO buffer
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

10.1 HLGA-10L package information

Figure 26. HLGA-10L (2.0 x 2.0 x 0.73 mm typ.) package outline and mechanical dimensions

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DIMENSION [mm]</th>
<th>TOLERANCE [mm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length (L)</td>
<td>2</td>
<td>±0.1</td>
</tr>
<tr>
<td>Width (W)</td>
<td>2</td>
<td>±0.1</td>
</tr>
<tr>
<td>Height (H)</td>
<td>0.8 max</td>
<td>/</td>
</tr>
</tbody>
</table>

Dimensions are in millimeter unless otherwise specified
General Tolerance is ±0.1mm unless otherwise specified

DM00386636_1
10.2 HLGA-10L packing information

Figure 27. Carrier tape information for HLGA-10L package

Figure 28. HLGA-10L package orientation in carrier tape

NOTES:
1. ED SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.
Figure 29. Reel information for carrier tape of HLGA-10L package

Table 23. Reel dimensions for carrier tape of HLGA-10L package

<table>
<thead>
<tr>
<th>Reel dimensions (mm)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A (max)</td>
<td>330</td>
</tr>
<tr>
<td>B (min)</td>
<td>1.5</td>
</tr>
<tr>
<td>C</td>
<td>13 ±0.25</td>
</tr>
<tr>
<td>D (min)</td>
<td>20.2</td>
</tr>
<tr>
<td>N (min)</td>
<td>60</td>
</tr>
<tr>
<td>G</td>
<td>12.4 +2/-0</td>
</tr>
<tr>
<td>T (max)</td>
<td>18.4</td>
</tr>
</tbody>
</table>
11 Revision history

Table 24. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>22-Aug-2018</td>
<td>1</td>
<td>Initial release</td>
</tr>
<tr>
<td>04-Feb-2019</td>
<td>2</td>
<td>Updated description of SETDASA in Table 16: MIPI I3C\textsuperscript{SM} CCC commands</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated text concerning BOOT bit in CTRL_REG2 (11h)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated bit 7 in INT_SOURCE (24h)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated Figure 27: Carrier tape information for HLGA-10L package</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved