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M24256X-G

Datasheet

256-Kbit serial I²C bus EEPROM with configurable device address and software write protection and I/Os 1.2 V

WLCSP (CU)

Product status link

M24256X-G

Product label

Features

I²C interface

- Compatible with following I²C bus modes:
  - 1 MHz (fast mode plus)
  - 400 kHz (fast mode)
  - 100 kHz (standard mode)

Memory

- 256-Kbit (32-Kbyte) of EEPROM
- Page size: 64-byte
- Additional 64-byte identification page

Input-output

- I/Os 1.2 V compatible

Power supply

- Voltage range: 1.8 V ± 5 %

Temperature

- Operating temperature range: From -40 °C up to +85 °C

Fast write cycle time

- Byte and page write within 5 ms (3.4 ms typical)

Performance

- Enhanced ESD/latch-up protection
- More than 4 million write cycles
- More than 200-year data retention
- Fast wake-up time (less than 5µs)

Ultra-low power current consumption

- 350 nA (typ) in Standby mode
- 100 µA (typ) for read current
- 150 µA (typ) for write current

Advanced features

- Configurable device address register
- Software write protection register
- Random and sequential read modes

Package

- WLCSP 4-ball (ECOPACK2)

1 Description

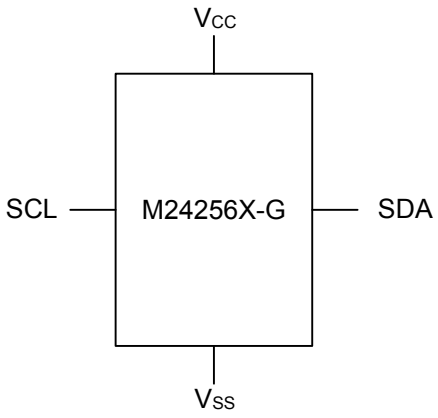
The M24256X-G is a 256-Kbit I^2C-compatible EEPROM (electrically erasable programmable memory) organized as 32 K × 8 bits.

The M24256X-G can operate with a supply voltage of 1.8 V ± 5% (from 1.71 V to 1.89 V), with a clock frequency of 1 MHz (or less), over an ambient temperature range of -40 °C/+85 °C.

The M24256X-G product offers the I/Os compatible with 1.2 V and delivery in a 4-pin package.

The M24256X-G offers three features, namely a 64-byte page, called the identification page, which can be used to store sensitive application parameters that can be user (later) permanently locked in red-only mode; a first 8-bit register, called the configurable device address (CDA) register authorizing the user, through software, to configure up to eight possibilities of chip enable address; a second 8-bit register, named the software write protection (SWP) register authorizing the user, through software, to write protect partially or fully the memory array.

Figure 1. Logic diagram



DT73070V1

Table 1. Signal names

Signal name	Function	Direction
SDA	Serial data	I/O
SCL	Serial clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. WLCSP connections

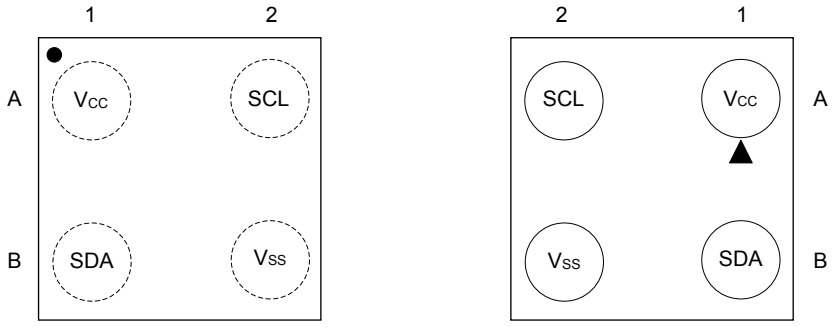


Table 2. **Signals versus bump position**

Signal name	Bump position
V_{CC}	A1
SCL	A2
SDA	B1
V_{SS}	B2

2 Signal description

2.1 Serial clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wired-AND with other open drain or open collector signals on the bus. A pull-up resistor must be connected from serial data (SDA) to V_{CC} (Figure 23 and Figure 24 indicate how to calculate the value of the pull-up resistor).

2.3 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Table 11). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from 10 nF to 100 nF) close to the V_{CC} / V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.4.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Table 11 in Section 9 DC and AC parameters).

Once the V_{CC} is greater than, or equal to, the minimum V_{CC} level, the controller must wait for at least T_{WU} before sending the first command to the device. See Table 17 and Table 18 for the value of the wake-up time parameter.

2.4.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see operating conditions in Section 9 DC and AC parameters). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see operating conditions in Section 9 DC and AC parameters).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

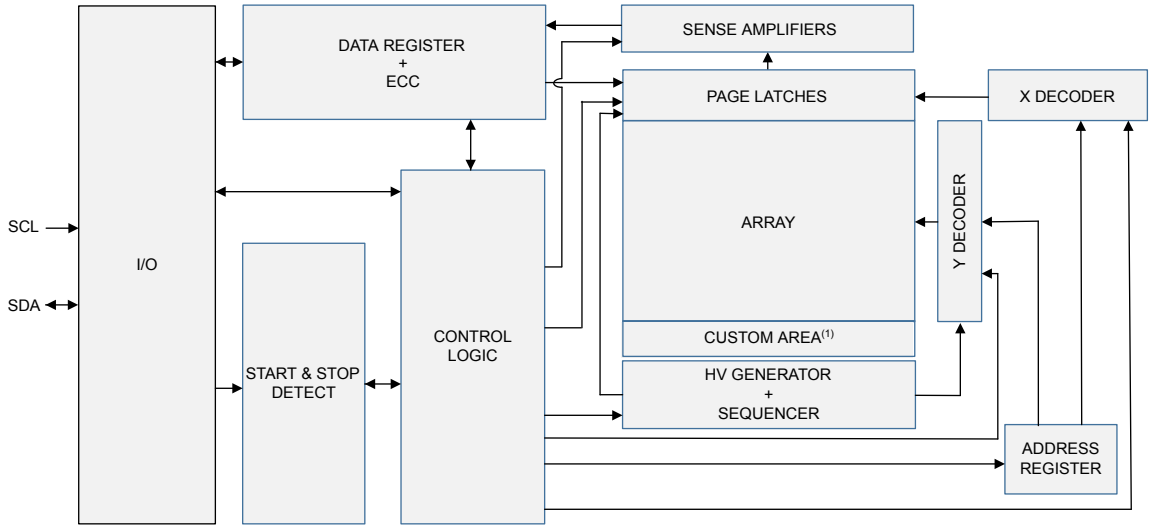
2.4.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the standby power mode (mode reached after decoding a stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

Figure 3. Block diagram



1. ID page, SWP and CDA register area

4 Device features

4.1 Configurable device address register (CDA)

As the M24256X-G is delivered in 4-ball WLCSP without chip enable inputs, the device provides a nonvolatile 8-bit register allowing the user to define a configurable device address (CDA) and a specific bit, named device address lock, to freeze the configurable device address register. This register can be read and written by issuing the read or write configurable device address instruction. These instructions use the same protocol and format as the random address read or page write (from/into memory array) except for the following differences (refer to Table 7, Table 8, and Table 9):

- Device type identifier = 1010b
- MSB address bits A15/A14/A13 must be equal to '110' (A15=1, A14=1 and A13=0)
- MSB address bits A12/A8 are don't care
- LSB address bits A7/A0 are don't care

C2, C1, C0, and DAL are defining the chip enable address in the device select code and the device address lock.

These bits can be written and reconfigured with a write command. At power-up or after reprogramming, the device load the last configuration of C2, C1, C0, and DAL values. To prevent an unwanted change of configurable device address bits, the M24256X-G proposes to protect the CDA register, permanently freezing it in read-only mode.

The update of the CDA register is disabled (read-only) when the DAL bit is set to '1' (DAL=1b).

In the same way, the update of the CDA register is enabled when the DAL bit is set to '0' (DAL= 0b). Sending more than one byte during a write configurable device address command aborts the write cycle (CDA register content does not change).

Note: Updating the DAL bit from '0' to '1' is an irreversible action: the C2, C1, C0, and DAL bits cannot be updated anymore.

The description of the configurable device address register is given Table 3.

Table 3. Configurable device address register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x (1)	x (1)	x (1)	x(1)	C2	C1	C0	DAL

1. *x = Don't care bits. Read as 0*

Note: Factory delivery of the register is 00000000b.

Table 4. **Configurable device address register description**

Bit	Function
Bit b7:b4	Don't care bits - Read as '0'. (b7,b6,b5,b4)=(0,0,0,0)
Bit b3:b1	**C2, C1, C0**: Configurable device address bits b3, b2, b1 are used to configure up to eight possibilities of chip enable address: • (b3, b2, b1) = (0, 0, 0): the chip enable address is 000 (factory delivery value) • (b3, b2, b1) = (0, 0, 1): the chip enable address is 001 • (b3, b2, b1) = (0, 1, 0): the chip enable address is 010 • (b3, b2, b1) = (0, 1, 1): the chip enable address is 011 • (b3, b2, b1) = (1, 0, 0): the chip enable address is 100 • (b3, b2, b1) = (1, 0, 1): the chip enable address is 101 • (b3, b2, b1) = (1, 1 0): the chip enable address is 110 • (b3, b2, b1) = (1, 1, 1): the chip enable address is 111
Bit b0	**DAL**: Device address lock bit b0 locks the CDA register in read-only mode: • b0 = 0: bits b3, b2, b1, b0 can be modified • b0 = 1: bits b3, b2, b1, b0 can't be modified and therefore the CDA register is frozen *Note: bits b3 to b0 can be updated (if b0 = 0) in the same write instruction. Setting b0 from 0 to 1 is an irreversible action.*

4.2 Software write protection register (SWP)

As the M24256X-G is delivered in 4-ball WLCSP without write control ($\overline{WC}$) input, the device provides a nonvolatile

8-bit register allowing the user to protect a specific area of the memory against the write instructions. The

SWP offers four nonvolatile bits to configure by the user:

- Two bits for setting the size of the write-protected memory. They are identified as the block protect bits (BPn) bits.
- One bit to enable / disable the write protection of the desired area. It is identified as the write protect activation (WPA) bit.
- One bit to definitively freeze the SWP register in read-only mode. It is identified as the write protection lock (WPL) bit.

This register can be written and read by issuing the read or write configurable device address instruction. These instructions use the same protocol and format as the random address read or page write (from/into memory array) except for the following differences (refer to Table 7, Table 8, and Table 9):

- Device type identifier = 1010b
- MSB address bits A15/A14/A13 must be equal to '101' (A15=1;A14=0;A13=1)
- MSB address bits A12/A8 are don't care
- LSB address bits A7/A0 are don't care

BP1 and BP0 are the block protection bits. WPL is the write protect lock bit and WPA is the write protect activation bit. These bits can be written and reconfigured with a write command. At power-up, the device loads the last configuration of the SWP register value.

The user can update the SWP register as often as the WPL bit stays at '0'. Writing more than one byte discard the write cycle (software write protection register content is not changed).

To prevent unwanted change of software write-protection register bits, the M24256X-G proposes to protect the SWP register, freezing it permanently in read-only mode. The update of the SWP register is disabled (read only) when the WPL bit is set to '1' (WPL=1b). In the same way, the update of the SWP register is enabled when the WPL bit is set to '0' (WPL = 0b).

When SWP is set to '1' and in the case of write software write protection register, the device select and address bytes are acknowledged, the data byte is not acknowledged and the write cycle does not start.

Note: Updating the SWP bit from '0' to '1' is an irreversible action: the WPA, BP1, BP0, and WPL bits cannot be updated anymore.

The description of the software write protection register is given in the table below:

Table 5. Software write protection register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X(1)	X(1)	X(1)	X(1)	WPA	BP1	BP0	WPL

1. *x = Don't care bits. Read as 0.*

Note: Factory delivery of the register is 00000000b.

Table 6. Software write protection register description

Bit	Function
Bits b7:b4	Don't care bits - Read as '0'. (b7,b6,b5,b4)=(0,0,0,0)
Bit b3	**WPA**: write protect activation bit b3 enables or disables the write protection • b3 = 0: no write protection. The whole memory can be written • b3 = 1: write protection active. The memory block is protected according to the BP bits setting
Bits b2:b1	**BP1, BP0**: block protection bits b2 and b1 define the size of the memory block to be protected against write instruction: • (b2, b1) = (0, 0): the upper quarter of memory is write-protected • (b2, b1) = (0, 1): the upper half of memory is write-protected • (b2, b1) = (1, 0): the upper 3/4 of memory is write-protected • (b2, b1) = (1, 1): the WHOLE memory is write-protected
Bit b0	**WPL**: write protect lock bit b0 locks the write protection register value: • b0 = 0: bits [b3: b0] can be modified • b0 = 1: bits [b3: b0] cannot be modified and therefore the write protection register is frozen *Note: Bits b3 to b0 can be updated (if b0 = 0) in the same write instruction. Setting b0 from 0 to 1 is an irreversible action.*

4.3 Identification page

The identification page (64 bytes) is an additional page which can be read or written and (later) permanently locked in read-only mode. It is read or written by issuing the read or write identification page instruction. These instructions use the same protocol and format as the random address read or page write (from/into memory array) except for the following differences (refer to Table 7, Table 8 and Table 9):

- Device type identifier = 1011b
- MSB address bits A15/A6 are don't care except for address bit A10 which must be ‘0’
- LSB address bits A5/A0 define the byte address inside the Identification page

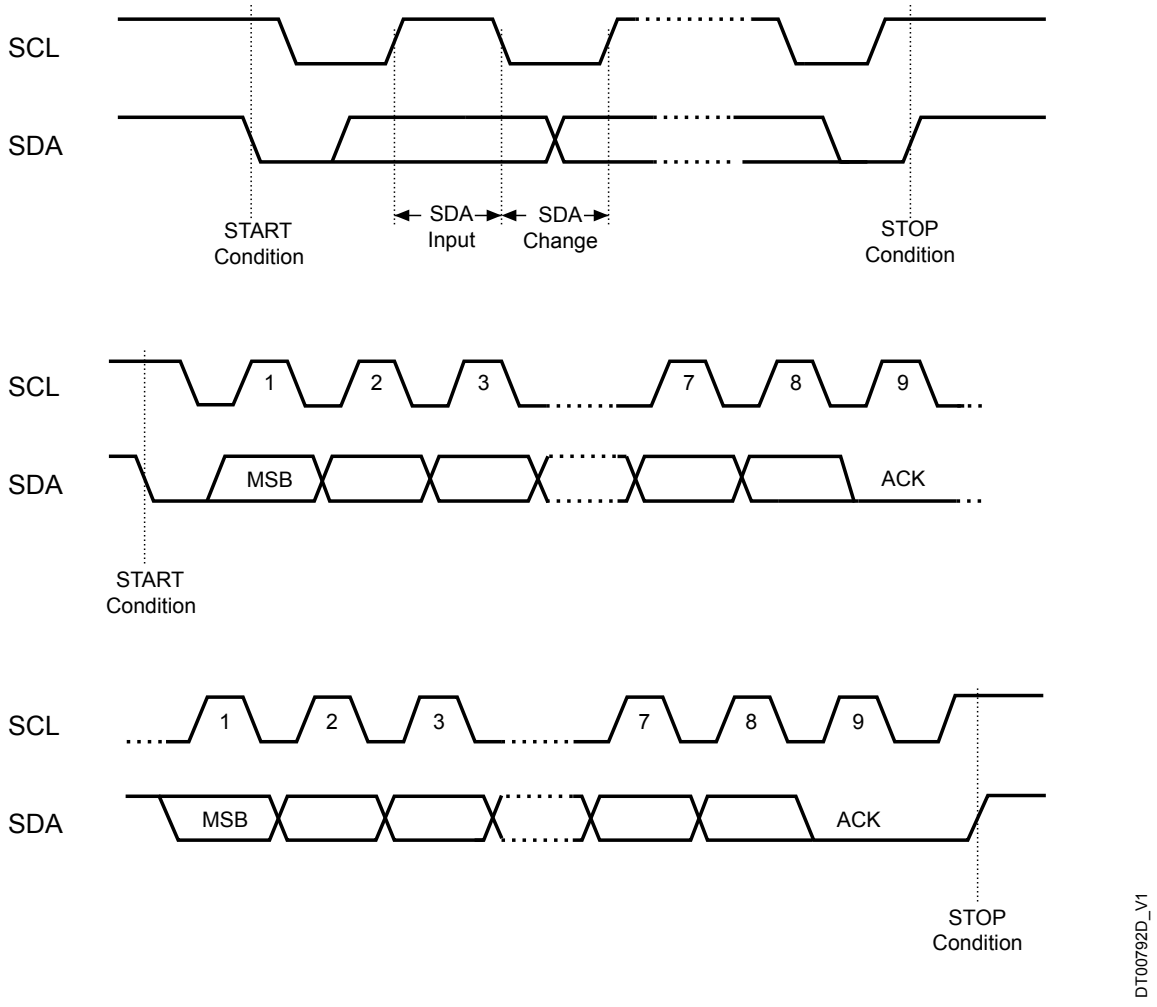
If the identification page is locked, the data bytes transferred during the write identification page instruction are not acknowledged (NoACK).

The identification page is filled with all bytes written to FFh.

5 Device operation

The device supports the I²C protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data is defined to be a receiver. The device that controls the data transfer is known as the bus controller, and the other as the target device. A data transfer can only be initiated by the bus controller, which also provides the serial clock for synchronization. The device is always a target in all communications.

Figure 4. I²C bus protocol



5.1 Start condition

Start is identified by a falling edge of serial data (SDA) while serial clock (SCL) is stable in the high state. A start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) serial data (SDA) and serial clock (SCL) for a start condition.

5.2 Stop condition

Stop is identified by a rising edge of serial data (SDA) while the serial clock (SCL) is stable in the high state. A stop condition terminates communication between the device and the bus controller. A read instruction that is followed by no ACK can be followed by a stop condition to force the device into the standby mode.

A stop condition at the end of a write instruction triggers the internal write cycle.

5.3 Data input

During data input, the device samples serial data (SDA) on the rising edge of serial clock (SCL). For correct device operation,serial data (SDA) must be stable during the rising edge of serial clock (SCL), and the serial data (SDA) signal must change only when serial clock (SCL) is driven low.

5.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be a bus controller or a target device, releases serial data (SDA) after sending eight bits of data. During the ninth clock pulse period, the receiver pulls serial data (SDA) low to acknowledge the receipt of the eight data bits.

5.5 Device addressing

To start communication between the bus controller and the target device, the bus controller must initiate a start condition. Following this, the bus controller sends the device select code, on serial data (SDA), the most significant bit first.

When the device select code is received, the device responds only if the b3, b2, and b1 values match the values of the C2, C1, and C0 bits programmed in the configurable device address register.

If a match occurs, the corresponding device gives an acknowledgment on serial data (SDA) during the ninth bit time.

If the device does not acknowledge the device select code, the device deselects itself from the bus, and goes into Standby mode (therefore does not acknowledge the device select code).

The eighth bit is the Read/Write bit ($R\overline{W}$). This bit is set to 1 for Read and 0 for write operations.

Table 7. Device select code

Features	Device type identifier				Chip enable address(1)			$R\overline{W}$
	Bit 7 (MSB)(2)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	1	0	1	0	C2	C1	C0	$R\overline{W}$
Identification page	1	0	1	1	C2	C1	C0	$R\overline{W}$
Identification page lock	1	0	1	1	C2	C1	C0	$R\overline{W}$
Configurable device address	1	0	1	0	C2	C1	C0	$R\overline{W}$
Software write protection	1	0	1	0	C2	C1	C0	$R\overline{W}$

1. *C0, C1, and C2 are compared with the value read on bits b1, b2, and b3 of the CDA register.*
2. *The most significant bit, b7, is sent first.*

Table 8. First byte address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A15 = 0	A14	A13	A12	A11	A10	A9	A8
Identification page	X(2)	X	X	X	X	0	X	X
Identification page lock	X	X	X	X	X	1	X	X
Configurable device address	1	1	0	X	X	X	X	X
Software write protection	1	0	1	X	X	X	X	X

1. *The most significant bit, b7, is sent first.*
2. *X = Don't care bit.*

Table 9. Second byte address

Features	Bit 7 (MSB)(1)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Memory	A7	A6	A5	A4	A3	A2	A1	A0
Identification page	X(2)	X	A5	A4	A3	A2	A1	A0
Identification page lock	X	X	X	X	X	X	X	X
Configurable device address	X	X	X	X	X	X	X	X
Software write protection	X	X	X	X	X	X	X	X

1. *The most significant bit, b7, is sent first.*
2. *X = Don't care bit.*

6 Instructions

6.1 Write operations on memory array

Following a start condition the bus controller sends a device select code with the R/W bit ($R\overline{W}$) reset to 0. The device acknowledges this, as shown in Figure 5, and waits for two address bytes. The MSB address bit A15 must be equal to 0.The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 7, Table 8 and Table 9) how to address the memory array.

When the bus controller generates a stop condition immediately after a data byte ack bit (in the "10^{th} bit" time slot), either at the end of a byte write or a page write, the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

After the stop condition and the successful completion of an internal write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

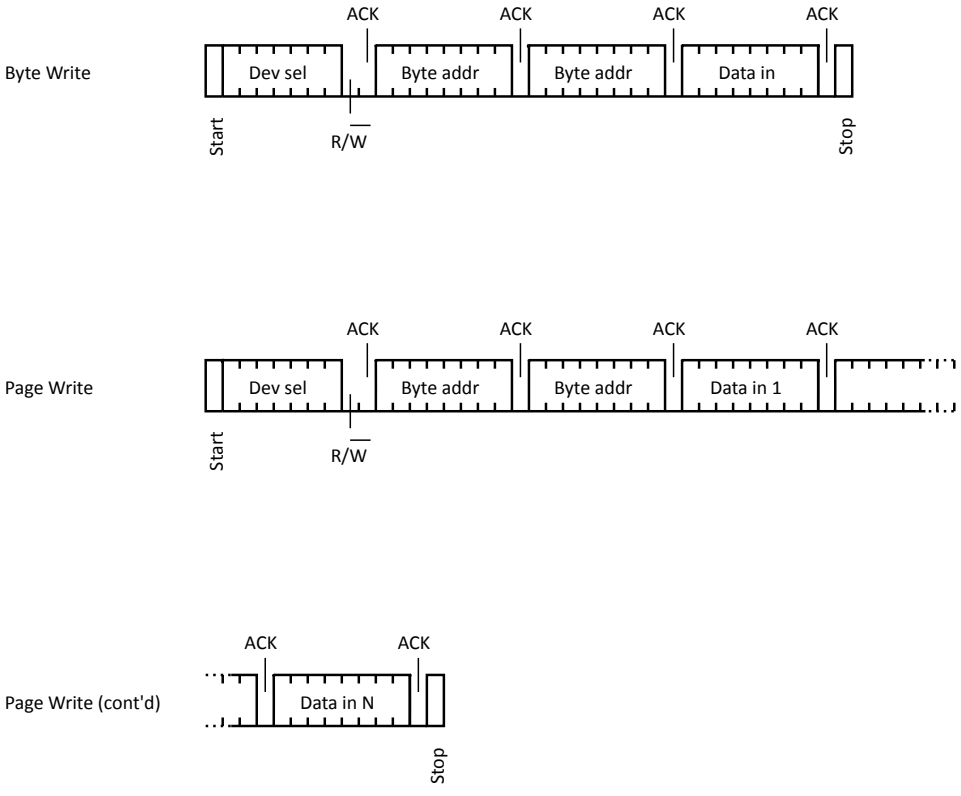
During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests.

If the addressed area is write protected through the SWP setting, the write instruction is not executed and the accompanying data bytes are not acknowledged, as shown in Figure 5.

6.1.1 Byte write

After the device select code and the address bytes with the MSB bit A15 equal to 0, the bus controller sends one data byte. If the addressed location is write-protected, the device replies with no ACK, and the location is not modified, as shown in Figure 6. If, instead, the addressed location is not write-protected, the device replies with ACK. The bus controller terminates the transfer by generating a stop condition, as shown in Figure 5.

Figure 5. Write mode sequence (data write enabled)



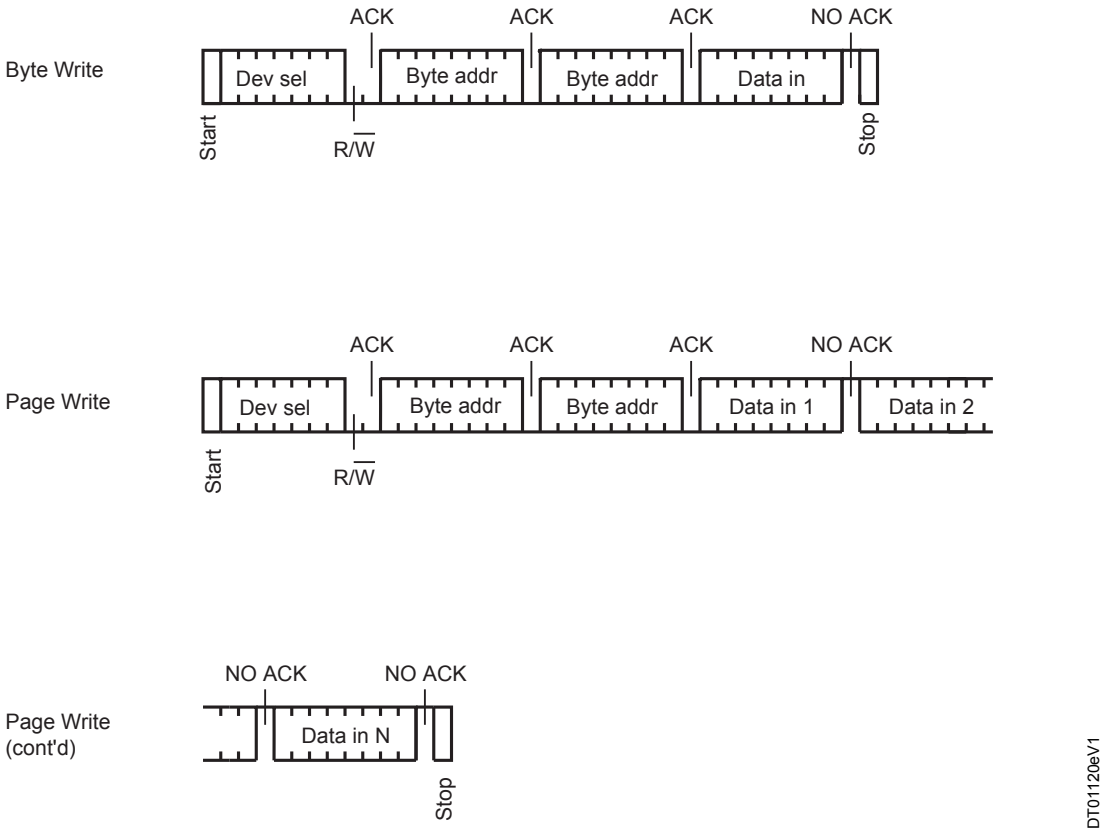
6.1.2 Page write

The page write mode allows up to 64 bytes to be written in a single write cycle, provided they are all located in the same page in the memory: that is, the most significant memory address bits, A14/A6, are the same. The MSB bit A15 of the address transmitted must be equal to 0.If more bytes than those that fit up to the end of the page are sent, a “roll-over” occurs, that is, the bytes exceeding the page end are written on the same page, from location 0.

The bus controller sends from 1 to 64 bytes of data, each one is acknowledged by the device, if the addressed bytes are not write-protected with the SWP settings. In the opposite case, when the addressed bytes are write-protected by SWP settings, the contents of the addressed memory location are not modified, and each data byte is followed by a no ACK, as shown in Figure 6. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus controller generating a stop condition.

Figure 6. Write mode sequence (data write inhibited)



6.2 Write operations on features

6.2.1 Write operations on configurable device address register (CDA)

Write operations on configurable device address register are performed according to the state of the device address lock bit (DAL).

If the DAL bit is set to '1', the CDA register is in read-only mode. The write operation on this register is not executed and the accompanying data byte is not acknowledged as shown in Figure 8.

When the DAL bit is set to '0', the user can update the CDA register value.

Following a start condition the bus controller sends a device select code with the R/W bit ($R\overline{W}$) set to 0. The device acknowledges this, as shown in Figure 7, and waits for the address bytes where the register is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the configurable device address register.

When the bus controller generates a stop condition immediately after the data byte ACK bit (in the "10^{th} bit" time slot), the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (no ACK).

If the three bits C2, C1 and C0 have been reconfigured with a correct write command, the device acknowledges if the chip enable address of the device select code is equal to the new values of C2, C1, and C0, otherwise no ACK.

Sending more than one byte aborts the write cycle (chip enable register content do not be changed).

Bits (C2, C1, C0 + DAL) can be updated (DAL = '0' to '1') in the same program instruction.

Figure 7. Write configurable device address register (data write enabled)

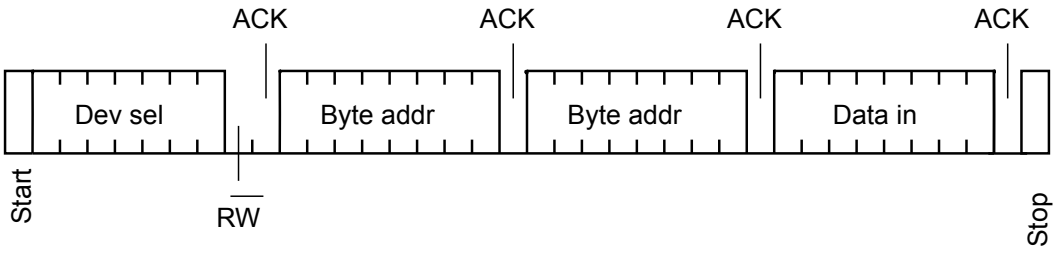
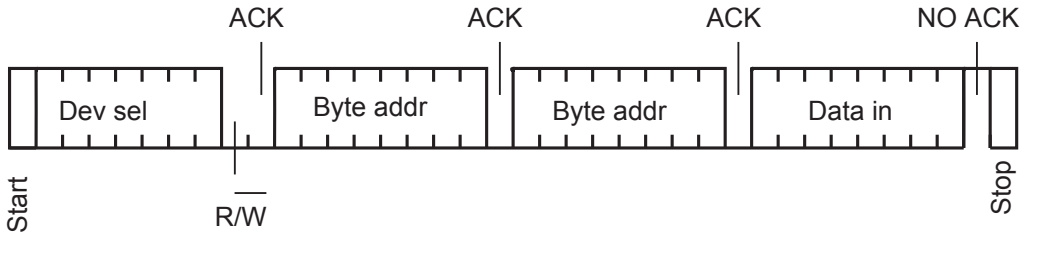


Figure 8. Write configurable device address register (data write inhibited)



6.2.2 Write operations on software write protection register (SWP)

Write operations on SWP register are performed according to the state of the write protect lock bit (WPL).

When the WPL bit is set to '1', the SWP register is in read-only mode. The write operation on this register is not executed and the accompanying data byte is not acknowledged as shown in Figure 10.

When the WPL bit is set to '0', the user can update the SWP register value.

Following a start condition the bus controller sends a device select code with the R/W bit ($R\overline{W}$) set to 0. The device acknowledges this, as shown in Figure 9, and waits for the address bytes where the SWP register is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the software write protection register.

When the bus controller generates a stop condition immediately after the data byte ACK bit (in the "10^{th} bit" time slot), the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (no ACK).

Sending more than one byte aborts the write cycle (write protection register content do not be changed).

Figure 9. Write software write protection register (data write enabled)

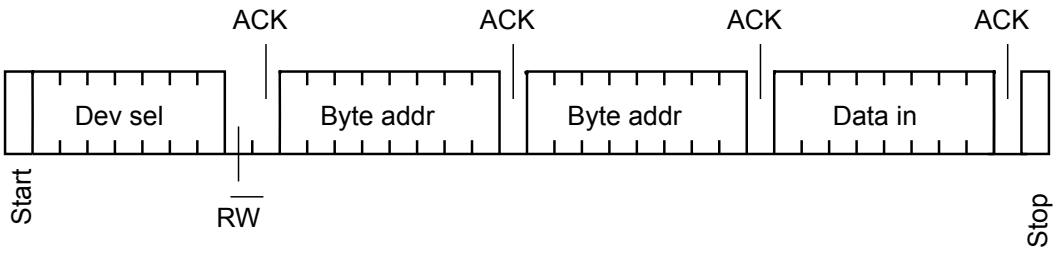
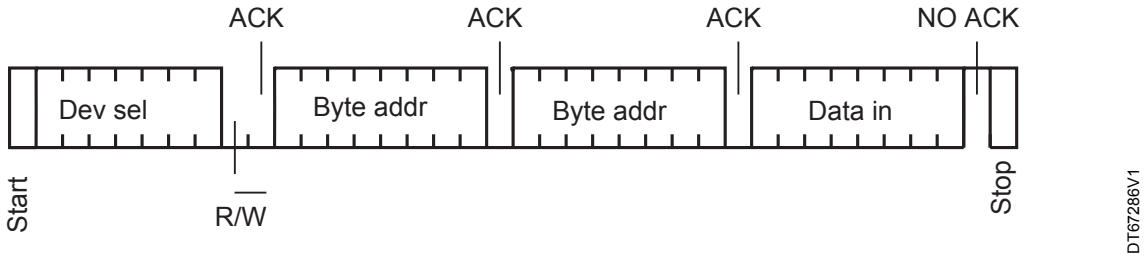


Figure 10. Write software write protection register (data write inhibited by software)



6.2.3 Write operation on identification page

Write operations on the identification page are performed according to the state of the lock/unlock status.

Following a start condition the bus controller sends a device select code with the R/W bit ($\overline{RW}$) set to 0. The device acknowledges this, as shown in Figure 11, and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the identification page.

When the bus controller generates a stop condition immediately after the data byte ACK bit (in the "10th bit" time slot), the internal write cycle t_W is triggered. The device internal address counter is automatically incremented to point to the next byte after the last modified byte.

A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (no ACK).

If the identification page is already locked in read-only mode (lock status) the write operation on the identification page is not executed and the accompanying data bytes are not acknowledged as shown in Figure 12.

Figure 11. Write identification page (page unlocked)

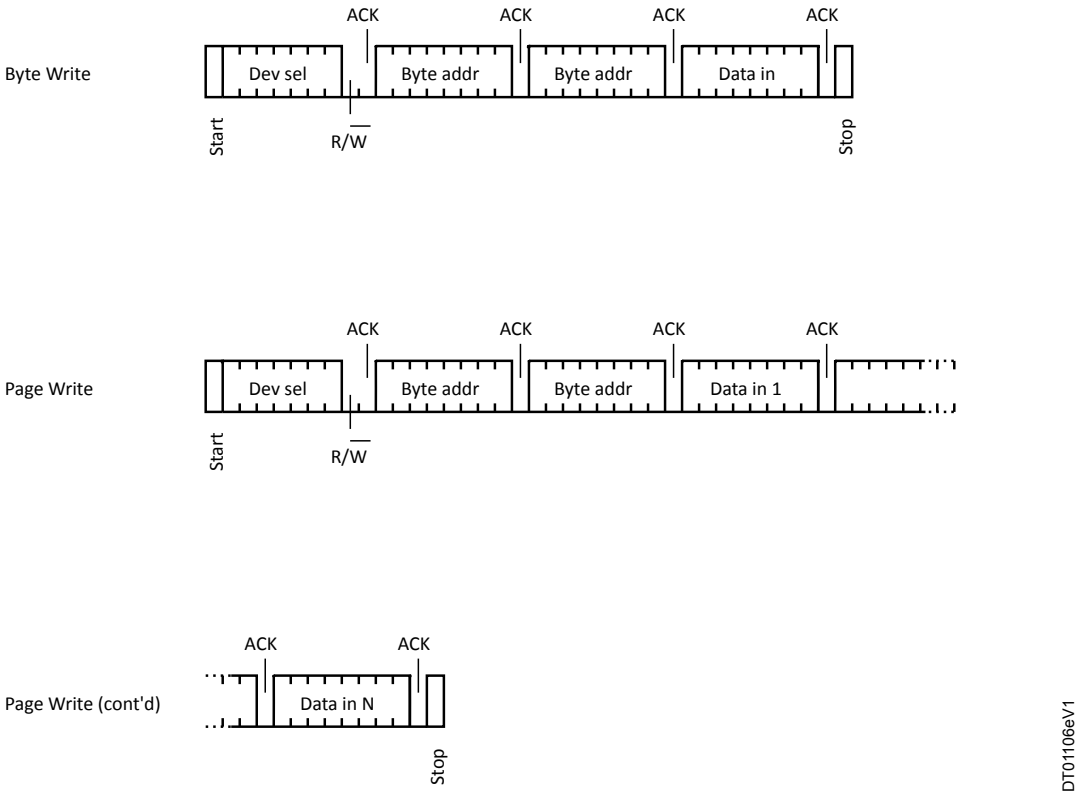
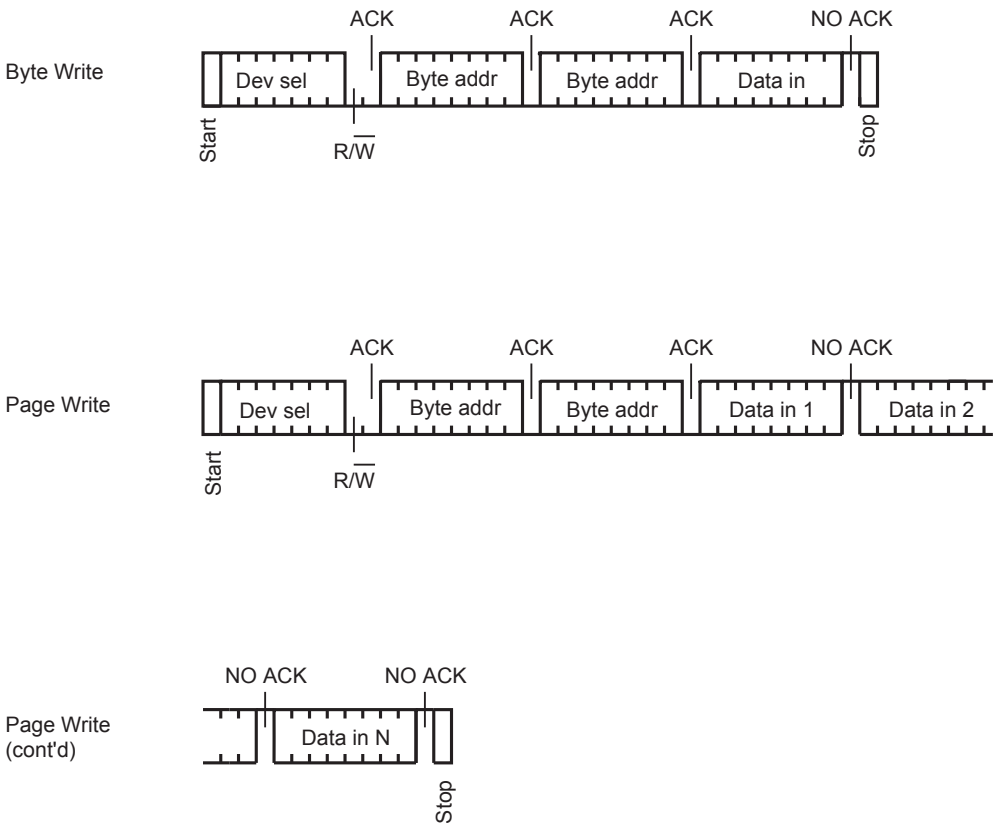


Figure 12. Write identification page (page locked)



6.2.4 Lock operation on identification page

The lock identification page instruction (lock ID) permanently locks the identification page in read-only mode.

Following a start condition the bus controller sends a device select code with the R/W bit ($\overline{RW}$) set to 0. The device acknowledges this, as shown in Figure 13, and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit, and then waits for a specific data byte value. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the identification page.

The data byte must be equal to the binary value xxxx xx1x, where x is don't care.

When the bus controller generates a stop condition immediately after the data byte ACK bit (in the "10th bit" time slot), the internal write cycle t_W is triggered. A stop condition at any other time slot does not trigger the internal write cycle.

During the internal write cycle, serial data (SDA) is disabled internally, and the device does not respond to any requests (no ACK).

If the identification page is already locked, the write operation is not executed and the accompanying data bytes are not acknowledged as shown in Figure 14.

Figure 13. Lock operation on identification page (unlocked)

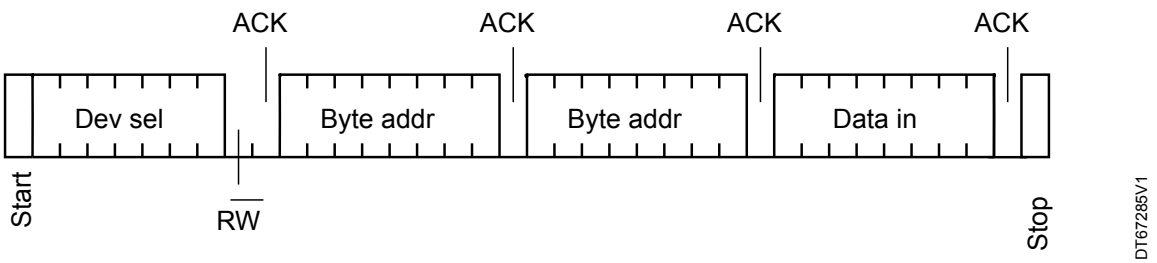
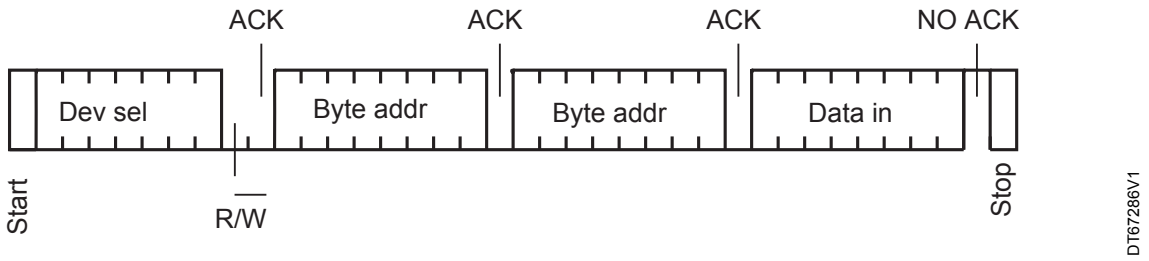


Figure 14. Lock operation on identification page (already locked)



6.3 ECC (error correction code) and write cycling

The error correction code (ECC) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes. Inside a group, if a single bit out of the four bytes happens to be erroneous during a read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group (a group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.)

As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte 0, byte 1, byte 2 and byte 3 of the same group must remain below the maximum value defined in Table 14.

6.4 Minimizing write delays by polling on ACK

During the internal write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in the AC characteristics tables in Section 9 DC and AC parameters, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus controller.

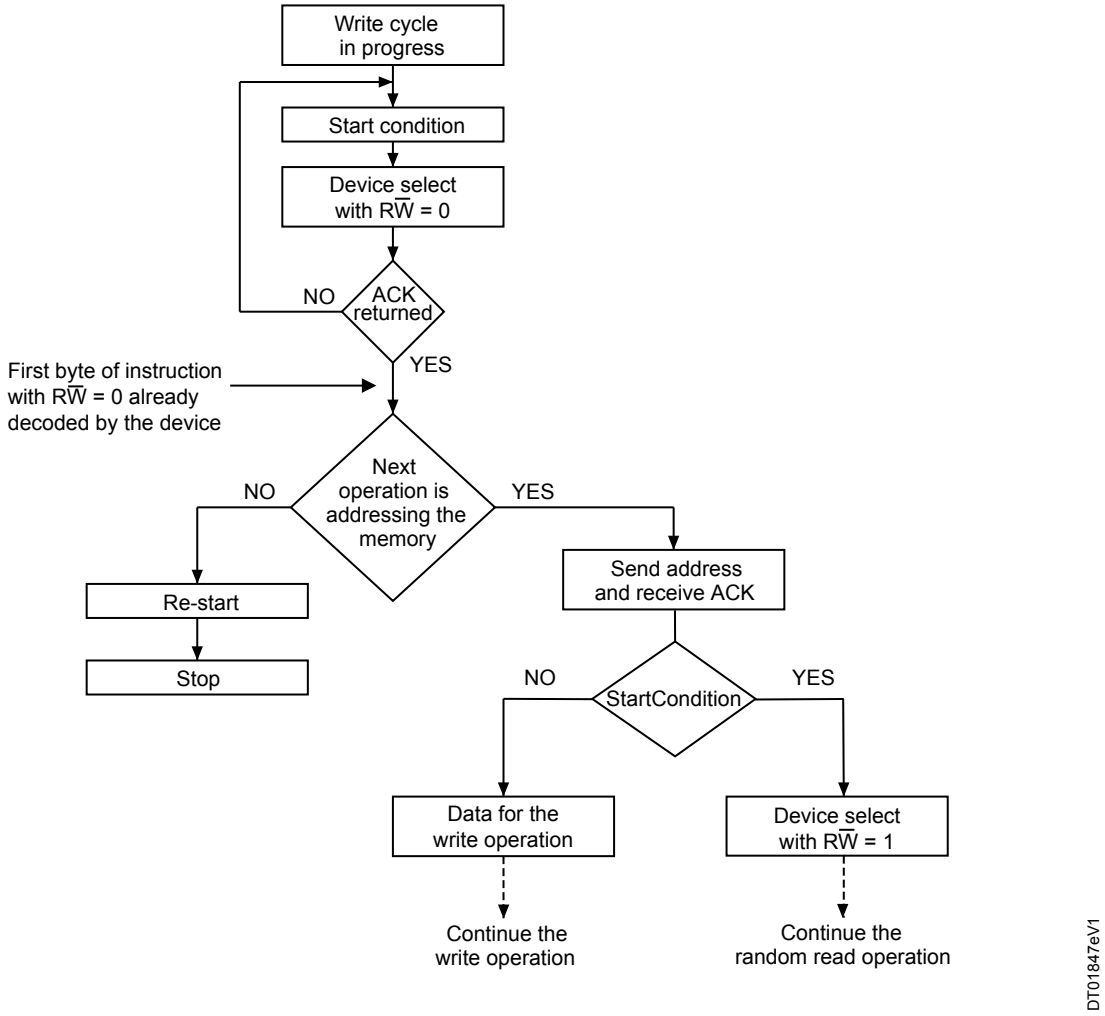
The sequence, as shown in Figure 15, is:

- Initial condition: a write cycle is in progress.
- Step 1: the bus controller issues a start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal write cycle, no ACK is returned and the bus controller goes back to step 1.
- Step 3: if the device has terminated the internal write cycle, it responds with an ACK, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during step 1).

Note: In case of write to configurable device address register when C2, C1 and C0 are reconfigured, the device returns ACK only if:

- *Chip enable address of the device select code is equal to the new C2, C1, and C0 values*
- *An internal write cycle is completed (new C2, C1, and C0 values have been programmed in the chip enable register).*

Figure 15. Write cycle polling flowchart using ACK



1. The seven most significant bits of the device select code of a random read (bottom right box in the figure) must be identical to the seven most significant bits of the device select code of the write (polling instruction in the figure).

6.5 Read operations on memory array

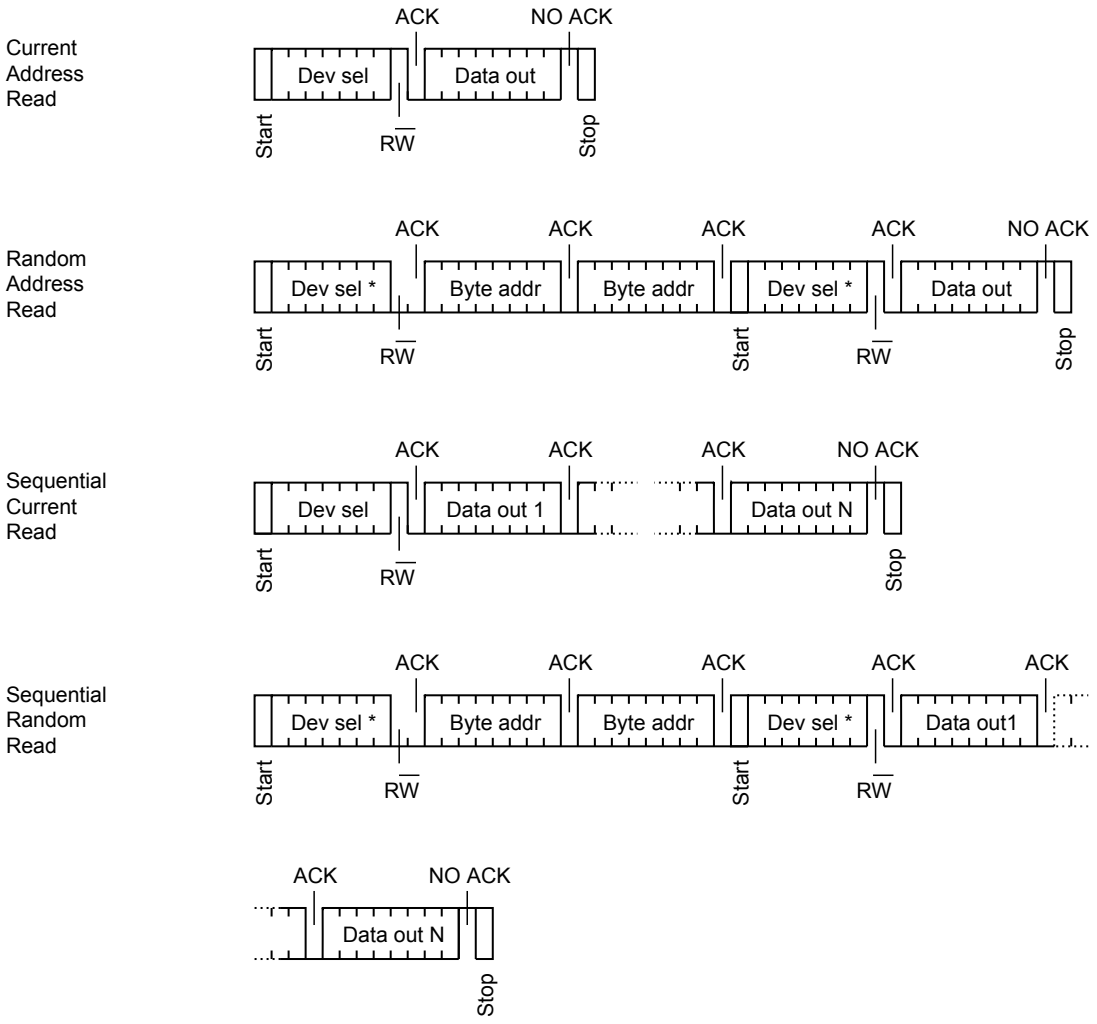
Read operations are performed independently of the SWP register value. MSB bit A15 of the address must be equal to 0.

Following a start condition the bus controller sends a device select code with the RW bit (RW) set to '0'. The device acknowledges this and waits for the two-bytes address. The device responds to each address byte with an acknowledge bit. Then, the bus controller sends another start condition, and repeats the device select code, with the RW bit set to '1'. The device acknowledges this, and outputs the contents of the data. See in Section 5.5 Device addressing (Table 7, Table 8 and Table 9) how to address the memory array.

After each byte read (data out), the device waits for an acknowledgment (data in) during the ninth bit time. If the bus controller does not acknowledge during this ninth time, the device terminates the data transfer and switches to its standby mode.

After the successful completion of a read operation, the device internal address counter is incremented by one, to point to the next byte address.

Figure 16. Read mode sequences



Note: The seven most significant bits of the first device select code of a random read must be identical to the seven most significant bits of the device select code of the write.

6.5.1 Random address read

A dummy write is first performed to load the address into this address counter (as shown in Figure 16) but without sending a stop condition. Then, the bus controller sends another start condition, and repeats the device select code, with the R$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus controller terminates the transfer with a stop condition, as shown in Figure 16, without acknowledging the byte.

6.5.2 Current address read

For the current address read operation, following a start condition, the bus controller only sends a device select code with the R/W bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus controller terminates the transfer with a stop condition, as shown in Figure 16, without acknowledging the byte.

Note: The address counter value is defined by instructions accessing either the memory or the registers or the identification page. When accessing the registers or the identification page, the address counter value is loaded with the registers or the identification page byte location, therefore the next current address read in the memory uses this new address counter value. When accessing the memory, it is safer to use the random address read instruction (this instruction loads the address counter with the byte location to read in the memory) instead of the current address read instruction.

6.5.3 Sequential read

This operation can be used after a current address read or a random address read. The bus controller does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus controller must not acknowledge the last byte, and must generate a stop condition, as shown in Figure 16.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from the memory address 00h.

6.6 Read operations on features

Only the random address read or sequential random read commands are authorized to access the three additional features. The address counter contains a meaningful address value only after these authorized commands have been performed.

6.6.1 Read operations on configurable device address register

Following a start condition the bus controller sends a device select code with the R/W bit ($R\overline{W}$) set to 0. The device acknowledges this and waits for the address bytes where the CDA register is located. The device responds to each address byte with an acknowledge bit. Then, the bus controller sends another start condition, and repeats the device select code, with the $R\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the CDA register. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the configurable device address register.

To terminate the stream of data byte, the bus controller must not acknowledge the byte, and must generate a stop condition, as shown in Figure 17.

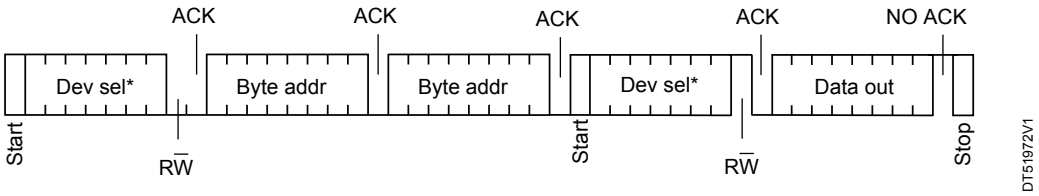
After the successful completion of a read configurable device address, the device internal address counter is not incremented by one, to point to the next byte address. Reading more than one byte occurs in a loop while reading the configurable device address register value.

The configurable device address register cannot be read while a write cycle (t_w) is ongoing.

The configurable device address bits (C2, C1, C0) values can be checked by sending the device select code.

- If the chip enable address b3, b2, b1 sent in the device select code is matching with the C2, C1 and C0 values, the device sends an ACK.
- Otherwise, the device answers no ACK.

Figure 17. Random read configurable device address register



6.6.2 Read operations on software write protection register

Read operations are performed independently of the software write protection register value.

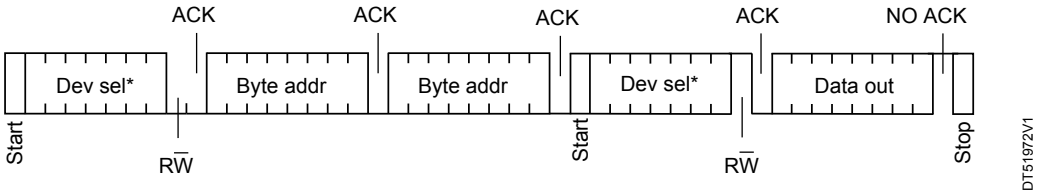
Following a start condition the bus controller sends a device select code with the R/W bit ($\overline{RW}$) set to 0. The device acknowledges this and waits for the address bytes where the SWP register is located. The device responds to each address byte with an acknowledge bit. Then, the bus controller sends another start condition, and repeats the device select code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the SWP register. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the software write protection register.

To terminate the stream of data byte, the bus controller must not acknowledge the byte, and must generate a stop condition, as shown in Figure 18.

After the successful completion of a read operation on SWP, the device internal address counter is not incremented by one, to point to the next byte address. Reading more than one byte loops on reading the SWP register value.

The SWP register cannot be read while a write cycle (t_w) is ongoing.

Figure 18. Random read SWP register



6.6.3 Read operations on identification page

Following a start condition the bus controller sends a device select code with the R/W bit ($R\overline{W}$) set to 0. The device acknowledges this and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit. Then, the bus controller sends another start condition, and repeats the device select code, with the $R\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the identification page. See in Section 5.5 Device addressing (Table 7, Table 8, and Table 9) how to address the identification page.

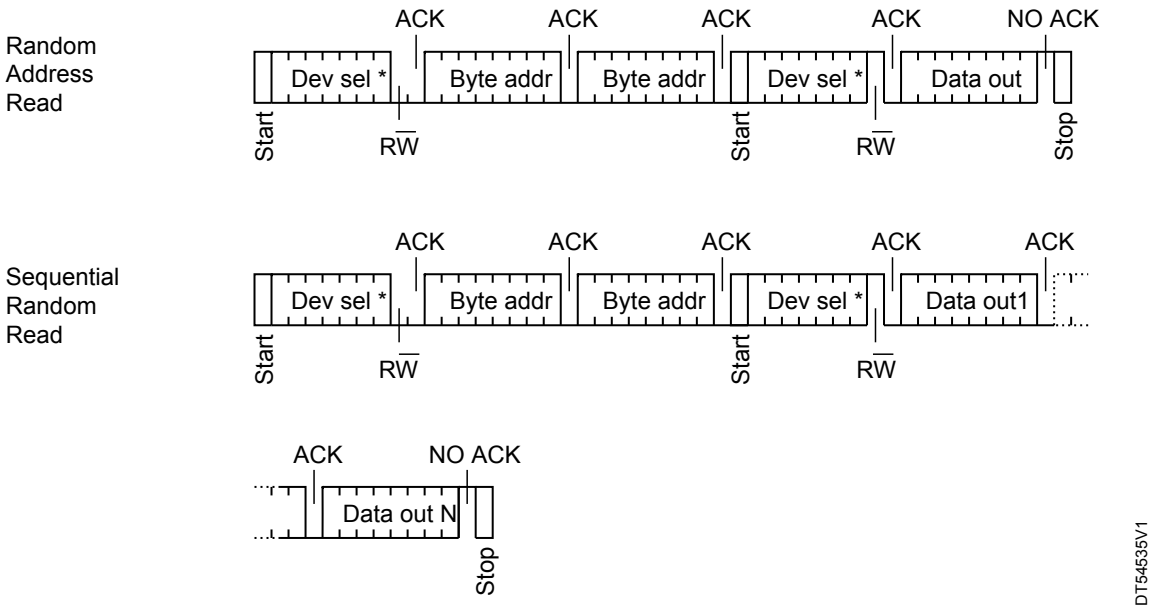
After each byte read (data out), the device waits for an acknowledgment (data in) during the ninth bit time.

The output data of the identification page comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last identification page address (FFh), the address counter “rolls-over”, and the device continues to output data from identification page address 00h.

To terminate the stream of data byte, the bus controller must not acknowledge the byte, and must generate a stop condition, as shown in Figure 19.

If the bus controller does not acknowledge during this ninth time, the device terminates the data transfer as shown in Figure 19 and switches to its standby mode.

Figure 19. Random read identification page



*Note: *: The seven most significant bits of the device select code of a random read must be identical.*

6.6.4 Read the lock status

The lock/unlock status of the identification page can be checked by transmitting a specific truncated command.

Following a start condition the bus controller sends a device select code with the R/W bit ($\overline{RW}$) set to 0. The device acknowledges this and waits for the address bytes where the identification page is located. The device responds to each address byte with an acknowledge bit, and then waits for the data byte. See in Device addressing (Table 1, Table 2, and Table 3) how to address the identification page.

The device returns an acknowledge bit after the data byte if the identification page is unlocked (unlock status) as shown in Figure 20, otherwise a NoAck bit as shown in Figure 21, if the identification page is locked (lock status).

Right after this, it is recommended to transmit to the device a start condition followed by a stop condition, so that:

- Start: the truncated command is not executed because the start condition resets the device internal logic
- Stop: the device is then set back into standby mode by the stop condition

Figure 20. Read lock status (identification page unlocked)

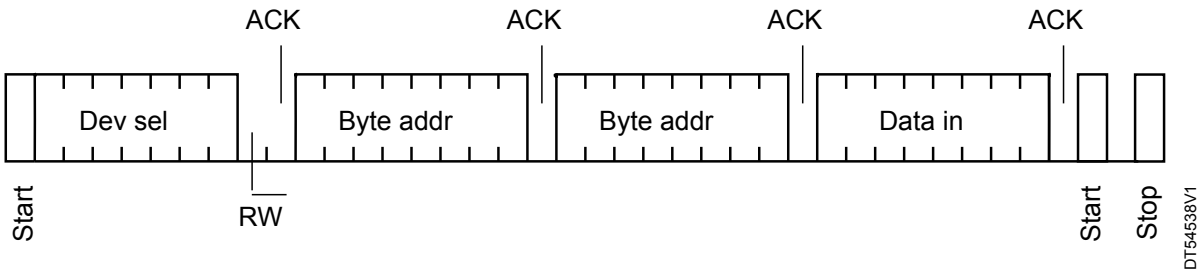
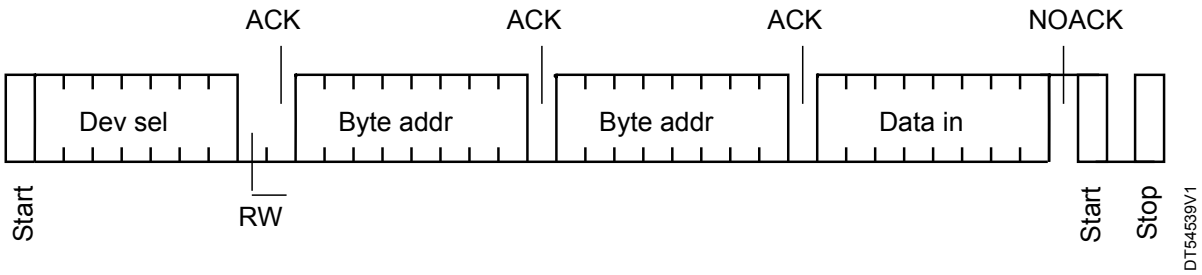


Figure 21. Read lock status (identification page locked)



7 Initial delivery state

At factory delivery, the device is delivered with:

- All the memory array bits set to 1 (each byte contains FFh)
- The CDA register set to 00000000b (00h)
- The SWP register set to 0000000b (00h)
- All the identification page bits set to 1 (each byte contains FFh)

8 Maximum ratings

Stressing the device outside the ratings listed in Table 10 may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	4.6	V
V_{CC}	Supply voltage	–0.50	4.6	V
V_{ESD}	Electrostatic pulse (Human Body model) (2)	-	4000	V

1. *Compliant with JEDEC standard J-STD-020 (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).*
2. *Positive and negative pulses applied on different combinations of pin connections, according to ANSI/ESDA/JEDEC JS-001 (C1=100 pF, R1=1500 Ω, R2 = 500 Ω).*

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 11. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.71	1.89	V
T_A	Ambient operating temperature	-40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 12. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	-	100	pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels(1)	0.252 to 0.912		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

1. *V_{ILmax} = 0.2 × (1.2 + 5%) = 0.252, and V_{IH} min = 0.8 × (1.2 - 5%) = 0.912*

Figure 22. AC measurement I/O waveform

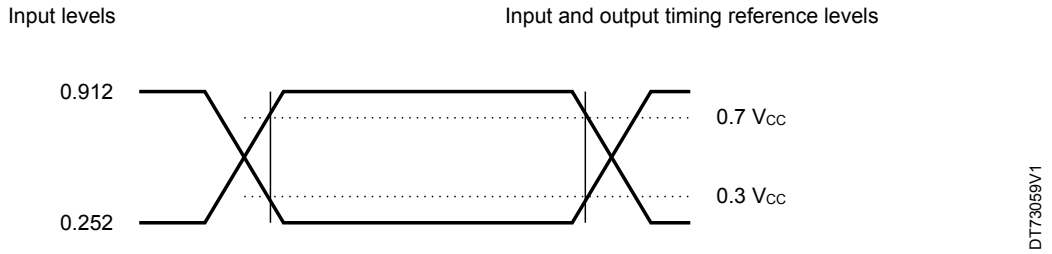


Table 13. Input parameters

Symbol	Parameter (1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF

1. *Evaluated by characterization and qualification - Not tested in production.*

Table 14. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance(1)	$T_A \le 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4 000 000	Write cycles(2)
		$T_A = 85$°C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1 200 000	

1. *The write cycle endurance is evaluated by characterization and qualification- Not tested in production. For devices embedding the ECC functionality, the write cycle endurance is defined for group of four bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer.*
2. *A write cycle is executed when either a write CDA, SWP register, a page write, a byte write , a write identification page or a lock identification page instruction is decoded. When using the byte write, the page write or the write identification page, refer also to Section 6.3 ECC (error correction code) and write cycling.*

Table 15. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention (1)	T_A = 55 °C	200	Year

1. *The data retention behaviour is evaluated by characterization and qualification- not tested in production, while the data retention limit defined in this table is extracted from characterization and qualification results.*

Table 16. DC characteristics

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC} device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	f_C = 400 kHz	-	0.5(1)	mA
		f_C = 1 MHz	-	1(2)	
I_{CC0}	Supply current (Write)	Value averaged over t_W	-	1 (3)	mA
I_{CC1}	Standby supply current	Device not selected, (4) V_{IN} = V_{SS} or 1.14 V	-	1(5)	µA
V_{IL}	Input low voltage (SCL, SDA)	V_{CC}= 1.8 V	–0.45	0.252	V
V_{IH}	Input high voltage (SCL, SDA)	V_{CC}= 1.8 V	0.912	1.32	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V	-	0.2	V

1. *80 µA typical value at 1.8V. Evaluated by characterization - Not tested in production.*
2. *100 µA typical value at 1.8V. Evaluated by characterization - Not tested in production.*
3. *150 µA typical value at 1.8V. Evaluated by characterization - Not tested in production.*
4. *The device is not selected after power-up, after a read instruction (after the stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a write instruction).*
5. *350 nA typical value at 1.8V. Evaluated by characterization - Not tested in production.*

Table 17. AC characteristics in fast mode

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2} (1)	t_F	SDA (out) fall time	20	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(2)	400 (2)	ns
t_{XL1XL2}	t_F	Input signal fall time	(2)	400 (2)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (3)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (4)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write cycle time	-	5	ms
t_{NS} (1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	50	ns
t_{WU} (1)	-	Wake up time (5)	-	5	µs

1. *Evaluated by characterization - Not tested in production.*
2. *It is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.*
3. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
4. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that R_{bus} × C_{bus} time constant is within the values specified in Figure 23.*
5. *Wake up time: Delay between the V_{CC}min stable and the first accepted command*

Table 18. AC characteristics in fast mode plus

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(1)	150 (1)	ns
t_{XL1XL2}	t_F	Input signal fall time	(1)	150(1)	ns
t_{QL1QL2} (2)	t_F	SDA (out) fall time	20(3)	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write cycle time	-	5	ms
t_{NS} (2)	-	Pulse width ignored (input filter on SCL and SDA)	-	50	ns
t_{WU}(2)	-	Wake up time(6)	-	5	µs

1. *There is no min. or max. values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.*
2. *Evaluated by characterization - Not tested in production.*
3. *With CL = 10 pF.*
4. *To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.*
5. *t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in Figure 24.*
6. *Wake up time: Delay between the V_{CC}min stable and the first accepted command*

Figure 23. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

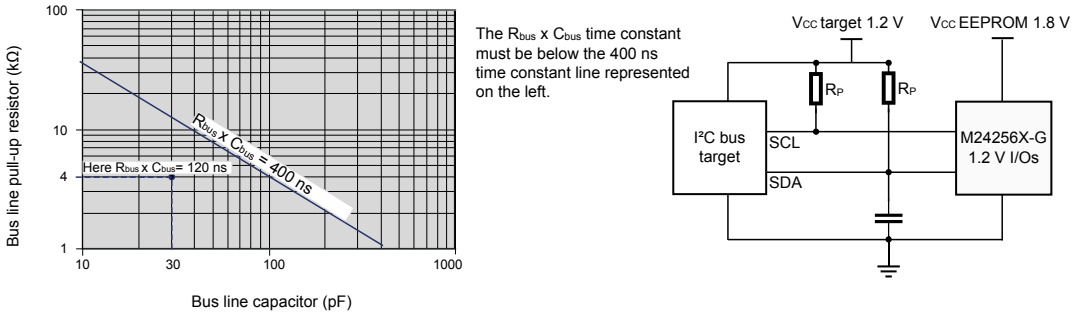


Figure 24. Maximum Rbus value vs. bus parasitic capacitance (Cbus) for an I^2C bus at f_C = 1MHz

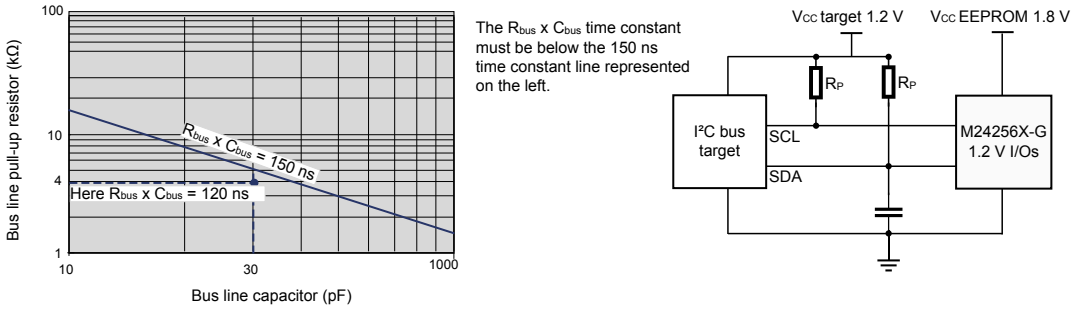
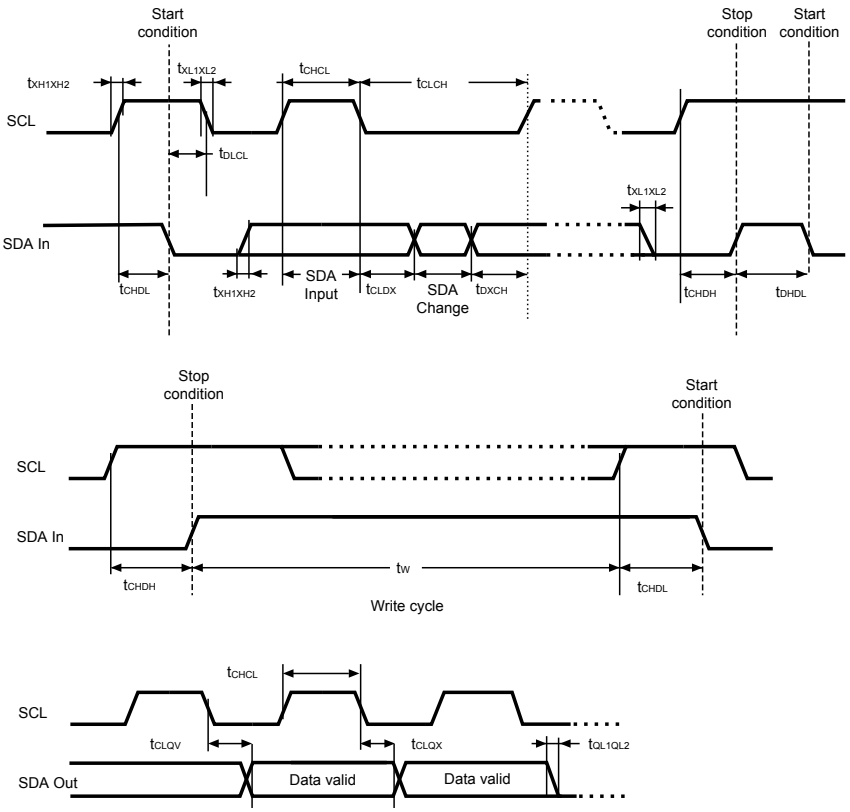


Figure 25. AC waveforms



DT00795j_V1

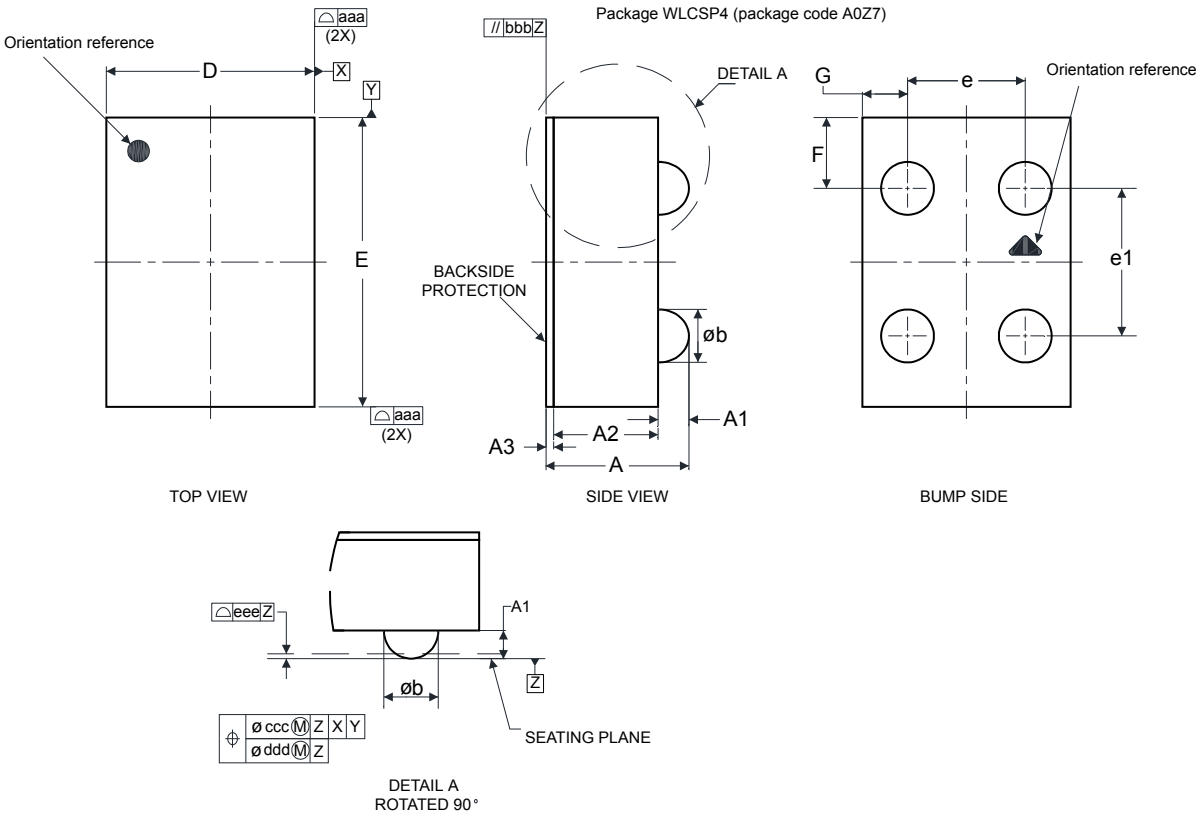
10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 WLCSP4 package information

WLCSP4 is a 4 bumps, 0.703 x 0.977 mm, 0.4 x 0.5 mm pitch thin wafer level chip scale package.

Figure 26. WLCSP4 - Outline



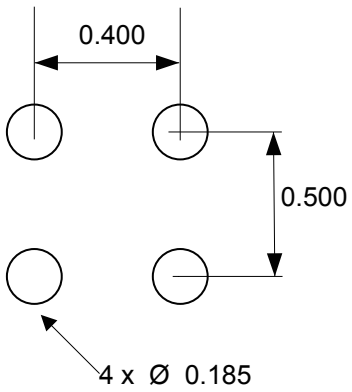
1. Drawing is not to scale.

Table 19. **WLCSP4 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.262	0.295	0.328	0.0103	0.0116	0.0129
A1	-	0.095	0.115	-	0.0037	0.0045
A2	-	0.175	0.190	-	0.0069	0.0075
A3	-	0.025		-	0.0010	-
b[2]	0.165	0.185	0.205	0.0065	0.0073	0.0081
D	0.679	0.703	0.727	0.0267	0.0277	0.0286
E	0.953	0.977	1.001	0.0375	0.0385	0.0394
e	-	0.400	-	-	0.0157	-
e1	-	0.500	-	-	0.0197	-
F	-	0.239	-	-	0.0094	-
G	-	0.152	-	-	0.0060	-
N	-	4	-	-	4	-
aaa	-	-	0.11	-	-	0.0043
bbb	-	-	0.11	-	-	0.0043
ccc	-	-	0.11	-	-	0.0043
ddd	-	-	0.06	-	-	0.0024
eee	-	-	0.06	-	-	0.0024

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *Dimensions measured at the maximum bump diameter parallel to primary datum Z.*

Figure 27. **WLCSP4 - Footprint example**



1. Dimensions are expressed in millimeters.

11 Ordering information

Table 20. Ordering information scheme

Example: M24 256X - G CU 6 T /V F

Device type

M24 = I²C serial access EEPROM

Device function

256X = 256 Kbit (32 K x 8 bit)

Operating voltage

G = V_{CC} = 1.8 V +/- 5% and 1.2 V on I/Os

Package (1)

CU = WLCSP4

Device grade

6 = Industrial: device tested with standard test flow over -40 to 85 °C

Option

T = Tape and reel packing

blank = Tube packing

Process

/V = Manufacturing technology code

Option

Blank = No back side coating

F = Back side coating

1. *ECOPACK2 (RoHS compliant and free of brominated, chlorinated, and antimony oxide flame retardants).*

Note: Parts marked as "ES" or "E" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 21. **Document revision history**

Date	Version	Changes
07-Sep-2023	1	Initial release.

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