MASTERGAN7

Datasheet

650 V GaN half-bridge with gate driver and protections

Features

- Power system-in-package integrating 650 V GaN transistors half-bridge with high-voltage gate driver
- 270 mΩ typ low-side and high-side RDS(ON) with IDS(MAX) = 6 A
- Linear regulators to regulate high-side and low-side driver supply voltage
- Overall driver's propagation delay of 45 ns and 35 ns minimum pulse
- Very fast wake-up time of high-side driver
- Externally adjustable turn-on resistors
- UVLO protection on VCC and high-side driver supply voltage
- Interlocking function
- Dedicated pins for standby and shutdown with fault pin for remote signal
- 3.3 V to 15 V (typ.) compatible inputs with hysteresis and pull-down
- Thermal shutdown protection

Application

- Battery chargers and adapters
- Solar inverters
- Resonant converters
- High-voltage DC-DC converters (Buck, Buck-boost)
- High-voltage PFC, including totem pole configuration

Product status link

MASTERGAN7

Product label

SUSTAINABLE TECHNOLOGY

Description

The MASTERGAN7 is an advanced power system-in-package integrating two enhancement mode GaN transistors in a half-bridge configuration driven by a high-voltage, high frequency gate driver.

The integrated power GaNs have typical RDS(ON) of 270 mΩ and 650 V drain source blocking voltage.

The MASTERGAN7 features linear regulators on both the lower and upper driving sections to optimize driving efficiency. The high side of the embedded gate driver can be supplied by the integrated bootstrap diode. The interlocking function avoids cross-conduction conditions.

The advanced driver section, thanks to small propagation delay, very short wake-up time, and short, minimum on-times, enables high frequency switching operation.

The extended range of input pins as well as the remote signaling pin (FLT) allow easy interfacing with controllers, microcontrollers, or DSP units. The standby pin allows to reduce the power consumption of the device during inactive periods.

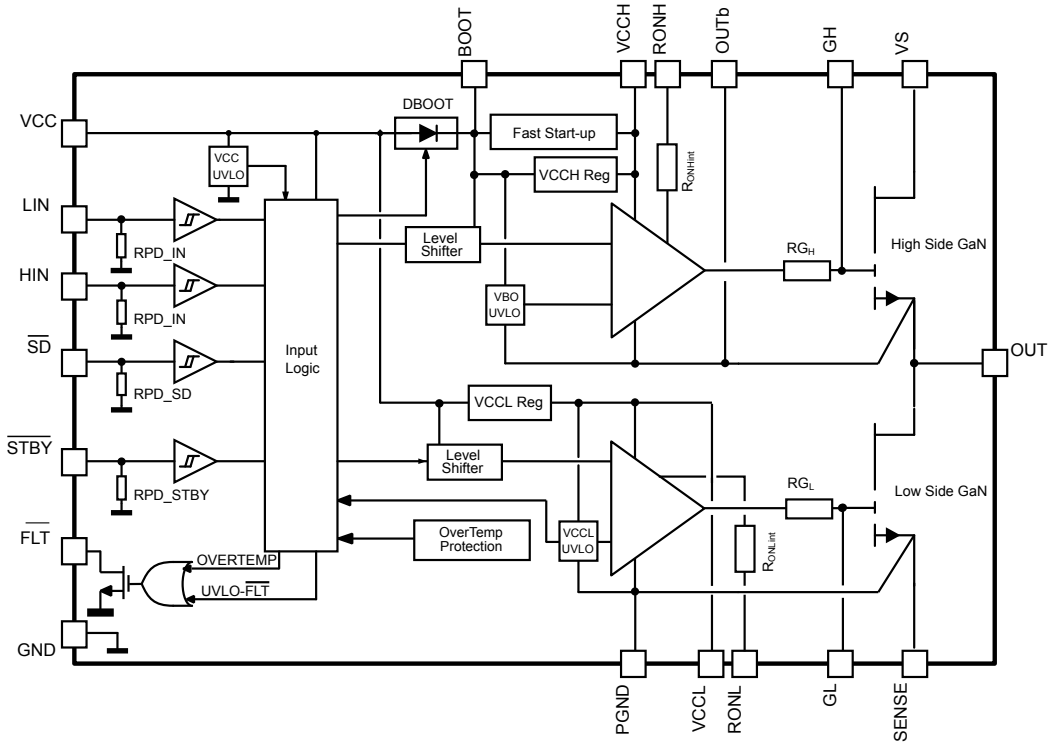
The MASTERGAN7 operates in the industrial temperature range, -40 °C to 125 °C.

The device is available in a compact 9x9x1 mm QFN package.

1 Application diagrams

1.1 Block diagram

Figure 1. **MASTERGAN7 block diagram**



1.2 Typical application schematic

Figure 2. **Typical application schematic – active clamp flyback**

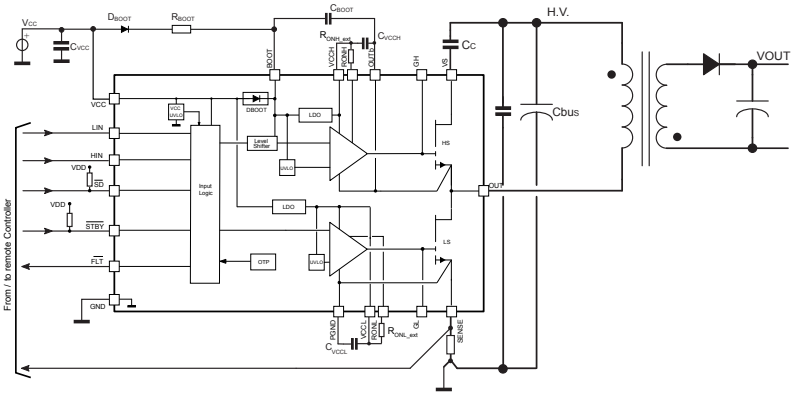


Figure 3. **Typical application schematic – LLC converter**

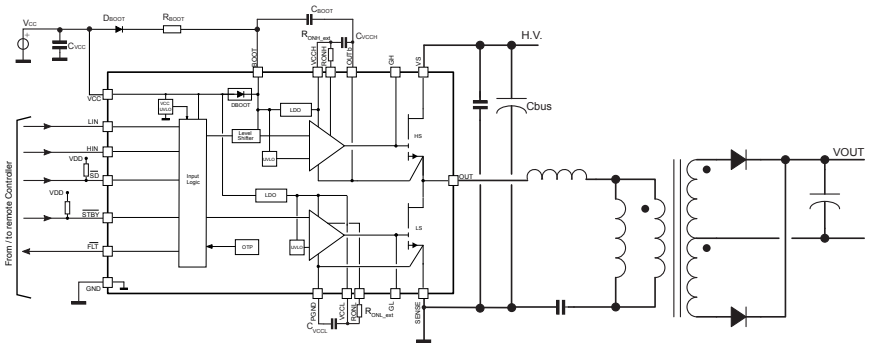
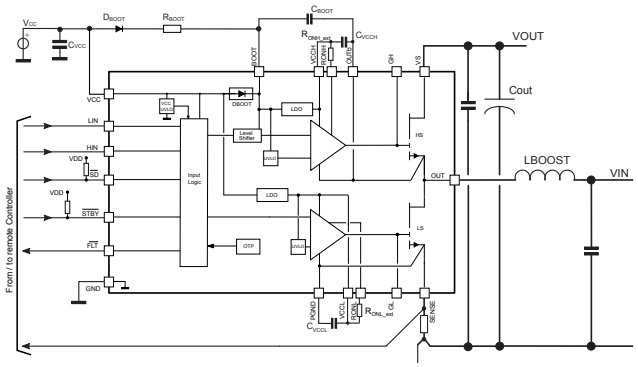


Figure 4. **Typical application schematic – boost converter**



2 Pin description

Figure 5. **MASTERGAN7 pin connection**

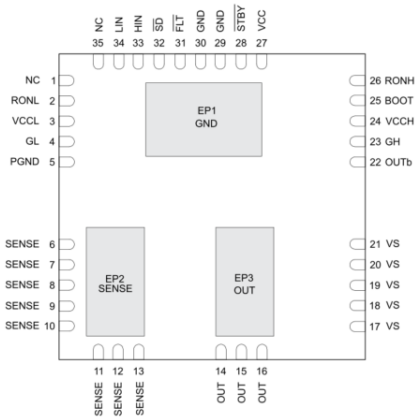


Table 1. **MASTERGAN7 pin list**

Pin N.	Name	Type	Function
1, 35	NC	-	Not connected pin. The pins can be either connected to GND or left floating.
2	RONL	Output	A resistor connected between this pin and VCCL sets the turn-on resistor of the low-side driver. Mounting the resistor as close as possible to the RONL pin optimizes the operation of the driver. It is possible to drive the GaN with minimum internal resistance connecting the RONL pin to the VCCL pin.
3	VCCL	Power	Output of a linear regulator that supplies the output stage of the low-side driver. To optimize the driver's operation, a ceramic capacitor having a typ. value equal to 47 nF (X7R, 16 V) must be placed as close as possible between this pin and PGND.
4	GL	Output	Gate of low-side GaN transistor.
5	PGND	Power	Reference potential of low-side driver and relevant external components (VCCL capacitor and components connected to GL). This pin is internally connected to the source of the low-side GaN transistor.
6,.., 13, EP2	SENSE	Power	Source of the low-side GaN transistor. The exposed pad has both an electrical and thermal purpose: power losses of the low-side transistor are dissipated soldering EP2 to the proper copper area.
14,.., 16, EP3	OUT	Power	Middle point of half-bridge. The exposed pad has both an electrical and thermal purpose: power losses of the high-side transistor are dissipated soldering EP3 to the proper copper area.
17...21	VS	Power	Drain of high-side GaN transistor.
22	OUTb	Power	Reference potential of the high-side driver and relevant external components (BOOT capacitor, VCCH capacitor, and components connected to GH). This pin is internally connected to the source of the high-side GaN transistor.
23	GH	Output	Gate of the high-side GaN transistor.
24	VCCH	Power	Output of the linear regulator that supplies the output stage of the high-side driver. To optimize the driver's operation, a ceramic capacitor having a value equal to 47 nF (X7R, 16 V) must be placed as close as possible between this pin and OUTb.

Pin N.	Name	Type	Function
25	BOOT	Power	Supply voltage of the high-side floating driver. A ceramic capacitor equal or greater than 47 nF (X7R, 50 V) must be placed as close as possible between this pin and OUTb. The input of the high-side driver regulator is internally connected to this pin.
26	RONH	Output	A resistor connected between this pin and VCCH sets the turn-on resistor of the high-side driver. Mounting the resistor as close as possible to the RONH pin optimizes the operation of the driver. It is possible to drive the GaN with minimum internal resistance connecting the RONH pin to the VCCH pin.
27	VCC	Power	Supply voltage of logic section. A small bypass capacitor (100 nF typ.), very close to the pin, is required to get a clean bias voltage for the signal part of the IC. The large bulk capacitor that is normally used to supply the controller is sufficient to supply MasterGaN as well: if not present, a value larger than 2.2 µF is suggested. The input of the low-side driver regulator is internally connected to this pin.
28	STBY	Input	Standby mode activation pin. Setting this pin to GND, the IC enters a low consumption mode to facilitate the design of low-consumption topologies. An internal pull-down resistor is there to avoid uncertain voltage application when the IC is not biased.
29, 30, EP1	GND	Power	Ground pin. Common potential of the logic section of the device. The exposed pad has both an electrical and thermal purpose: power dissipation of linear regulators, drivers, and level shifter units (especially during high frequency operation) can be dissipated soldering EP1 to the proper copper area.
31	FLT	Output	Fault signaling pin. An open drain MOSFET is turned on to pull the FLT pin down when UVLO, standby, and overtemperature protection are active. Connect to GND if not used.
32	SD	Input	Shutdown pin. When this pin is pulled to GND, the IC immediately interrupts the switching activity defined by LIN and HIN. The internal pull-down resistor is there to avoid uncertain voltage application when the IC is not biased.
33	HIN	Input	High-side logic input pin. Driving pulses to control the high-side switch can be applied to this pin. The Schmitt trigger comparator, 20 V tolerant, buffers the input signal before driving level shifters.
34	LIN	Input	Low-side logic input pin. Driving pulses to control the low-side switch can be applied to this pin. The Schmitt trigger comparator, 20 V tolerant, buffers the input signal before driving level shifters.

3 Electrical data

3.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 2 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages referred to ground pins unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
$V_{VS-OUT,max}$	High-side GaN drain-to-source blocking voltage	T_J = 25 °C, OUT = GND, DC voltage, I_{VS} < 20 µA	650	V
		t_{PULSE} < 10 µs(1)	750	V
I_{D_max}	Drain current (per GaN transistor)	DC @ T_{CB} = 25 °C(2)(1)	6	A
		DC @ T_{CB} = 100 °C(2)(1)	4	A
		Peak @ T_{CB} = 25 °C(2)(1)(3)	8	A
VCC	Logic supply voltage		-0.3 to 21	V
PGND	Low-side driver ground vs. logic ground	VCC = 14 V	-7 to 7	V
$V_{VCC-PGND}$	Logic supply vs. low-side driver ground		-0.3 to 21	V
V_{VCCL_max}	Regulated low-side driver supply vs. logic ground		-0.3 to 14	V
V_{LS}, V_{HS}	Regulated drivers supply voltage(4)(5)(6)		-0.3 to 7	V
I_{LS_OUT}, I_{HS_OUT}	Internal regulators maximum current(4)(5) (6)		Self-limited	V
$V_{VCC-VCCL\_max}$	Maximum low-side dropout voltage		-0.3 to self-regulated	V
V_{GL_max}	Low-side gate to PGND voltage	DC values	-0.3 to VCCL+0.3	V
V_{RONL_max}	Low-side turn-on resistor pin max. voltage		(V_{GL}-0.3 V) to (VCCL+0.3 V)	V
V_{BOOT}	BOOT pin voltage referred to GND		-0.3 to 621	V
V_{BO}	High-side regulator input voltage(7)(5)		-0.3 to 21	V
$V_{BOOT-VCCH\_max}$	Maximum high-side dropout voltage		-0.3 to self-regulated	V
V_{GH_max}	High-side gate to OUTb voltage(7)		-0.3 to VCCH+0.3	V
V_{RONH_max}	High-side turn-on resistor pin max. voltage		(V_{GH}-0.3 V) to (VCCH+0.3 V)	V
$P_{LossRint}$	Maximum power dissipation of internal resistances(8)(6)		20	mW
R_{BOOT}	Minimum external bootstrap diode series resistance (if present)		2.7	Ω
dV_{OUT}/dt_max	Maximum OUT voltage slew rate		120	V/ns
V_{in_max}	Logic inputs voltage range (LIN, HIN, SD, STBY, FLT)		-0.3 to 21	V
I_{FLT_max}	Maximum FLT pin current (inward)	VCC = 7.0 V	10	mA

Symbol	Parameter	Test condition	Value	Unit
T_J	Junction temperature		-40 to 150	°C
T_s	Storage temperature		-55 to 150	°C

1. *Range estimated by characterization, not tested in production.*
2. *T_{CB} is the temperature of the case-exposed pad.*
3. *Value specified by design factor, pulse duration limited to 10 µs and junction temperature.*
4. *PGND internally connected to SENSE.*
5. *$V_{LS} = V_{VCCL-PGND}$, $V_{HS} = V_{VCCH-OUTb}$, $V_{BO} = V_{BOOT-OUTb}$*
6. *The outputs of internal low-side and high-side voltage regulators (V_{LS} and V_{HS}) must not be connected to external load or voltage sources. External components connected to gate drivers must comply with $P_{LossRint}$ AMR value.*
7. *OUTb internally connected to OUT.*
8. *See GaN transistor for power losses estimation.*

3.2 Recommended operating conditions

All voltages referred to ground pins unless otherwise specified. The junction temperature must be maintained within the recommended operating condition with proper thermal design.

Table 3. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCC	Logic supply voltage		9		18	V
$V_{VCC-PGND}$	Logic supply voltage vs. PGND		7.5		18	V
PGND	Low-side driver ground		-3		3	V
V_{BO}	$V_{BOOT-OUTb}$ pin voltage	(1)	7.5		20	V
V_{OUT}	OUT pin voltage bus		-11(2)		520(3)	V
VCCL	Low side driver voltage vs. GND		3			
V_{BOOT}	BOOT to GND voltage	(4)	0		540	V
V_i	Logic inputs voltage range		0		20	V
R_{RONL}, R_{RONH}	External RON resistors		0		220	Ω
C_{VCCH}, C_{VCCL}	Driver supply voltage bypass capacitors(5)		47			nF
C_{BO}	High-side driver linear regulator input capacitors(5)		C_{VCCH}			nF
t_{DT}	Typical deadtime		50			ns
t_{IN_MIN}	Minimum duration of input pulse	LIN at VBO > 6 V	50			ns
		LIN at VBO < 6 V(6)	250			ns
$t_{IN\_MIN\_N}$	Minimum duration of input voltage drop		120			ns
F_{sw}	Switching frequency(7)	Duty cycle = 50%			2	MHz
T_{J-op}	Junction temperature		-40		125	°C

1. *$V_{BO} = V_{BOOT}$-V_{OUTb}*
2. *V_{BO} = 20 V, VCC= 9 V*
3. *Recommended DC voltage applied to half bridge during normal hard switching operation is 450 V*
4. *BOOT to GND must be ≥ 5 V to propagate high-side commands*
5. *See Table 1*
6. *Recommended LIN pulse duration to ensure a sufficient VBO charge when external components are $C_{BO} = C_{VCCH}$ = 47 nF and external Dboot with RBOOT = 3.3 Ω. Refer to GaN transistor for further details.*

7. *Actual limit depends on power dissipation constraints.*

3.3 Thermal data

Thermal values are calculated by simulation with the following boundary conditions.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
Rth(J-CB)	Thermal resistance junction to each GaN transistor exposed pad, typical	2.8	°C/W
Rth(J-A)	Thermal resistance junction-to-ambient(1)	17.8	°C/W

1. *The junction to ambient thermal resistance is obtained simulating the device mounted on a 2s2p (4 layer) FR4 board such as JESD51-5.7 with 6 thermal vias for each exposed pad. Power dissipation is uniformly distributed over the two GaN transistors.*

3.4 Electrical sensitivity characteristics

Table 5. ESD protection ratings

Symbol	Parameter	Test condition	Value	Unit
HBM	All pins to GND		2	kV
CDM	All pins to GND		1	kV

4 Electrical characteristics

Testing conditions: T_J = 25 °C, VCC = V_{BO} = SD = STBY = 12 V; FLT = floating; RONL = VCCL; RONH = VCCH, SENSE = GND = 0 V; C_{VCCH} = C_{VCCL} = 47 nF (X7R,16 V), C_{BO} = 220 nF (X7R, 50 V), all voltages referred to GND, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
GaN power transistor - electrical characteristics						
$V_{(BR)DS\_H}$	Drain to source blocking voltage	V_{VS-OUT}; DC voltage, I_{DSS} < 12 µA; GH = OUTb(1)	650			V
		V_{VS-OUT}; t_{PULSE} = 0.1 µs(2)	750			
$V_{GS(th)}$	Gate to source threshold voltage	LIN = 3.3 V, RONL = GL = 10 k to OUT, SENSE = GND, $I_{OUT-SENSE}$ =1.7 mA		1.7		V
		HIN = 3.3 V, OUT = GND, RONH = GH = 10 k to VS, I_{VS-OUT} = 1.7 mA				
I_{DSS}	Zero gate voltage drain current	V_{VS-OUT} = 650 V; GH = OUTb		0.6	12	µA
		$V_{OUT-SENSE}$ = 650 V; GL = PGND				
I_{GS}	Gate to source current	V_{VS-OUT} = 0V, RONH = GH, OUT = GND, $V_{GH-OUTb}$ = 6 V		30		µA
		$V_{OUT-SENSE}$ = 0V, RONL = GL, $V_{GL-PGND}$ = 6 V				µA
$R_{DS(on)}$	GaN transistors drain source resistance	$I_{OUT-SENSE}$ or I_{VS-OUT} = 2 A		270	350	mΩ
		$I_{OUT-SENSE}$ or I_{VS-OUT} = 2 A; T_J = 125°C(2)		520		
GaN power transistor – characterization values						
Q_G	Total gate charge	LS: $V_{OUT-SENSE}$ = 400 V; $V_{GL-PGND}$ = 0 to 6V (2) HS: V_{VS-OUT} = 400 V; $V_{GH-OUTb}$ = 0 to 6V (2)		1.5		nC
Q_{OSS}	Output charge	LS: V_{GL} = PGND; $V_{OUT-SENSE}$ = 400 V; F = 100 kHz(2) HS: V_{GH} = OUTb; V_{VS-OUT} = 400 V; F = 100 kHz(2)		13		nC
E_{OSS}	Output capacitance stored energy			1.6		µJ
C_{OSS}	Output capacitance			15		pF
$C_{O(ER)}$	Effective output capacitance energy related	LS: V_{GL} = PGND; $V_{OUT-SENSE}$ = 0 to 400 V(2) HS: V_{GH} = OUTb; V_{VS-OUT} = 0 to 400V (2)		20		pF
$C_{O(TR)}$	Effective output capacitance time related			28		pF
Q_{RR}	Reverse recovery charge	(2)		0		nC
I_{RRM}	Reverse recovery current	(2)		0		A

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SD}	Reverse conduction source to drain voltage	LS: $V_{SD} = V_{SOURCE} - V_{OUT}$; V_{GL} = PGND; I_{SOURCE} = 1.1 A(2) HS: $V_{SD} = V_{OUT} - V_{VS}$; V_{GH} = OUTb; I_{OUT} = 1.1 A(2)		2.1		V
GaN power transistor – inductive load switching characteristics						
$td_{(on)}$	Turn-on time	LS: $V_{OUT} = V_{VS}$ = 400 V; V_{SENSE} = 0 V, I_D = 1.1 A HS: V_S = 400 V;		70		ns
t_{fall}	Drain to source voltage fall time			4		ns
$td_{(off)}$	Turn-off time			70		ns
t_{rise}	Drain to source voltage rise time	$V_{OUT} = V_{SENSE}$ = 0 V, I_D = 1.1 A See Figure 1 for definitions(2)		4		ns
E_{on}	Turn-on switching losses			16		µJ
E_{off}	Turn-off switching losses			3		µJ
Logic section supply						
VCC_{thON}	VCC UVLO turn-on threshold		8	8.5	9	V
VCC_{thOFF}	VCC UVLO turn-off threshold		7.5	8	8.5	V
VCC_{hys}	VCC UV hysteresis		0.3	0.5	0.7	V
I_{QVCCU}	VCC undervoltage quiescent supply current	VCC = 7.0 V		570	760	µA
I_{QVCC}	VCC quiescent supply current(3)	STBY = SD = 3.3 V; LIN = HIN = 0 V; V_{BO} = 15 V		860	1100	µA
		LIN = STBY = SD = 3.3 V; HIN = 0 V; V_{BO} = 15 V		1030	1290	µA
I_{SBVCC}	VCC standby supply current(3)	STBY = 0 V		500	650	µA
I_{SVCC}	VCC switching supply current(3)	STBY = SD = 5 V; V_{BO} = 15 V; V_{OUT} = 0 V; fsw = 500 kHz (dc = 50%)		1.3		mA
$t_{startup}$	VCC startup time from VCC = 9 V to GL=on	LIN = STBY = SD = 3.3 V; HIN = 0 V;		3	12	µs
Low-side regulator and driver section						
V_{LDOL}	Low-side regulator output voltage	I_{VCCL} < 10 mA_{DC}	5.55	6	6.45	V
		T_J = -40 °C to +125 °C(2)	5.4		6.6	V
V_{DROP_L}	Low-side regulator drop-out voltage	VCC = 9 V; PGND = 3 V; I_{VCCL} = 10 mA			0.6	V
V_{LSthON}	V_{LS} UVLO turn-on voltage		4.45	4.8	5.15	V
		T_J = -40 to +125 °C(2)			5.25	V
$V_{LSthOFF}$	Low-side driver UVLO turn-off voltage		4.3	4.65	4.95	V
		T_J = -40 to +125 °C(2)	4.2			V
$V_{LSthHYS}$	Low-side driver UVLO hysteresis			0.2		V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{BLEED}	Low-side gate bleeder	VCCL = VCC = 0 V, PGND = GND, VGL = 0.1 V	75	100	125	kΩ
RON_{INTL}	Low-side internal RON resistor	LIN = 3.3 V, I_{RONL_in} = 20 mA, GL=PGND		75		Ω
$ROFF_L$	Low-side ROFF resistor	LIN = 0 V, I_{GL_in} = 20 mA		2.2		Ω
High-side driver section (supply +LDO + driver out)						
$VLDO_H$	High-side regulator output voltage	I_{VCCL} < 10 mA_{DC}	5.55	6	6.45	V
		T_J = -40 °C to +125 °C(2)	5.4		6.6	V
V_{BOthON}	High-side output driver enable voltage			3.1		V
		T_J = -40 °C to +125 °C(2)	2.54		3.5	V
V_{DROP_H}	High-side regulator drop-out voltage	BOOT = 12 V; OUTb = 6 V; I_{VCCH} = 10 mA			0.6	V
I_{QBO}	VBO quiescent supply current	STBY = SD = 3.3 V; LIN = HIN = 0 V; VBO = 12 V		280	380	µA
		HIN = STBY = SD = 3.3 V; LIN = 0 V; VBO = 12 V		350	470	µA
I_{SBO}	VBO switching supply current	SD = STBY = 3.3 V; VS = 0; V_{BOOT} = 12 V fsw = 500 kHz		2.3		mA
$t_{BOstart}$	High-side startup time	HIN = STBY = SD = 3.3 V; LIN = 0 V to 3.3 V;		210	350	ns
I_{LK}	High-voltage leakage current	BOOT = OUT = 600 V			11	µA
R_{DBOOT}	Bootstrap diode on resistance	LIN = STBY = SD = 3.3 V; HIN = 0 V; $V_{VCC\ -\ BOOT}$ = 0.5 V		120	140	Ω
RON_{INTH}	High-side internal RON resistor	HIN = 3.3 V, I_{RONH_in} = 20 mA, GH = OUTb		75		Ω
$ROFF_H$	High-side ROFF resistor	HIN = 0 V, I_{GL_in} = 20 mA		2.2		Ω
Logic inputs and timings						
V_{il}	Low-level logic threshold voltage	T_J = 25 °C	1.1	1.3	1.45	V
		T_J = -40 °C to +125 °C(2)	0.8			
V_{ih}	High-level logic threshold voltage	T_J = 25 °C	2	2.27	2.5	V
		T_J = -40 °C to +125 °C(2)			2.7	
V_{ihys}	Logic input threshold hysteresis		0.7	0.96	1.2	V
I_{INh}	LIN, HIN logic ‘1’ input bias current	LIN, HIN = 3.3 V	15	22	36	µA
I_{INl}	LIN, HIN logic ‘0’ input bias current	LIN, HIN = 0 V			1	µA
R_{PD_IN}	LIN, HIN pull-down resistor	LIN, HIN = 3.3 V		150		kΩ
I_{SDh}	SD logic ‘1’ input bias current	SD = 3.3 V	7	10	15	µA
I_{SDl}	SD logic ‘0’ input bias current	SD = 0 V			1	µA

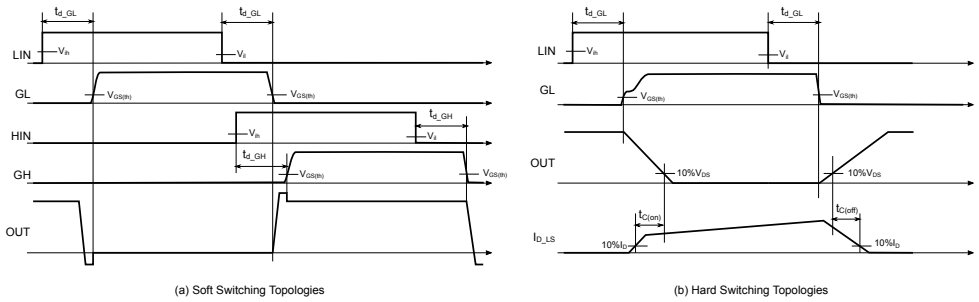
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{PD_SD}	SD pull-down resistor	SD = 3.3 V		330		kΩ
I_{STBYh}	STBY logic '1' input bias current	STBY = 3.3 V	7	10	15	µA
I_{STBYl}	STBY logic '0' input bias current	STBY = 0 V			1	µA
R_{PD_STBY}	STBY pull-down resistor	STBY = 3.3 V		330		kΩ
R_{ON_FLT}	FLT on resistance	V_{FLT} = 400 mV; VCC = 12 V	60	80	135	Ω
		V_{FLT} = 400 mV; VCC = 3.3 V	90	145	200	Ω
I_{OL_FLT}	FLT low-level sink current	T_J = 25 °C; V_{FLT} = 400 mV; VCC = 3.3 V	3	5	7	mA
I_{FLTh}	FLT high-level bias current (when off)	V_{FLT} = 3.3 V			1	µA
I_{FLTl}	FLT low-level bias current (when off)	V_{FLT} = 0 V			1	µA
$V_{VCC-FLT}$	Min. VCC voltage forcing FLT low	(2)			3.3	V
t_{Don_GL}, t_{Don_GH}	LIN to GL (HIN to GH) turn-on propagation delay	SD = STBY = 3.3 V; t_{PULSE} > 60 ns;	40	55	70	ns
t_{Doff_GL}, t_{Doff_GH}	LIN to GL (HIN to GH) turn-off propagation delay	SD = STBY = 3.3 V; t_{PULSE} > 120 ns;	40	55	70	ns
t_{INmin}	Minimum input positive pulse width				35	ns
		T_J = -40 °C to +125 °C(2)			40	ns
t_{INmin_N}	Minimum input voltage drop width	(2)			110	ns
		T_J = -40 °C to +125 °C(2)			120	ns
t_r	GL / GH rise time	(2)		5		ns
t_f	GL / GH fall time	(2)		5		ns
t_{SDon}	SD to Gx turn-on propagation delay	LIN or HIN = STBY = 3.3 V; t_{PULSE} > 120 ns;	45	75	105	ns
t_{SDoff}	SD to Gx turn-off propagation delay	LIN or HIN = STBY = 3.3 V; t_{PULSE} > 120 ns;	40	70	100	ns
$t_{STBYoff}$	Standby to output turn-off delay time	STBY = 3.3 V to 0 V	40	70	100	ns
t_{STBY}	Minimum time to enter low consumption	STBY = 3.3 V to 0 V(2)	0.7		2	µs
$t_{STBY-FLT}$	Time to signal standby mode entering	STBY = 3.3 V to 0 V, FLT = 10 kΩ pull up to VCC		1		µs
t_{WU}	Wake-up time from standby	STBY = 0 V to 3.3 V, LIN = 3.3 V; *(time from STBY rising to GL = high)*			500	ns
t_{WU_FLT}	Standby end signaling	STBY = 0 V to 3.3 V, FLT = 10 kΩ pull up to STBY *(Time from STBY rise to VFLT 1.8 V)*		0.5	3.5	µs
Overtemperature protection						

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature	(2)		175		°C
T_{HYS}	Temperature hysteresis	(2)		20		°C
t_{TSD}	OT protection enabling time after STBY=high	(2)			20	µs

1. *Tested on wafer*
2. *Not tested in production: value estimated by characterization*
3. *OUTb internally connected to OUT*

4.1 Characterization figures

Figure 6. Switching waves diagram



(a) Soft Switching Topologies

(b) Hard Switching Topologies

Figure 7. Typ. I_D vs. V_{DS} at T_J = 25 °C

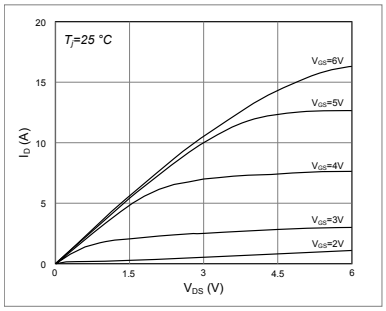


Figure 8. Typ. I_D vs. V_{DS} at T_J = 125 °C

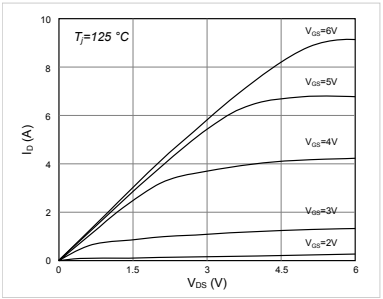


Figure 9. R_{DSON} vs. V_{GS} @ 25 °C

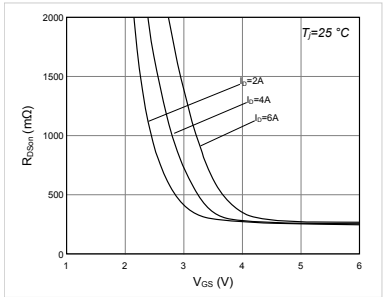


Figure 10. R_{DSON} vs. V_{GS} @ 125 °C

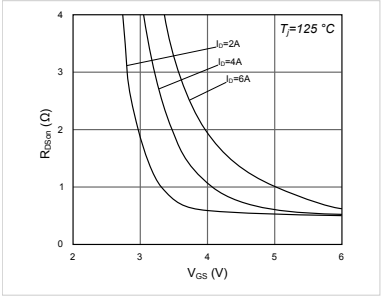


Figure 11. I_D vs. V_{GS}

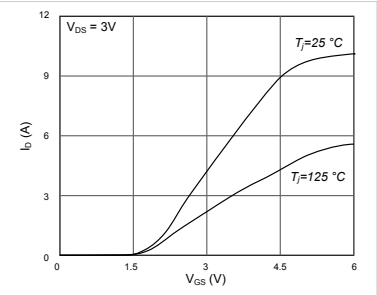


Figure 12. R_{DSON} vs. T_J (normalized to R_{DSON} @ 25 °C)

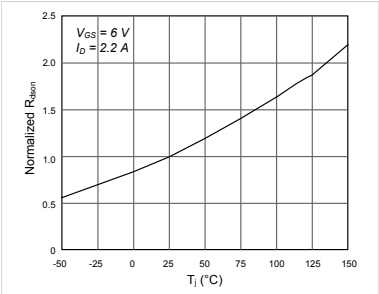


Figure 13. Reverse conduction @ 25 °C

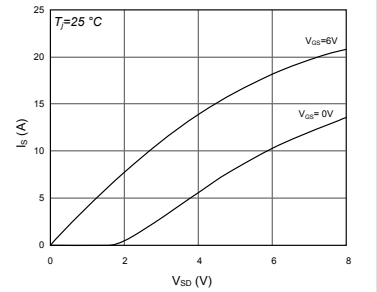


Figure 14. Reverse conduction @ 125 °C

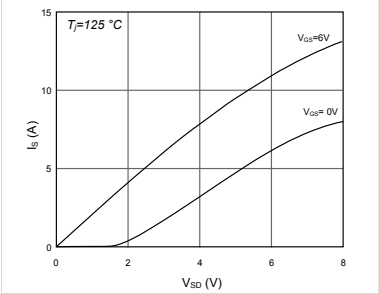


Figure 15. Vth vs. TJ, (normalized to Vth @ T_J = 25 °C)

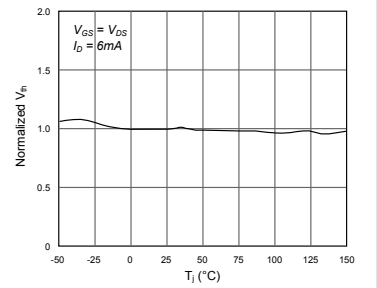


Figure 16. I_G vs. V_{GS}

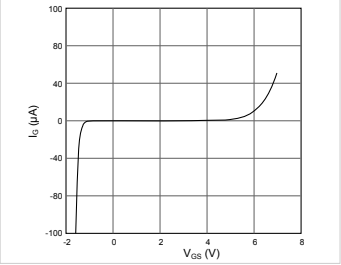


Figure 17. Max dissipated power vs. T_{CB}

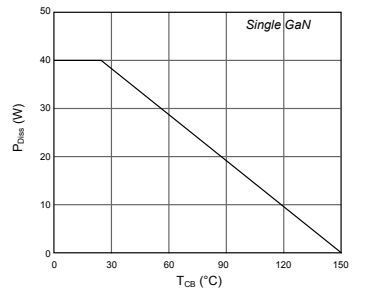


Figure 18. Safe operating area

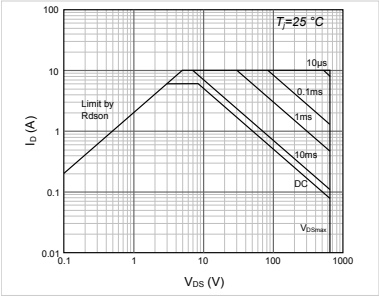


Figure 19. Typ. gate charge

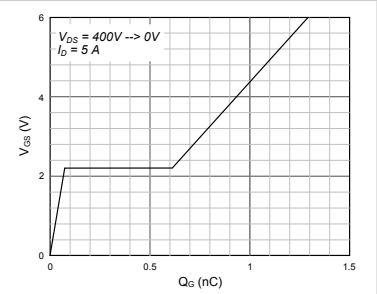


Figure 20. Typ. drain capacitance vs. V_{DS}

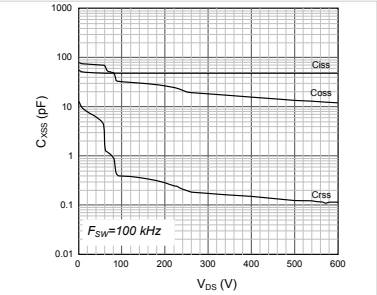


Figure 21. Typ. E_{oss} vs. V_{DS}

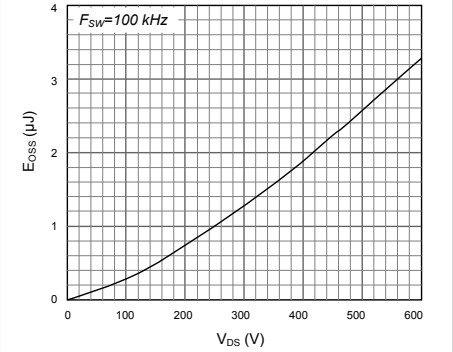


Figure 22. Internal bootstrap diode resistance vs. T_J

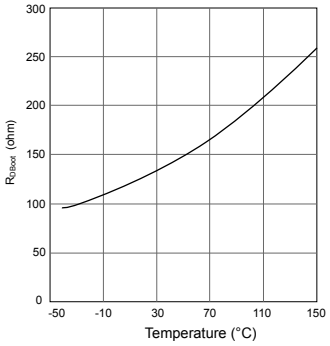


Figure 23. VCC_{thon} / VCC_{thoff} vs. T_J

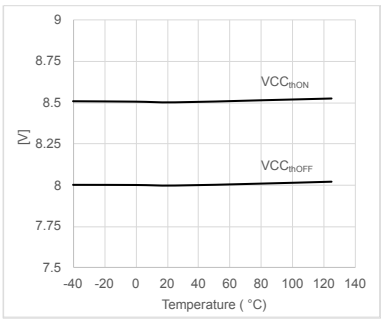


Figure 24. V_{LDOX} vs. T_J

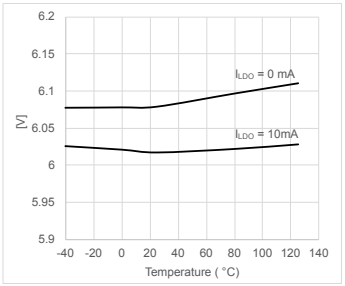


Figure 25. Quiescent current vs. T_J (I_{QCC}, I_{QBO}, I_{SBY})

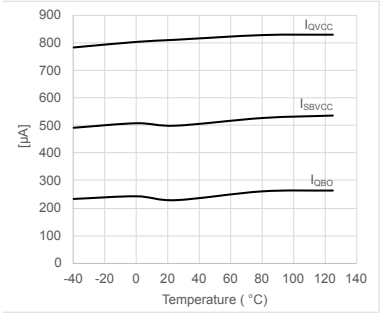


Figure 26. Switching current consumption vs. T_J (I_{SCC}, I_{SBO})

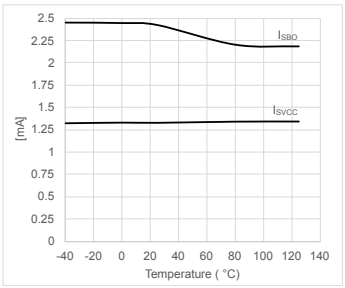


Figure 27. Vix vs. TJ

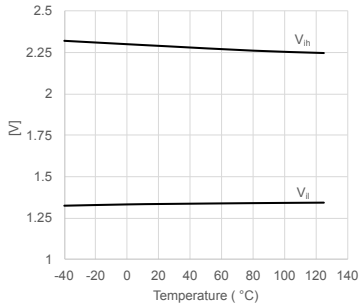


Figure 28. Tdelay vs. T_J

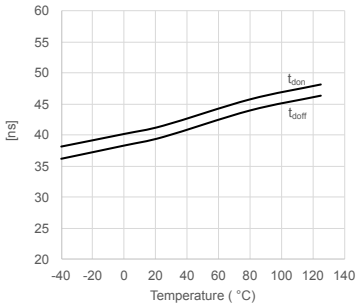


Figure 29. OUT falling slope vs. RONL @ LS on (20% - 80%)

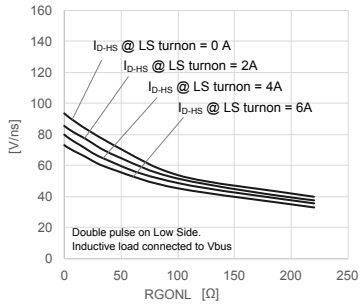
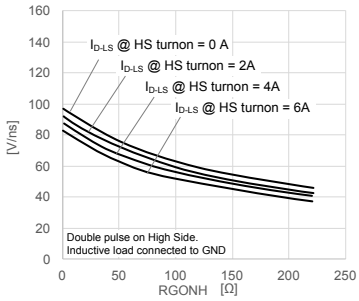


Figure 30. OUT rising slope vs. RONH @ HS on



5 Device description

5.1 Device structure

Figure 1 is a simplified version of the block diagram of the MASTERGAN7. It consists of basic structures described in the following sections.

5.1.1 GaN transistors

They are the power switches that implement the switching stage of the power topology. Integrated driving resistors are also embedded. Furthermore, GaN's gate terminal is externally accessible.

5.1.2 Logic section

This section receives the input signals, manages the system protection (UVLO, standby, overtemperature, and remote signaling), and transfers the input pulses to the relevant drivers through level shifters.

It is electrically referred to GND pin and supplied by the VCC pin.

5.1.3 Low-side driver

This block receives input pulses from the level shifter and provides driving action to the low-side GaN transistor.

It is electrically referred to PGND, which is connected to the kelvin source connection of the low-side GaN transistor. Its input circuitry is supplied by VCC, while an integrated voltage regulator tightly stabilizes the supply voltage of the output stage of the driver (V_{LS}). A UVLO comparator interrupts the half-bridge activity if the regulator's output voltage is insufficient for a proper GaN's driving. A dedicated description of UVLO protection is described in the related section.

A dedicated pin can be used to externally adjust the turn-on resistor, while the turn-off driving resistor is internally fixed.

5.1.4 High-side driver

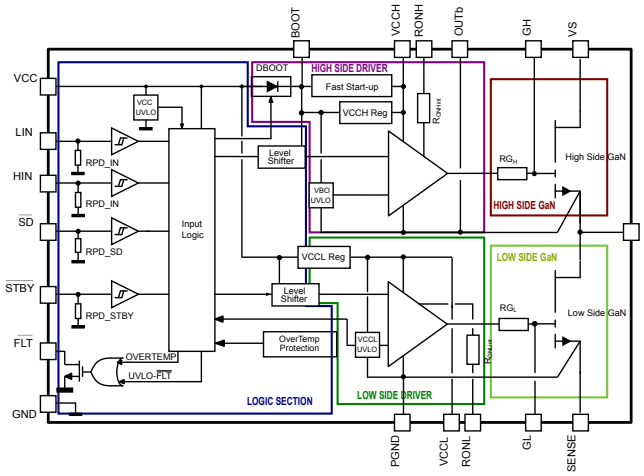
This block receives input pulses from the logic section through the level shifter and provides driving action to the high-side GaN transistor.

It is electrically referred to OUTb, which is connected to the kelvin source connection of the high-side GaN transistor. Its input circuitry is supplied by the voltage present at the BOOT pin, while an integrated voltage regulator tightly stabilizes the supply voltage of the output stage of the driver (V_{HS}). A UVLO comparator interrupts the high-side GaN activity if the regulator's output voltage is insufficient for a proper GaN's driving. A dedicated description of UVLO protection is described in the related section.

A dedicated pin can be used to externally adjust the turn-on resistor, while the turn-off driving resistor is internally fixed.

This section includes an equivalent bootstrap diode, synchronous with low-side on-time that generates a floating supply voltage (V_{BO}), starting from the VCC voltage.

Figure 31. MASTERGAN7 simplified block diagram



5.2 GaN transistor

The MASTERGAN7 embeds two 650 V enhanced mode GaN transistors, connected in a half-bridge configuration. The technology of the embedded GaN transistors does not need bipolar driving: for this reason, a negative voltage to turn off the transistor is not necessary.

The low-side GaN transistor is electrically connected between the OUT pin set (drain) and SENSE pin set (source): the SENSE exposed pad also represents a thermal buffer for this transistor. A suitable copper area and several thermal vias are required to dissipate the power losses generated during normal operation.

The high-side GaN transistor is electrically connected between VS pins (drain) and OUT pins (source): the OUT exposed pad also represents a thermal buffer for this transistor. As suggested for low-side connection, a suitable copper area, and several thermal vias are required to dissipate the power losses generated during normal operation.

The embedded GaN transistors do not have an intrinsic body diode and, consequently, exhibit zero reverse recovery losses. Nevertheless, the reverse conduction is permitted both during on-state and during off-state (see Figure 11, Figure 12, and Figure 13). Anti-parallel didoes are not required for proper functionality of the MASTERGAN7 in both resonant and hard switching operation; they can be used to improve efficiency when reverse conduction has a major impact on power losses.

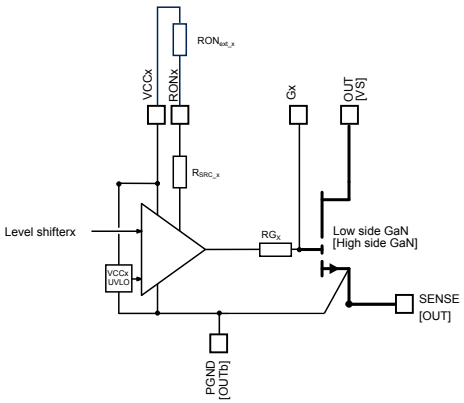
The driver output stage acts between the gate and kelvin source of the GaN transistor: a positive voltage, equal to (V_{LS} or V_{HS}), turns the GaN on while zero voltage turns the GaN off.

The turn-on gate resistance can be externally adjusted to adjust the turn-on slew rate, connecting a discrete resistor between RONx pins and VCCx pins (x = L or H). The measured value for internal minimum resistance (RON_{INTx}) is the series of an internal discrete resistance (R_{SRCx}), the driver's on-resistance, and RG_X.

The turn-off resistance is internally fixed to R_{OFFx}: this value includes the value of an internal discrete resistor R_{G_x} and the on-resistance of the sink portion of the driver.

Intrinsic gate resistance of the GaN transistor, approximately equal to 4.5 Ω, is not accessible from the MASTERGAN7 pins and is then excluded from the values enlisted in Table 6.

Figure 32. Ron resistor configuration



In some circumstances, the external pull-down resistors and external capacitors can be connected between GL and PGND or GH and OUTb. The maximum attachable Load, Cload, and Rload, must not overcome the maximum power rating of internal resistances, that equals:

$$P_{LOSS,Rinx} = VCCx^2 \cdot \left[\left(\frac{QG}{VCCx} + C_{LOAD}\right) \cdot fsw + \left(\frac{RONintx + ROFFx}{(RONintx + ROFFx + RONextx + R_{LOAD})^2}\right) \cdot \delta c\right] \quad (1)$$

Where *fsw* represents the switching frequency and *δc* is the duty cycle of the transistor under consideration.

5.3 Truth table and control inputs

The MASTERGAN7 has four logic inputs to control the embedded high-side and low-side power transistors.

- LIN: low-side driver input, active high;
- HIN: high-side driver inputs, active high;
- STBY: standby input, active low;
- SD: shutdown input, active low.

An open drain output is there (FLT) to communicate externally the operating status of the device. For a proper level of this function, the VCC must be higher than $V_{VCC-FLT}$.

Table 7 summarizes the different IC operating mode depending on the input pin configurations.

Output pin configuration and IC consumption are also reported.

Table 7. Truth table

Mode	INPUT				OUTPUT			Consumption	
	STBY	SD	LIN	HIN	GL	GH	FLT	IVCC	IVCCH
Standby	L	X	X	X	L	L	L	I_{SBVCC}	I_{QBO}
Shutdown	H	L	X	X	L	L	HiZ	I_{QVCC}	I_{QBO}
High-Z	H	H	L	L	L	L	HiZ	I_{QVCC}	I_{QBO}
Low-side on	H	H	H	L	H	L	HiZ	I_{QVCC}	I_{QBO}
High-side on	H	H	L	H	L	H	HiZ	I_{QVCC}	I_{QBO}

Mode	INPUT				OUTPUT			Consumption	
	STBY	SD	LIN	HIN	GL	GH	FLT	IVCC	IVCCH
Interlocking	H	H	H	H	L	L	HiZ	I_{QVCC}	I_{QBO}

The logic inputs have internal pull-down resistors to set a defined logic level even in case of high impedance on signal lines. As a result, the transistors are set off in case of unconnected input pins.

The front end of logic inputs consists of a comparator having a fixed threshold and defined hysteresis to ensure precise and robust level detection. The input pins can accept an input voltage up to 20 V independently from the VCC voltage level.

Propagation delays between LIN, HIN, or SD input pins and the transistor's gates are matched to obtain the best symmetry and minimum pulse width distortion providing the duration of the input pulse is longer than 50 ns and the duration of the input voltage drop is longer than 120 ns.

The minimum duration of the pulse that can be transferred from HIN, LIN, or SD to the transistor gate is longer than t_{INmin}; shorter pulses may be blanked or transferred with some time distortion. Considering that the on-time duration of the first low-side applied after a long inactivity period defines the charging voltage of the bootstrap capacitor; a further design constraint for low-side on-time and bootstrap related components must be applied to ensure a proper high-side driving (Section 5.4.3).

The minimum duration of the voltage drop that can be transferred from HIN, LIN, or SD to the transistor gate is longer than t_{INmin_N}; shorter pulses may be blanked or transferred with some time distortion.

If a remote controller or monitoring unit can exploit the FLT function, a pull-up current or an external resistor (R_{PU_FLText}) is required to properly detect the activation of the internal open-drain unit. In this case, the high-level voltage can be set to a maximum level of 20 V independently from VCC. When unused, this pin must be connected to GND.

The STBY pin is intended to activate standby mode to reduce the IC consumption during long-lasting inactive times. The description of this mode is reported in (Section 5.5).

5.4 Supply rails, LDOs, UVLO protections, and bootstrap diode

The MASTERGAN7 is supplied by two rails: VCC, referred to GND, and BOOT, referred to OUTb.

Integrated LDOs generate supply voltages for low-side and high-side output stages (V_{LS} and V_{HS}) including UVLO protections.

The integrated bootstrap diode is there to generate a floating supply voltage for the high-side structure.

5.4.1 VCC supply structure and relevant UVLO protection

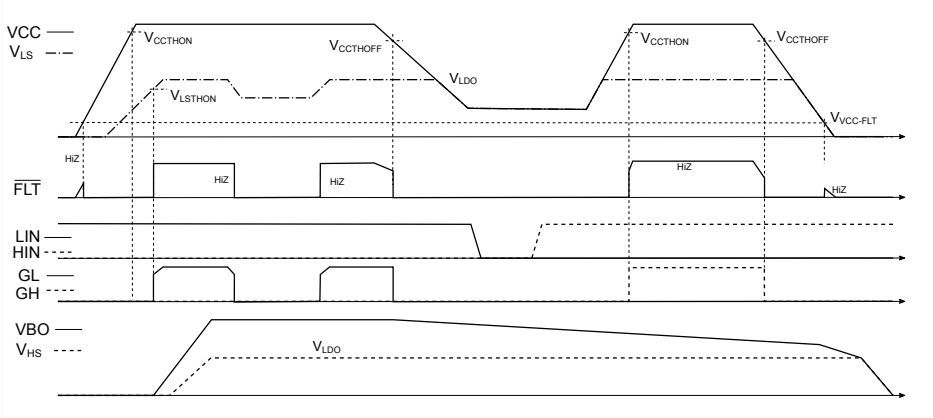
The VCC pin supplies the logic circuit, the input structure of the low-side driver, and the anode of the integrated bootstrap diode (DBOOT). Low-ESR ceramic capacitors are connected as close as possible between VCC and GND (100 nF typ., X7R, 50 V). Undervoltage protection is available on the VCC supply pin. A hysteresis sets the turn-off threshold.

When VCC voltage reaches the V_{CCthON} threshold, the device enters normal operation; if V_{LS} is above the UVLO level and the STBY pin is high, the FLT pin is released, and the device sets driver output according to actual input pins.

When VCC voltage goes below the $V_{CCthOFF}$ threshold, both high-side and low-side gate driver outputs are forced low and the FLT pin is forced low to signal the state to remote controllers.

The device can force the FLT pin low when VCC > $V_{VCC-FLT}$.

Figure 33. **VCC UVLO algorithm**



5.4.2 V_{LS} supply structure and relevant UVLO protection

An integrated low-drop-out linear regulator (LDO_L) is fed by VCC voltage to stabilize the low-side driver output terminal (VCCL, referred to PGND or, shortly V_{LS}= 6 V typ.) providing that VCC is higher than V_{LS}+ $V_{VLS-DROP}$. Low-ESR ceramic capacitors are connected as close as possible between VCCL and PGND (the recommended value for CVCCL is 47 nF - X7R / 16 V) to obtain a clean supply voltage. Under recommended operating conditions, the LDOL can provide an average current of at least 10 mA. Undervoltage protection is available on V_{LS} supply voltage that biases the low-side driver output stage. When V_{LS} voltage reaches the V_{LSthON} threshold, the device enables the low-side driver normal operation; if no other protection is active, the FLT pin is released and the device sets the low-side driver output according to actual input pins and the high-side driver output. When V_{LS} voltage goes below the $V_{LSthOFF}$ threshold, both high-side and low-side gate driver outputs are forced low and the FLT pin has to signal this condition to remote controllers.

5.4.3 Bootstrap diode

The MASTERGAN7 integrates a bootstrap diode structure connected between the VCC and BOOT pins to supply the high-side floating supply voltage $V_{BOOT-OUTb}$ (or shortly V_{BO}). A very low ESR ceramic capacitor (C_{BOOT} to be selected typ. between 47 nF and 220 nF, X7R, 50 V) must be placed as close as possible between the BOOT and OUTb pins.

The bootstrap DC characteristics are detailed in Figure 22.

Eventually, the application characteristic is not able to generate a sufficient voltage on V_{BO} (high frequency, very small duty cycle, …) so an external bootstrap diode can be used (STTH1R06 or similar).

A resistor R_{BOOT} ≥ 2.7 ohm must be placed in series with the above mentioned external bootstrap diode to reduce the amount of C_{BOOT} charging current.

The C_{BOOT} value should be selected to ensure that the VBO voltage is charged form 0 V to, at least, V_{BOthON} (2.9 V typ.) during the first low-side on-time (T_{on_1st}) when VCC assumes the minimum value (eventually V_{CCthon}). This constraint ensures that the high-side driver is prompt to serve the first HIN signal. It is suggested to use $C_{BOOT} \geq C_{VCCH}$.

A useful equation is reported:

$$C_{VCCH} \leq C_{BOOT} \leq \left(\frac{T_{on\_1st}}{-R_{BOOT} \cdot \ln\left(1 - \frac{V_{BOoff}}{V_{CCmin}}\right)} \right) \quad (2)$$

5.4.4 VHS supply structure

The energy stored in the C_{BOOT} capacitor supplies the input circuitry of the high-side driver.

An integrated low-drop-out linear regulator (LDO_H) is connected to V_{BO} to stabilize the high-side driver output terminal (VCCH, referred to OUTb or, shortly, V_{HS} = 6 V typ.) providing that V_{BO} is higher than V_{HS}+ $V_{BO-DROP}$.

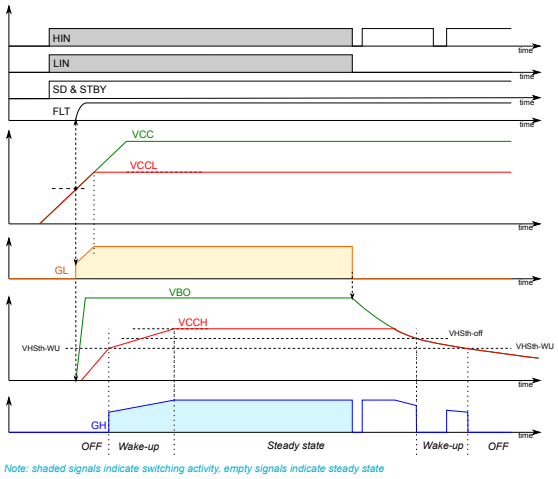
LDO_H is equipped with fast turn-on circuitry to minimize the wake-up time especially during intermittent operation (Burst mode).

Low-ESR ceramic capacitors are connected as close as possible between VCCH and OUTb (the recommended value for C_{VCCH} is 47 nF - X7R / 16 V) to obtain a clean supply voltage.

An internal comparator monitors VBO voltage to enable the driving of the high-side GaN when VBO is higher than 2.9 V typ. and forces the transistor off when VBO is lower than the said level.

Under recommended operating conditions, LDO_H can provide an average current of 10 mA with a peak current, to charge CVCCL, equal to approximately 200 mA.

Figure 34. V_{BO} and V_{HS} startup

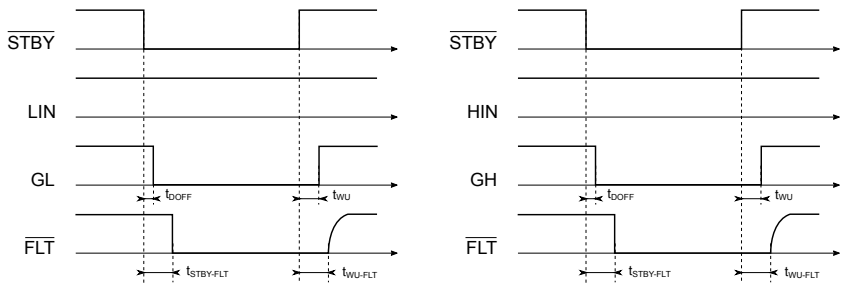


5.5 Standby

The MASTERGAN7 is designed to reduce the current consumption of both the logic portion and low-side driver when the STBY pin is pulled to GND. Low-side and high-side output are immediately set low to leave the half-bridge in 3-state, while the FLT pin is forced low, and consumption is reduced providing that the STBY pin is pulled to GND for at least t_{STBY}. The overtemperature protection is disabled in this operating condition.

Setting the STBY pin high, the device wakes up and operation is restored; the FLT pin is released within t_{WU-FLT} while driver outputs are set according to inputs, providing relevant UVLOs are not active, within t_{WU}.

Figure 35. STBY pin behavior



5.6 Thermal shutdown

The MASTERGAN7 provides a thermal shutdown protection feature.

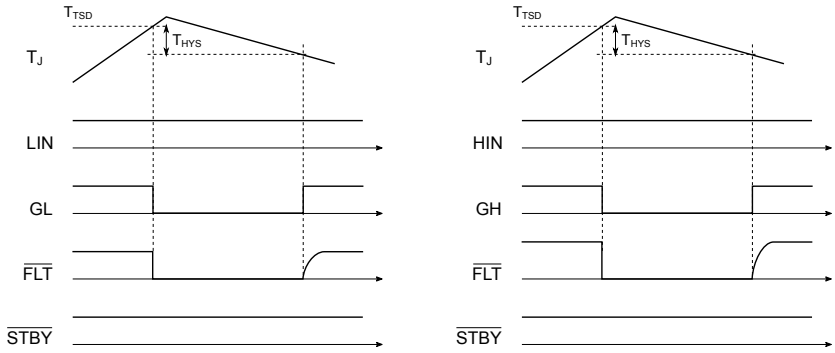
When, during active mode, the junction temperature reaches the T_{TSD} temperature threshold, the device turns the driver outputs off to leave the half-bridge in 3-state, and signals this condition forcing the FLT pin low. The status of all the input pins is ignored.

When the junction temperature is lower than T_{TSD}-T_{HYS}, the device operation is restored and the FLT pin is released.

Overtemperature protection is active after a time equal to t_{TSD} since the V_{CCthON} threshold is crossed or after standby state exit. During this time, the gate driver outputs operate according to input levels and independently from T_J.

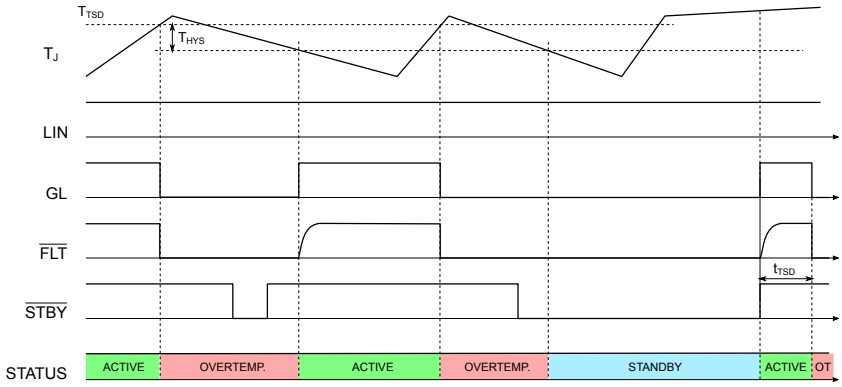
If VCC drops below VCC_{thOFF}, the thermal protection feature is reset. On the contrary, if VCCL drops below $VLDO_{L\text{-}off}$, the thermal protection is maintained on.

Figure 36. Thermal shutdown vs. input status



The overtemperature detection is inactive when the device is operating in standby mode to minimize consumption.

Figure 37. Thermal shutdown and standby



6 Application example

6.1 PCB suggestions

This section enlists some tips to facilitate the PCB routing of the MASTERGAN7.

6.1.1 External BOM values selection and placing

A list of recommended value ranges for some key components are reported.

The bulk capacitors required for VCC, VCCL, VCCH, and BOOT must be placed as close as possible to the relevant pins and references. Such capacitors must be low ESR/ESL ceramic components with rated voltages that are almost twice the maximum operating voltages to overcome the well-known value modulation versus bias voltage.

The eventual external bootstrap diode requires a series resistance larger than 2.7 Ω. In case an external bootstrap diode is used, the CBOOT capacitor must be placed on the PCB in a way that the negative terminal is put as close as possible to the OUTb pin: this arrangement ensures that the charging current flows in the shortest track possible.

Turn-on resistors (RONx) need to be placed close to the IC to minimize the length of the track connected to the RONx pin.

Table 8. External component summary

Symbol	Function	Typ. value (range)	Technology	Min. rating
C_{VCC}	VCC large bulk capacitor (it is normally used as bulk capacitor of controller too)	10 µF	EL-Cap	25 V (50 V)
	VCC bypass capacitor	100 nF	X7R	50 V
C_{BOOT}	BOOT to OUTb bypass capacitor	47 nF … 220 nF	X7R	50 V
C_{VCCL}	VCCL to PGND bypass capacitor	47 nF	X7R	16 V
C_{VCCH}	VCCH to OUTb bypass capacitor	47 nF	X7R	16 V
R_{BOOT}	Current limiting resistor of external DBOOT	≥ 2.7 Ω		
D_{BOOT}	External bootstrap diode (if needed)	STTH1R06 or equivalent	Turbofast	600 V / 1 A
RONx	Turn-on resistors of LS and HS GaNs	0 Ω to 220 Ω		

PGND is internally connected to the SENSE pin: do not connect externally to any other GND or SENSE route.

OUTb is internally connected to the OUT pin: do not connect externally to the OUT route.

VCCL and VCCH are the output access to the internal voltage regulator: forcing these pins to external voltage regulators may result in unrecoverable damage of the IC.

6.1.2 Distances

The QNF9x9x1 package is designed to simplify the respect of the safety norms regarding creepage distances. The gray area depicted in Figure 38 represents the distances to maintain the creepages at PCB level. The pin sets are colored differently to represent the pins that are referred to the same voltage reference.

Figure 38. Keepout regions for safety

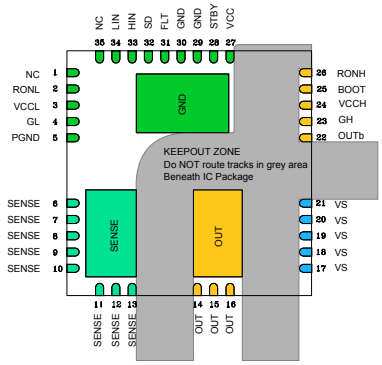


Figure 39. Example of placement of low-side driver components

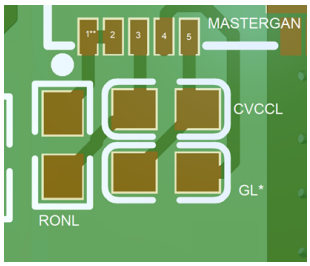
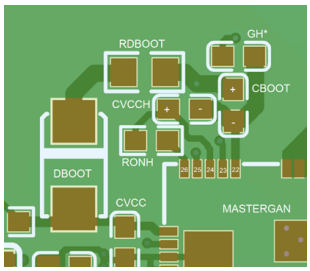


Figure 40. Example of placement of high-side driver components



6.1.3 Noise reduction and thermal management

To minimize the noise generation during normal operation of typical applications, a few simple hints can be exploited:

1. Connect signal GND and power GND to a single star point. Signal ground consists of controller GND and Signal GND of MASTERGAN7.
2. If a shunt resistor is necessary, this component should have a very small ELS and be placed as close as possible to the MASTERGAN7. A cheap alternative to a low ESL resistor consists of the parallel of multiple smaller resistors (for example, 3x 0603 SMD resistors have similar ESL of 1020 package shunt resistors and is much lower than a 2010 standard package).
3. The OUT pin is high frequency switching: it should be routed very closely to the load (transformer or inductor) minimizing the overlap with any other nets. This avoids undesired parasitic capacitance and noise injection.
4. Keep the current loops as small as possible. A high-voltage ceramic capacitor connected between the high-voltage bus and power ground, and placed as close as possible to the MASTERGAN7, facilitates the reduction of such loops.
5. The CBOOT capacitor must be placed on the PCB pin in such a way that the negative terminal is put as close as possible to the OUTb pin.
6. RONx needs to be placed close to the IC to minimize the length of the track connected to the RONx pin.

Heat generated by the IC can be dissipated using exposed pads.

1. SENSE and OUT exposed pads are intended to spread out the heat generated by the GaN during switching activity. The use of standard vias beneath the EPs helps to both transfer heat between different layers and minimize the risk of voids (air bubbles) between the IC's exposed pads and PCB footprint.
2. GND exposed pad is useful at very high switching frequency to maintain the driver's temperature low.
3. VS pin set is not responsible for thermal dissipation: the net connected to this potential has to be sized for RMS current only.
4. High copper thickness (2 oz) improves the heat spreading and helps to transfer it far from the IC. Smaller support thickness (for example, FR4 – 1 mm instead of 1.6 mm) helps to transfer the heat between copper layers, but care should be taken on parasitic capacitance generation and board robustness.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Package information

Figure 41. Package outline

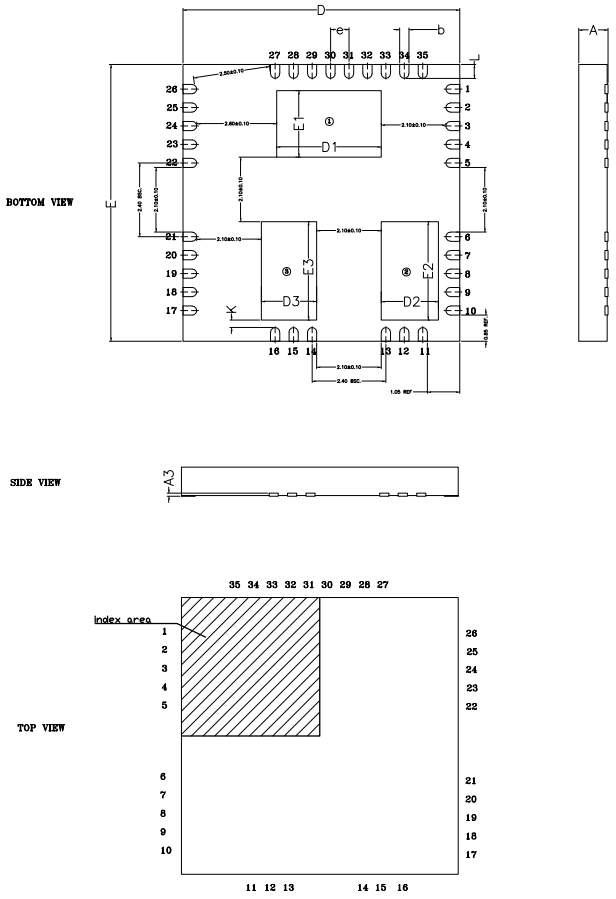
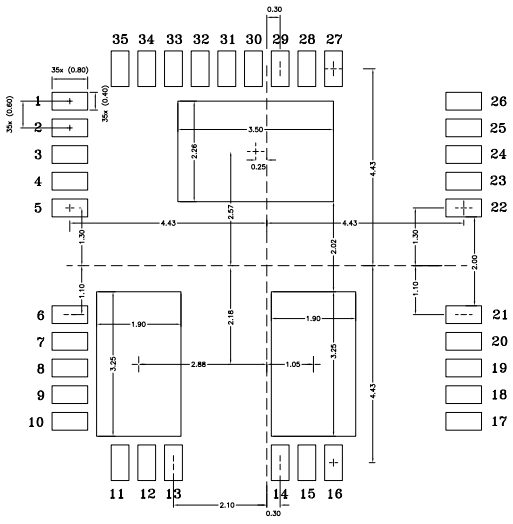


Table 9. Mechanical data

Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
A	0.90	0.95	1.00
A3	-	0.10	-
b	0.25	0.30	0.35
D	8.96	9.00	9.04
E	8.96	9.00	9.04
D1	3.30	3.40	3.50
E1	2.06	2.16	2.26

Symbol	Dimensions [mm]		
	Min.	Nom.	Max.
D2	1.76	1.86	1.96
E2	3.10	3.20	3.30
D3	1.70	1.80	1.90
E3	3.10	3.20	3.30
e	-	0.6Ref	-
K	-	0.24Ref	-
L	0.35	0.45	0.55
n		35	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
Ref		1	

Figure 42. Suggested footprint



8 Ordering information

Table 10. **Ordering information**

Order code	Package	Package marking	Packaging
MASTERGAN7TR	QFN 9 x 9 x 1 mm	MASTERGAN7	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
25-Nov-2025	1	Initial release.

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