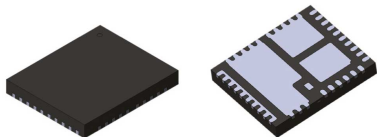


## Smart power stage with current sensing, temperature monitor and fault reporting



### Features

- Optimized MOSFET switching performance with integrated Schottky diode in LS MOSFET
- 110 A peak and 60 A continuous current capability
- High frequency operation up to 1.5 MHz
- 3.3 V PWM logic with tri-state and hold-off
- PWM minimum controllable on-time of 30 ns
- Low PWM propagation delay (< 20 ns)
- Current sense monitor output 5mV/A ( $I_{MON}$ ) and 2% accuracy
- Temperature monitor output 8mV/C ( $T_{MON}$ ) and 2% accuracy
- Fault reporting and mapping through both  $I_{MON}$  and  $T_{MON}$ 
  - High Side MOSFET Short
  - Accurate over-current protection
  - Over-temperature protection
  - Under-voltage lockout for  $V_{IN}/V_{CC}/V_{DRV}/BOOT$
- Thermally enhanced QFN 5x6 41L package

### Application

- High performance synchronous buck converter
  - Intel, AMD CPU power supply
  - GPU, ASIC and AI chip power supply
  - Cloud computing and AI
- DC/DC converters
- Telecom and networking

### Description

The **PM7080A** is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density solution. Packaged in 5x6 mm QFN package, the **PM7080A** enables voltage regulator design to deliver above 110 A per phase peak current.

The internal power MOSFETs utilize state-of-the-art technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

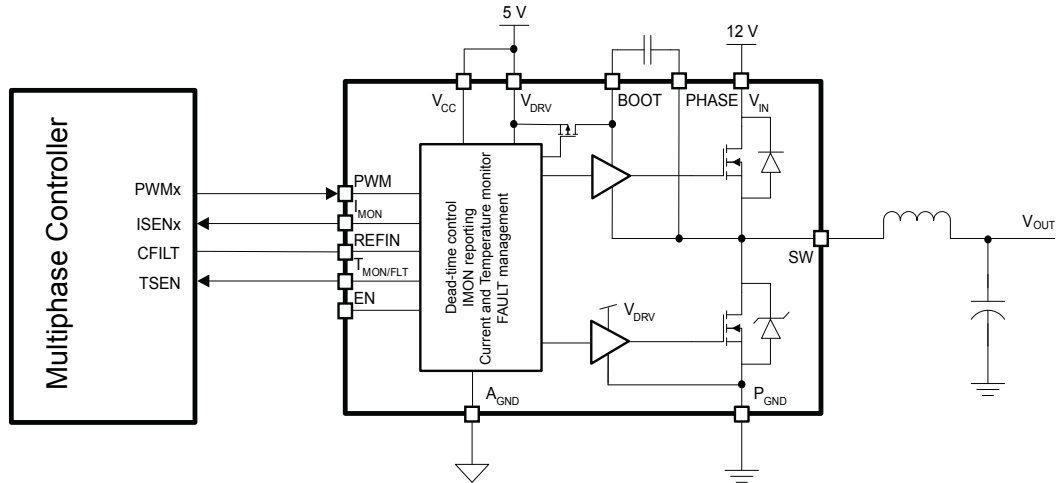
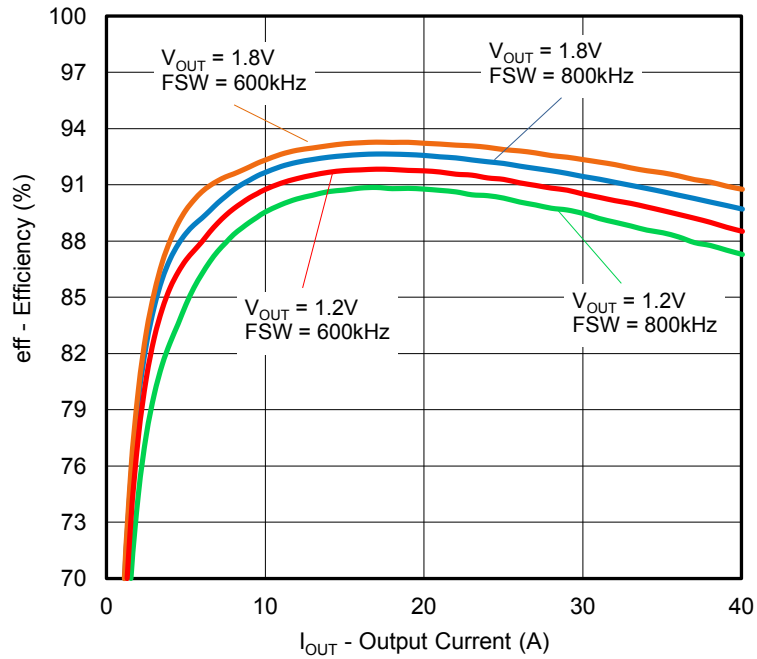
The **PM7080A** incorporates an advanced MOSFET gate driver IC that features high current diving capability, adaptive dead-time control and integrated bootstrap switch to enable high frequency switching up to 1.5MHz.

The device incorporates an innovative inductor current emulation algorithm with thermal compensation to achieve best-in-class reporting accuracy. It also includes a temperature monitor function with 2% accuracy. The **PM7080A** provides comprehensive protection features, including cycle-by-cycle over-current protection, over-temperature protection, high-side MOSFET short protection,  $V_{IN}/V_{CC}/V_{DRV}/BOOT$  UVLO protection. In addition to their analog reporting capability, the combined logic outputs of  $I_{MON}$  and  $T_{MON}$  provide fault mapping to the PWM controller for specific fault condition deciphering.

The **PM7080A** is compatible with industry-standard footprint.

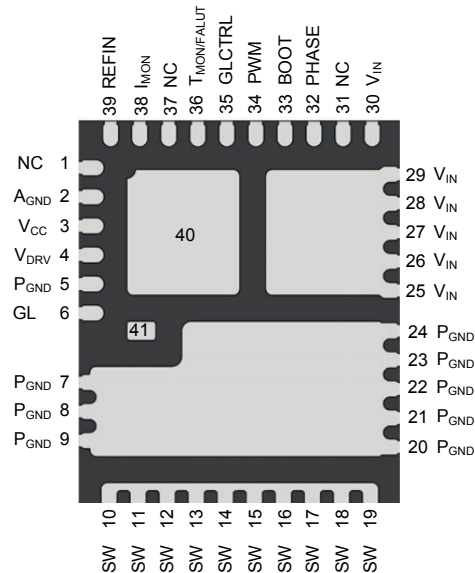
Product status link	
<a href="#">PM7080A</a>	
Product summary	
Order code	PM7080A
Temperature range	-40 to +125
Package	QFN 5x6 41L
Packing	Tape & reel

# 1 Typical application and efficiency

**Figure 1. Typical application circuit**

**Figure 2. Efficiency vs. output current ( $V_{IN} = 12\text{ V}$ ,  $L = 150\text{ nH}$ ,  $V_{CC} = V_{DRV} = 5\text{ V}$ )**


## 2 Pins description

**Figure 3. Pinout (Top transparent view)**



**Table 1. Pin description**

Pin no.	Pin name	Description
1, 31, 37	NC	This pin can be left floating or connected to A <sub>GND</sub>
2	A <sub>GND</sub>	Ground for internal circuitry (not a ground for the drivers)
3	V <sub>CC</sub>	Supply voltage for internal circuitry (does not power the drivers)
4	V <sub>DRV</sub>	Supply voltage for internal gate drive
5, 7 to 9, 20 to 24, 40	P <sub>GND</sub>	Power ground (note: pin 5 is intended to be used as a Kelvin pickup of the P <sub>GND</sub> for I <sub>MON</sub> sensing)
6, 41	GATEL (GL)	Low side MOSFET gate signal for observation purposes - do not connect externally
10 to 19	SW	Switch node of the power stage. Connect directly to output inductor
25 to 30	V <sub>IN</sub>	Power stage input voltage. Drain of high side MOSFET
32	PHASE	Return path of HS gate driver and the boot capacitor. Connected internally to the SW node. Do not connect this pin to the switch node externally
33	BOOT	High side driver bootstrap voltage. Connect a 0.1 μF to 1 μF capacitor between BOOT and PHASE pins
34	PWM	PWM input logic. tri-state PWM input signal means both HS and LS MOSFETs are turned off
35	EN	Enables the driver
36	T <sub>MON/FAULT</sub>	Temperature monitor with a conversion factor of 8 mV/°C with 0.8 V offset / catastrophic fault pin
38	I <sub>MON</sub>	Output voltage representative of the inductor current with a ratio of 5 mV/A
39	REFIN	Internal reference voltage for I <sub>OUT</sub> , but can be overdriven externally if desired

### 3 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Operating outside maximum recommended conditions for any periods of time is not recommended, may impact product reliability and result in device failures.

**Table 2. Absolute maximum ratings ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)**

Electrical parameter	Symbol	Limits	Unit
Input voltage	$V_{IN}$	-0.3 to +25	V
Logic bias voltage	$V_{CC}$	-0.3 to +6.5	
Drive input voltage	$V_{DRV}$	-0.3 to +6.5	
SW and PHASE	$V_{SW}$ , (DC)	-0.3 to +25	
	$V_{SW}$ , (AC) <sup>(1)</sup>	-8 to 30	
BOOT - $P_{GND}$ voltage	$V_{BOOT}$	-0.3 to +32	
BOOT - PHASE voltage	$V_{BOOT-PH}$	-0.3 to +6.6	
All logic inputs and outputs (PWM, EN, $I_{MON}$ , REFIN, $T_{MON/FAULT}$ )		-0.3 to $V_{CC} + 0.3$	°C
Max. operating junction temperature	$T_J$	150	
Operating ambient temperature	$T_A$	-40 to +125	
Storage temperature	$T_{stg}$	-65 to +150	V
ESD / HBM		2000	
ESD / CDM		500	

1. The specification values indicated "AC" is  $V_{SW}$  to  $P_{GND}$  - 8 V (< 20 nSec, 10  $\mu$ J), min. and 30 V (< 50 nSec), max.

#### 3.1 Recommended operating conditions

**Table 3. Recommended operating conditions**

Electrical parameter	Min.	Typ.	Max.	Unit
Input voltage ( $V_{IN}$ )	4.5	12	16	V
Logic bias voltage ( $V_{CC}$ )	4.5	5	5.5	
Drive input voltage ( $V_{DRV}$ )	4.5	5	5.5	
SW and PHASE (DC)	-	-	25	
BOOT - PHASE voltage	4.5	5	5.5	
DC current	-	-	60	A
Peak current (less than 5 s)	-	-	110	
Switching frequency	-	-	1.5	MHz
Ambient temperature	-40	-	+100	°C

## 4 Electrical characteristics

**Table 4. Electrical specifications**

 (EN = 5 V, V<sub>IN</sub> = 12 V, V<sub>DRV</sub> and V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C)

 min./max. values are V<sub>IN</sub> = 12 V, V<sub>CC</sub> = V<sub>DRV</sub> = 5 V ± 10 % and T<sub>J</sub> = T<sub>A</sub> = -40 to 125 °C unless otherwise specified

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
<b>Power supplies</b>						
V <sub>CC</sub> UVLO rising	V <sub>CC_R</sub>		3.7	3.9	4.1	V
V <sub>CC</sub> UVLO hysteresis	V <sub>CC_HYS</sub>		-	200	-	mV
V <sub>DRV</sub> UVLO rising	V <sub>DRV_R</sub>		3.7	3.9	4.1	V
V <sub>DRV</sub> UVLO hysteresis	V <sub>DRV_HYS</sub>		-	200	-	mV
V <sub>IN</sub> UVLO rising	V <sub>IN_R</sub>		-	4.2	-	V
V <sub>IN</sub> UVLO hysteresis	V <sub>IN_HYS</sub>		-	400	-	mV
BOOT-PH UVLO rising	V <sub>BOOTR</sub>		-	3.7	4	V
BOOT-PH UVLO hysteresis	V <sub>BOOTHYS</sub>		-	300	-	mV
Driver current	I <sub>VDRV</sub>	EN = High, f <sub>SW</sub> = 600 kHz, D = 15 %	-	25	-	mA
		EN = High, f <sub>SW</sub> = 1000 kHz, D = 15 %	-	40	-	mA
		EN = High, PWM = float	-	1	-	mA
		EN = Low	-	0.5	-	mA
<b>PWM and EN control logic</b>						
PWM high level	V <sub>PWM_H_3p3</sub>		2.2	-	-	V
PWM low level	V <sub>PWM_L_3p3</sub>		-	-	0.8	V
Tri-state window	V <sub>TRI</sub>		1.2	-	1.8	V
PWM HiZ voltage	V <sub>PWM_HIZ</sub>		1.3	1.5	1.7	V
PWM sink impedance	R <sub>PWM_SINK_3p3</sub>	EN = High	-	20	-	kΩ
PWM source impedance	R <sub>PWM_SRC_3p3</sub>	EN = High	-	46.7	-	kΩ
Minimum PWM on time	T <sub>PWM_MIN_ON</sub>		20	30	40	nSec
PWM rising propagation delay	T <sub>PWM_PROG_DLY_R</sub>	PWM high to SW rising	-	30	-	nSec
PWM falling propagation delay	T <sub>PWM_PROG_DLY_F</sub>	PWM low to SW falling	-	30	-	nSec
PWM tri-state hold-off time	T <sub>TRI_HOLD</sub>		-	40	-	nSec
PWM tri-state entry delay	T <sub>PWM_TRI_DLY_R</sub>	PWM tri-state to GL falling		50		nSec
PWM tri-state exit delay	T <sub>PWM_TRI_DLY_F</sub>	PWM tri-state to GL rising	-	50	-	nSec
EN logic high threshold	V <sub>EN_H</sub>		-	-	1.9	V
EN logic low threshold	V <sub>EN_L</sub>		0.9	-	-	V
EN delay	T <sub>DELAY_EN</sub>	EN = high to T <sub>MON</sub> = 0.8V	-	4	-	μs
<b>Current sensings</b>						
Current sense gain	I <sub>MON_GAIN</sub>		-	5	-	mV/A
Current sense offset	I <sub>MON_OS</sub>	0 A load	-2.5	-	2.5	mV

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Current sense accuracy	$I_{MON\_ACC}$	$I_{OUT} > 20\text{ A}$	-2	-	2	%
		$10\text{ A} < I_{OUT} < 20\text{ A}$	-3	-	3	%
		$5\text{ A} < I_{OUT} < 10\text{ A}$	-4	-	4	%
		$I_{OUT} < 5\text{ A}$	-8	-	8	%
Current sense negative range			-	-50	-	A
Current sense positive range			-	130	-	A
REFIN voltage range	REFIN		1	-	2	V
<b>Temperature reporting</b>						
Temperature reporting gain	$T_{MON\_GAIN}$		-	8	-	mV/C
Temperature reporting offset	$T_{MON\_OS}$	Junct. temperature = 0 C	-	0.6	-	V
Temperature reporting accuracy	$T_{MON\_ACC}$		-3	-	3	%
$T_{MON}$ source current	$I_{TMON}$		5	-	-	mA
$T_{MON\_FAULT}$ level	$V_{TMON\_FLT}$		2.6	-	3.6	V
<b>Over-current protection</b>						
Accurate positive OCP	$I_{OCP\_A\_P}$		120	130	140	A
Accurate negative OCP	$I_{OCP\_A\_N}$		-50	-60	-70	A
Crude positive OCP	$I_{OCP\_C\_P}$		-	150	-	A
Crude negative OCP	$I_{OCP\_C\_N}$		-	-100	-	A
OCP mask time	$T_{MASK\_OCP}$		-	100	-	nSec
<b>Over temperature protection</b>						
OTP rising threshold	$T_{OTP\_R}$		-	150	-	C
OTP hysteresis	$T_{OTP\_HYS}$		-	10	-	C
<b>MOSFET driver</b>						
HS GATE pull down resistor	$R_{HG\_PH}$		-	20	-	k $\Omega$
LS GATE pull down resistor	$R_{GL\_PGND}$		-	20	-	k $\Omega$
Bootstrap forward voltage	$V_{BOOT\_F}$		-	0.4	-	V

## 5 Functional block and PWM timing diagrams

Figure 4. Functional block diagram

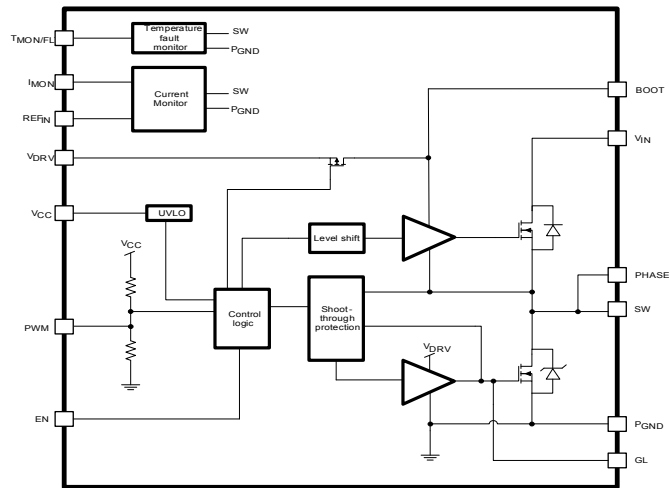
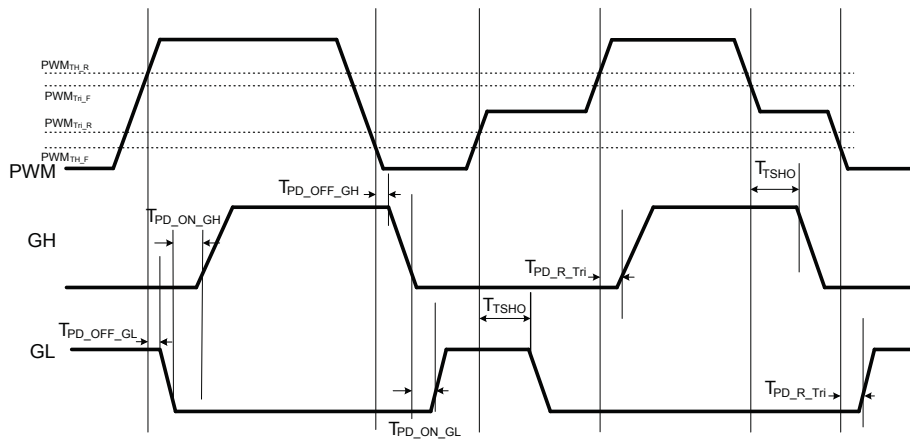


Figure 5. PWM timing diagram



## 6 Detailed operational description

### 6.1 PWM input and tri-state function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L, and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is high, the low side is turned OFF and the high side is turned ON. When PWM input is driven low, the high side turns off and the low side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is a third state that is entered into as the PWM output of the tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the device to pull the PWM input into the tri-state region (see the tri-state voltage threshold diagram below). If the PWM input stays in this region for the tri-state hold-off period,  $t_{TSHO}$ , both high side and low side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The PM7080A incorporates PWM voltage thresholds that are compatible with 3.3 V logic.

### 6.2 Temperature sensing and fault reporting ( $T_{MON/FAULT}$ )

The  $T_{MON/FAULT}$  signal is a dual function pin:

1. It is a voltage signal proportional to the internal temperature of the power stage device with a conversion factor of 8 mV/°C. In a multi-phase solution, all  $T_{MON/FAULT}$  signals are “wired-or” connected to the PWM controller and will indicate the temperature of the highest device
2. It indicates a catastrophic fault condition in the powerstage by pulling the signal to logic high (3.3 V logic compatible). The catastrophic fault conditions are:
  - a. HS FET over-current for 10 consecutive cycles
  - b. OT trip for the device maximum junction temperature
  - c. High side MOSFET drain to source short
  - d. High side BOOT UVLO
3. It indicates other UVLO fault condition in the powerstage by pulling the signal to logic low (0 V). The UVLO fault conditions are:
  - a.  $V_{CC}/V_{DRV}$  UVLO
  - b.  $V_{IN}$  VULO

### 6.3 Voltage input ( $V_{IN}$ )

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.

### 6.4 Switch node (sw and phase)

The switch node (SW) is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node (SW). This pin (PHASE) is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that  $V_{DRV}$  goes to zero while  $V_{IN}$  is still applied.



## 6.5 Ground connections (AGND and PGND)

Internal to the PM7080A, the AGND is shorted to the PGND through the lead frame. To avoid parasitic ground loops, the AGND for each individual instantiation of the device on the PCB should be derived from the PGND of the same device. It is not advised to connect all of the AGND connections at the system level together. If decoupling capacitance to AGND is used for each device I<sub>MON\_REF</sub> pin, it should be tied to the local AGND. Further, if possible, it is recommended to use the provided I<sub>MON\_REF</sub> signal from each device to accompany the I<sub>MON</sub> signal to provide a true differential output and avoid ground coupled cross-talk between I<sub>MON</sub> channels. AGND decoupling capacitance to V<sub>CC</sub> should be kept as close as possible to the device. Typically, a 1 Ω/1 μF capacitor decoupling capacitor network on V<sub>CC</sub> to AGND should be used. The 1 Ω resistor feeding V<sub>CC</sub> is connected to V<sub>DRV</sub> for its unfiltered voltage. V<sub>DRV</sub> should have its own 1 μF capacitor to PGND.

## 6.6 Control and drive supply voltage input (V<sub>DRV</sub>, V<sub>CC</sub>)

V<sub>CC</sub> is the bias supply for the gate drive control IC. V<sub>DRV</sub> is the bias supply for the gate drivers. It is recommended to separate these pins through a 1 Ω resistor with 1 μF//10 nF decoupling capacitance. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC's sensitive analog circuits.

## 6.7 Bootstrap circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a bootstrap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

## 6.8 Current sensing and report I<sub>MON</sub>

A current sense circuit monitors the low side MOSFET and reproduces a real-time representative signal for the entire switching period. The I<sub>MON</sub> pin is a voltage source output signal that duplicates the real-time waveform of inductor current proportional to the load current by a ratio of 5 uA/A and is differentially referenced to I<sub>MON\_REF</sub> voltage which is provided internally (1.5 V), but can be driven externally.

## 6.9 I<sub>MON\_REF</sub>

I<sub>MON\_REF</sub> should be terminated to an external voltage reference from 1.2V to 1.8V to provide a return path for I<sub>MON</sub> current source.

## 6.10 Shoot through protection and adaptive dead time

The PM7080A has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high side and low side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1 V), that and built in delays ensure each power MOS is turned off before the other turns on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

## 6.11 Under voltage lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high side and low side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The PM7080A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET. Additionally, there is a UVLO that monitors the BOOT voltage. If the BOOT voltage droops low, the low side drive will be momentarily activated to recharge the BOOT capacitor.

## 6.12 Advanced fault report

PM7080A use  $I_{MON}$  and  $T_{MON/FLT}$  outputs as combination to report various fault conditions. The below table summarizes the fault types in relationship with  $I_{MON}$  and  $T_{MON/FLT}$  levels.

**Table 5. Advanced fault report**

Type of fault	I <sub>mon</sub>	T <sub>mon</sub>	Latch
V <sub>CC</sub> /V <sub>DRV</sub> UVLO	REFIN	0V	No
V <sub>IN</sub> UVLO	REFIN	0V	No
HS BOOT UVLO	0V	3.0 V	No
OCP	1.4 V	3.0 V	No
OTP	0.8 V	3.0 V	No
HS short protection	3.0 V	3.0 V	Yes

## 7 PM7080A electrical curves

### ELECTRICAL CHARACTERISTICS

( $V_{IN} = 12\text{ V}$ ,  $V_{DRV} = V_{CC} = 5\text{ V}$ ,  $L_{OUT} = 150\text{ nH}$ . Power loss includes inductor loss, driver and controller loss unless otherwise stated)

Figure 6. Driver current vs. driver voltage

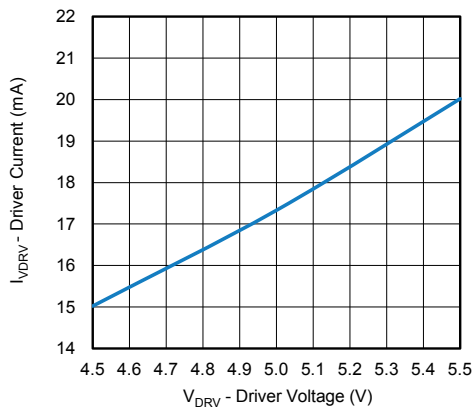


Figure 7. Driver current vs. switching frequency

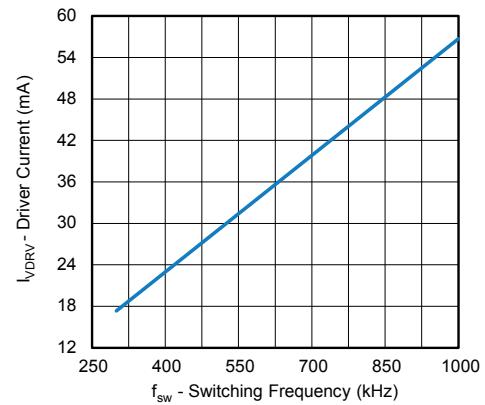


Figure 8. Threshold voltage vs. temperature

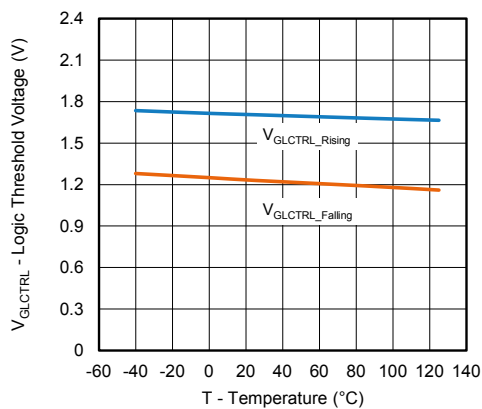


Figure 9. Quiescent current vs. temperature

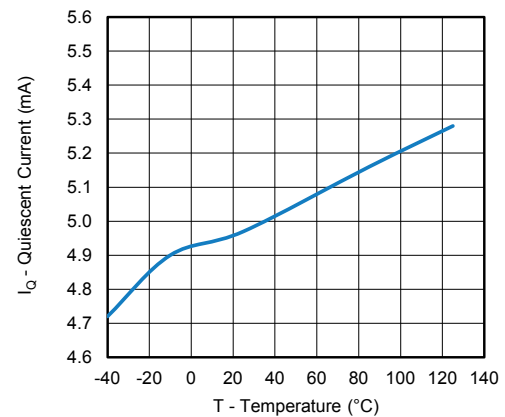


Figure 10. Threshold voltage vs. temperature

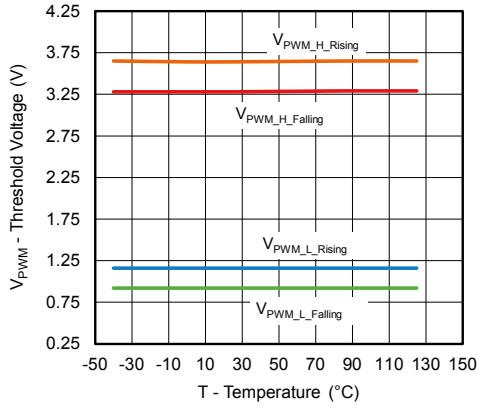


Figure 11. Threshold voltage vs. driver voltage

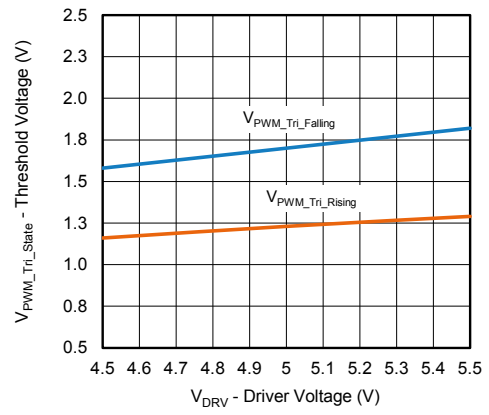


Figure 12. Quiescent current vs. driver voltage

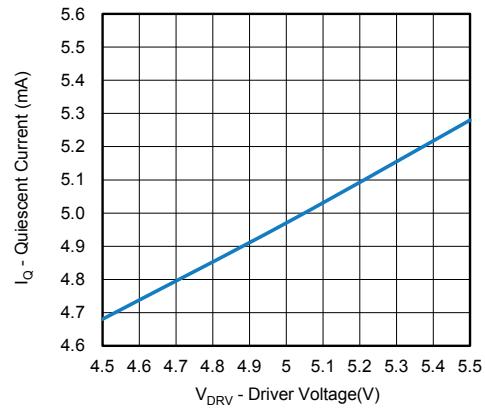


Figure 13. Threshold voltage vs. driver voltage

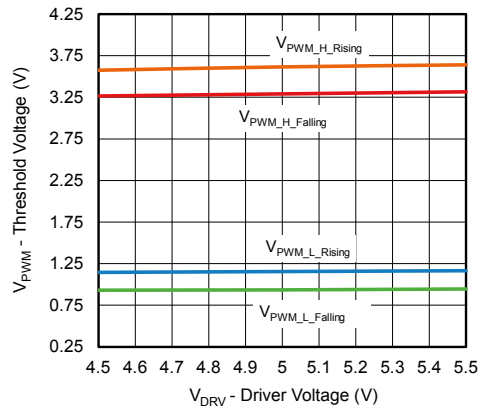
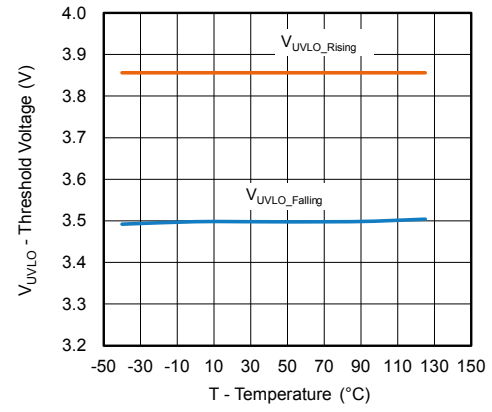


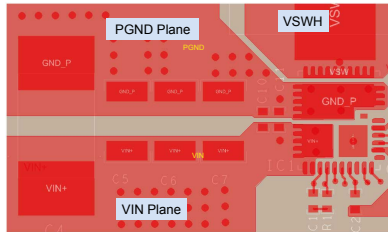
Figure 14. Threshold voltage vs. temperature



## 8 PCB layout recommendations

Step 1:  $V_{IN}/GND$  planes and decoupling

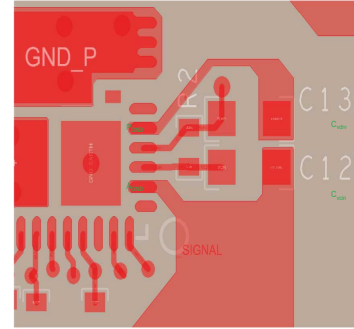
**Figure 15.  $V_{IN}/P_{GND}$  planes and decoupling**



1. Layout  $V_{IN}$  and  $P_{GND}$  planes as shown above.
2. Ceramic capacitors should be placed right between  $V_{IN}$  and  $P_{GND}$ , and very close to the device for best decoupling effect to reduce the high current power loop inductance and input current ripple induced by the MOSFET switching operation.
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, and 0402.
4. Smaller capacitance value, closer to device  $V_{IN}$  pin (s)
  - a. better high frequency noise absorbing

Step 2: VSWH plane

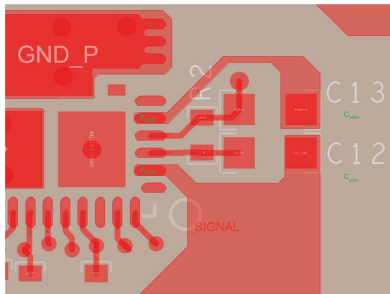
**Figure 16. VSWH plane**



1. Connect output inductor to DrMOS with large plane to lower the resistance and minimize the conduction loss due to the PCB trace. GND plane can be placed next to VSWH plane (SW pins) to shield the switching noise.
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom.

Step 3:  $V_{CIN}/V_{DRV}$  input filter

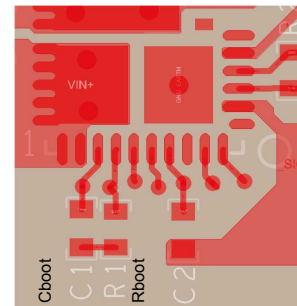
**Figure 17.  $V_{CIN}/V_{DRV}$  input filter**



1. The  $V_{CIN}/V_{DRV}$  input filter ceramic cap should be placed very close to DrMOS. It's recommended to connect two caps separately with one resistor in between.
2.  $C_{VCIN}$  cap should be placed between pin 3 and pin 2 ( $A_{GND}$  of driver IC) to achieve best noise filtering.
3.  $C_{VDRV}$  cap should be placed between pin 5 ( $P_{GND}$  of driver IC) and pin 4 to provide maximum instantaneous driver current for low side MOSFET during switching cycle.
4. For connecting  $C_{VCIN}$  analog ground, it is recommended to use large plane to reduce parasitic inductance.

Step 4: BOOT resistor and capacitor placement

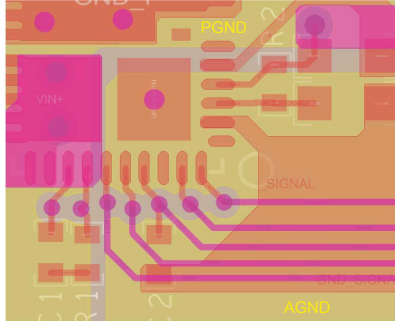
**Figure 18. BOOT resistor and capacitor placement**



1. These components need to be placed very close to DrMOS, right between PHASE (pin 32) and BOOT (pin 33).
2. To reduce parasitic inductance, chip size 0402 can be used.

Step 5: signal routing

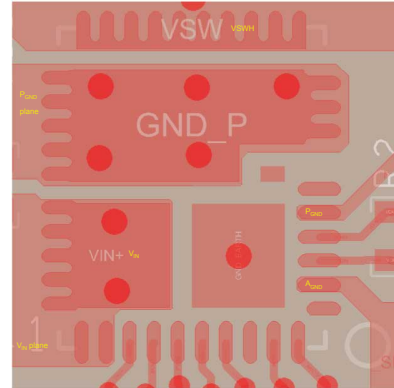
**Figure 19. Signal routing**



1. Route the PWM/T<sub>out</sub>/I<sub>mon</sub>/I<sub>monref</sub>/GLCTRL signal traces out of the bottom right corner next DrMOS pin 1.
2. These signals are sensitive. Both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer.
3. A small cap can be placed between T<sub>out</sub> and A<sub>GND</sub> to absorb the noise if necessary.
4. It is best to “shield” them with GND island form power switching nodes, e.g. V<sub>SWH</sub>, to improve signal integrity.
5. GL (pin 6) has been connected with GL pad (pin 41) internally and does not need to connect externally

Step 6: Adding thermal relief vias

**Figure 20. Adding thermal relief vias**



1. Thermal relief Vias can be added on the V<sub>IN</sub> and GND pads to utilize inner layers for high current and thermal dissipation.
2. To achieve better thermal performance, additional Vias can be put on V<sub>IN</sub> plane and P<sub>GND</sub> plane
3. VSWH pad is a noise source and not recommended to put Vias on this plane.
4. 8 mils drill for pads and 10 mils drill for plane can be the optional Via size. The Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline.

Step 7: Ground connection

**Figure 21. Ground connection**



1. Pin 2 A<sub>GND</sub>, pin 5 P<sub>GND</sub>, pin 40 GND pad and P<sub>GND</sub> pad have been connected internally already. Do NOT connect them externally in order to avoid GND loops.
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into A<sub>GND</sub> and P<sub>GND</sub> plane.
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 9.1 QFN 5x6 41L package information

Figure 22. QFN 5x6 41L package outline

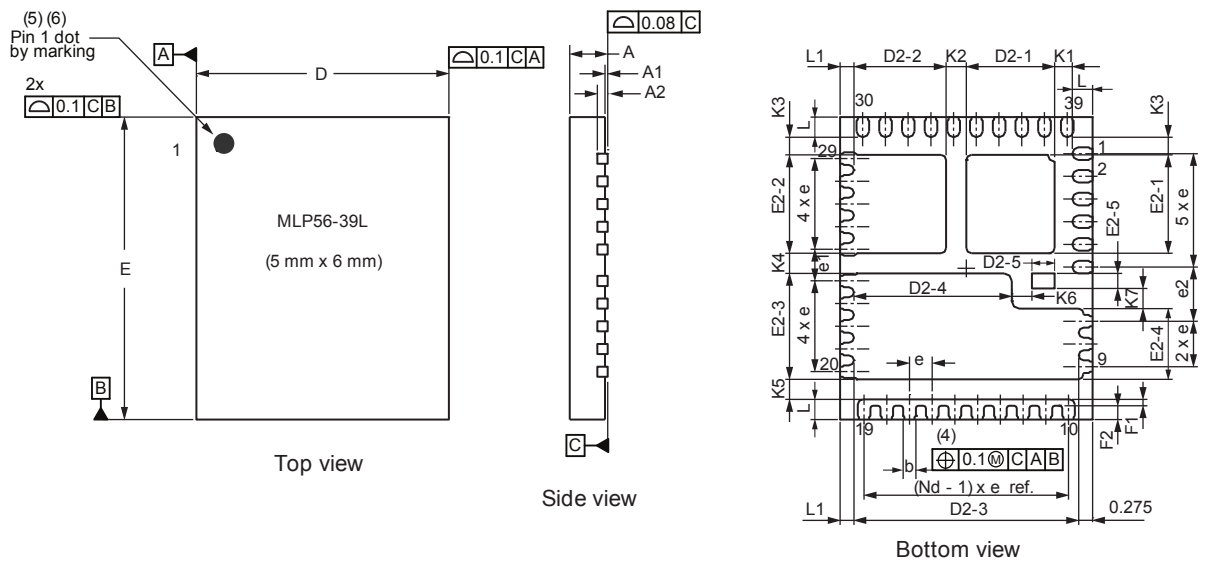


Table 6. QFN 5x6 41L mechanical data

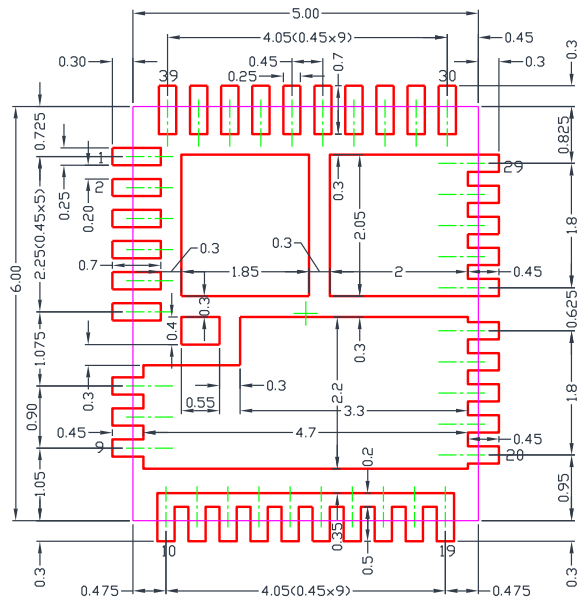
Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A <sup>(1)</sup>	0.70	0.75	0.80
A1	0.00	-	0.05
A2		0.20 ref.	
b <sup>(2)</sup>	0.20	0.25	0.30
D		5.00 BSC	
e		0.45 BSC	
e1		0.625 BSC	
e2		1.075 BSC	
E		6.00 BSC	
D2-1	1.70	1.75	1.80
D2-2	1.775	1.825	1.875
D2-3	4.40	4.45	4.50
D2-4	3.075	3.125	3.175
D2-5	0.40	0.45	0.50
E2-1	1.90	1.95	2.00



Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
E2-2	1.90	1.95	2.00
E2-3	2.05	2.10	2.15
E2-4	1.35	1.40	1.45
E2-5	0.25	0.30	0.35
L	0.35	0.40	0.45
L1	0.225	0.275	0.325
F1		0.125 BSC	
F2		0.275 BSC	
K1		0.35 ref.	
K2		0.40 ref.	
K3		0.35 ref.	
K4		0.40 ref.	
K5		0.40 ref.	
K6		0.40 ref.	
K7		0.40 ref.	
N <sup>(3)</sup>		39	
Nd <sup>(3)</sup>		10	
Ne <sup>(3)</sup>		10	

1. Applied only for terminals
2. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
3. N is the number of terminals, Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction

Figure 23. QFN 5x6 41L footprint



## Revision history

**Table 7. Document revision history**

Date	Version	Changes
19-Apr-2022	1	Initial release.

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