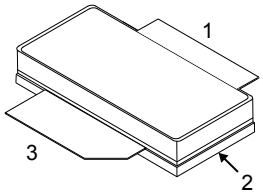
RF2L16180CF2

Datasheet

180 W, 28 V, 1.3 to 1.7 GHz RF power LDMOS transistor



B2

Pin connection	
Pin	**Connection**
1	Gate
2	Source (bottom side)
3	Drain

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF2L16180CF2	1470 MHz	28 V	180 W	17.5 dB	56%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internal input matching for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- Base stations
- L-band radars
- Industrial, scientific and medical (ISM)

Description

The RF2L16180CF2 is a 180 W internally matched LDMOS transistor designed for multicarrier WCDMA/PCS/DCS/LTE base stations and ISM applications in the frequency range from 1.3 to 1.7 GHz. It can be used in class AB, B or C for all typical modulation formats.

Product status link
RF2L16180CF2

Product summary	
Order code	RF2L16180CF2
Marking	2L16180
Package	B2
Packing	Tape and reel 13"
Base/Bulk quantity	120/120

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	0.38	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	0B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 100 µA	65			V
I_{DSS}	Zero-gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
		V_{GS} = 0 V, V_{DS} = 50 V				
I_{GSS}	Gate-body leakage current	V_{GS} = -6/10 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 28 V, I_D = 600 µA	1.75		2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 1V, I_D = 800 mA	2		4	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 5 A			0.5	V
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, V_{DS} = 100 mV			1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		1300		1700	MHz
P_{OUT}	Output power	f = 1470 MHz, at 1dB compression point		180		W
G_{PS}	Power gain			17.5		dB
η_D	Drain efficiency			56		%
VSWR	Load mismatch	P_{OUT} = 180 W, all phases			10:1	

Note: V_{DD} = 28 V, I_{DQ} = 800 mA , Pulsed CW, pulse width = 10 µs, duty cycle = 12%.

3 Typical performances

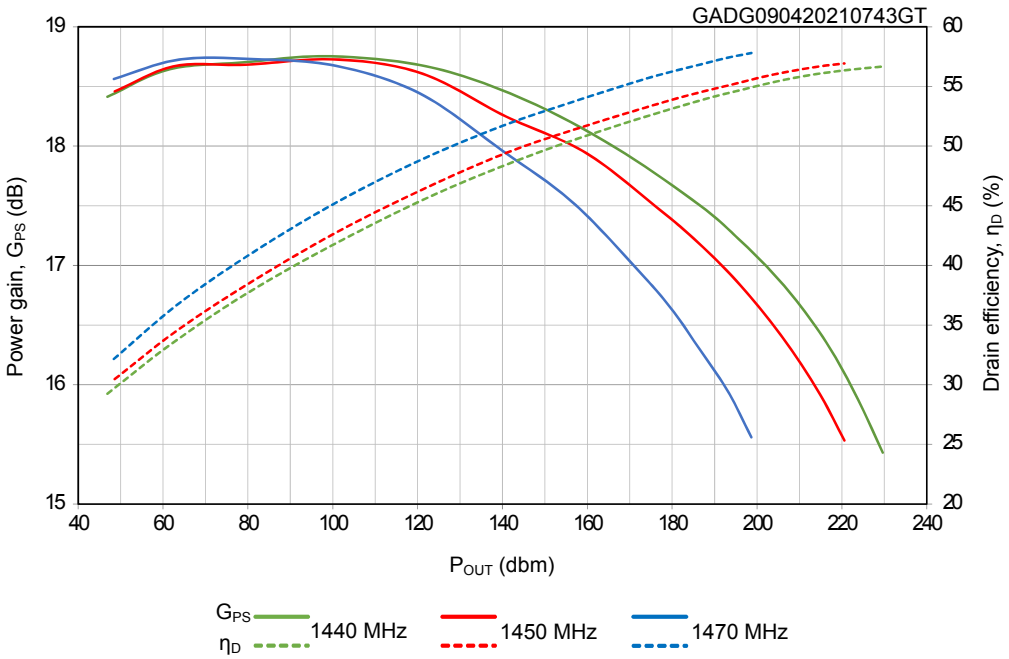
3.1 Pulsed CW performance

Table 6. Typical performance vs frequency

f (MHz)	G_{PS} @P_{1dB}(dB)	P_{1dB}(W)	P_{3dB}(W)	η_D @P_{3dB}(%)
1440	17.6	182	227	56.6
1450	17.4	177	222	57
1470	17.2	165	201	58

Note: V_{DD} = 28 Volts, I_{DQ} = 800 mA, pulsed CW, pulse width = 10 µs, duty cycle = 12%

Figure 1. Power gain and drain efficiency vs output power (1440 to 1470 MHz)



3.2 WCDMA performance

Table 7. Typical single-carrier W-CDMA performance ($P_{OUT,avg}$ = 45 dBm)

f (MHz)	G_{PS} (dB)	η_D (%)	PAR out (dB)	ACPR1 low (dBc)	ACPR1 high (dBc)	ACPR2 low (dBc)	ACPR2 high (dBc)
1440	18.2	26.4	8.10	-30.7	-30.6	-54.0	-53.0
1450	17.6	27.0	7.91	-31.3	-31.7	-53.0	-54.0
1470	18.2	28.6	7.86	-31.3	-30.6	-53.2	-51.5

Note: V_{DD} = 28 V, I_{DQ} = 600 mA, WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; channel bandwidth = 3.84 MHz, PAR = 10 dB at 0.01 % probability on CCDF. Test performed at 45 dBm average output power level .

4 Test circuits

Figure 2. **Test circuit layout (1440 to 1470 MHz)**

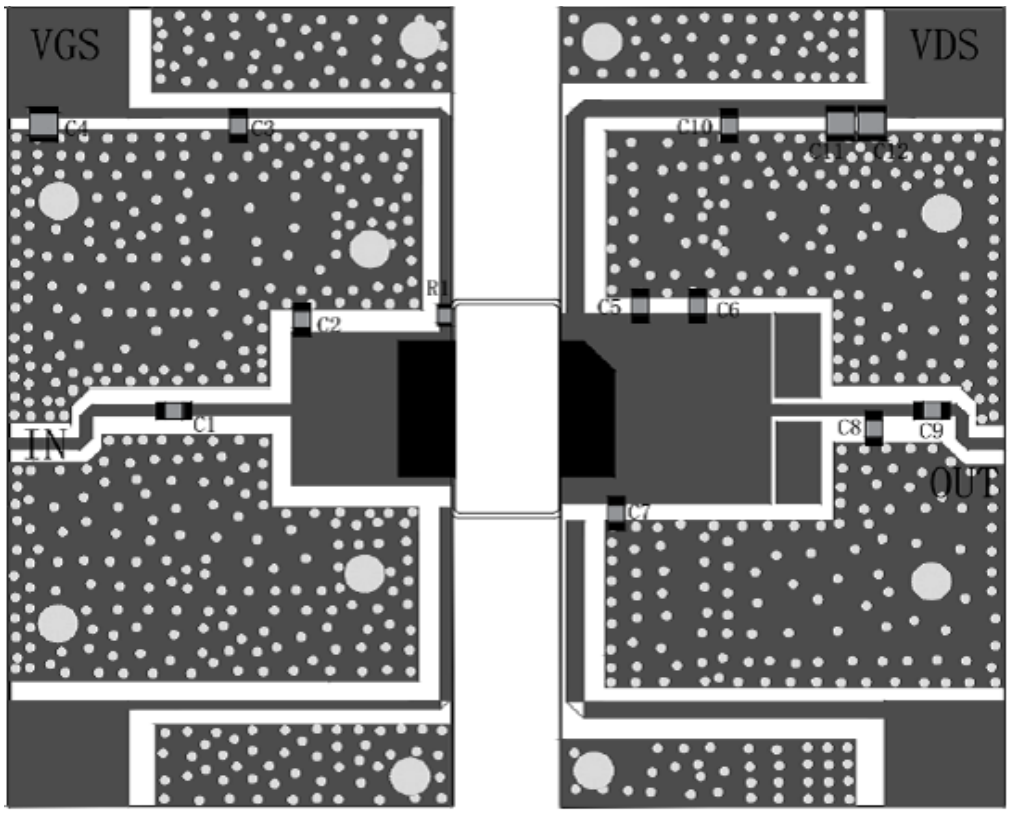


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Figure 3. **Test circuit photo**

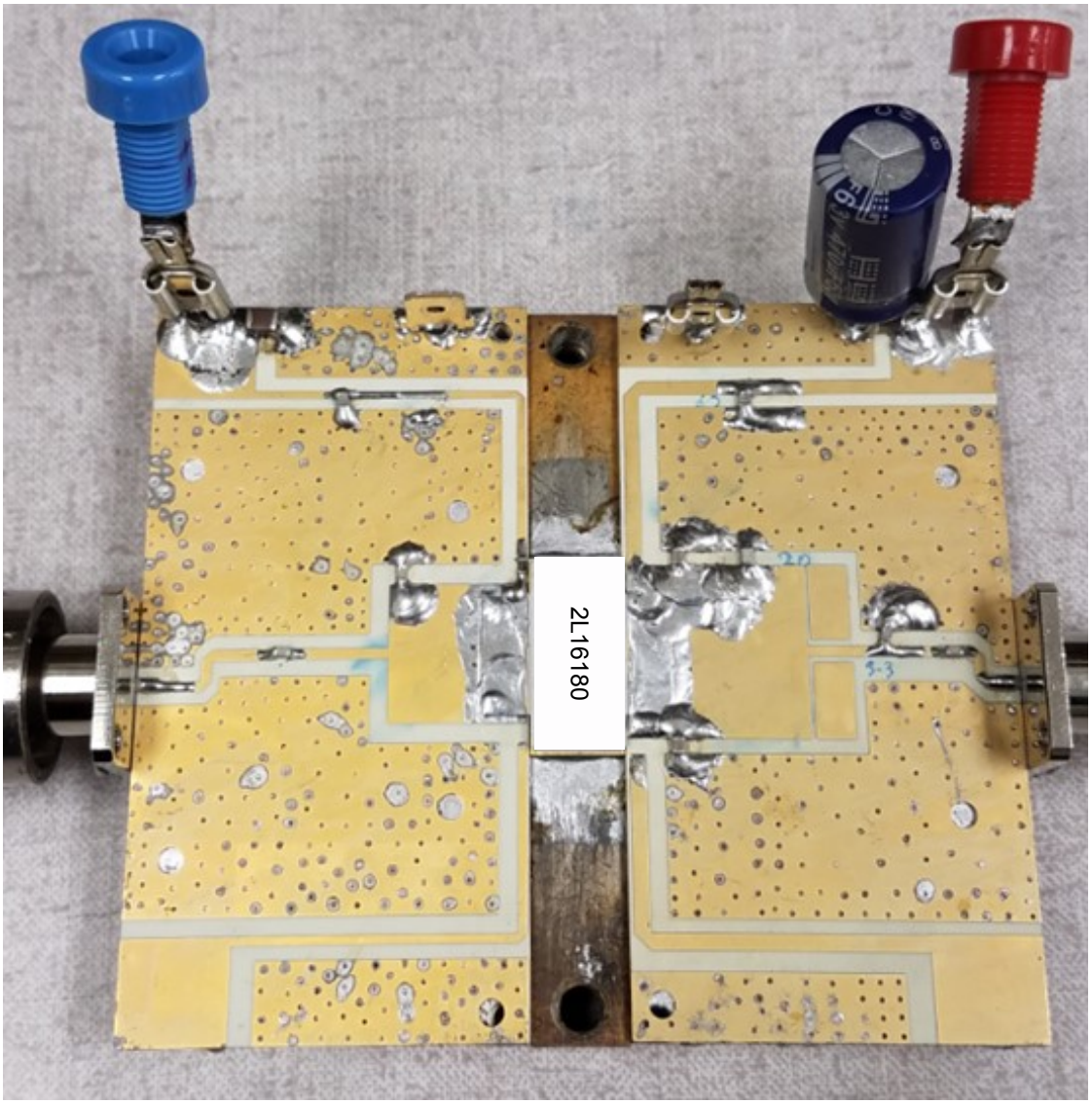


Table 8. Components list

Component	Value	Size	Reference
Q1	RF2L16180CF2		
C1	30 pF	0805	ATC600F 300
C2	2.2 pF	0805	ATC600F 2R2
C3, C10	27 pF	0805	ATC600F 270
R1	10 Ω	0603	Digi-Key P10ECT-ND
C4, C11, C12	10 uF	1210	Murata GRM32DF51H106
C5	4.7 pF	0805	ATC600F 4R7
C6	3.9 pF	0805	ATC600F 3R9
C7	5.6 pF	0805	ATC600F 5R6
C8	3.0 pF	0805	ATC600F 3R0
C9	33 pF	0805	ATC600F 330
PCB	0.508 mm (0.020") thick, εr = 3.48, Rogers RO4350B, 1 oz. copper		

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 B2 package information

Figure 4. B2 package outline

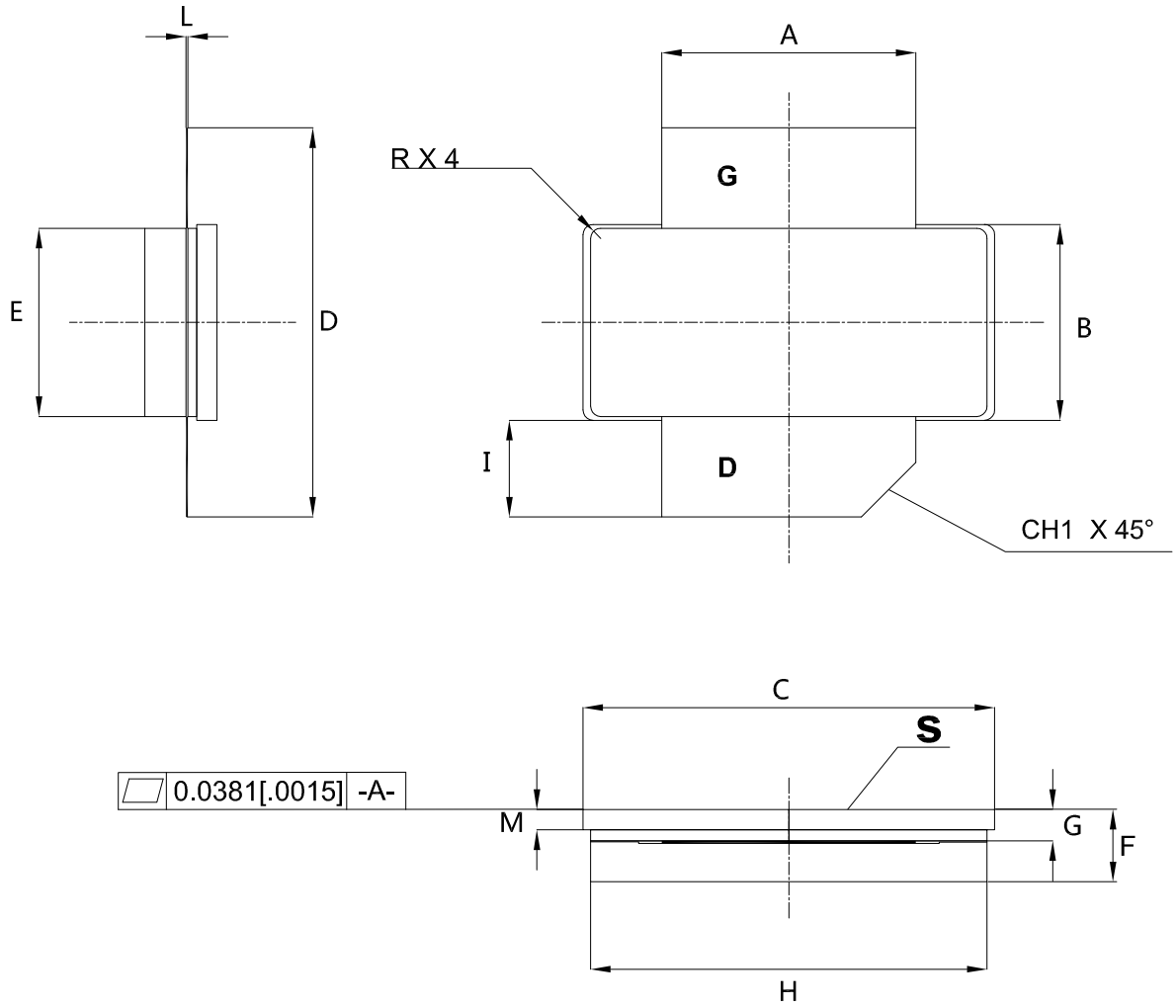
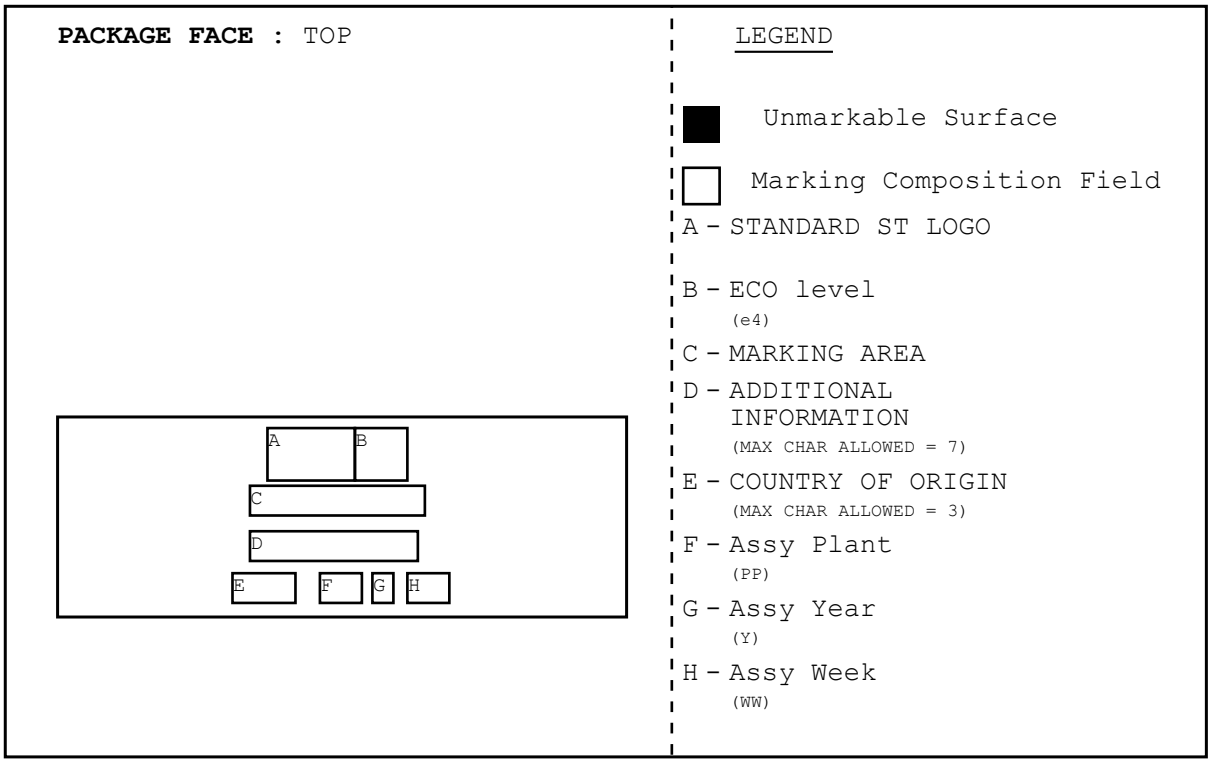


Table 9. **B2 mechanical data**

Symbol	Millimetres		
	Min	Typ	Max
A	12.57	12.7	12.83
B	9.65	9.78	9.91
C	20.44	20.57	20.70
D	19.31	19.44	19.57
E	9.27	9.40	9.53
F	3.23	3.61	3.99
G	1.44	1.57	1.70
H	19.68	19.81	19.94
I	4.70	4.83	4.96
L	0.07	0.10	0.15
M	0.89	1.02	1.15
CH1		2.72	
R		0.51	

5.2 Marking information

Figure 5. **Marking composition**



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Revision history

Table 10. **Document revision history**

Date	Version	Changes
20-Jul-2020	1	Initial release
14-Apr-2021	2	Updated Features, Description and Device summary in cover page. Updated Table 1. Absolute maximum ratings (T_C = 25 °C). and Table 3. ESD protection. Updated Table 4. Static and Table 5. Dynamic. Updated Figure 1. Power gain and drain efficiency vs output power (1440 to 1470 MHz). Updated Table 8. Components list. Added Section 5.2 Marking information. Minor text changes.

Contents

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