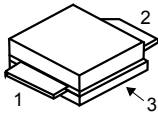


40 W, 28 V, 2.7 to 3.6 GHz RF power LDMOS transistor


A2

Pin connection	
Pin	Connection
1	Gate
2	Drain
3	Source (bottom side)



Product status link
RF2L36040CF2

Product summary	
Order code	RF2L36040CF2
Marking	2L36040
Package	A2
Packing	Tape and reel 13"
Base/bulk quantity	160/160

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF2L36040CF2	3600 MHz	28 V	40 W	14 dB	48%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- Telecom
- S-band radar

Description

The **RF2L36040CF2** is a 40 W, 28 V internally matched LDMOS FET, designed for cellular and S-band radar applications at frequencies from 2.7 to 3.6 GHz. It can be used in class AB, B or C for all typical modulation formats.

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.7	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$				
I_{GSS}	Gate-body leakage current	$V_{GS} = -6/10\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 1\text{ V}, I_D = 600\text{ }\mu\text{A}$	1.75		2.5	V
		$V_{DS} = 28\text{ V}, I_D = 600\text{ }\mu\text{A}$				
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 28\text{ V}, I_D = 380\text{ mA}$		2.8		V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}, I_D = 800\text{ mA}$	100		300	mV
		$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	300		700	
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$			1	Ω
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$			2.5	A

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		2700		3600	MHz
P_{OUT}	Output power	f = 3600 MHz, @ 1 dB compression point		40		W
G_{PS}	Power gain			14		dB
η_D	Drain efficiency			48		%
VSWR	Load mismatch	$P_{OUT} = 40\text{ W}$, all phases			10:1	

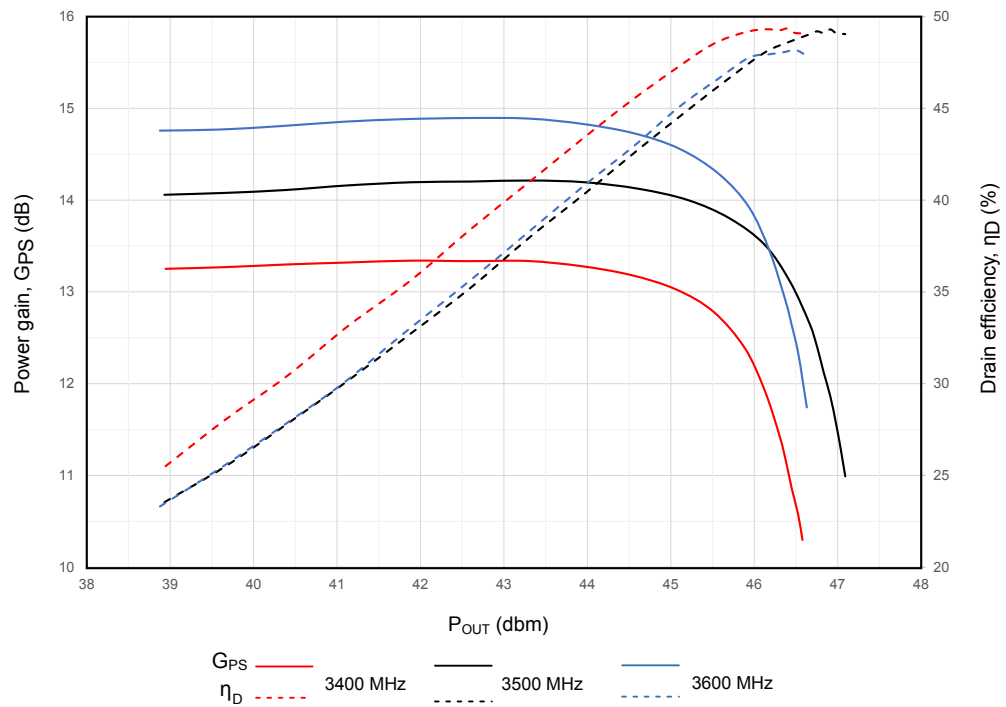
Note: $V_{DD} = 28\text{ V}, I_{DQ} = 380\text{ mA}$, pulsed CW test signal, pulse width=100 μs , duty cycle=10%.

3 Typical performances

3.1 Pulsed CW performance

Table 6. Typical performance over 3.4 - 3.6 GHz frequency band ($V_{DD}=28V$, $I_{DQ}=380\text{ mA}$)

f(MHz)	G_{PS} @ P_{1dB} (dB)	P_{3dB} (W)	η_D @ P_{3dB} (%)
3400	12.3	45.5	49
3500	13.2	50.5	49
3600	13.9	45.5	48

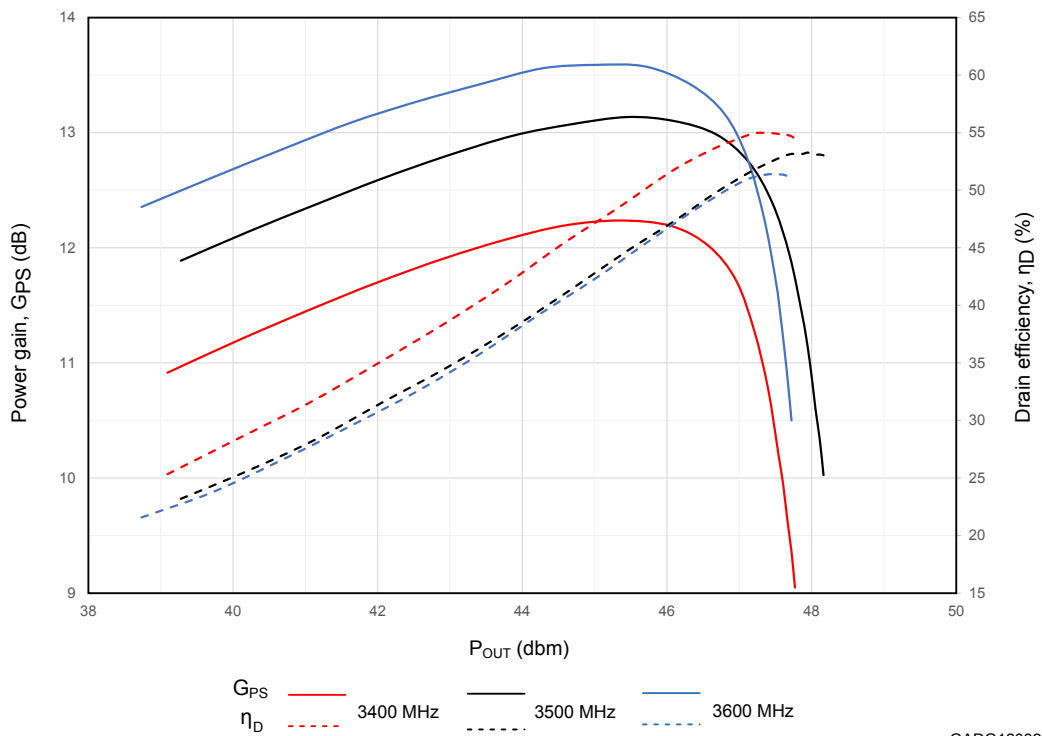
Figure 1. Power gain and drain efficiency vs output power (3.4 - 3.6 GHz frequency band, $V_{DD}=28\text{ V}$, $I_{DQ}=380\text{ mA}$)


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Table 7. Typical performance over 3.4 - 3.6 GHz frequency band ($V_{DD}=32\text{ V}$, $I_{DQ}=500\text{ mA}$)

f(MHz)	G_{PS} @ P_{1dB} (dB)	P_{3dB} (W)	η_D @ P_{3dB} (%)
3400	11.2	59.8	54.4
3500	12.2	65.5	53
3600	12.5	59	51

Figure 2. Power gain and drain efficiency vs output power (3.4 - 3.6 GHz frequency band, $V_{DD}=32\text{ V}$, $I_{DQ}=500\text{ mA}$)



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Note: Pulse width=100 μ s, duty cycle=10%.

3.2 WCDMA performance

Table 8. Typical performance vs frequency (3400 - 3600 MHz) at P_{OUT}=38 dBm

f(MHz)	P _{OUT, avg} (dBm)	CCDF(dB)	P _{OUT, peak} (dBm)	P _{OUT, peak} (W)	ACPR(dBc)	G _{PS} (dB)	η _D (%)
3400	38	8.75	46.75	47.32	38.88	13.54	23.72
3500	38	8.98	46.98	49.89	39.48	14.24	21.90
3600	38	8.65	46.65	46.24	37.45	14.39	21.54

Table 9. Typical performance vs frequency (3400 - 3600 MHz) at P_{OUT}=39 dBm

f(MHz)	P _{OUT, avg} (dbm)	CCDF(dB)	P _{OUT, peak} (dBm)	P _{OUT, peak} (W)	ACPR(dBc)	G _{PS} (dB)	η _D (%)
3400	39	8.1	47.1	51.29	35.28	13.49	26.61
3500	39	8.36	47.36	54.45	36.52	14.21	24.60
3600	39	8.01	47.01	50.23	34.46	14.27	24.35

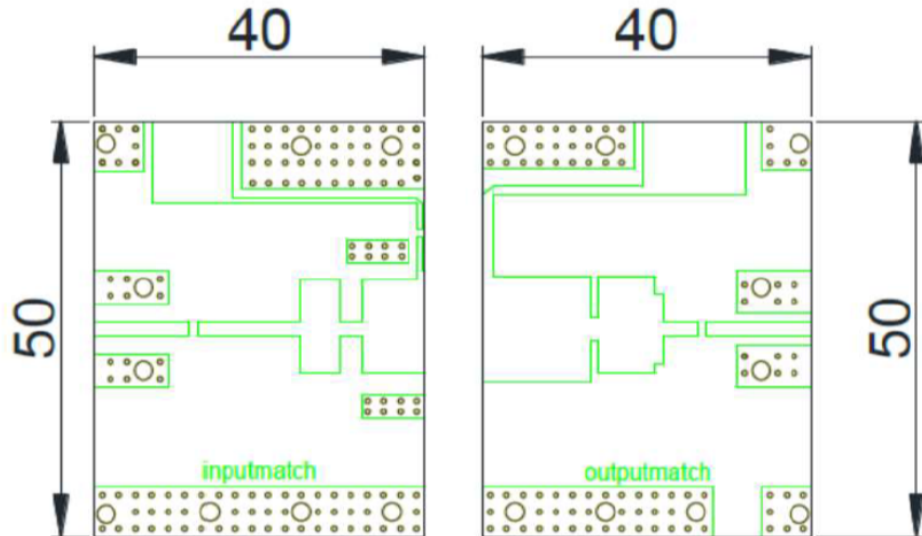
Table 10. Typical performance vs frequency (3400 - 3600 MHz) at P_{OUT}=40 dBm

f(MHz)	P _{OUT, avg} (dbm)	CCDF(dB)	P _{OUT, peak} (dBm)	P _{OUT, peak} (W)	ACPR(dBc)	G _{PS} (dB)	η _D (%)
3400	40	7.41	47.4	55.08	33.15	13.44	29.79
3500	40	7.76	47.76	59.70	33.88	14.12	27.73
3600	40	7.30	47.30	53.70	32.02	14.13	27.16

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 380\text{ mA}$, test signal WCDMA_1C (PAR=10.5 dB @0.01% probability).

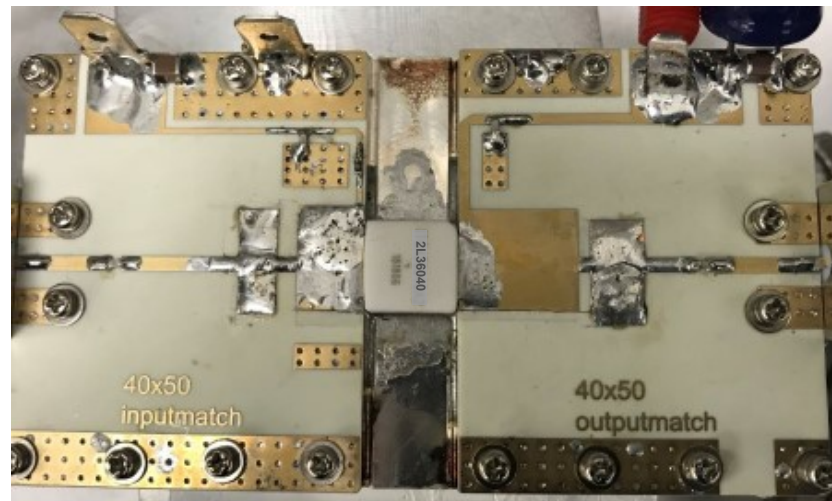
4 Test circuits

Figure 3. Test circuit layout (3400 - 3600 MHz)



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Figure 4. Test circuit photo (3400 - 3600 MHz)



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Table 11. Components list (3400 – 3600 MHz)

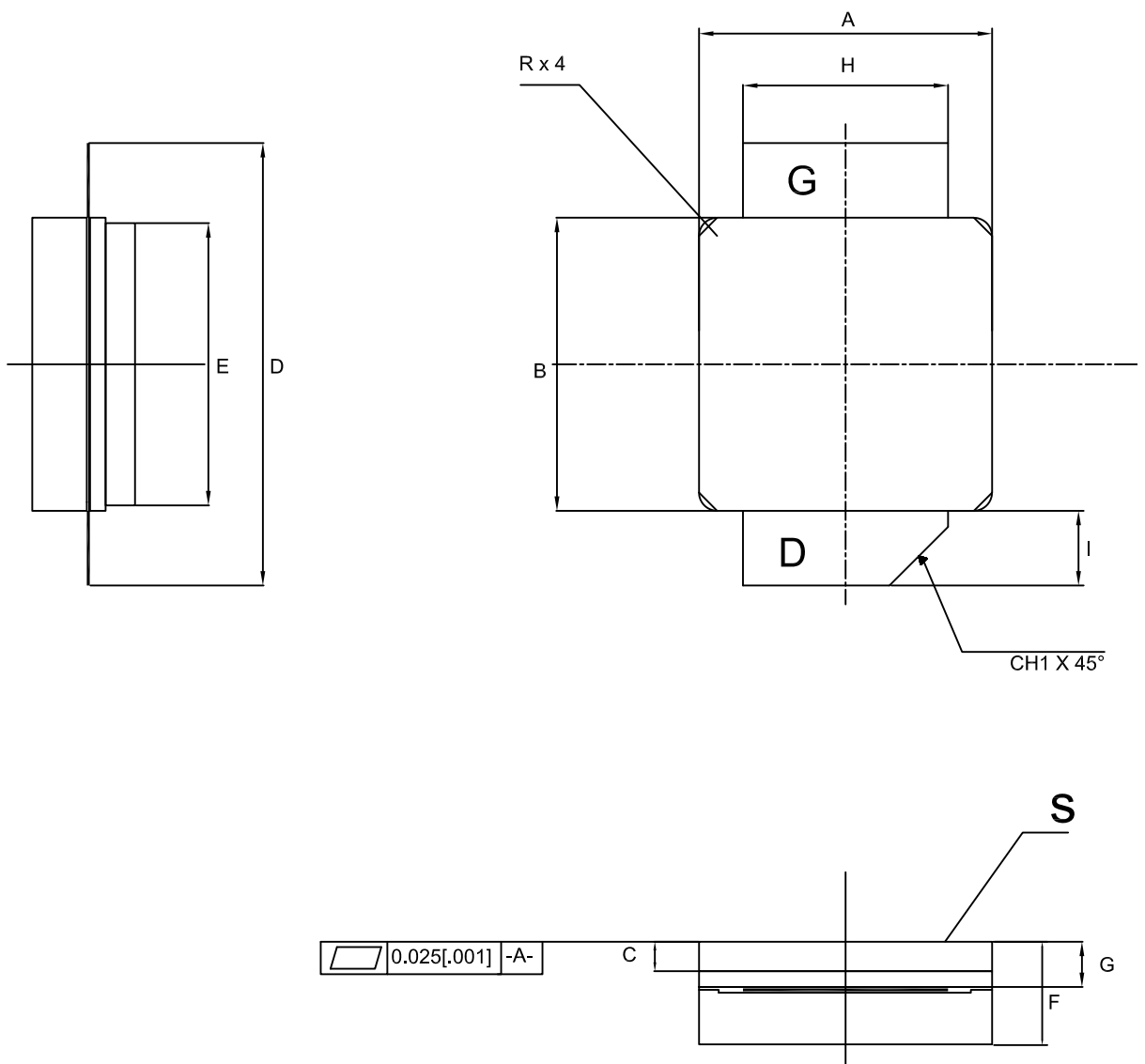
Reference	Value	Size	Reference
C1,C2,C3,C4	8.2 pF	0805	ATC600F
C3, C6, C8	10 μ F	1210	50 V ceramic multilayer capacitor
R1	10 Ω	0603	Chip resistor
PCB	0.762 mm [0.030"] thick, $\epsilon_r = 3.48$, Rogers RO4350B, 1 oz. copper		

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 A2 package information

Figure 5. A2 package outline



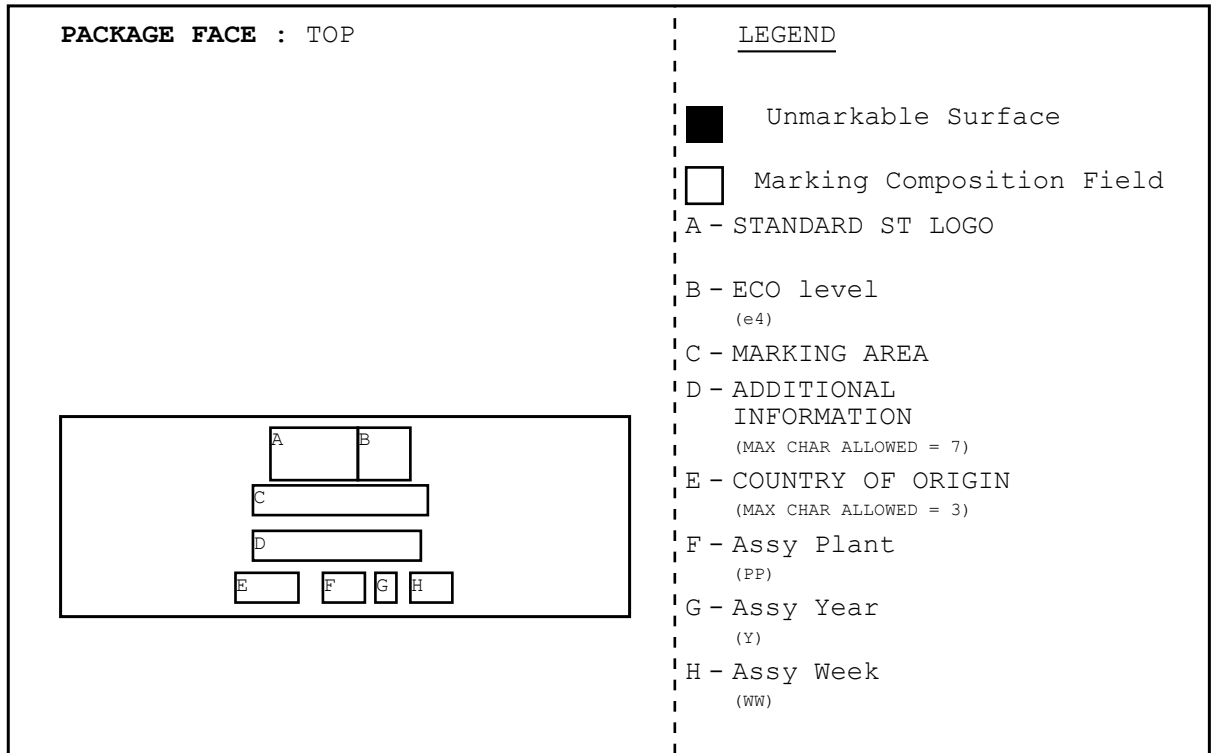
DM00418526_2

Table 12. A2 mechanical data

Symbol	Millimetres		
	Min.	Typ.	Max.
A	10.03	10.16	10.29
B	10.03	10.16	10.29
C	0.89	1.02	1.15
D	15.21	15.34	15.47
E	9.65	9.78	9.91
F	3.43	3.56	3.69
G	1.44	1.57	1.70
H	6.98	7.11	7.24
I	2.08	2.59	3.10
CH1		2.03	
R			0.63

6 Marking information

Figure 6. Marking composition



GADG040220211644GT

Revision history

Table 13. Document revision history

Date	Version	Changes
04-May-2020	1	First release.
22-Apr-2021	2	<p>Modified efficiency value and marking on cover page.</p> <p>Modified Table 1. Absolute maximum ratings ($T_C = 25\text{ }^\circ\text{C}$), Table 2. Thermal data and Table 3. ESD protection.</p> <p>Modified Table 4. Static and Table 5. Dynamic.</p> <p>Modified Figure 1. Power gain and drain efficiency vs output power (3.4 - 3.6 GHz frequency band, $V_{DD}=28\text{ V}$, $I_{DQ}=380\text{ mA}$) and Figure 2. Power gain and drain efficiency vs output power (3.4 - 3.6 GHz frequency band, $V_{DD}= 32\text{ V}$, $I_{DQ}=500\text{ mA}$).</p> <p>Modified Figure 4. Test circuit photo (3400 - 3600 MHz) and added Table 11. Components list (3400 – 3600 MHz).</p> <p>Added Section 6 Marking information.</p> <p>Minor text changes.</p>

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