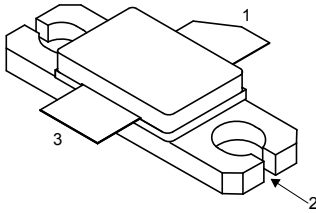


## 30 W, 50 V, HF to 1.5 GHz RF power LDMOS transistor


**GXB**

Pin connection	
Pin	Connection
1	Drain
2	Source (bottom side)
3	Gate

### Features

Order code	Frequency	V <sub>DD</sub>	P <sub>OUT</sub>	Gain	Efficiency
RF5L15030CB2	1 GHz	50 V	30 W	23.5 dB	50%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the European directive 2002/95/EC

### Applications

- Industrial, scientific and medical from HF to 1.5 GHz
- FM and TV broadcast
- HV/VHF ground communications
- Avionics and L-band radar
- Wideband communications

### Description

The RF5L15030CB2 is a 30 W, 50 V, LDMOS FET designed for applications in the frequency range from HF to 1.5 GHz. It can be used in class AB, B or C for all typical modulation formats.



Product status link
<a href="#">RF5L15030CB2</a>

Product summary	
Order code	RF5L15030CB2
Marking	5L15030
Package	GXB
Packing	Tape and reel 13"
Base/bulk quantity	180/180

# 1 Electrical ratings

**Table 1. Absolute maximum ratings ( $T_C = 25\text{ °C}$ )**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	110	V
$V_{GS}$	Gate-source voltage	-8 to 10	V
$V_{DD}$	Maximum operating voltage	55	V
$T_{STG}$	Storage temperature range	-65 to 150	°C
$T_J$	Maximum junction temperature	200	°C

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	2.9	°C/W

1.  $T_C = 85\text{ °C}$ ,  $P_{OUT} = 30\text{ W}$ , DC test.

**Table 3. ESD protection**

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	H2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

## 2 Electrical characteristics

**Table 4. Static**

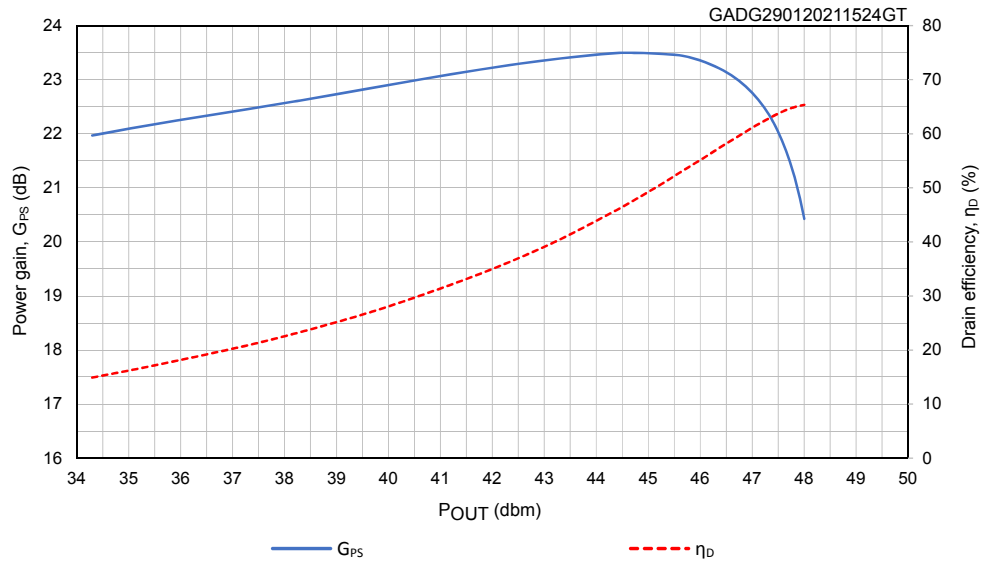
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_{DS} = 100\ \mu\text{A}$	110			V
$I_{DSS}$	Zero gate voltage drain leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 90\text{ V}$				
$I_{GSS}$	Gate-source leakage current	$V_{GS} = -8/10\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 50\text{ V}, I_{DS} = 600\ \mu\text{A}$	1		3	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}, I_{DS} = 100\text{ mA}$	2		5	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}, I_{DS} = 1\text{ A}$			1.1	V
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}, V_{DS} = 0.1\text{ V}$			1	$\Omega$
$C_{iss}$	Common source input capacitance	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V}, f = 1\text{ MHz}$		28		pF
$C_{rSS}$	Common source feedback capacitance			0.4		pF
$C_{oss}$	Common source output capacitance			12		pF

**Table 5. Dynamic**

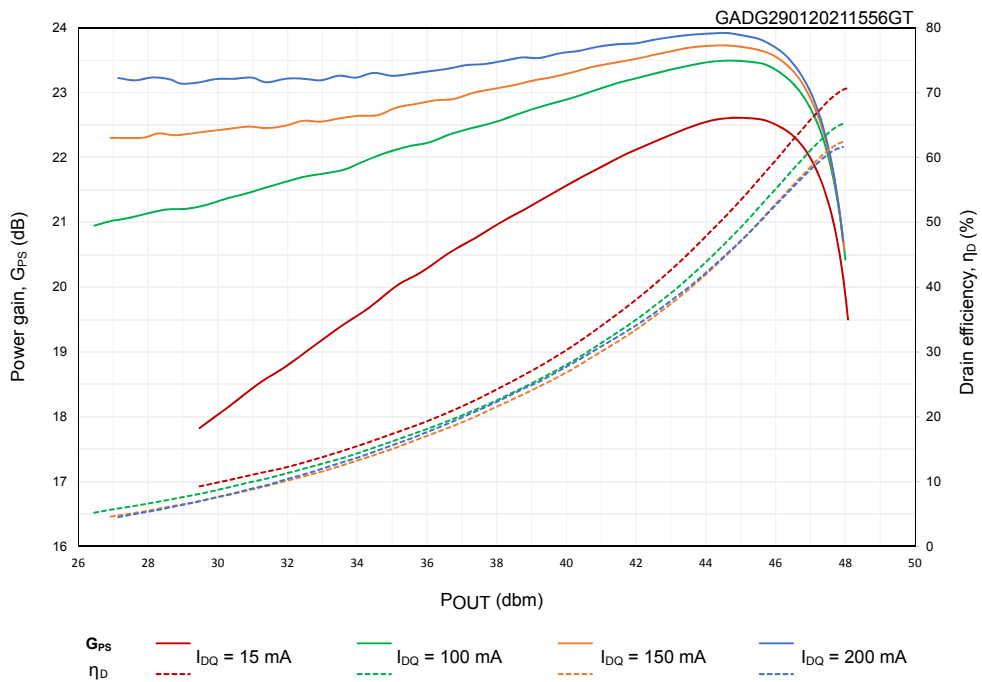
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{OUT}$	Output power	$f = 1\text{ GHz}$	-	30		W
$G_{PS}$	Power gain		-	23.5		dB
$\eta_D$	Drain efficiency		-	50		%
VSWR	Load mismatch	$P_{OUT} = 30\text{ W}$ , all phases	-		10:1	

Note:  $V_{DD} = 50\text{ V}, I_{DQ} = 0.1\text{ A}$ , pulsed CW, pulse width = 100  $\mu\text{s}$ , duty cycle = 10%.

### 3 Typical performances

**Figure 1. Power gain and drain efficiency versus output power (f = 1 GHz)**


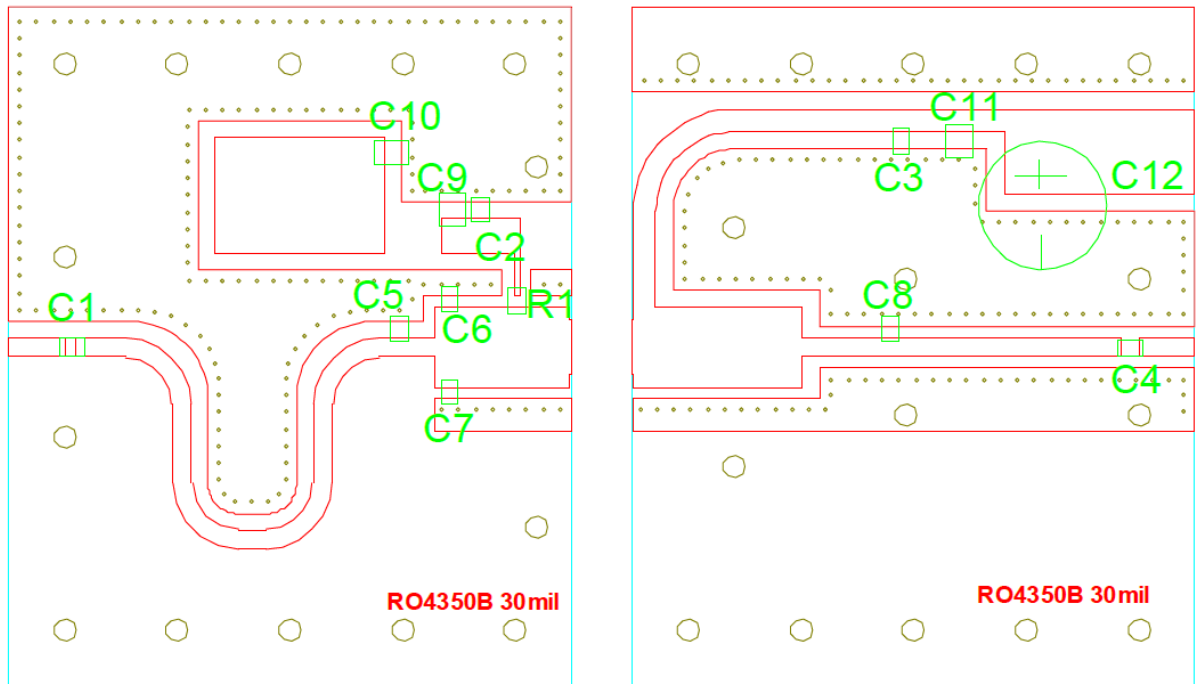
Note:  $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 0.1\text{ A}$ , pulsed CW, pulse width = 100  $\mu\text{s}$ , duty cycle = 10%.

**Figure 2. Power gain and drain efficiency versus output power at different  $I_{DQ}$  (f = 1 GHz)**


Note:  $V_{DD} = 50\text{ V}$ , pulsed CW, pulse width = 100  $\mu\text{s}$ , duty cycle = 10%.

## 4 Test circuits

Figure 3. Test circuit layout

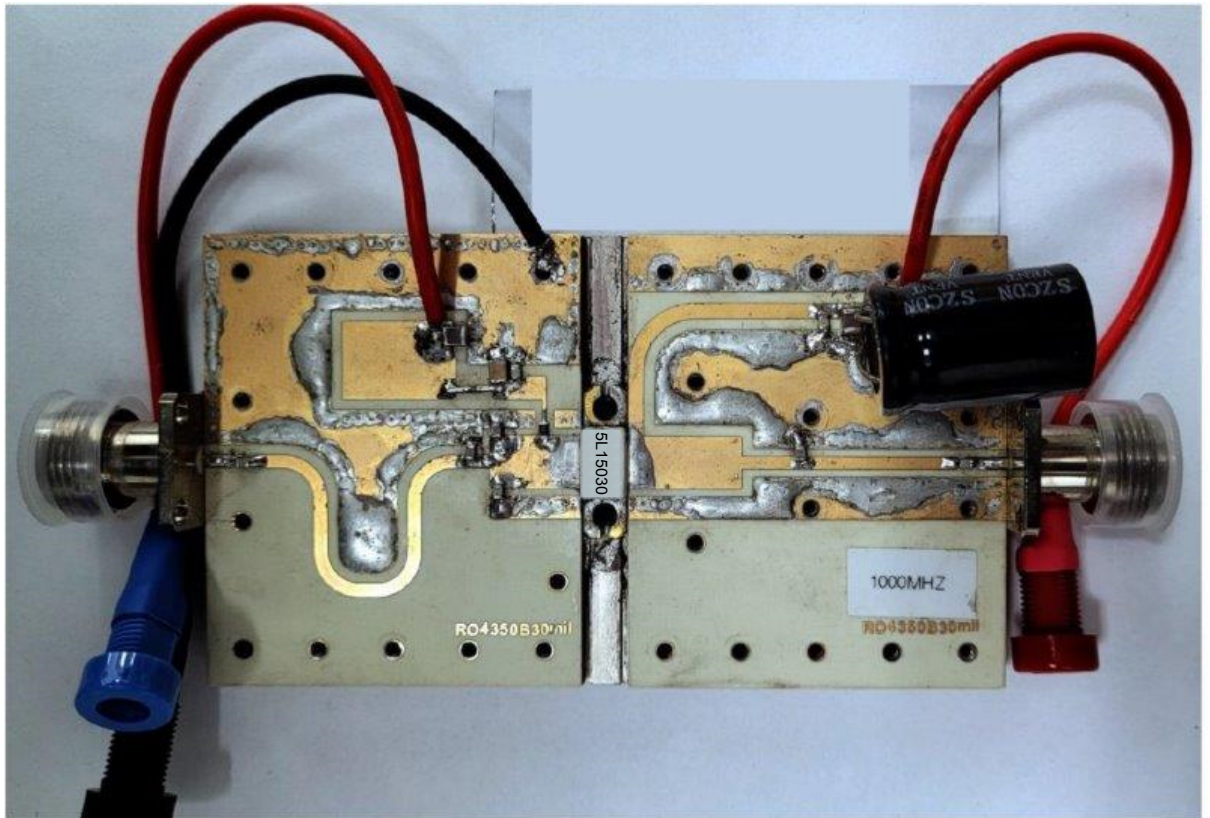


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Table 6. Components list

Component	Value	Size	Reference
C1, C2, C3, C4	39 pF	0805	ATC600F
C5, C6, C7	8.2 pF	0805	ATC600F
C8	6.8 pF	0805	ATC600F
C9	10 nF	1210	
C10, C11	10 $\mu$ F	1210	X7R
C12	1000 $\mu$ F		Aluminium electrolytic capacitor
R1	15 $\Omega$	0805	
PCB	0.762 mm (0.030") thick, $\epsilon_r = 3.48$ , Rogers RO4350B, 1 oz. copper		

Figure 4. Test circuit photo



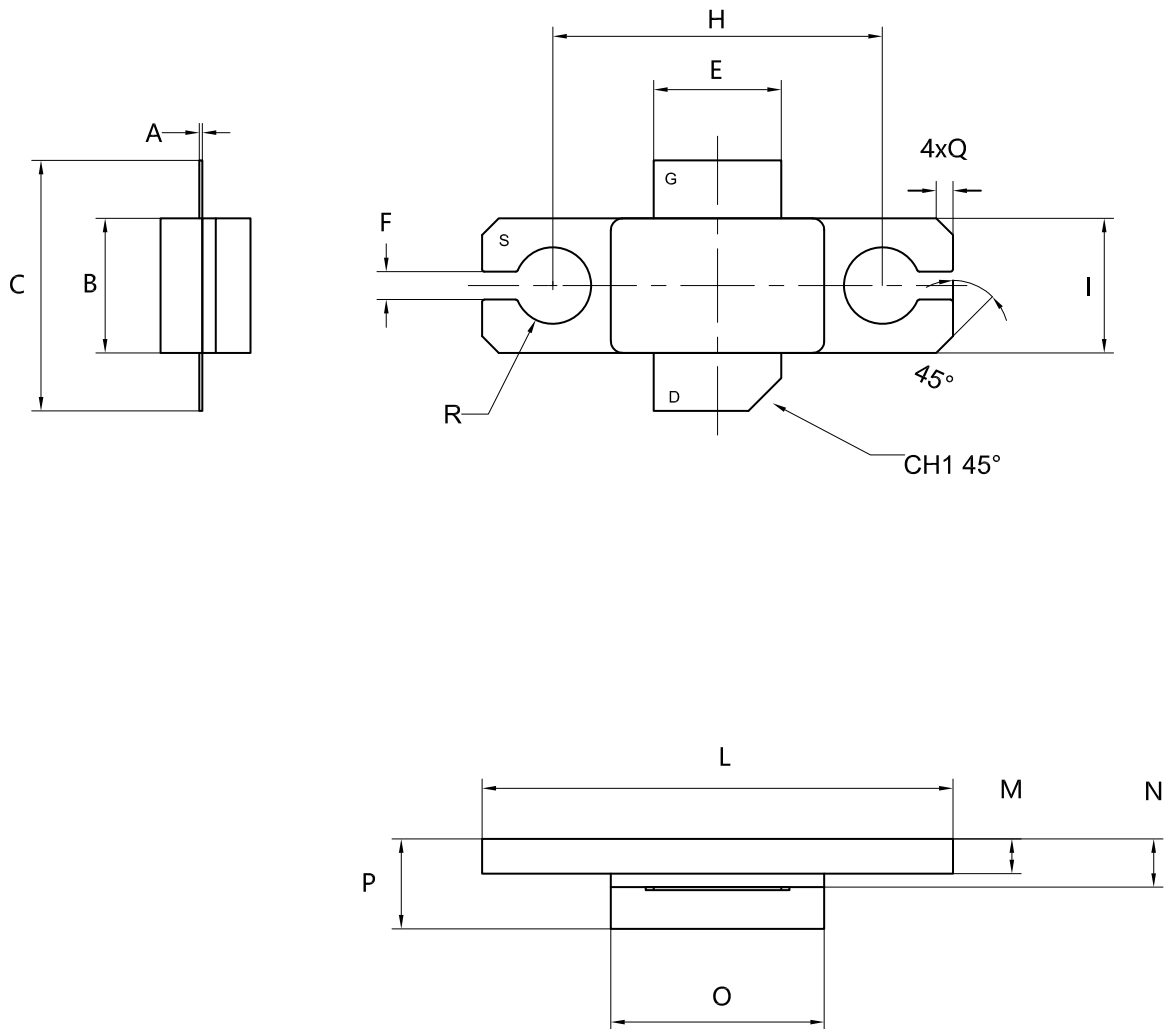
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## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 5.1 GBX package information

Figure 5. GXB package outline



DM00666716\_2

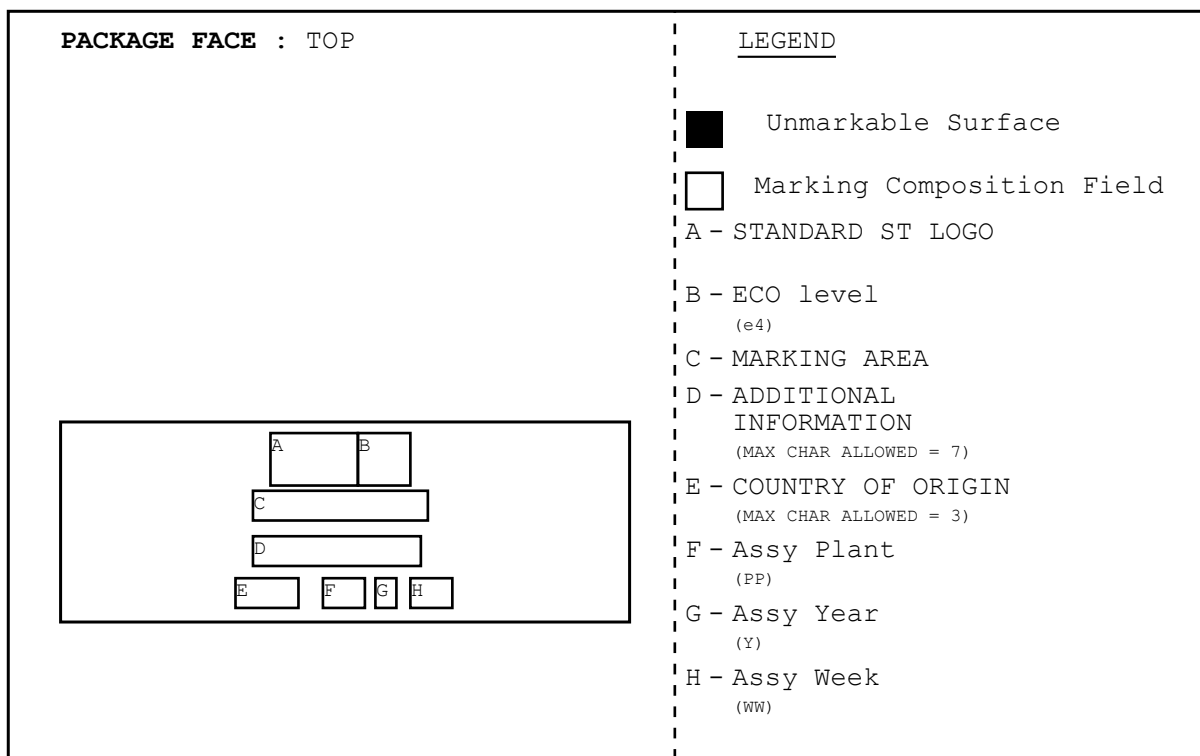
**Table 7. GXB package mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.11	0.13	0.15
B	5.75		5.80
C	10.30	10.80	11.30
E	5.45	5.50	5.55
F	1.15	1.20	1.25
H	14.15	14.20	14.25
I	5.75	5.80	5.85
L	20.25	20.30	20.35
M	1.45	1.50	1.55
N	2.03	2.08	2.13
O	9.15		9.20
P	3.78	3.88	4.18
Q	0.73	1.00	1.27
R	3.17	3.30	3.43
CH1		2.00	



## 5.2 Marking information

Figure 6. Marking composition



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## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
10-Feb-2021	1	First release.
28-Sep-2021	2	Updated <a href="#">Table 3</a> . ESD protection. Updated <a href="#">Table 4</a> . Static. Minor text changes.

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