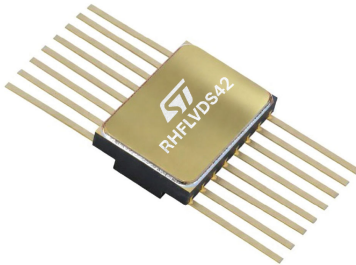


## Rad-hard 2.5 V quad LVDS receiver



Flat-16 hermetic ceramic  
(with metallic lid electrically  
connected to ground)

Maturity status link

[RHFLVDS42](#)

### Features

- 600 Mbps (300 MHz)
- 2.5 V and 3.3 V power supply compatibility
- LVCMOS outputs as per JESD80 (2.5) and JESD64-A (2.5/3.3)
- 4.8 V absolute rating
- Large input common-mode: -4 V to +5 V
- 8 kV HDM on LVDS input pins
- Flow-through pinout for reduced crosstalk
- Enable/disable function with high-impedance pull-up, pull-down
- Fail-safe function on all I/Os
- Cold spare
- Hermetic package
- Guaranteed up to 300 krad TID (Si)
- No SEL at 122.6 MeV.cm<sup>2</sup>/mg
- No SET/SEU at 61.3 MeV.cm<sup>2</sup>/mg
- Mass: 0.65 g
- SMD pin number: coming soon

### Applications

- High data rate communication in satellites

### Description

The **RHFLVDS42** is a quad, low-voltage, differential signaling (LVDS) receiver specifically designed, packaged, and qualified for use in aerospace environments in a low-power and fast point-to-point baseband data transmission standard.

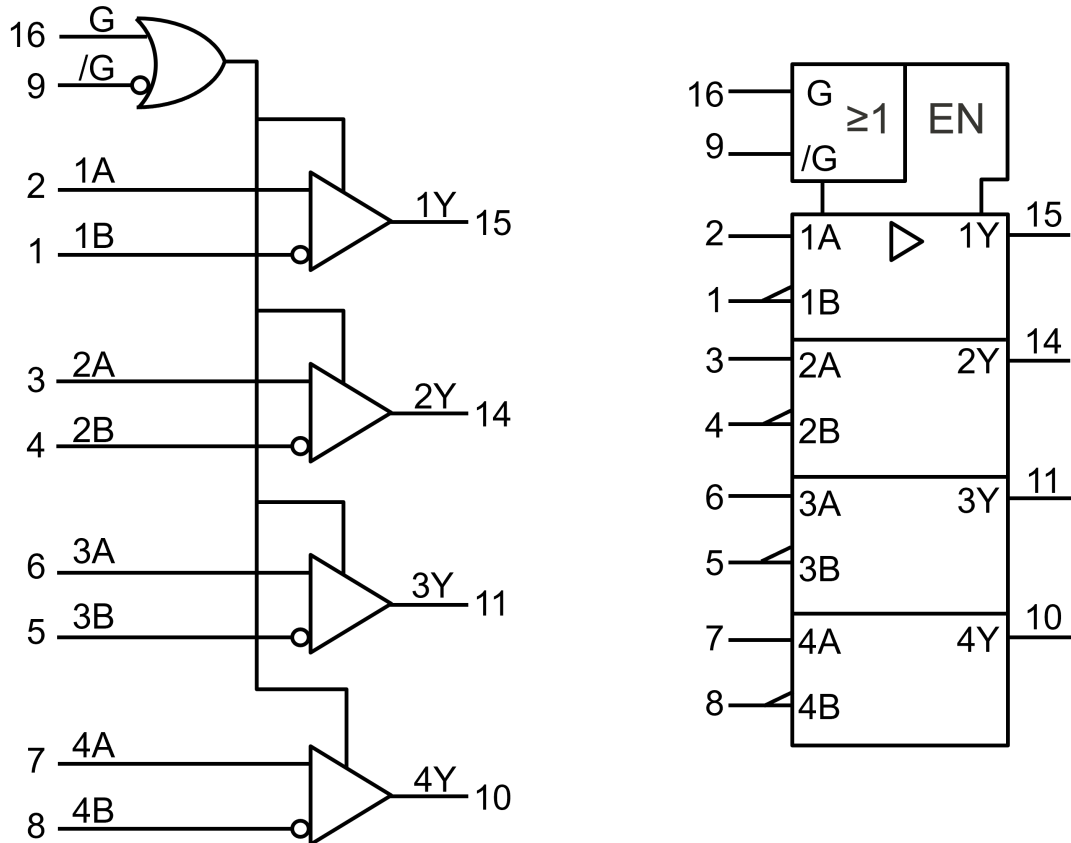
Operating from a 2.3 V to 3.6 V power supply, the **RHFLVDS42** operates over a controlled impedance of 100 Ω transmission media, which may be printed circuit board traces, back planes or cables, and it features an extended input common-mode from -4 V to +5 V to prevent difference in groundings.

The circuit features an internal fail-safe function to ensure a known state in case of floating input.

Designed on ST's proprietary CMOS process with specific mitigation techniques, the **RHFLVDS42** achieves "best in the class" for hardness to total ionizing dose and heavy ions.

The **RHFLVDS42** can operate over a -55 °C to +125 °C range and it is housed in a hermetic ceramic Flat-16 package.

# 1 Functional description

**Figure 1. Logic diagram and logic symbol**

**Table 1. Truth table**

Differential input A, B	Enables		Output
	G	/G	Y
$V_{ID} \geq 100 \text{ mV}$	H	X	H
	X	L	H
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	H	X	Indeterminate level
	X	L	Indeterminate level
$V_{ID} \leq -100 \text{ mV}$	H	X	L
	X	L	L
X	L	H	Z
Open / short or terminated	H	X	H
	X	L	H

Note: 1) The G input features an internal pull-up network. The /G input features an internal pull-down network. If they are floating, the circuit is enabled.

2)  $V_{ID} = V_{IA} - V_{IB}$

3) L = low level, H = high level, X = whatever the level, Z = high impedance (off)

## 2 Pin connections

Figure 2. Pin connections (top view). Flow-through pinout

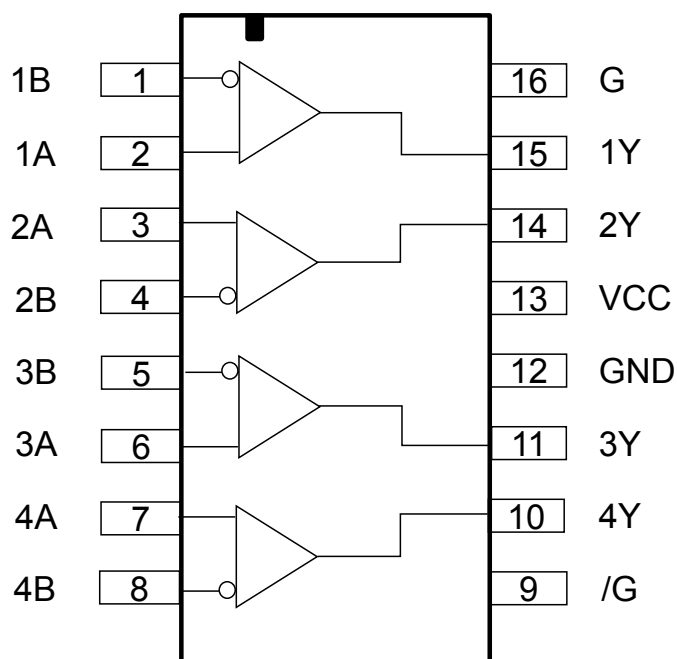


Table 2. Pin description

Pin number	Symbol	Name and function
2, 3, 6, 7	1A to 4A	Receiver inputs
1, 4, 5, 8	1B to 4B	Negated receiver inputs
15, 14, 11, 10	1Y to 4Y	Receiver outputs
16	G	Enable/disable inputs
9	/G	
13	GND	Ground
12	V <sub>CC</sub>	Supply voltage

### 3 Maximum ratings and operating conditions

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
VCC <sup>(1)</sup>	Maximum power supply between VCC and GND	4.8	V
VIN	CMOS inputs (G, /G)	-0.3 to 4.8	
VOOUT	LVC MOS outputs (nY)	-0.3 to 4.8	
VIN	LVDS inputs (nA and nB) (operating or cold-spares)	-5 to +6	V <sub>pp</sub>
VID	Differential amplitude on LVDS input, over -3.5 V to +4.5 V VCM range (operating or cold-spares)	5	
Tstg	Storage temperature range	-65 to +150	°C
Tj <sup>(2)</sup>	Maximum junction temperature	+150	
Rth <sup>(3)</sup>	Junction-to-ambient thermal resistance (Rthja)	80	°C/W
	Junction-to-case thermal resistance (Rthjc)	22	
ESD	HBM (Human Body Model) on all pins, pin to pin (protections are GG MOS type, snapback behavior).	2 k	V
	HBM on LVDS outputs, versus GND protections are SCR (Silicon Control Rectifier) type, snapback behavior.	8 k	
	CDM: Charge device model	500	

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.
2. Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions as per the method 5004 of MIL-STD-883.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

**Note:** Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

**Table 4. Operating conditions**

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply voltage vs. GND	2.3	3.6	V
VCM	Static common-mode on LVDS input	-4	+5	V
VIN	Input voltage on LVC MOS inputs (G, /G)	0	3.6 (whatever VCC)	V
Ta	Ambient temperature range	-55	+125	°C

## 4 Radiations

### Total ionizing dose (TID):

The RHFLVDS42 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, in high-dose rate only (full CMOS technology), between 50 and 300 rad/s, followed by annealing at room temperature.

When applicable, parameters provided in Table 6 apply to both pre- and post-irradiation and annealing, as follows:

- All TID tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883.
- The initial characterization is performed in qualification on both biased and unbiased parts.
- Each new wafer lot is tested at high-dose rate, in the worst bias case condition, based on the results obtained during the initial qualification.

### Heavy ions:

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

**Table 5. Radiations**

Symbol	Characteristics		Value	Unit
TID <sup>(1)</sup>	High-dose rate (50 to 300 rad (Si)/s)		300	krad
SEL <sup>(2) (3)</sup>	Temperature: 125 °C Fluence: 1 x 10 ions/cm <sup>2</sup> V <sub>CC</sub> = 3.6 V (max. operating)	For a particle angle of 60°, no SEL observed at :	122.6	MeV.cm <sup>2</sup> /mg
		For a particle angle of 0°, no SEL observed at :	61.3	
SET/SEU <sup>(4)</sup>	Particle angle: 0° Temperature: 25 °C Fluence: 1 x 10 <sup>7</sup> ions/cm <sup>2</sup> V <sub>CC</sub> = 2.3 V (min. operating)	No SET/SEU observed at :	61.3	

1. A total ionizing dose (TID) of 300 krad (Si) is equivalent to 3000 Gy (Si), (1 gray = 100 rad).

2. SEL: single event latch-up.

3. Fluence: number (n) of particles on a specified area (cm<sup>2</sup>). 1x10<sup>7</sup> n/cm<sup>2</sup> is equivalent to 10 million particles per cm<sup>2</sup>.

4. SET, SEU: single-event transient, single-event upset.

## 5 Electrical characteristics

### 5.1 For 2.5 V power supply

$V_{CC} = 2.3 \text{ V}$  to  $2.7 \text{ V}$ , capa-load ( $C_L$ ) =  $10 \text{ pF}$ , typical values are at ambient  $T_a = +25 \text{ }^\circ\text{C}$ , min. and max values are at  $T_a = -55 \text{ }^\circ\text{C}$  and  $+125 \text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 6. Electrical characteristics**

Symbol	Parameters	Test conditions	Min.	Typ.	Max	Unit
$I_{CC}$	Total enabled supply current, receivers not switching	$V_{ID} = 400 \text{ mV}$		12	13.5	mA
$I_{CCZ}$	Total disabled supply current, receivers loaded or not loaded	$V_{ID} = 400 \text{ mV}$ , $G = \text{GND}$ , $/G = V_{CC}$			4	mA
$V_{IH}$	Input voltage high	G and /G inputs	1.7			V
$V_{IL}$	Input voltage low				0.8	
$I_{IH}$	High-level input current	G and /G inputs $V_{CC} = 2.7 \text{ V}$ , $V_{IN} = V_{CC}$	-10		10	$\mu\text{A}$
$I_{IL}$	Low-level input current	G and /G inputs $V_{CC} = 2.7 \text{ V}$ , $V_{IN} = 0$	-10		10	
$I_{OFF}^{(1)}$	LVDS inputs power-off leakage current	$V_{CC} = 0 \text{ V}$ , $V_{IN} = -4 \text{ V}$ to $+5 \text{ V}$	-60		60	
	LVC MOS I/Os power-off leakage current	$V_{CC} = 0 \text{ V}$ , $2.7 \text{ V}$ on $V_{OUT}$			10	
	G, /G power-off leakage current	$V_{CC} = 0 \text{ V}$ , $2.7 \text{ V}$ on G and /G			10	
$V_{TL}$	Differential input low threshold	$0 \text{ V} < V_{CM} < +2.4 \text{ V}$			-100	mV
		$-4 \text{ V} < V_{CM} < +5 \text{ V}$			-130	
$V_{TH}$	Differential input high threshold	$0 \text{ V} < V_{CM} < +2.4 \text{ V}$	+100			
		$-4 \text{ V} < V_{CM} < +5 \text{ V}$	+130			
$V_{CL}$	Input clamp voltage on G /G	$I_{CL} = 18 \text{ mA}$	-1.5			V
$I_{ID}$	Differential input current	$V_{ID} = 400 \text{ mVp-p}$	-10		+10	$\mu\text{A}$
$I_{ICM}$	Common-mode input current	$-4 \text{ V} < V_{CM} < +5 \text{ V}$	-70		+70	
$V_{OH}$	Output voltage high	$I_{OH} = -100 \text{ } \mu\text{A}$ , $V_{CC} = 2.3 \text{ V}$	2.1			V
$V_{OL}$	Output voltage low	$I_{OH} = 100 \text{ } \mu\text{A}$ , $V_{CC} = 2.3 \text{ V}$			0.2	
$I_{OS}$	Output short-circuit current	$V_{OUT} = 0 \text{ V}$ , $V_{CC} = 2.7 \text{ V}$	-70		-20	mA
$I_{OZ}$	Output tri-state current	Disabled, $V_{OUT} = 0 \text{ V}$ or $V_{CC}$	-10		+10	$\mu\text{A}$
$C_{IN}$	Input capacitance	IN+ or IN- to GND		3		pF
$R_{OUT}$	Output resistance	$I_{OUT} = \pm 2 \text{ mA}$ , $V_{CC} = 2.7 \text{ V}$	45		68	$\Omega$
$T_{PHLD}$	Propagation delay time, high to low output (see Figure 6)	$V_{ID} = 200 \text{ mVp-p}$ , input pulse from $1.1 \text{ V}$ to $1.3 \text{ V}$ ,	1.3		3	ns
$T_{PLHD}$	Propagation delay time, low to high output (see Figure 6)	$V_{CM} = 1.2 \text{ V}$ , load: $10 \text{ pF}$ (see Figure 3)	1.3		3	
$T_r^{(2)}$	Output signal rise time (see Figure 6)	Load: $10 \text{ pF}$ (see Figure 3)	1.1		1.8	ns
		Load: $4 \text{ pF}$ (see Figure 4)	0.5		0.8	
		No load (see Figure 5)	0.2	0.4	0.6	
$T_f^{(2)}$	Output signal fall time (see Figure 6)	Load: $10 \text{ pF}$ (see Figure 3)	1.1		1.8	ps
		Load: $4 \text{ pF}$ (see Figure 4)	0.5		0.8	
		No load (see Figure 5)	0.2	0.4	0.6	

Symbol	Parameters	Test conditions	Min.	Typ.	Max	Unit
Freq	Operating frequency	No load (see Figure 5)		250		MHz
T <sub>SK1</sub> <sup>(3)</sup>	Channel-to-channel skew	V <sub>ID</sub> = 200 mVp-p Load: refer to Figure 3			350	ps
T <sub>SK2</sub> <sup>(4)</sup>	Chip-to-chip skew				700	
T <sub>SKD</sub> <sup>(5)</sup>	Differential skew (T <sub>PHLD</sub> - T <sub>PLHD</sub> )				500	
T <sub>PHZ</sub>	Propagation delay time, high level to high impedance output	Refer to Figure 7			6	ns
T <sub>PLZ</sub>	Propagation delay time, low level to high impedance output				6	
T <sub>PZH</sub>	Propagation delay time, high impedance to high-level output				6	
T <sub>PZL</sub>	Propagation delay time, high impedance to low-level output				6	
TD1	Fail-safe to active time			2.5		μs
TD2	Active to fail-safe time			2.1		
Cpd <sup>(6)</sup>	Power dissipation capacitance	F <sub>in</sub> = 100 MHz		40		pF

1. All pins except pin under test and V<sub>CC</sub> are floating.
2. Guaranteed by design and characterization.
3. T<sub>SK1</sub> is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).
4. T<sub>SK2</sub> is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature. T<sub>SK2</sub> is guaranteed by design and characterization.
5. T<sub>SKD</sub> is the maximum delay time difference between T<sub>PHLD</sub> and T<sub>PLHD</sub>.
6. Cpd is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to test circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$  (per circuit).

## 5.2 For 3.3 V power supply

$V_{CC} = 3\text{ V}$  to  $3.6\text{ V}$ , capa-load ( $C_L$ ) =  $10\text{ pF}$ , typical values are at ambient  $T_a = +25\text{ }^\circ\text{C}$ , min. and max values are at  $T_a = -55\text{ }^\circ\text{C}$  and  $+125\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 7. Electrical characteristics**

Symbol	Parameters	Test conditions	Min.	Typ.	Max	Unit
$I_{CC}$	Total enabled supply current, receivers not switching	$V_{ID} = 400\text{ mV}$		13	15	mA
$I_{CCZ}$	Total disabled supply current, receivers loaded or not loaded	$V_{ID} = 400\text{ mV}$ $G = \text{GND}, /G = V_{CC}$			4	mA
$V_{IH}$	Input voltage high	G and /G inputs	2			V
$V_{IL}$	Input voltage low				0.8	
$I_{IH}$	High-level input current	G and /G inputs $V_{CC} = 3.6\text{ V}$ , $V_{IN} = V_{CC}$	-10		10	$\mu\text{A}$
$I_{IL}$	Low-level input current	G and /G inputs $V_{CC} = 3.6\text{ V}$ , $V_{IN} = 0$	-10		10	
$I_{OFF}^{(1)}$	LVDS inputs power-off leakage current	$V_{CC} = 0\text{ V}, V_{IN} = -4\text{ V to }+5\text{ V}$	-60		60	
	LVC MOS I/Os power-off leakage current	$V_{CC} = 0\text{ V}, 3.6\text{ V on }V_{OUT}$			10	
	G, /G power-off leakage current	$V_{CC} = 0\text{ V}, 3.6\text{ V on G and /G}$			10	
$V_{TL}$	Differential input low threshold	$0\text{ V} < V_{CM} < +2.4\text{ V}$			-100	mV
		$-4\text{ V} < V_{CM} < +5\text{ V}$			-130	
$V_{TH}$	Differential input high threshold	$0\text{ V} < V_{CM} < +2.4\text{ V}$	+100			
		$-4\text{ V} < V_{CM} < +5\text{ V}$	+130			
$V_{CL}$	Input clamp voltage on G /G	$I_{CL} = 18\text{ mA}$	-1.5			V
$I_{ID}$	Differential input current	$V_{ID} = 400\text{ mVp-p}$	-10		+10	$\mu\text{A}$
$I_{ICM}$	Common-mode input current	$-4\text{ V} < V_{CM} < +5\text{ V}$	-70		+70	
$V_{OH}$	Output voltage high	$I_{OH} = -100\text{ }\mu\text{A}, V_{CC} = 3\text{ V}$	2.8			V
$V_{OL}$	Output voltage low	$I_{OH} = 100\text{ }\mu\text{A}, V_{CC} = 3\text{ V}$			0.2	
$I_{OS}$	Output short-circuit current	$V_{OUT} = 0\text{ V}, V_{CC} = 3.6\text{ V}$	-90		-30	mA
$I_{OZ}$	Output tri-state current	Disabled, $V_{OUT} = 0\text{ V or }V_{CC}$	-10		+10	$\mu\text{A}$
$C_{IN}$	Input capacitance	IN+ or IN- to GND		3		pF
$R_{OUT}$	Output resistance	$I_{OUT} = \pm 2\text{ mA}, V_{CC} = 3.6\text{ V}$	43		65	$\Omega$
$T_{PHLD}$	Propagation delay time, high to low output (see Figure 6)	$V_{ID} = 200\text{ mVp-p}$ , input pulse from 1.1 V to 1.3 V, $V_{CM} = 1.2\text{ V}$ , load: $10\text{ pF}$ (see Figure 3)	1		2.5	ns
$T_{PLHD}$	Propagation delay time, low to high output (see Figure 6)		1		2.5	
$T_r^{(2)}$	Output signal rise time (see Figure 6)	Load: $10\text{ pF}$ (see Figure 3)	1.1		1.7	ns
		Load: $4\text{ pF}$ (see Figure 4)	0.5		0.7	
		No load (see Figure 5)	0.2	0.35	0.5	
$T_f^{(2)}$	Output signal fall time (see Figure 6)	Load: $10\text{ pF}$ (see Figure 3)	1		1.7	ps
		Load: $4\text{ pF}$ (see Figure 4)	0.5		0.7	
		No load (see Figure 5)	0.2	0.35	0.5	

Symbol	Parameters	Test conditions	Min.	Typ.	Max	Unit
Freq	Operating frequency	No load (see Figure 5)		300		MHz
T <sub>SK1</sub> <sup>(3)</sup>	Channel-to-channel skew	V <sub>ID</sub> = 200 mVp-p Load: refer to Figure 3			350	ps
T <sub>SK2</sub> <sup>(4)</sup>	Chip-to-chip skew				700	
T <sub>SKD</sub> <sup>(5)</sup>	Differential skew (T <sub>PHLD</sub> - T <sub>PLHD</sub> )				400	
T <sub>PHZ</sub>	Propagation delay time, high level to high impedance output	Refer to Figure 7			4.5	ns
T <sub>PLZ</sub>	Propagation delay time, low level to high impedance output				4.5	
T <sub>PZH</sub>	Propagation delay time, high impedance to high-level output				4.5	
T <sub>PZL</sub>	Propagation delay time, high impedance to low-level output				4.5	
TD1	Fail-safe to active time			2.5		μs
TD2	Active to fail-safe time			2.1		
Cpd <sup>(6)</sup>	Power dissipation capacitance	F <sub>in</sub> = 100 MHz		40		pF

1. All pins except pin under test and V<sub>CC</sub> are floating.
2. Guaranteed by design and characterization.
3. T<sub>SK1</sub> is the maximum delay time difference between all outputs of the same device (measured with all inputs connected together).
4. T<sub>SK2</sub> is the maximum delay time difference between outputs of all devices when they operate with the same supply voltage, at the same temperature. T<sub>SK2</sub> is guaranteed by design and characterization.
5. T<sub>SKD</sub> is the maximum delay time difference between T<sub>PHLD</sub> and T<sub>PLHD</sub>.
6. Cpd is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load (refer to test circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$  (per circuit).

## 6 Wave form and test circuit

Figure 3. Load A

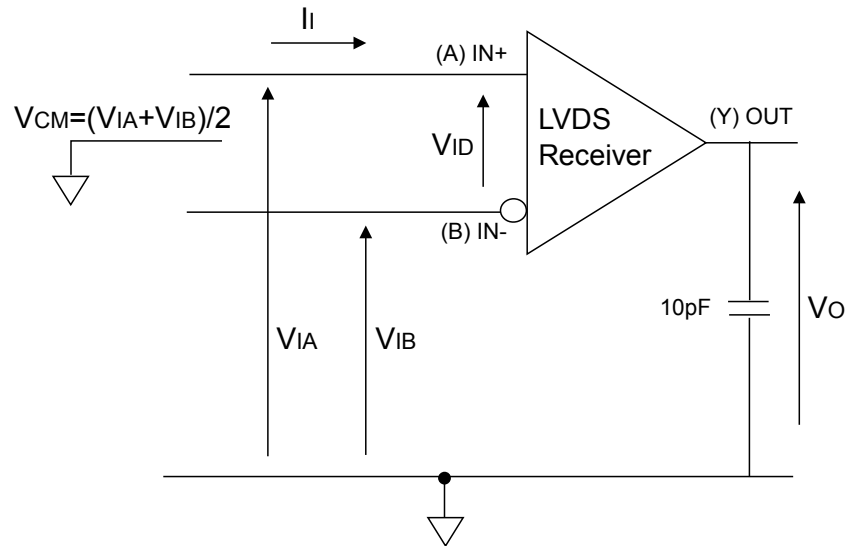


Figure 4. Load B

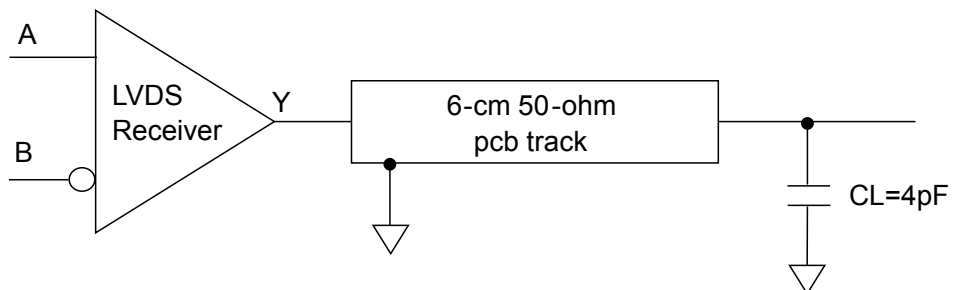


Figure 5. Load C

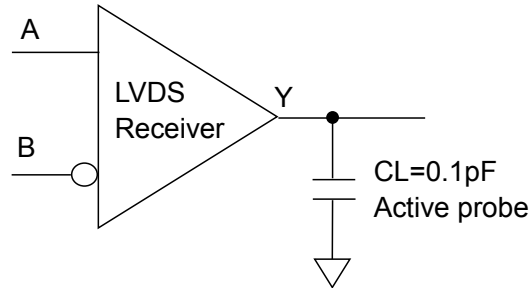
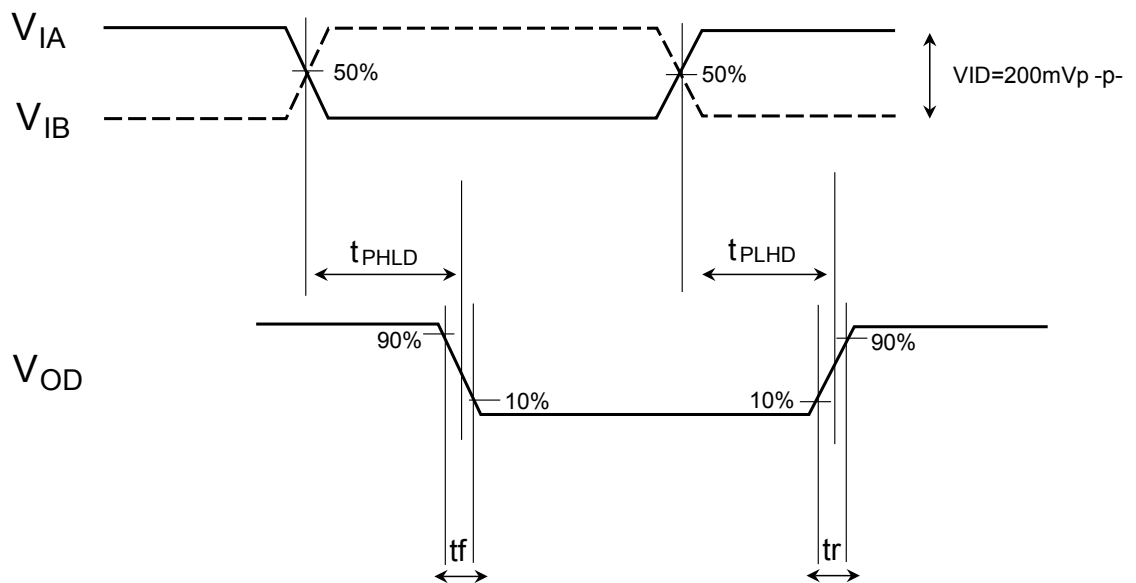


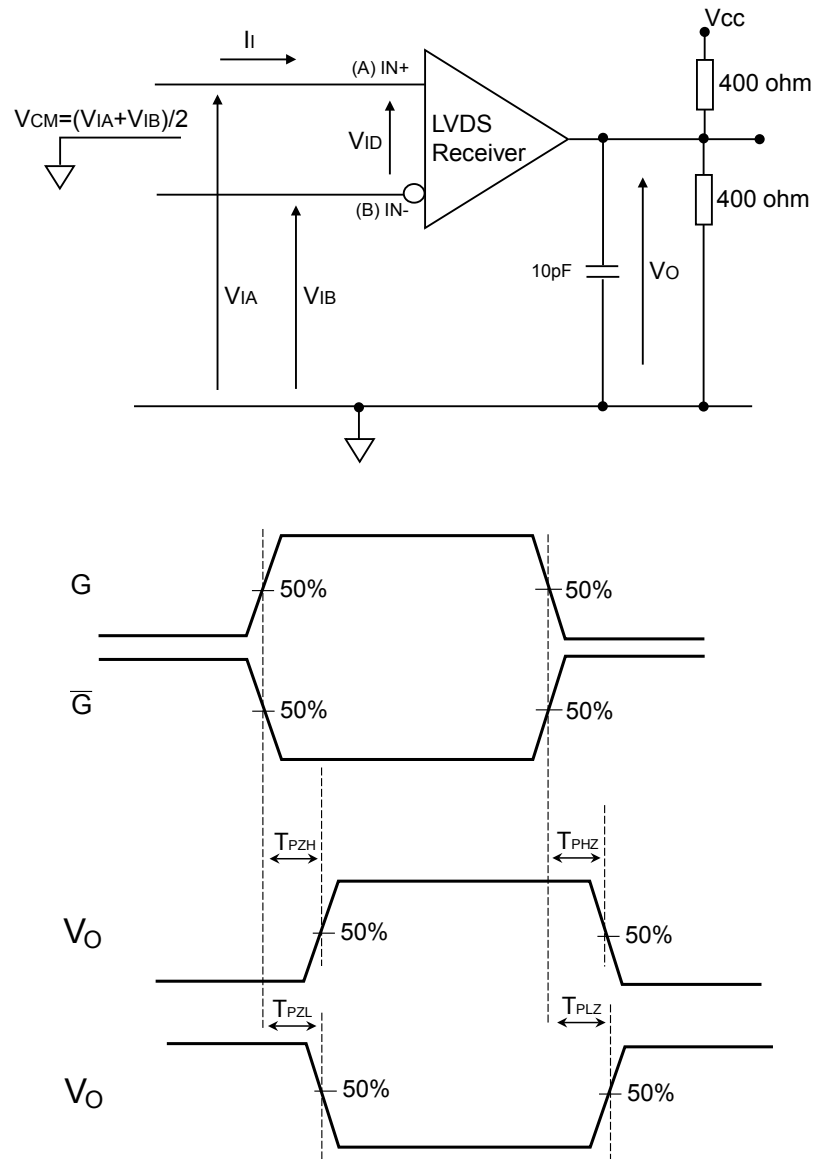
Figure 6. Timing definition



Note:

1. All input pulses are supplied by a generator with the following characteristics:  $t_r$  or  $t_f \leq 1$  ns,  $f = 1$  MHz,  $Z_0 = 50 \Omega$ , and duty cycle = 50%.
2. The product is guaranteed in test with  $C_L = 10$  pF.
3. **Fail-safe:** In many applications, inputs need a fail-safe function to avoid an uncertain output state when the inputs are not connected properly. In case of an LVDS input short-circuit or floating inputs, the TTL outputs remain in stable logic-high state.

Figure 7. Enable and disable time test circuit and timing diagram



- Note:
1. All input pulses (including G and /G) are supplied by a generator with the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency on G or /G = 500 kHz, and pulse width on G or /G = 500 ns.
  2. The product is guaranteed in test with  $C_L = 10$  pF.

## 7 Application

### 7.1 Cold spare

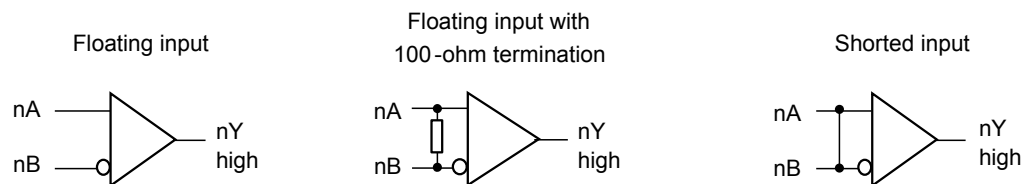
In order to support the cold spare functionality, all I/Os are fail safe according to JEP174 definition. There are no diodes between I/Os and the power supply in order to support cold spare functionality.

- The ESD protections have to be Snapback protection or IEC protection (JEP174)
- RC timed ESD protections are not allowed due to their side effect on signal dynamics
- All pull-ups have to be disconnected when the device is not supplied
- The outputs have to be connected through a diode, NMOS or a bulk control has to be implemented on the PMOS to prevent current flowing from the output to VCC when the device is not supplied

### 7.2 Fail-safe functionality of LVDS input

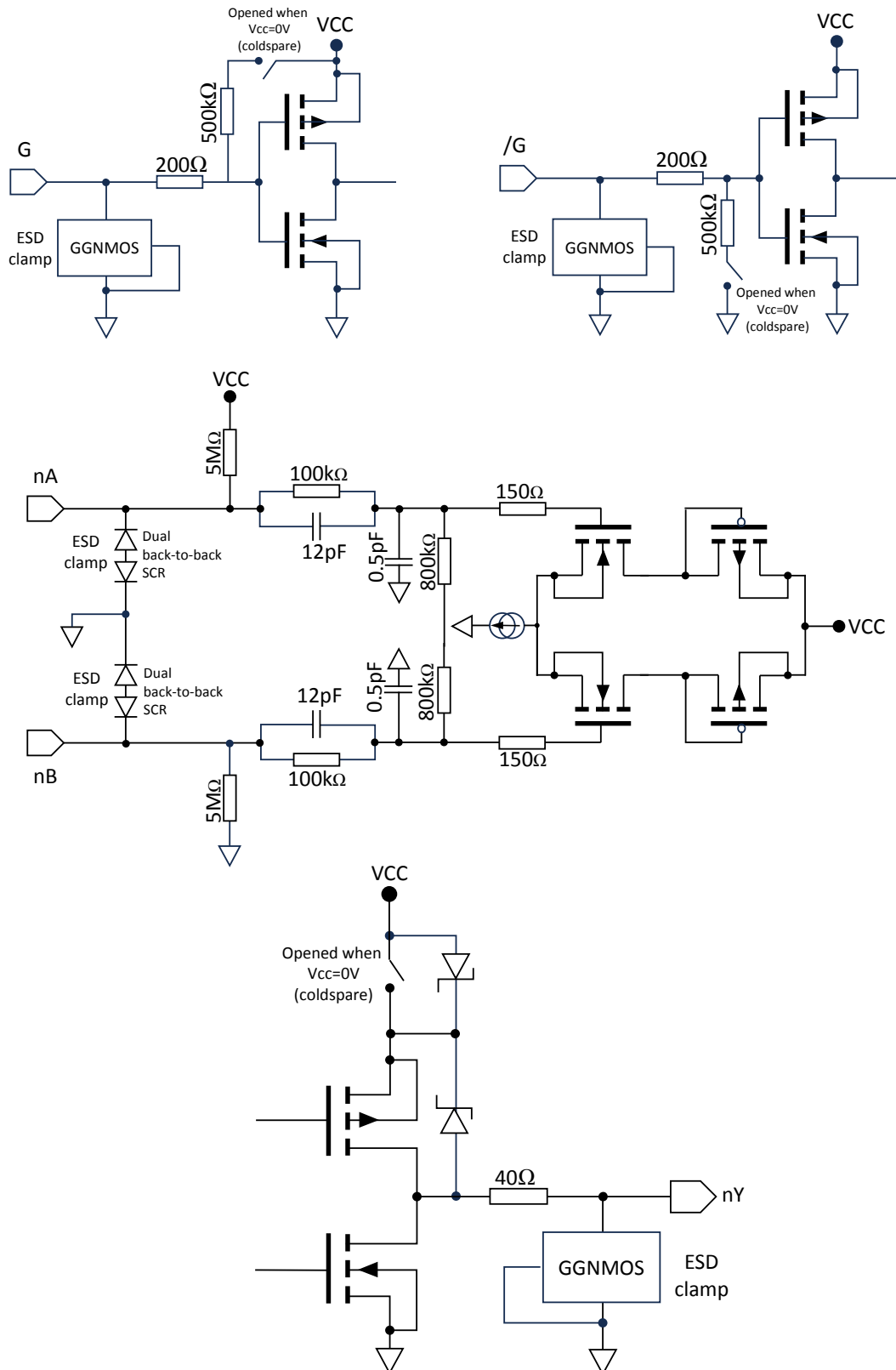
In many applications, inputs need a fail-safe function to avoid the propagation of an uncertain output state when the inputs are not connected properly. Thanks to its fail-safe function, the RHFLVDS42 forces the outputs (1Y, 2Y, 3Y, 4Y) into a stable and known logic-high state when its LVDS inputs (nA, nB) are floating (opened) or shorted. See Table 1 and Figure 8.

**Figure 8. Fail-safe condition**



## 8 Input output equivalent circuit diagram

Figure 9. I/Os schematic



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## 9 Package information

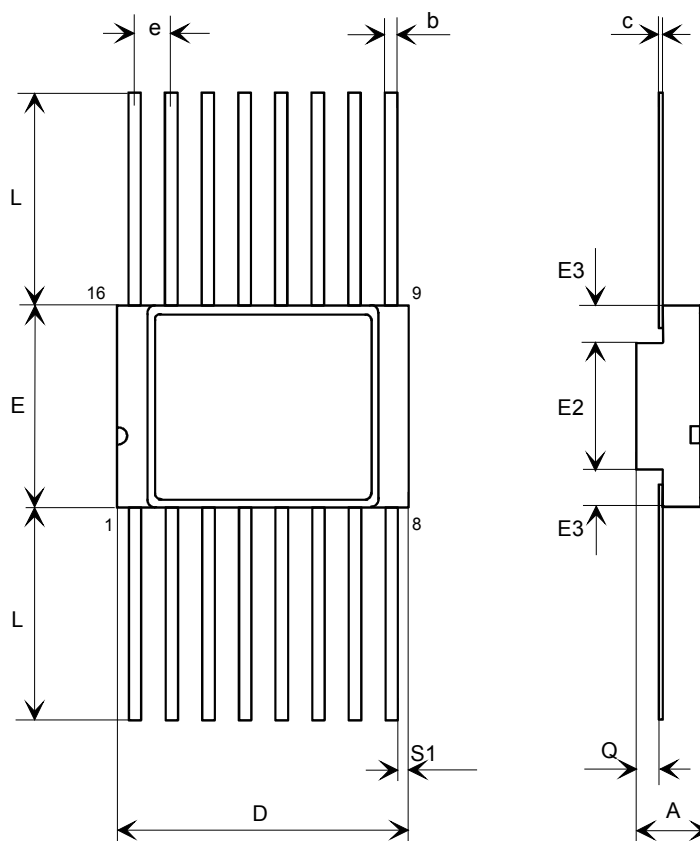
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To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 9.1 Flat-16 package information

The upper metallic lid is electrically connected to AGND and DGND.

**Figure 10. Flat-16 package information outline**



**Table 8. Flat-16 package mechanical data**

Ref.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31		2.72	0.091		0.107
b	0.38		0.48	0.015		0.019
c	0.10		0.18	0.004		0.007
D	9.75		10.13	0.384		0.399
E	6.75		7.06	0.266		0.278
E2		4.32			0.170	
E3	0.76			0.030		
e		1.27			0.050	
L	6.35		7.36	0.250		0.290
Q	0.66		1.14	0.026		0.045
S1	0.13			0.005		

## 10 Ordering information

**Table 9. Order codes**

Order code	Quality level	Package	Lead-finish	Marking	Packing
RH-LVDS42K1	Engineering Model	Flat-16 with grounded-lid	Gold	RH-LVDS42K1	Tray

*Note:* Contact your ST sales office for information about the specific conditions for products in die form.

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
10-Feb-2026	1	Initial release.
18-Mar-2026	2	Updated packing from Conductive Strip pack to Tray in Table 9.

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