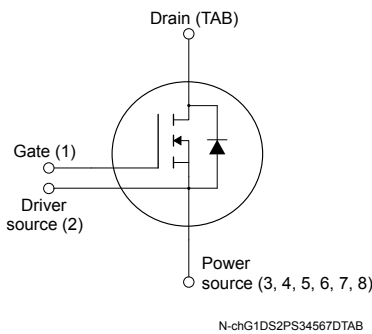
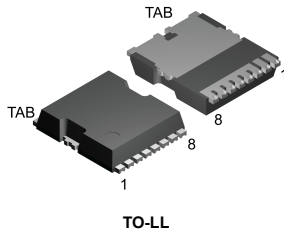


Silicon carbide Power MOSFET 650 V, 29 mΩ typ., 60 A in a TO-LL package



Product status link

[SCT027TO65G3](#)

Product summary

Order code	SCT027TO65G3
Marking	027TO65G3
Package	TO-LL
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} typ.	I _D
SCT027TO65G3	650 V	29 mΩ	60 A

- Very fast and robust intrinsic body diode
- Very low R_{DS(on)} over the entire temperature range
- High speed switching performances
- Source sensing pin for increased efficiency

Applications

- AC-DC converters
- DC-DC converters

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 3rd generation SiC MOSFET technology. The device features a very low R_{DS(on)} over the entire temperature range combined with low capacitances and very high switching operations, which improve application performance in frequency, energy efficiency, system size and weight reduction.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating values)	-5 to 18	
	Gate-source transient voltage, $t_p < 1 \mu s$, $t \leq 10$ hours over lifetime	-11 to 25	
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25 \text{ }^\circ\text{C}$	60	A
	Drain current (continuous) at $T_C = 100 \text{ }^\circ\text{C}$	60	
$I_{DM}^{(2)}$	Drain current (pulsed)	267	A
P_{TOT}	Total power dissipation at $T_C = 25 \text{ }^\circ\text{C}$	395	W
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Limited by bonding wires.
2. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.38	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = -10\text{ to }22\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$	1.8	3.0	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 15\text{ V}$, $I_D = 30\text{ A}$		32.8		m Ω
		$V_{GS} = 18\text{ V}$, $I_D = 30\text{ A}$		29	39.3	
		$V_{GS} = 18\text{ V}$, $I_D = 30\text{ A}$, $T_J = 175\text{ °C}$		39		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1173	-	pF
C_{oss}	Output capacitance		-	128	-	pF
C_{riss}	Reverse transfer capacitance		-	16	-	pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $V_{GS} = -5\text{ to }18\text{ V}$, $I_D = 30\text{ A}$	-	52.9	-	nC
Q_{gs}	Gate-source charge		-	15.4	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.5	-	Ω

Table 5. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	$V_{DD} = 400\text{ V}$, $I_D = 30\text{ A}$,	-	83.3	-	μJ
E_{off}	Turn-off switching energy	$R_G = 5.6\text{ }\Omega$, $V_{GS} = -5\text{ to }18\text{ V}$	-	99.6	-	μJ

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 30\text{ A}$, $R_G = 5.6\text{ }\Omega$, $V_{GS} = -5\text{ to }18\text{ V}$	-	15.9	-	ns
t_r	Rise time		-	6.9	-	ns
$t_{d(off)}$	Turn-off delay time		-	28.8	-	ns
t_f	Fall time		-	8.2	-	ns

Table 7. Reverse SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Continuous diode forward current	$T_C = 25\text{ }^\circ\text{C}$	-		60	A
		$T_C = 100\text{ }^\circ\text{C}$	-		60	
V_{SD}	Diode forward voltage	$I_{SD} = 30\text{ A}, V_{GS} = 0\text{ V}$	-	2.73		V
t_{rr}	Reverse recovery time	$I_{SD} = 30\text{ A}, 1\text{ kA}/\mu\text{s}, V_{DD} = 400\text{ V}$	-	15.4		ns
Q_{rr}	Reverse recovery charge		-	85.2		nC
I_{RRM}	Reverse recovery current		-	9.2		A

1. Limited by bonding wires.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

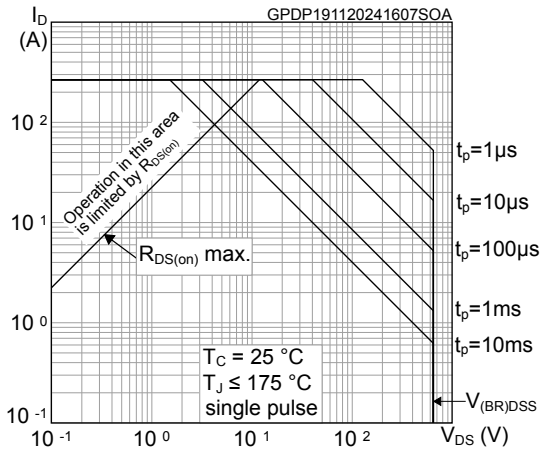


Figure 2. Maximum transient thermal impedance

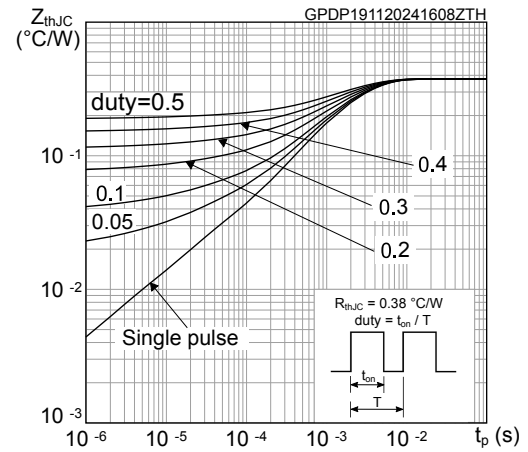


Figure 3. Typical output characteristics (T_J = 25 °C)

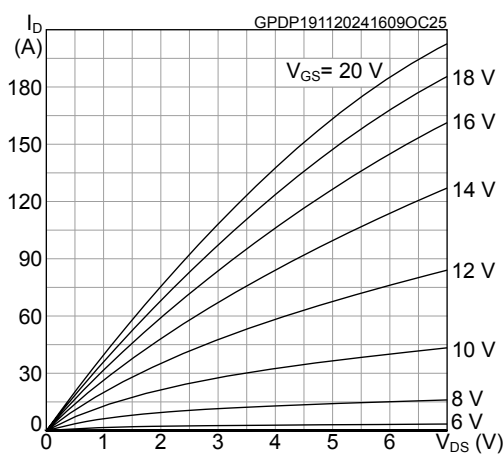


Figure 4. Typical output characteristics (T_J = 175 °C)

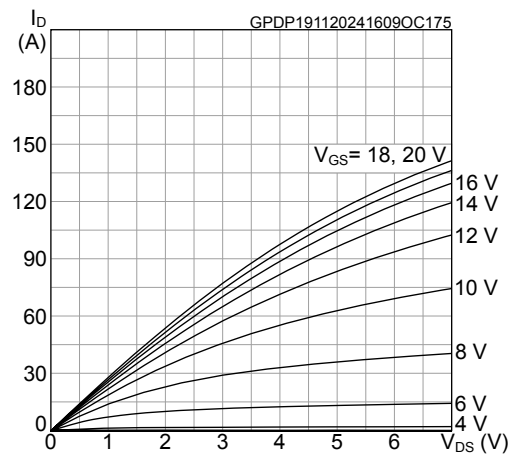


Figure 5. Typical transfer characteristics

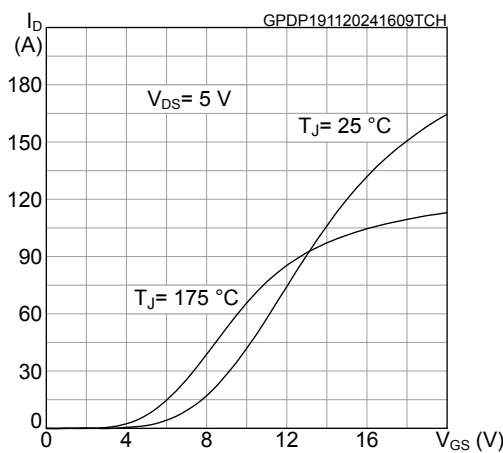


Figure 6. Total power dissipation

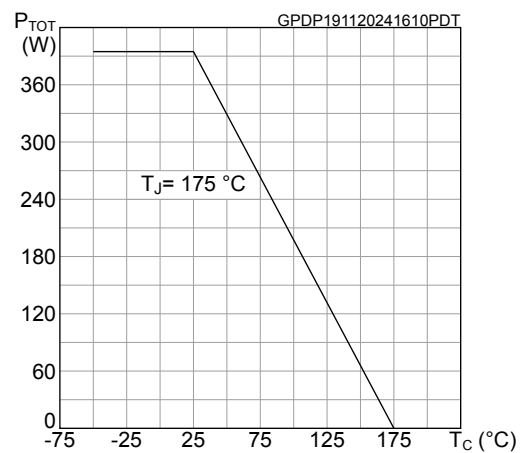


Figure 7. Maximum continuous drain current vs case temperature

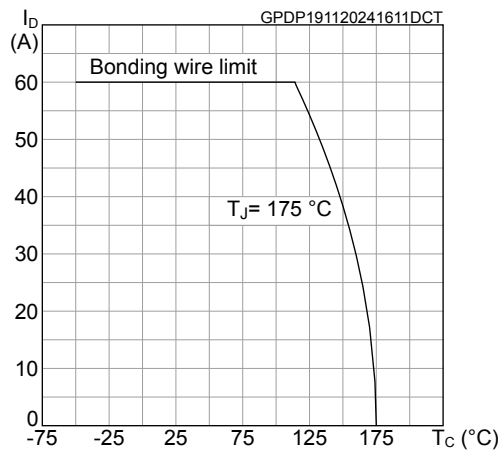


Figure 8. Normalized breakdown voltage vs temperature

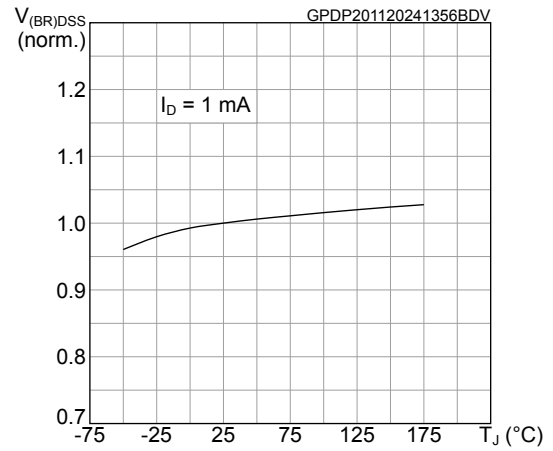


Figure 9. Normalized gate threshold vs temperature

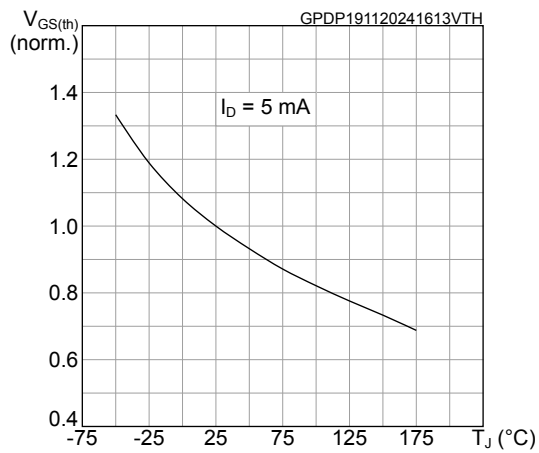


Figure 10. Normalized on-resistance vs temperature

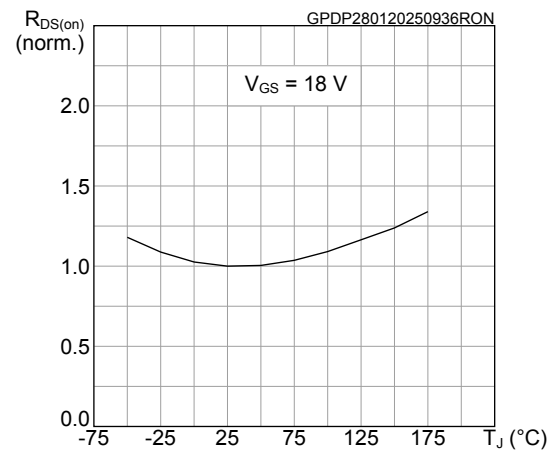


Figure 11. Typical capacitance characteristics

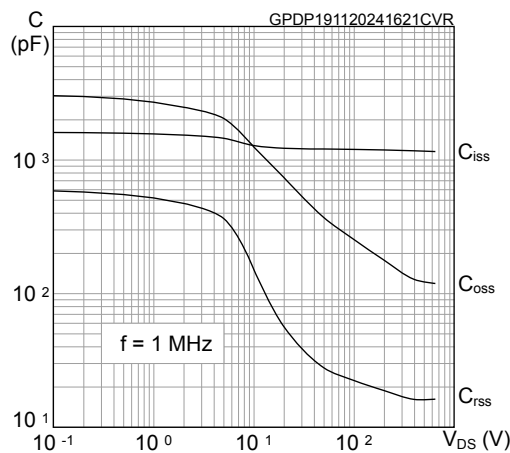


Figure 12. Typical gate charge characteristics

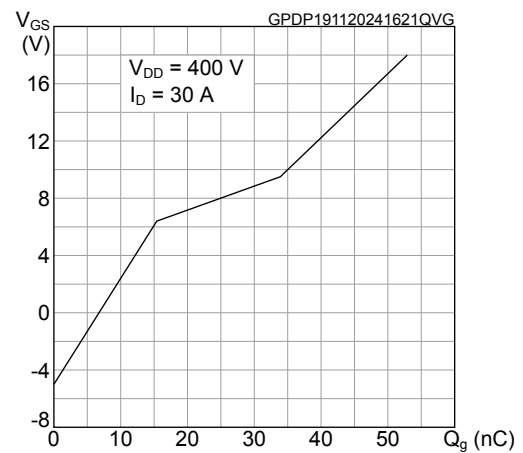


Figure 13. Typical reverse conduction characteristics ($T_J = 25\text{ }^\circ\text{C}$)

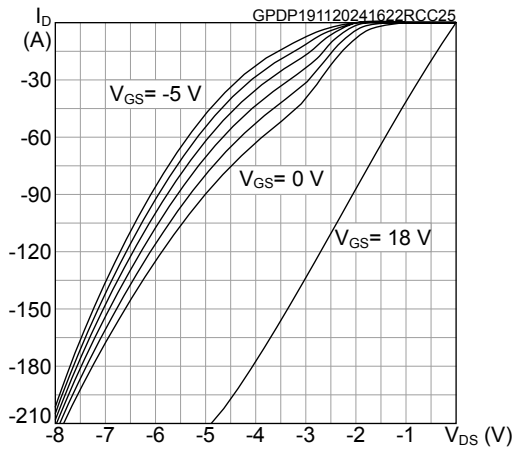


Figure 14. Typical reverse conduction characteristics ($T_J = 175\text{ }^\circ\text{C}$)

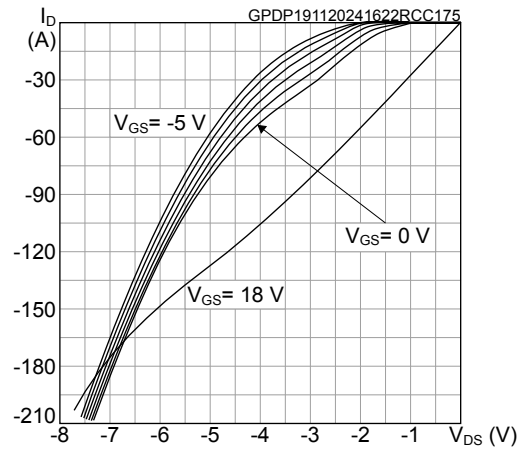


Figure 15. Typical switching energy vs drain current

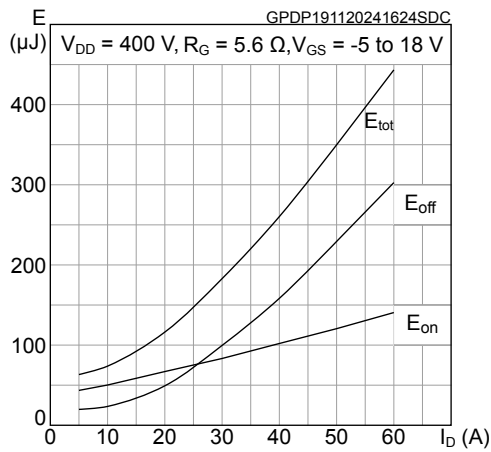


Figure 16. Typical switching energy vs supply voltage

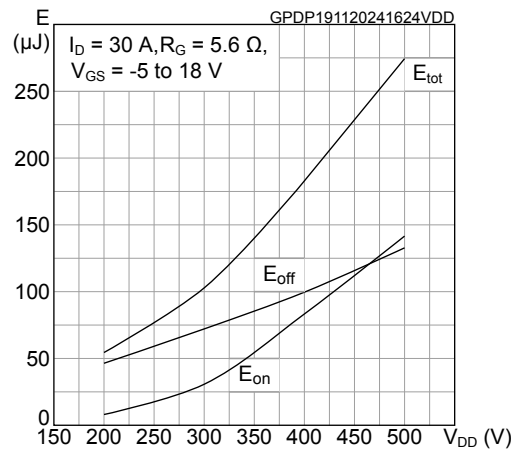
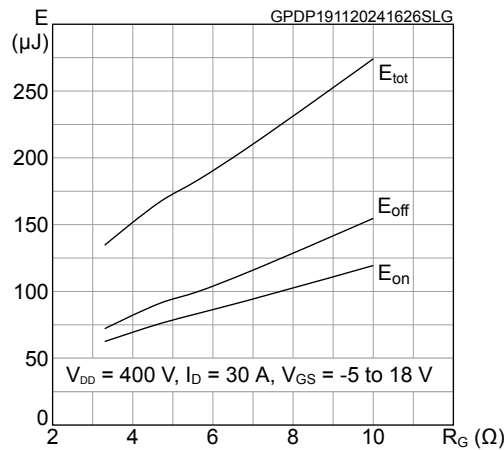


Figure 17. Typical switching energy vs gate resistance

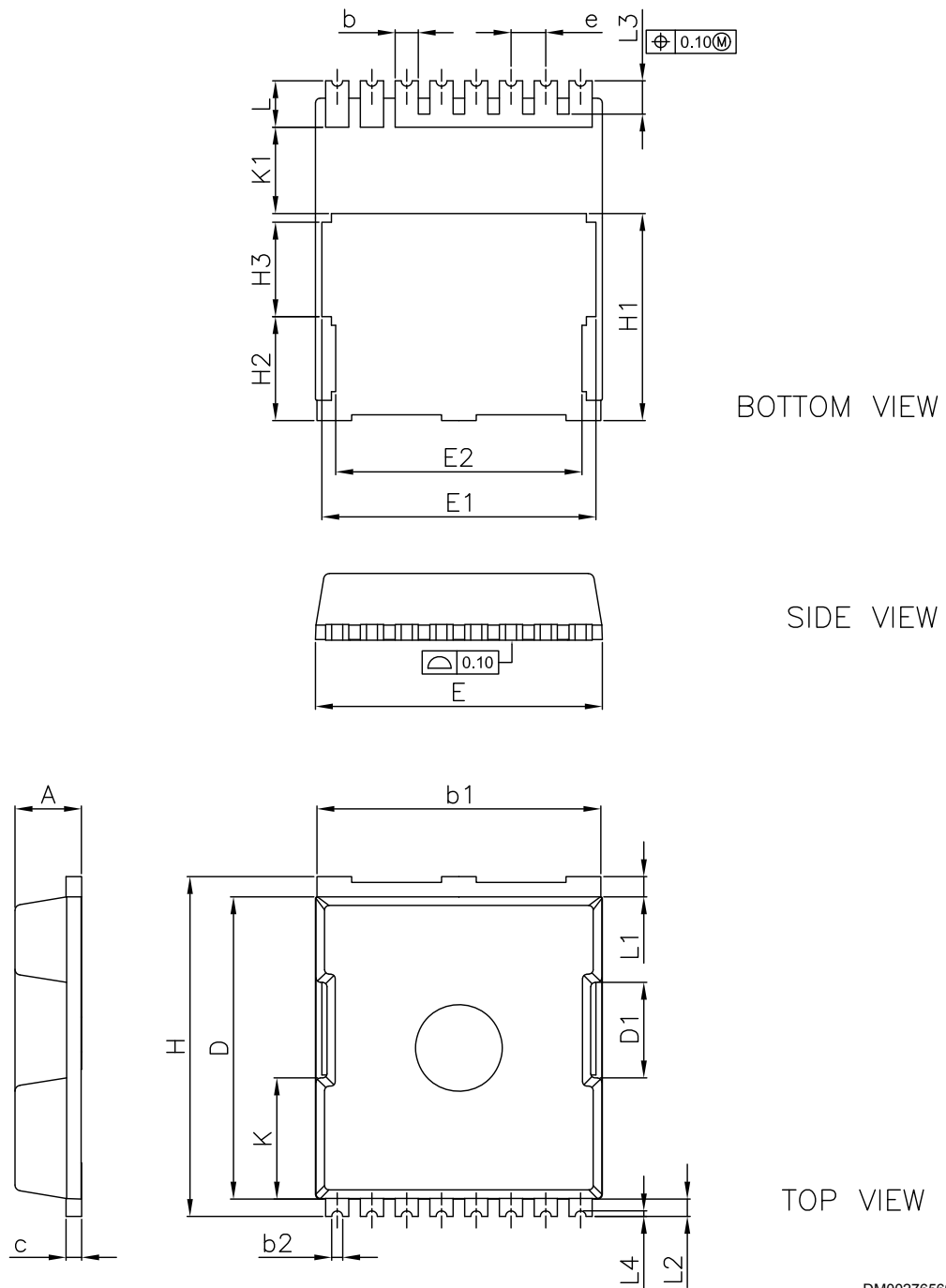


3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 TO-LL package information

Figure 18. TO-LL package outline

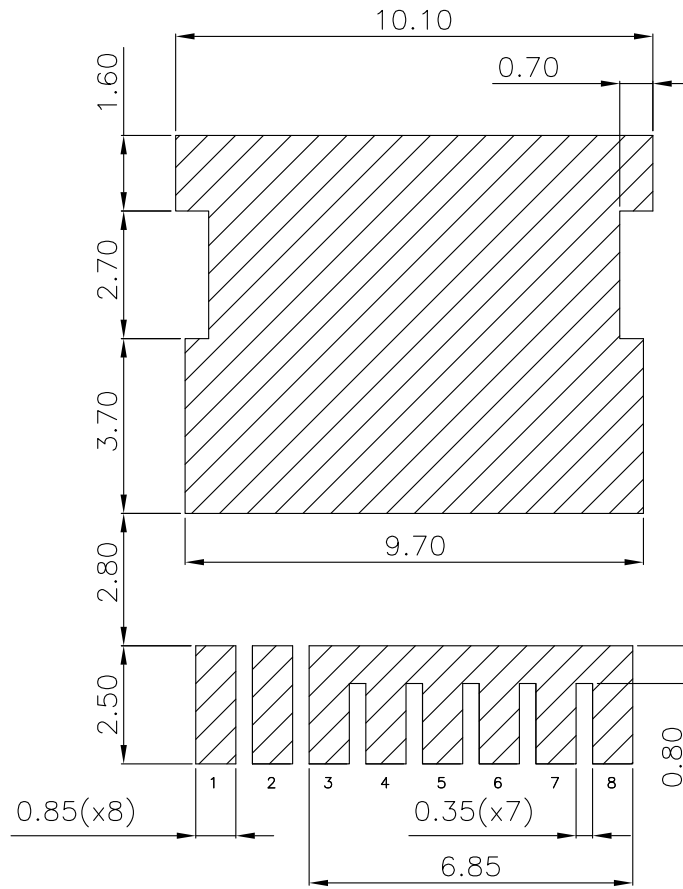


DM00276569_SiC_Rev_7

Table 8. TO-LL package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.60	0.80	0.90
b1	9.70	9.80	9.90
b2	0.20		0.50
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	9.31	9.46	9.61
E2	8.35	8.50	8.65
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	7.00	7.15	7.30
H2	3.34	3.59	3.84
H3	3.11	3.26	3.41
K	4.03	4.18	4.33
K1	2.70		
L	1.45	1.60	1.75
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
L4	0.05		0.40

Figure 19. TO-LL recommended footprint (dimensions are in mm)



DM00276569_7_SIC_FP

3.2 TO-LL packing information

Figure 20. Carrier tape outline and dimensions

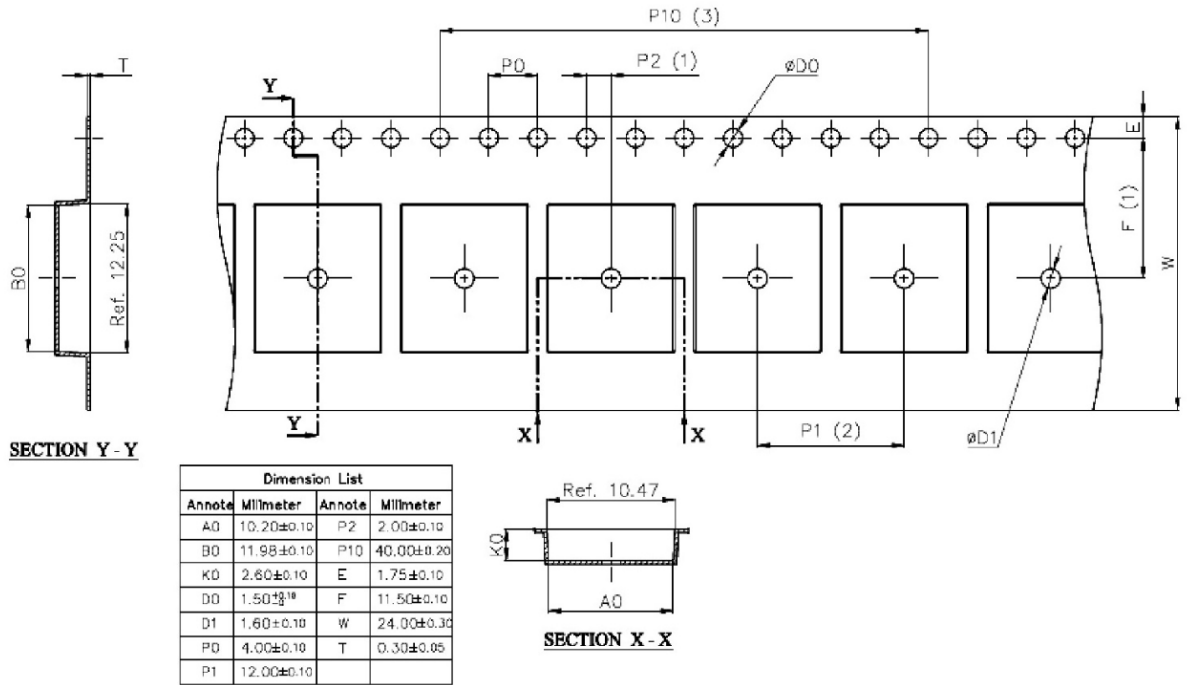


Figure 21. Reel outline and dimensions

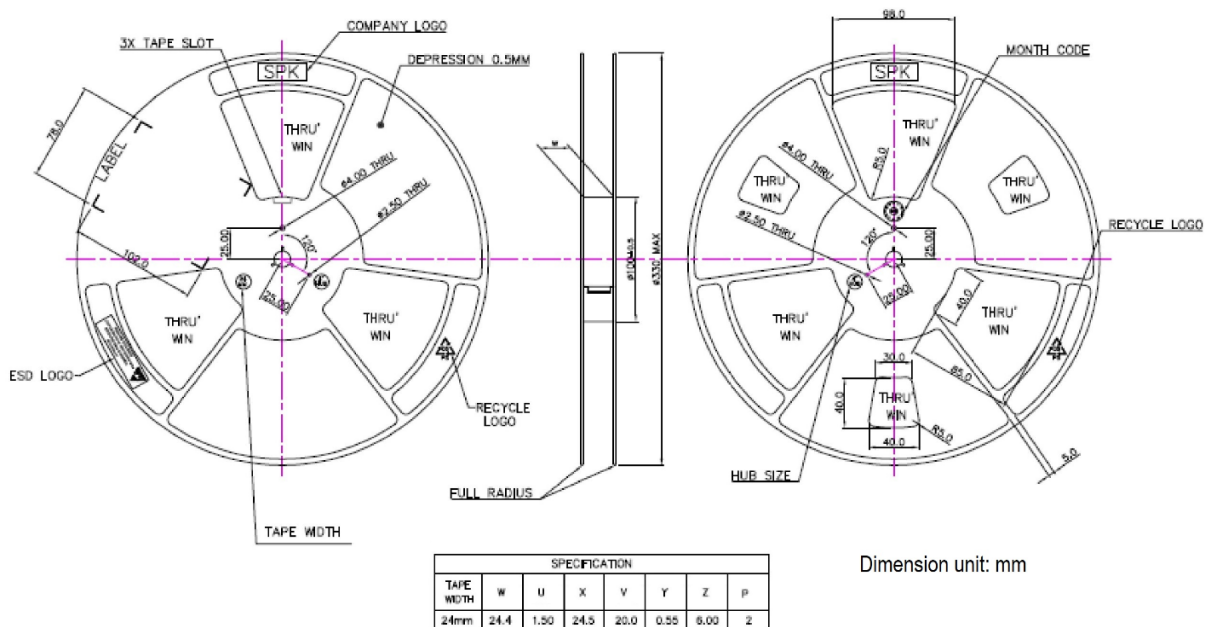
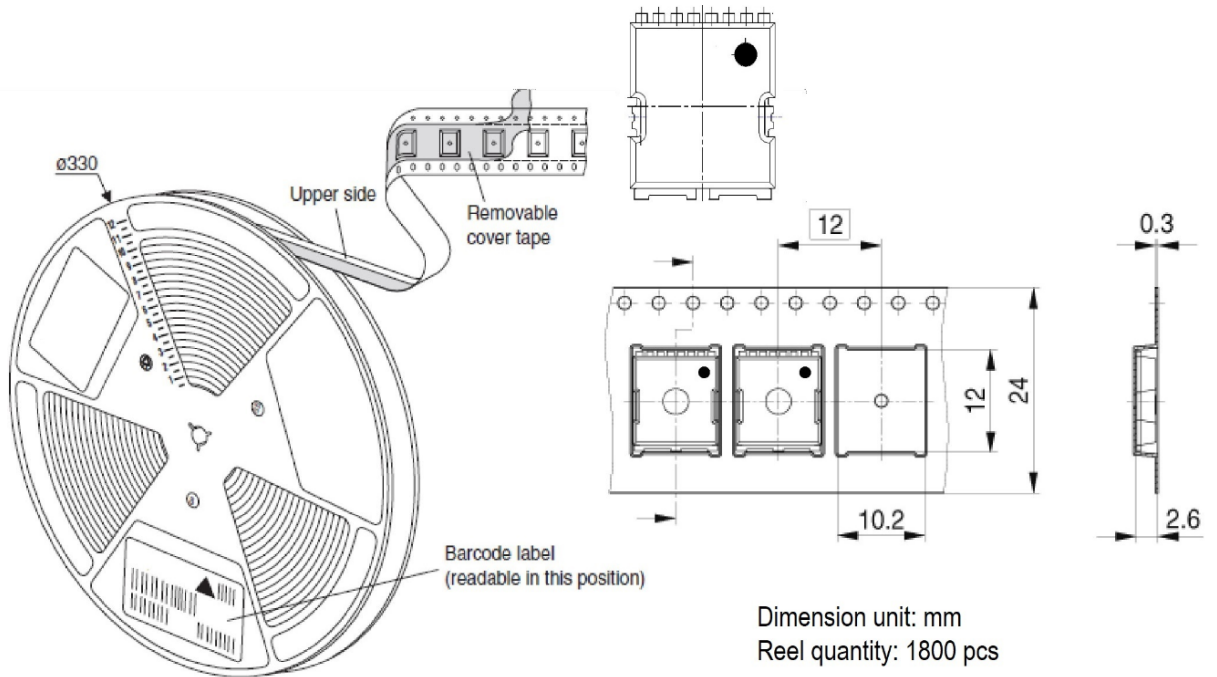


Figure 22. TO-LL orientation in tape pocket



Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Nov-2024	1	First release.
28-Jan-2025	2	Updated Figure 10 . Normalized on-resistance vs temperature. Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Package information	8
3.1	TO-LL package information	8
3.2	TO-LL packing information	11
	Revision history	13

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