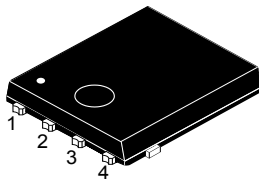
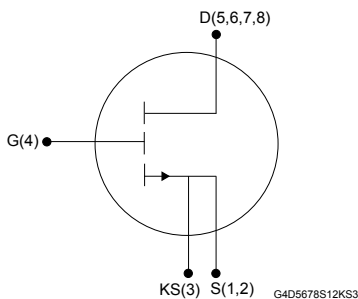


650 V, 75 mΩ typ., 15 A, e-mode PowerGaN transistor


 PowerFLAT 5x6 HV
for PowerGaN


Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT120R65AL	650 V	120 mΩ	15 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Kelvin source pad for optimum gate driving
- Zero reverse recovery charge

Applications

- Adapters for tablets, notebook and AIO
- USB type-C PD adapters and quick chargers
- Wireless chargers

Description

The SGT120R65AL is a 650 V, 15 A e-mode PowerGaN transistor combined with a well established packaging technology. The resulting G-HEMT device provides extremely low conduction losses, high current capability and ultra fast switching operation to enable high power density and unbeatable efficiency performances.



Product status link

[SGT120R65AL](#)

Product summary

Order code	SGT120R65AL
Marking	120R65A
Package	PowerFLAT 5x6 HV for PowerGaN
Packing	Tape and reel

1 Electrical ratings

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
	Drain-source voltage (transient, $t_p < 1\ \mu s$)	750	
V_{GS}	Gate-source voltage	-10 to 7	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	15	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	9	
I_{DM}	Pulse drain current ($t_p = 100\ \mu s$)	36	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	192	W
	Total power dissipation at $T_B = 25\text{ °C}$	6.25	
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.65	°C/W
$R_{thJB}^{(1)(2)}$	Thermal resistance, junction-to-board	20	°C/W

1. Specified by design, not tested in production.
2. Device mounted on 1.6 mm thick, FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm each. The PCB is mounted in horizontal position without air stream cooling.

Prerelease product(s)

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 25\text{ }\mu\text{A}$	650			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$		0.2		μA
		$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_J = 150\text{ }^\circ\text{C}$		20		
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 6\text{ V}$		50		μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 0.1\text{ V}, I_D = 12\text{ mA}$	1.2	1.8	2.6	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 6\text{ V}, I_D = 5\text{ A}$		75	120	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 5\text{ A}, T_J = 150\text{ }^\circ\text{C}$		185		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}, f = 1\text{ MHz}$	-	125	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{riss}	Reverse transfer capacitance		-	0.9	-	pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }400\text{ V}$	-	64	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related		-	83	-	pF
R_G	Intrinsic gate resistance	$f = 5\text{ MHz}, I_D = 0\text{ A}$	-	1.3	-	Ω
V_{plat}	Gate plateau voltage	$V_{DS} = 400\text{ V}, I_D = 10\text{ A}$	-	2.9	-	V
Q_g	Total gate charge	$V_{GS} = 0\text{ to }6\text{ V}, V_{DS} = 400\text{ V}, I_D = 10\text{ A}$ (see Figure 19. Test circuit for gate charge behavior)	-	3.00	-	nC
Q_{gs}	Gate-source charge		-	0.65	-	nC
Q_{gd}	Gate-drain charge		-	1.21	-	nC
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$	-	0	-	nC
Q_{oss}	Output charge		-	40	-	nC

- $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.
- $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 400\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }6\text{ V}$,	-	4.1	-	ns
t_f	Fall time	$R_{G(on)} = 10\ \Omega$, $R_{G(off)} = 3.3\ \Omega$, $L = 500\ \mu\text{H}$	-	9.7	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 20. test circuit for inductive load switching times and Figure 21. Switching time waveforms)	-	8.9	-	ns
t_r	Rise time		-	6.0	-	ns
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 400\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }6\text{ V}$,	-	4.6	-	ns
t_f	Fall time	$R_{G(on)} = 10\ \Omega$, $R_{G(off)} = 3.3\ \Omega$, $L = 500\ \mu\text{H}$,	-	10.4	-	ns
$t_{d(off)}$	Turn-off delay time	$T_C = 150\text{ }^\circ\text{C}$	-	8.4	-	ns
t_r	Rise time	(see Figure 20. test circuit for inductive load switching times and Figure 21. Switching time waveforms)	-	9.3	-	ns
E_{on}	Turn-on switching energy	$V_{DS} = 400\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }6\text{ V}$,	-	16.1	-	μJ
E_{off}	Turn-off switching energy	$R_{G(on)} = 10\ \Omega$, $R_{G(off)} = 3.3\ \Omega$, $L = 500\ \mu\text{H}$	-	6.6	-	μJ

Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 5\text{ A}$	-	2.5	-	V

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area ($T_C = 25\text{ }^\circ\text{C}$)

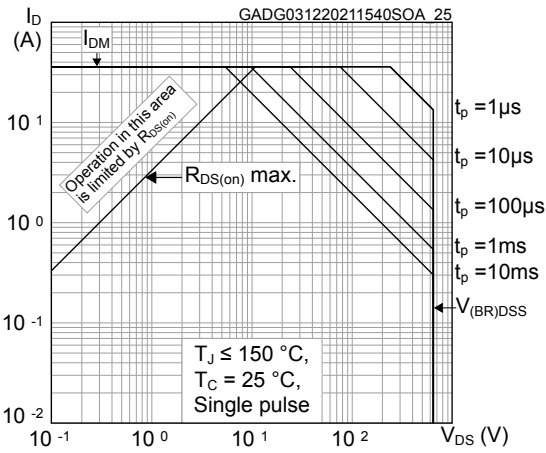


Figure 2. Safe operating area ($T_C = 125\text{ }^\circ\text{C}$)

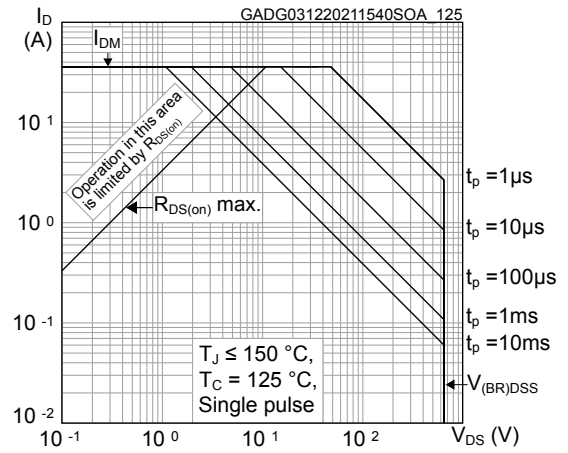


Figure 3. Maximum transient thermal impedance

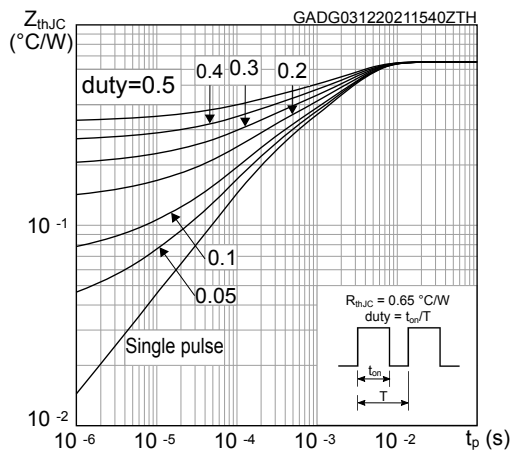


Figure 4. Total power dissipation

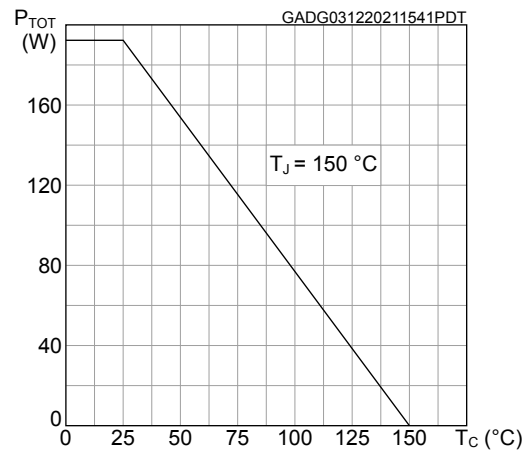


Figure 5. Typical output characteristics ($T_C = 25\text{ }^\circ\text{C}$)

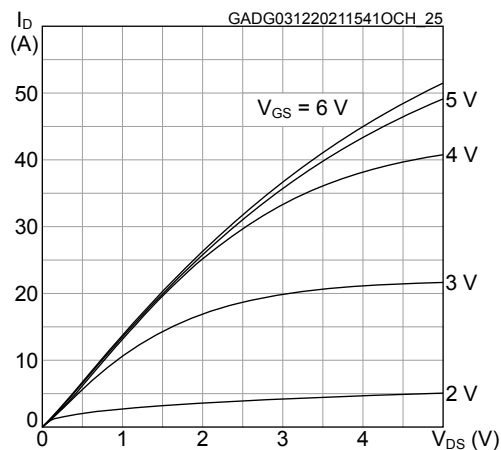
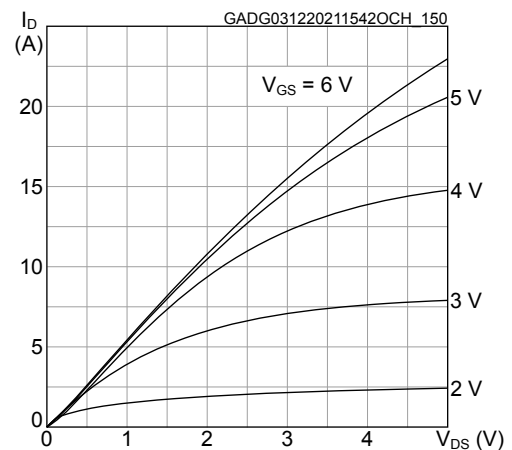


Figure 6. Typical output characteristics ($T_C = 150\text{ }^\circ\text{C}$)



Prerelease product(s)

Figure 7. Typical transfer characteristics

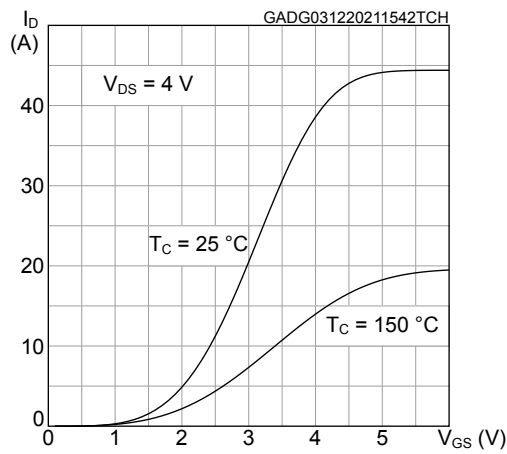


Figure 8. Typical gate charge characteristics

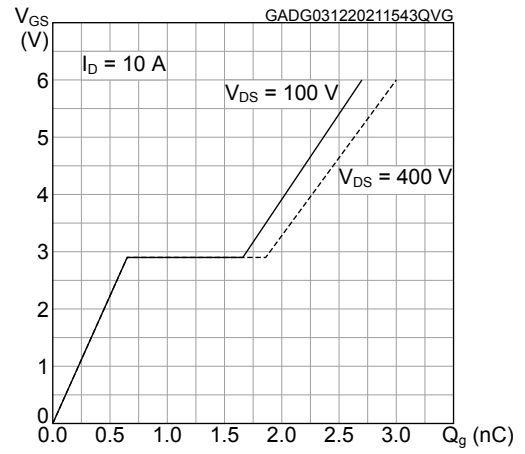


Figure 9. Typical capacitance characteristics

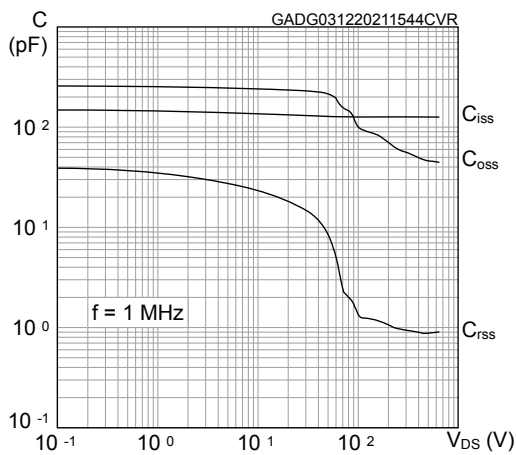


Figure 10. Typical output charge

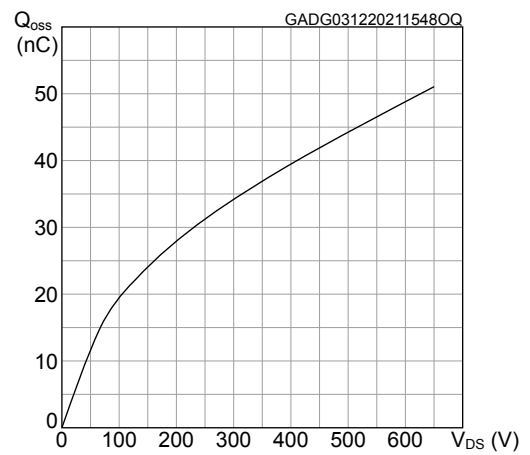


Figure 11. Typical output capacitance stored energy

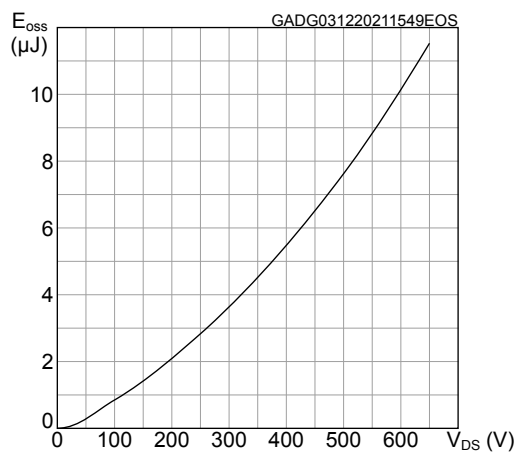
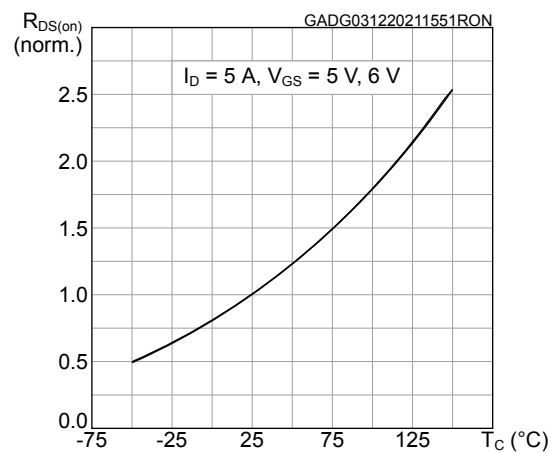


Figure 12. Normalized on-resistance vs temperature



Prerelease product(s)

Figure 13. Typical drain-source on-resistance ($T_C = 25\text{ }^\circ\text{C}$)

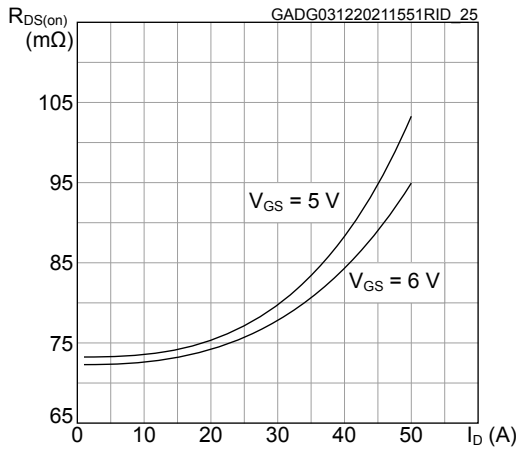


Figure 14. Typical drain-source on-resistance ($T_C = 150\text{ }^\circ\text{C}$)

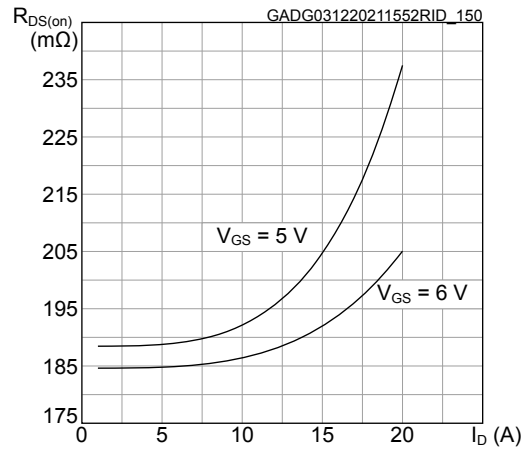


Figure 15. Typical reverse conduction characteristics ($T_C = 25\text{ }^\circ\text{C}$)

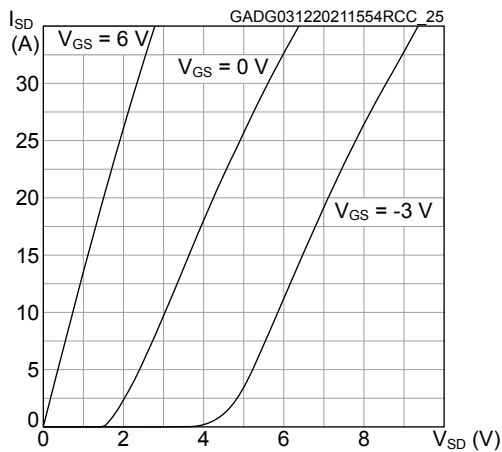


Figure 16. Typical reverse conduction characteristics ($T_C = 150\text{ }^\circ\text{C}$)

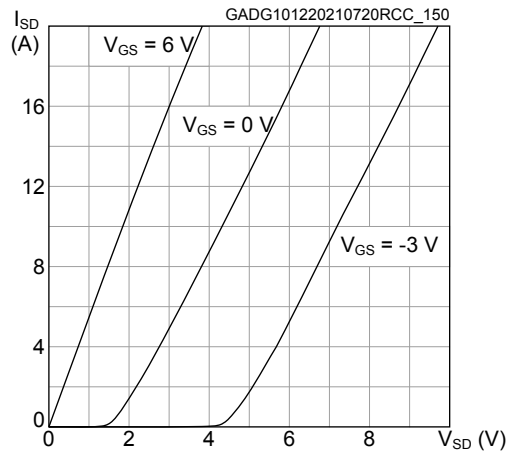
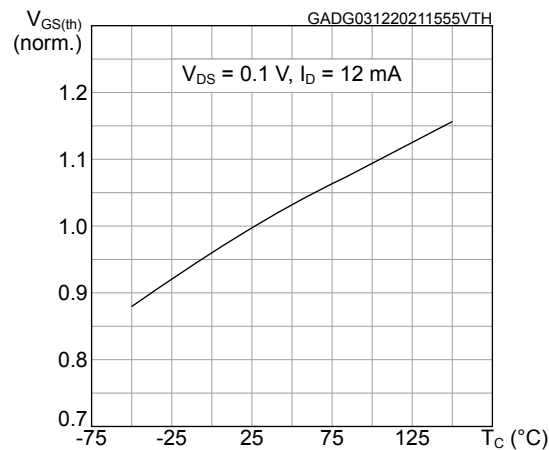


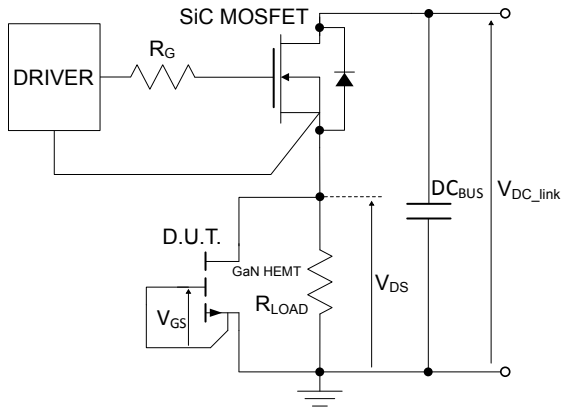
Figure 17. Normalized gate threshold vs temperature



Prerelease product(s)

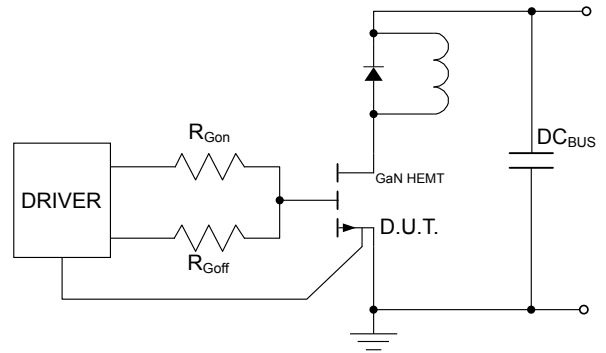
3 Test circuits

Figure 18. Test circuit for transient drain-source voltage



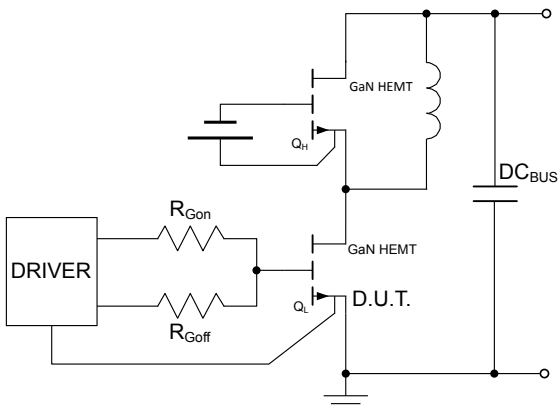
GADG031220211521GT

Figure 19. Test circuit for gate charge behavior



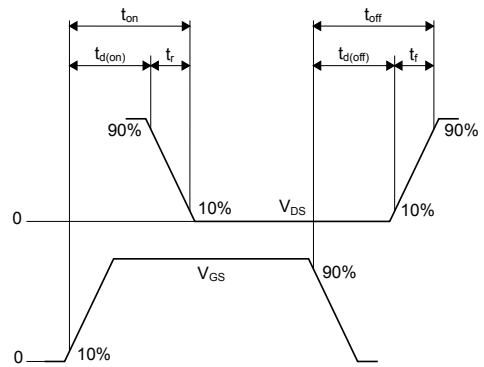
GADG270820210906SA

Figure 20. test circuit for inductive load switching times



GADG270820210909SA

Figure 21. Switching time waveforms



AM01473v1

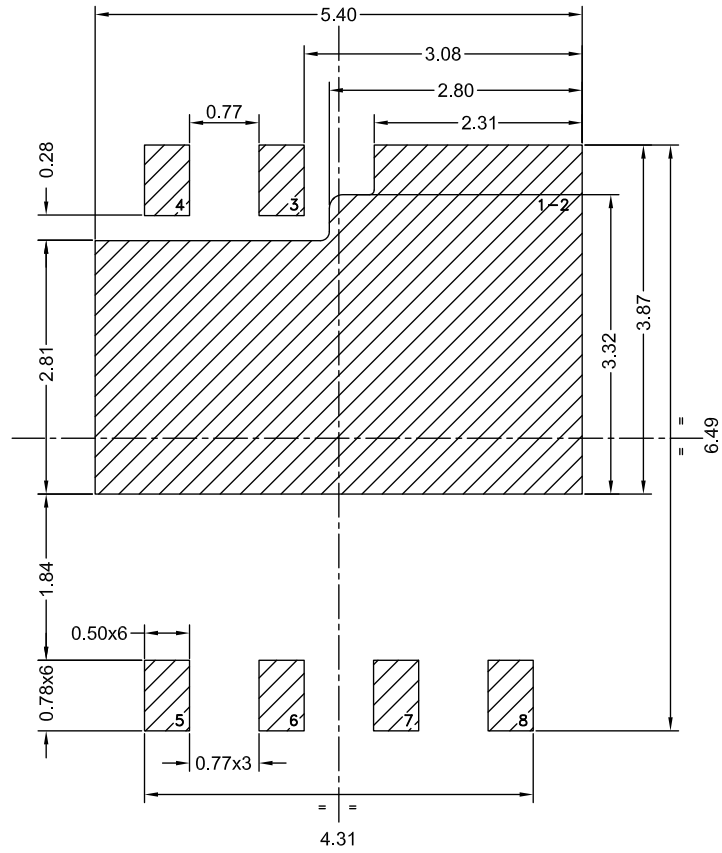
Prerelease product(s)

Table 7. PowerFLAT 5x6 HV for PowerGaN mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.95	1.00
A1			0.05
A2	0.20	0.25	0.30
b	0.30		0.50
C	5.65	5.85	6.05
D	5.10	5.20	5.30
D1	0.15	0.30	0.45
D2	4.30	4.40	4.50
D3	0.25	0.40	0.55
D4	4.80	5.00	5.20
D5	2.23	2.33	2.43
E	6.20	6.40	6.60
E1	3.62	3.72	3.82
E2	2.45	2.55	2.65
E4	0.40	0.50	0.60
E7	0.40	0.50	0.60
E8	0.39	0.49	0.59
E9	0.47	0.55	0.63
e		1.27	
L	0.58	0.68	0.78
K	1.90	2.00	2.10
aaa		0.15	
bbb		0.15	
ccc		0.10	
eee		0.10	

Prerelease product(s)

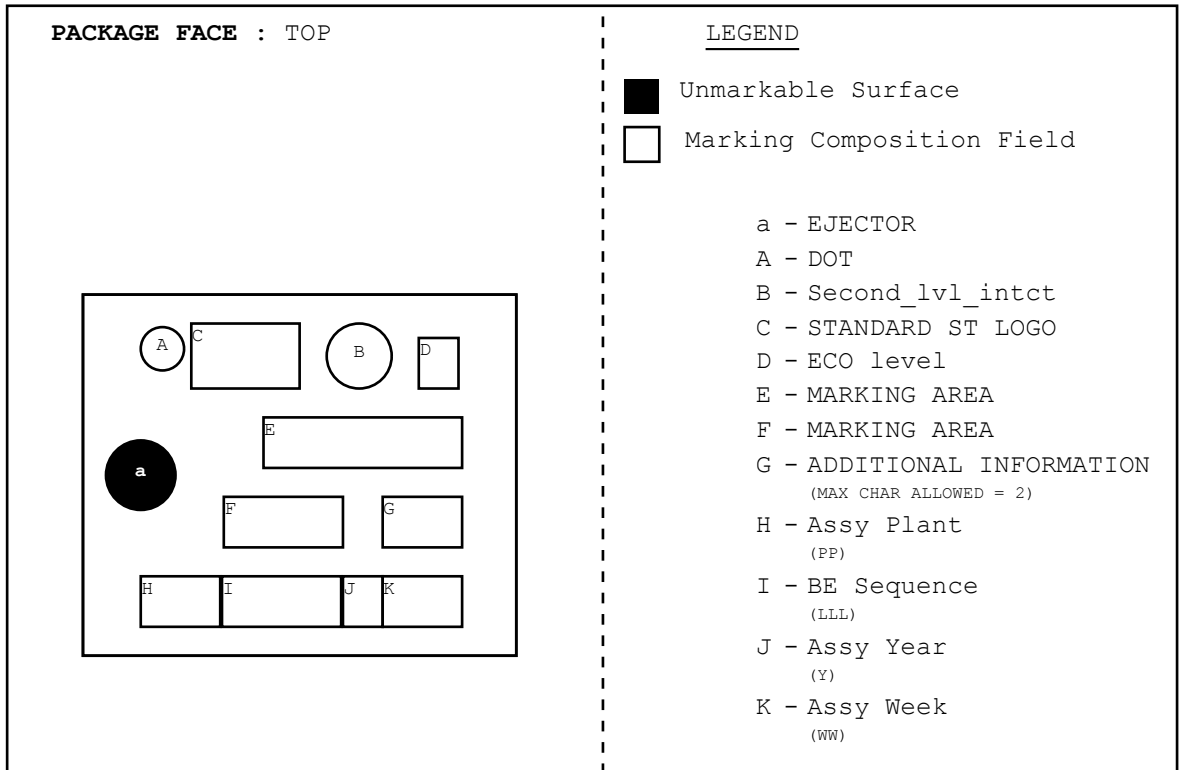
Figure 23. PowerFLAT 5x6 HV for PowerGaN recommended footprint (dimensions are in mm)



DM00649592_Rev_5_footprint_for_GaN

Prerelease product(s)

Figure 24. Marking composition for PowerFLAT 5x6 HV for PowerGaN



GADG230220210901SA

Engineering samples

These samples are clearly identified by “ES” digits in the marking additional information field of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

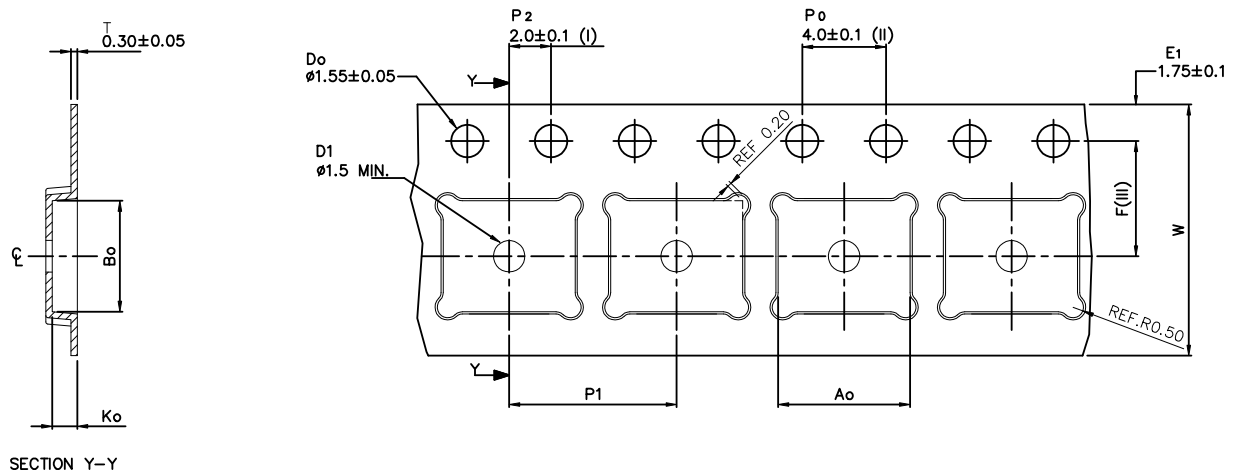
Commercial samples

Fully qualified parts from ST standard production with no limitations of use or special identification marking.

Prerelease product(s)

4.2 PowerFLAT 5x6 packing information

Figure 25. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30	+/-	0.1
Bo	5.30	+/-	0.1
Ko	1.20	+/-	0.1
F	5.50	+/-	0.1
P1	8.00	+/-	0.1
W	12.00	+/-	0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 26. PowerFLAT 5x6 package orientation in carrier tape

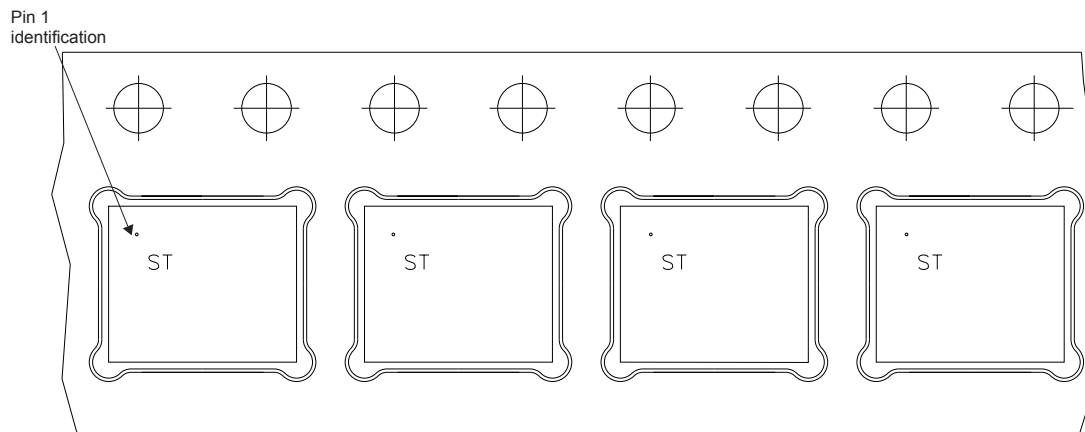
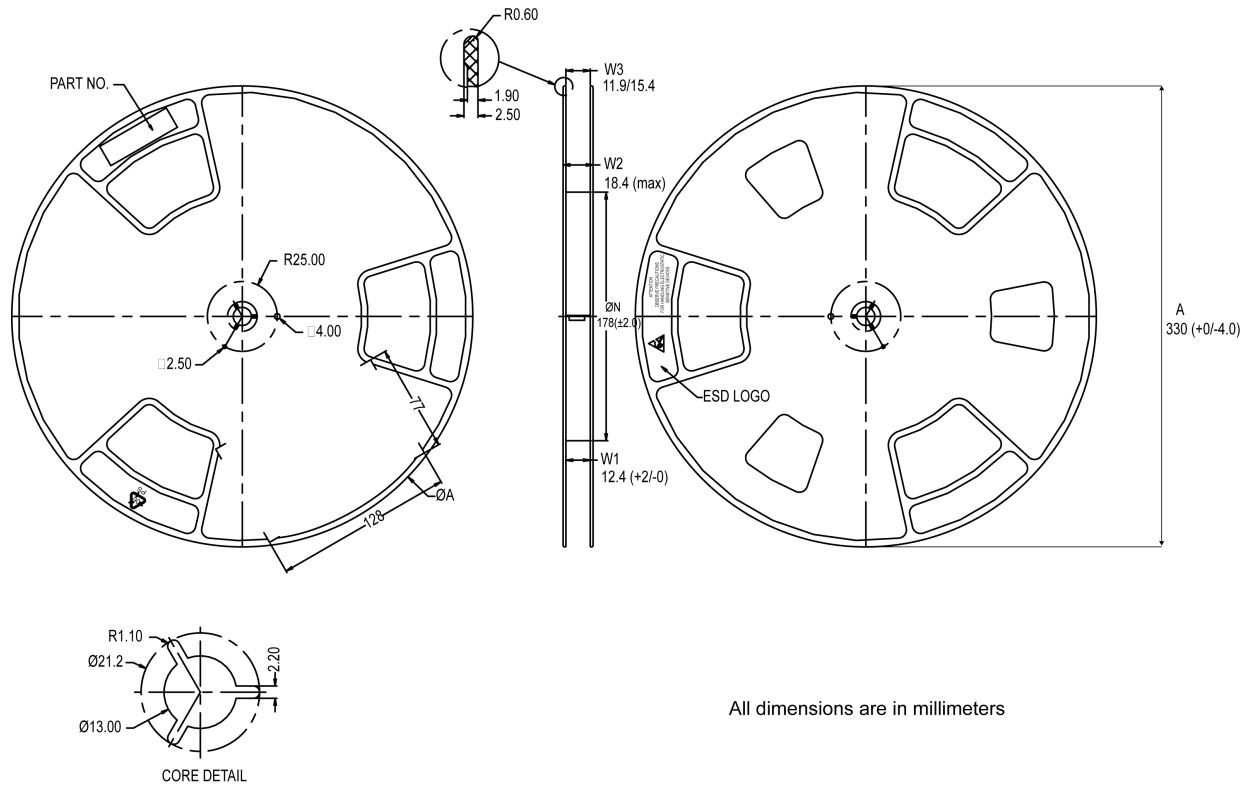


Figure 27. PowerFLAT 5x6 reel



All dimensions are in millimeters

8234350_Reel_rev_C

Prerelease product(s)

Revision history

Table 8. Document revision history

Date	Version	Changes
29-Apr-2020	1	First release.
08-Jul-2020	2	Updated <i>Section 3.1 PowerFLAT 5x6 HV for GaN package information</i> . Minor text changes.
18-Jan-2021	3	Updated <i>Table 3. Static</i> . Minor text changes.
06-Apr-2021	4	Added <i>Figure 3. Marking composition for PowerFLAT 5x6 HV</i> .
25-May-2021	5	Updated <i>Product status / summary in cover page</i> .
05-Oct-2021	6	Updated title, description, cover image and schematic in cover page. Updated <i>Table 1. Absolute maximum ratings</i> and <i>Table 2. Thermal data</i> . Updated <i>Table 3. Static</i> . Added <i>Table 4. Switching times</i> and <i>Table 5. Reverse conduction</i> . Added <i>Section 3 Test circuits</i> . Updated <i>Section 4 Package information</i> . Minor text changes.
10-Dec-2021	7	Updated <i>title</i> and <i>Features</i> on cover page. Updated <i>Section 1 Electrical ratings</i> . Updated <i>Section 2 Electrical characteristics</i> . Added <i>Section 2.1 Electrical characteristics (curves)</i> . Added <i>Figure 18. Test circuit for transient drain-source voltage</i> . Minor text changes.
07-Feb-2022	8	Modified <i>Applications</i> . Modified <i>Table 4. Dynamic</i> . Modified <i>Figure 8. Typical gate charge characteristics</i> . Minor text changes.

Prerelease product(s)

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3	Test circuits	8
4	Package information	9
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	Revision history	15

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