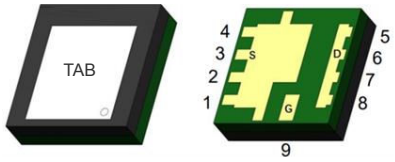
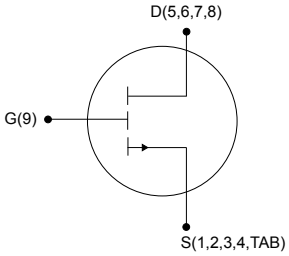
SGT3D5R10MEB

Datasheet

100 V, 2.7 mΩ typ., 201 A, e-mode PowerGaN transistor



En-FCLGA 3.3x3.3



Product status link
SGT3D5R10MEB

Product summary	
Order code	SGT3D5R10MEB
Marking	3D5R10M
Package	En-FCLGA 3.3x3.3
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT3D5R10MEB	100 V	3.5 mΩ	201 A	G-HEMT

- Dual side cooling package
- Enhancement mode normally off transistor
- Extremely low capacitances
- High power management capability
- Very high switching speed
- Zero reverse recovery charge

Applications

- DC-DC converters
- Motor driver
- Solar system MPPT

Description

The SGT3D5R10MEB is a 100 V, 201 A e-mode PowerGaN transistor. The resulting device provides extremely low conduction losses, high current capability and ultra-fast switching operation to enable high power density and unbeatable efficiency performances.

1 Electrical ratings

T_C = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
	Drain-source voltage (transient)	120	
V_{GS}	Gate-source voltage	-4 to 6	V
I_D	Drain current (continuous) at T_C = 25 °C	201	A
	Drain current (continuous) at T_C = 100 °C	127	
I_{DM}	Pulse drain current (t_p = 100 µs) at T_C = 25 °C	415	A
P_{TOT}	Total power dissipation at T_C = 25 °C	255	W
T_{stg}	Storage temperature range	-40 to 150	°C
T_J	Operating junction temperature range		°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.49	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	47.13(1)	°C/W

1. *R_{thJA} is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	V_{GS} = 0 V, V_{DS} = 100 V	-	1	100	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_J = 125 °C	-	100	-	
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = 6 V	-	0.5	100	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 7.6 mA	0.8	1.1	2.1	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 5 V, I_D = 25 A	-	2.7	3.5	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 100 kHz	-	868	-	pF
C_{oss}	Output capacitance		-	426	-	pF
C_{rss}	Reverse transfer capacitance		-	7	-	pF
$C_{o(er)}$[(1)]	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 50 V, f = 100 kHz	-	646	-	pF
$C_{o(tr)}$[(2)]	Equivalent output capacitance time related		-	821	-	pF
R_g	Intrinsic gate resistance	f = 5 MHz, I_D = 0 A	-	1.5	-	Ω
Q_g	Total gate charge	V_{GS} = 0 to 5 V, V_{DS} = 50 V, I_D = 25 A	-	6.3	-	nC
Q_{gs}	Gate-source charge		-	1.2	-	nC
Q_{gd}	Gate-drain charge		-	1.9	-	nC
$Q_{gs(th)}$	Gate charge at treshold		-	0.84	-	nC
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V, V_{DS} = 50 V	-	0	-	nC
Q_{oss}	Output charge		-	45	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DS} = 50 V, I_D = 25 A, V_{GS} = 0 to 5 V, $R_{G(on)}$ = 3 Ω, $R_{G(off)}$ = 2 Ω, L = 5.7 µH	-	2.56	-	ns
t_r	Rise time		-	6.08	-	ns
$t_{d(off)}$	Turn-off delay time		-	5.12	-	ns
t_f	Fall time		-	3.84	-	ns

Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	V_{GS} = 0 V, I_{SD} = 25 A	-	1.9	-	V

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area (T_C = 25 °C)

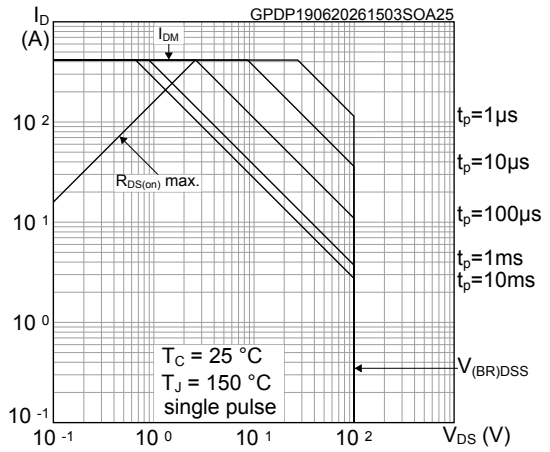


Figure 2. Safe operating area (T_C = 125 °C)

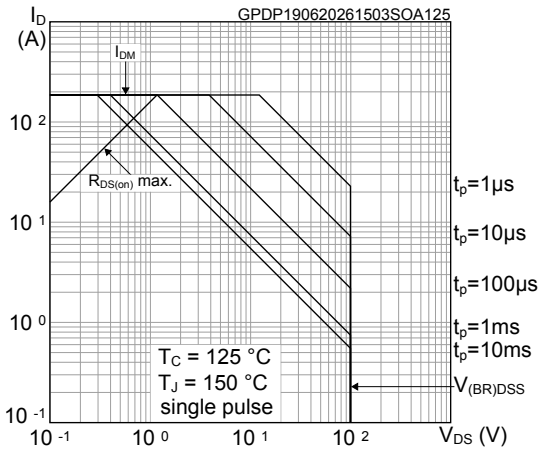


Figure 3. Maximum transient thermal impedance

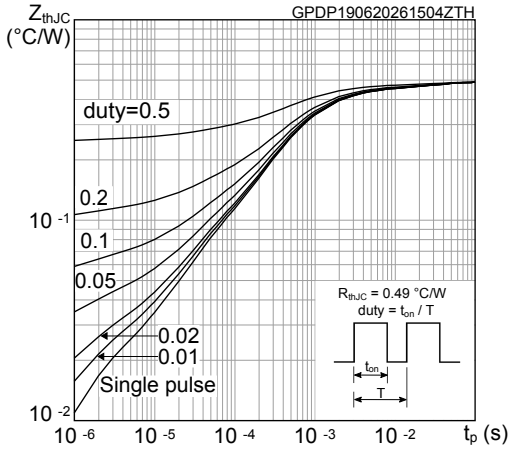


Figure 4. Total power dissipation

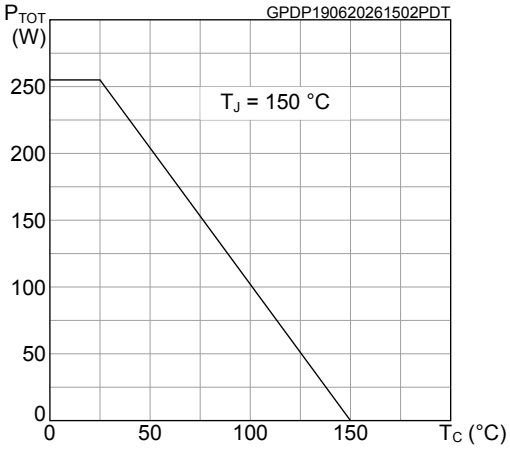


Figure 5. Typical output characteristics (T_J = 25 °C)

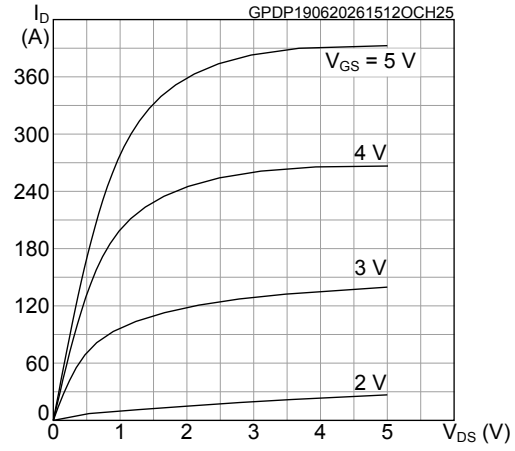


Figure 6. Typical output characteristics (T_J = 125 °C)

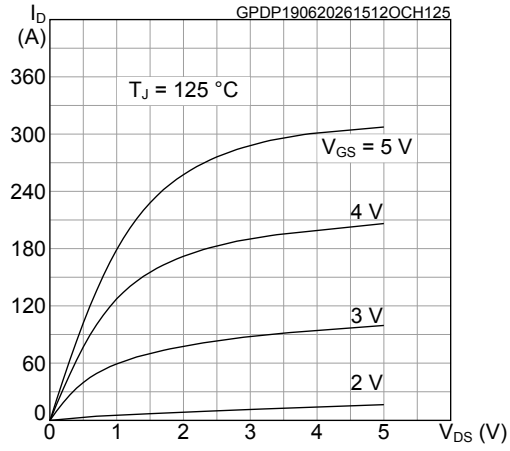


Figure 7. Typical transfer characteristics

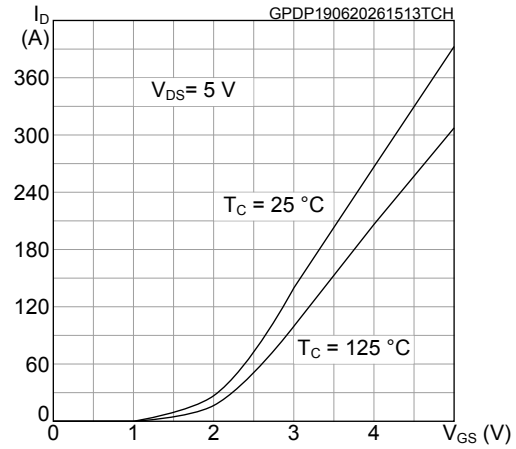


Figure 8. Normalized on-resistance vs temperature

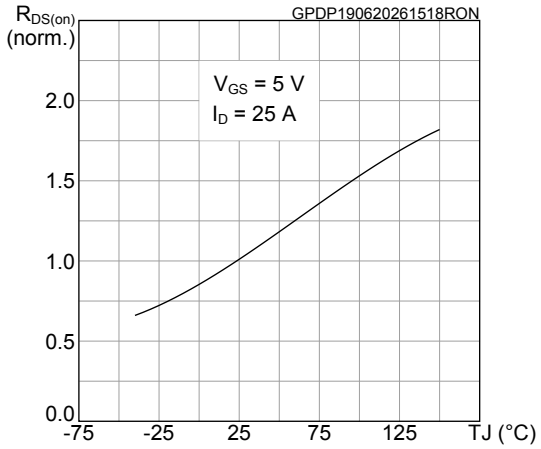


Figure 9. Typical drain-source on-resistance (T_J = 25 °C)

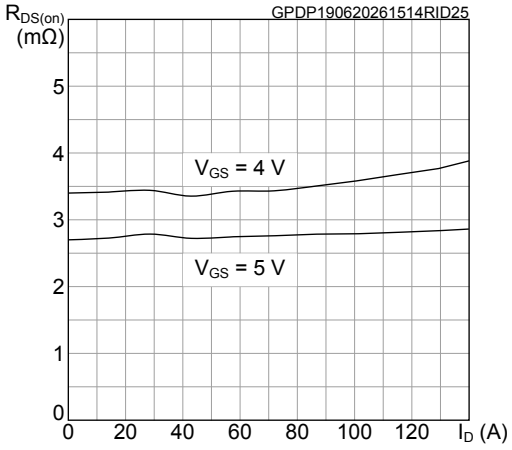


Figure 10. Typical drain-source on-resistance (T_J = 125 °C)

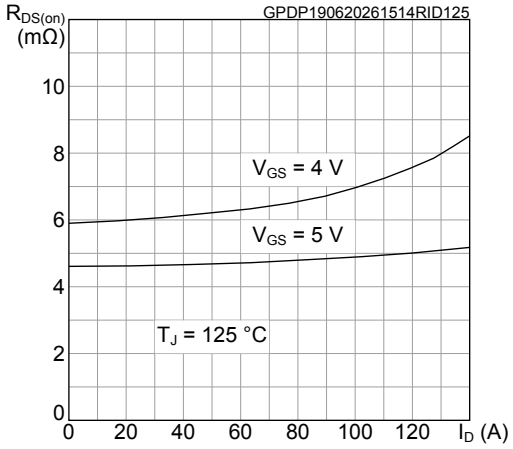


Figure 11. Typical gate charge characteristics

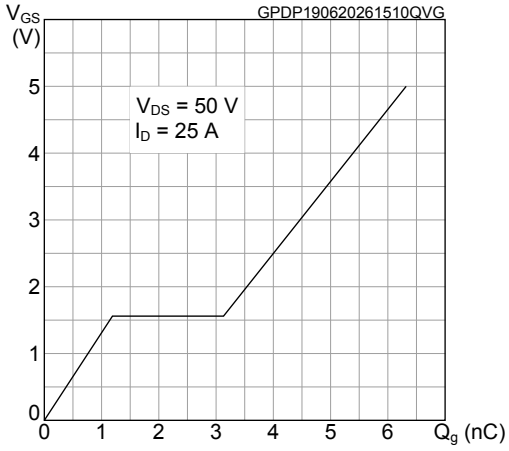


Figure 12. Typical capacitance characteristics

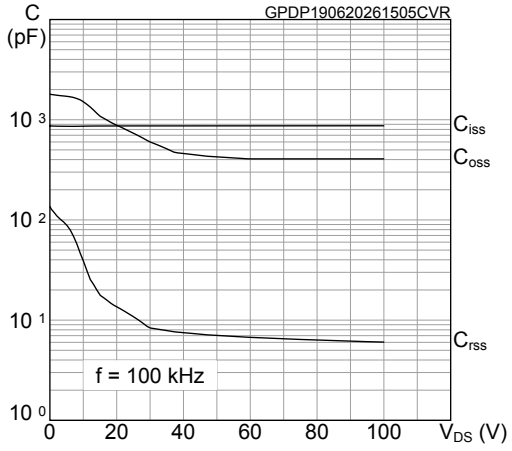


Figure 13. Typical output capacitance charge

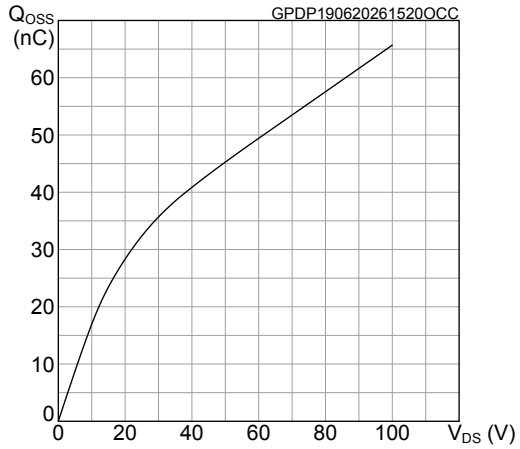


Figure 14. Typical output capacitance stored energy

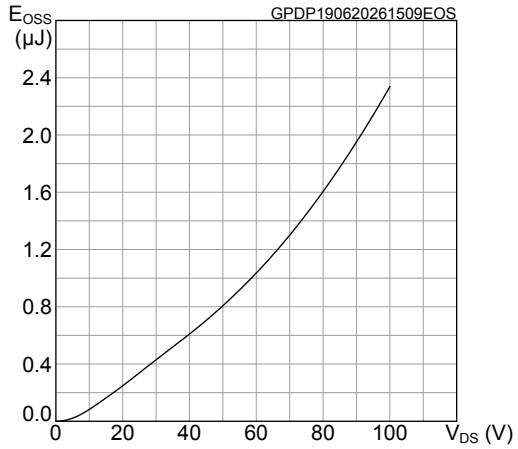


Figure 15. Typical reverse conduction characteristics (T_J = 25 °C)

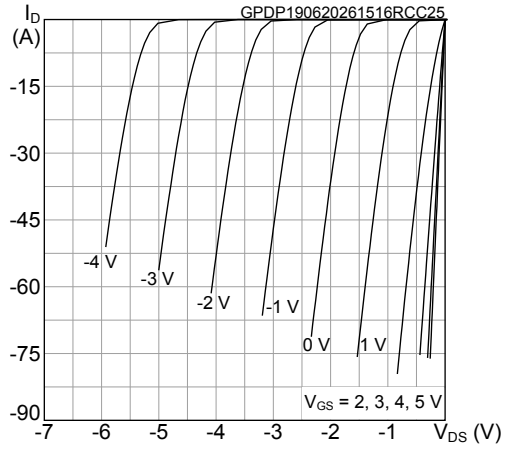


Figure 16. Typical reverse conduction characteristics (T_J = 125 °C)

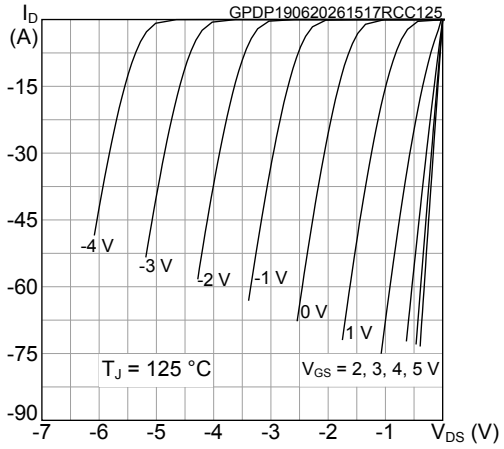
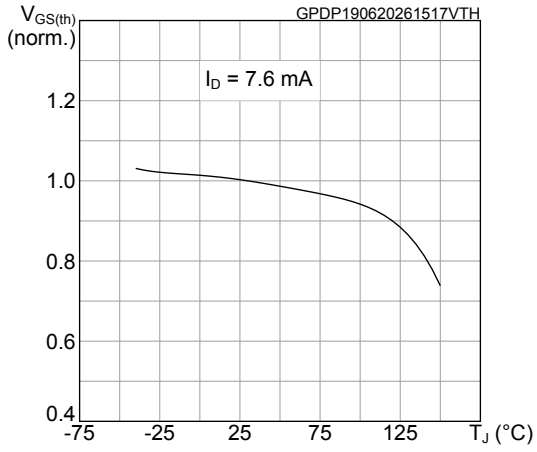


Figure 17. Normalized gate threshold vs temperature



3 Test circuits

Figure 18. Test circuit for inductive load switching times

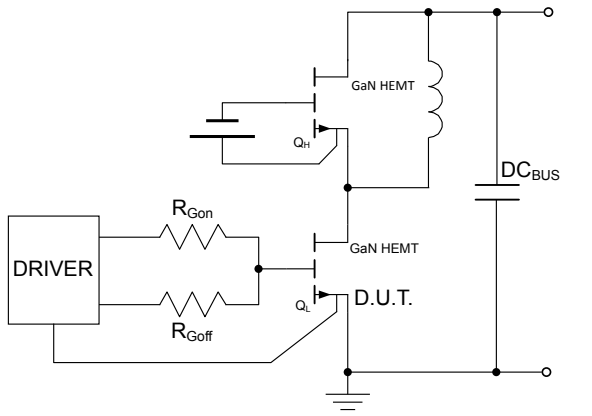


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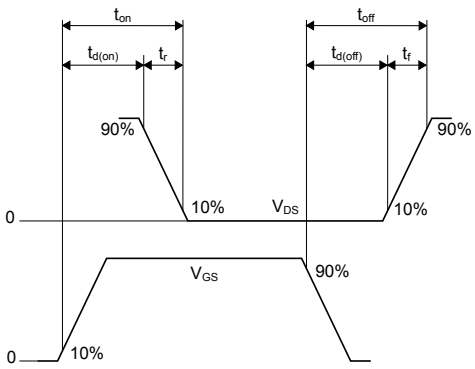
Figure 19. Switching time waveforms



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 En-FCLGA 3.3x3.3 package information

Figure 20. En-FCLGA 3.3x3.3 package outline

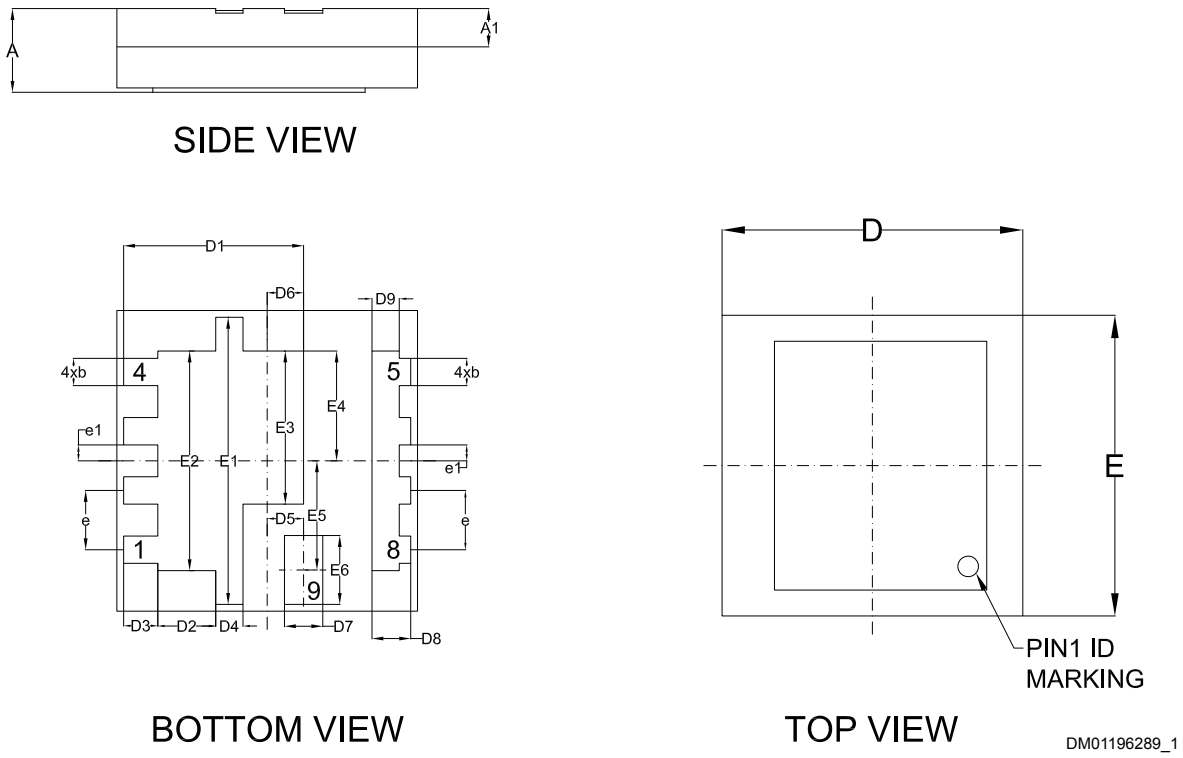
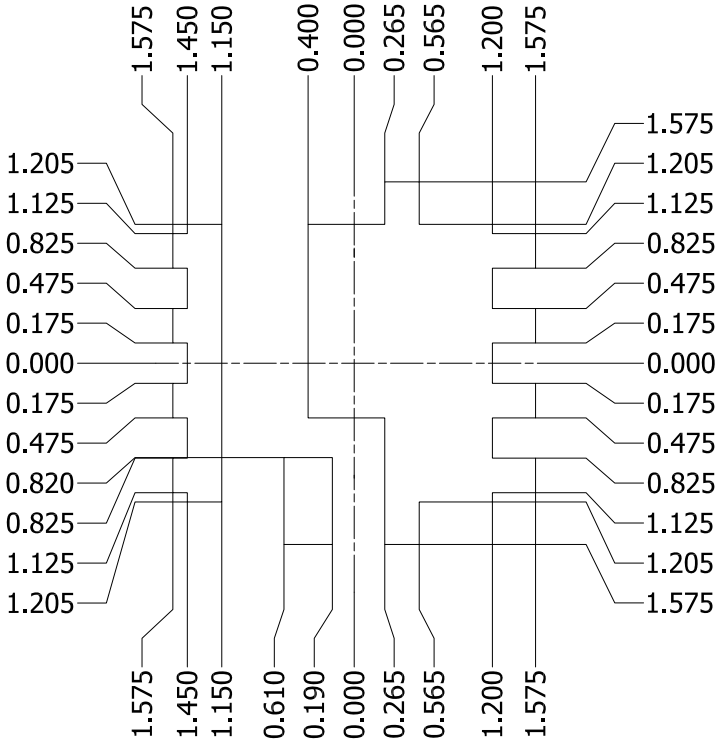


Table 7. **En-FCLGA 3.3x3.3 package mechanical data**

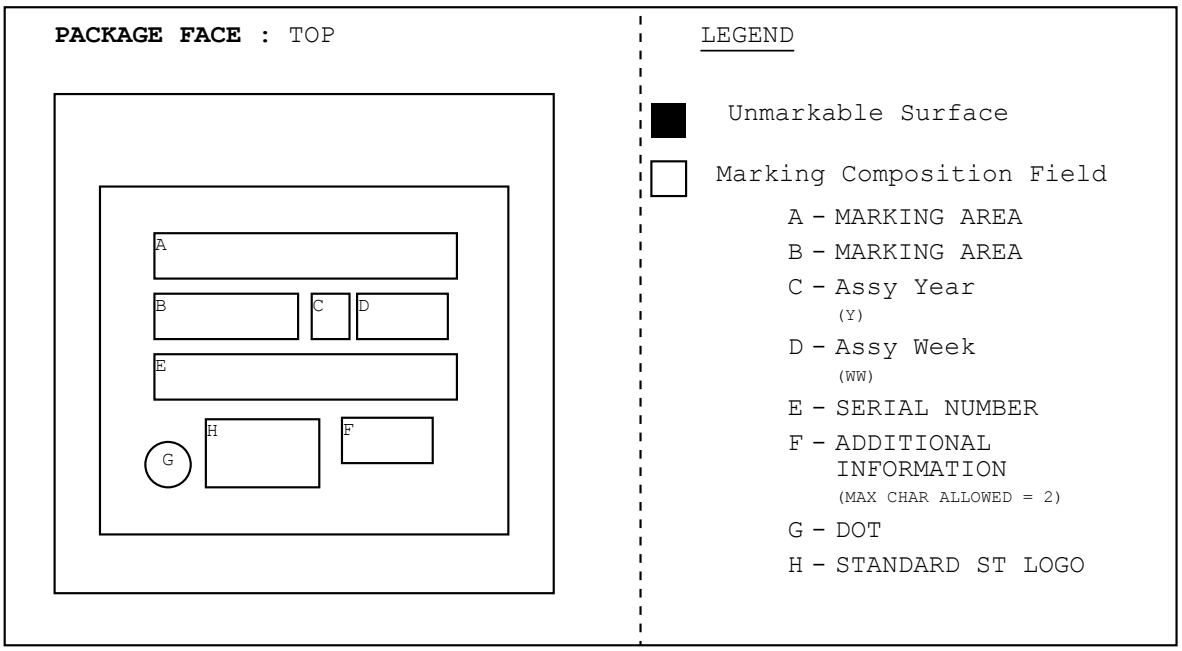
Dim.	mm		
	Min.	Typ.	Max.
A	0.77	0.87	0.97
A1	0.37	-	0.47
b	0.25	0.30	0.35
D	3.20	3.30	3.40
D1		1.975 REF	
D2		0.635 REF	
D3		0.375 REF	
D4		0.300 REF	
D5		0.400 REF	
D6		0.400 REF	
D7		0.420 REF	
D8		0.425 REF	
D9		0.300 REF	
E	3.20	3.30	3.40
E1		3.150 REF	
E2		2.410 REF	
E3		1.680 REF	
E4		1.205 REF	
E5		1.205 REF	
E6		0.755 REF	
e		0.650 BSC	
e1	-	0.175	-

Figure 21. **En-FCLGA 3.3x3.3 recommended footprint (dimensions are in mm)**



DM01196289_1_footprint

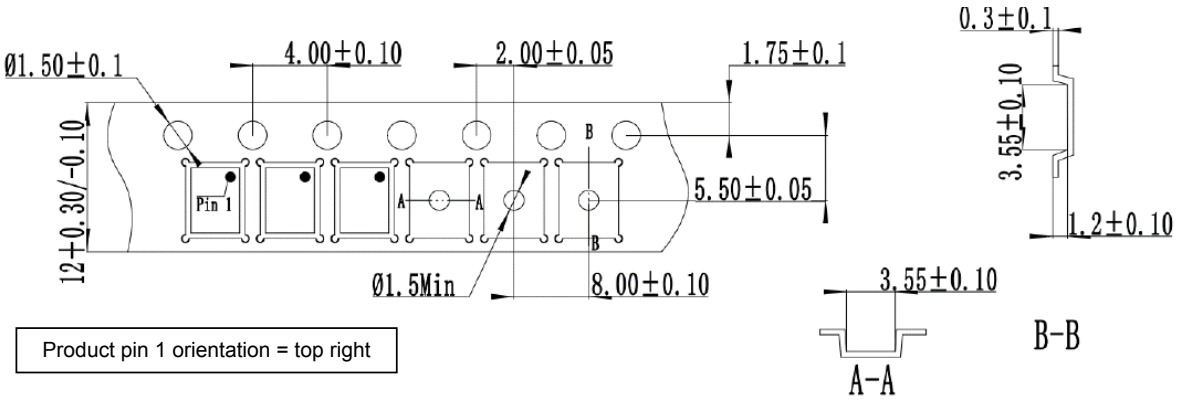
Figure 22. **Marking composition for En-FCLGA 3.3x3.3**



DM01266715_1_marking

4.2 En-FCLGA 3.3x3.3 packing information

Figure 23. **En-FCLGA 3.3x3.3 tape drawing (dimensions are in mm)**



DM01224218_1_tape

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
01-Jul-2026	1	First release.

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