Automotive-grade N-channel 650 V, 35 mΩ typ., 64 A MDmesh DM6 half-bridge topology Power MOSFET in an ACEPACK SMIT package

Features

<table>
<thead>
<tr>
<th>Order code</th>
<th>$V_{DS}$</th>
<th>$R_{DS(on)}$ max.</th>
<th>$I_D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SH68N65DM6AG</td>
<td>650 V</td>
<td>41 mΩ</td>
<td>64 A</td>
</tr>
</tbody>
</table>

- AQG 324 qualified
- Half-bridge power module
- 650 V blocking voltage
- Fast recovery body diode
- Very low switching energies
- Low package inductance
- Dice on direct bond copper (DBC) substrate
- Low thermal resistance
- Isolation rating of 3.4 kVrms/min

Applications

- Switching applications

Description

This device combines two MOSFETs in a half-bridge topology. The ACEPACK SMIT is a very compact and rugged power module in a surface mount package for easy assembly. Thanks to the DBC substrate, the ACEPACK SMIT package offers low thermal resistance coupled with an isolated top-side thermal pad. The high design flexibility of the package enables several configurations, including phase legs, boost, and single switch through different combinations of the internal power switches.
## Electrical ratings

### Table 1. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS}$</td>
<td>Gate-source voltage</td>
<td>±25</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current (continuous) at $T_C = 25 , ^\circ C$</td>
<td>64</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current (continuous) at $T_C = 100 , ^\circ C$</td>
<td>40</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$ (1)</td>
<td>Drain current (pulsed)</td>
<td>280</td>
<td>A</td>
</tr>
<tr>
<td>$P_{TOT}$</td>
<td>Total power dissipation at $T_C = 25 , ^\circ C$</td>
<td>379</td>
<td>W</td>
</tr>
<tr>
<td>$dv/dt$ (2)</td>
<td>Peak diode recovery voltage slope</td>
<td>100</td>
<td>V/ns</td>
</tr>
<tr>
<td>$di/dt$ (2)</td>
<td>Peak diode recovery current slope</td>
<td>1000</td>
<td>A/μs</td>
</tr>
<tr>
<td>$dv/dt$ (3)</td>
<td>MOSFET $dv/dt$ ruggedness</td>
<td>100</td>
<td>V/ns</td>
</tr>
<tr>
<td>$V_{ISO}$</td>
<td>Isolation withstand voltage applied between each pin and heat sink plate (AC voltage (50/60 Hz, $t = 60$ s))</td>
<td>3.4</td>
<td>kVrms</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage temperature range</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating junction temperature range</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

1. Pulse width limited by safe operating area.
2. $I_{SO} \leq 64$ A, $V_{DS}$ (peak) $< V_{(BR)DSS}$, $V_{DD} = 400$ V.
3. $V_{DS} \leq 520$ V.

### Table 2. Thermal data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JJC}$</td>
<td>Thermal resistance, junction-to-case</td>
<td>0.33</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

### Table 3. Avalanche characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{AR}$</td>
<td>Avalanche current, repetitive or not repetitive ($I_p$ limited by $T_J$ max)</td>
<td>9</td>
<td>A</td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single pulse avalanche energy (starting $T_J = 25 , ^\circ C$, $I_D = I_{AR}$)</td>
<td>1.9</td>
<td>J</td>
</tr>
</tbody>
</table>
2 Electrical characteristics

$T_C = 25 \, ^\circ\text{C}$ unless otherwise specified

### Table 4. On/off states

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR(DSS)}$</td>
<td>Drain-source breakdown voltage</td>
<td>$V_{GS} = 0 , \text{V}, I_D = 1 , \text{mA}$</td>
<td>650</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_DSS$</td>
<td>Zero gate voltage drain current</td>
<td>$V_{GS} = 0 , \text{V}, V_{DS} = 650 , \text{V}$</td>
<td>5</td>
<td></td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 0 , \text{V}, V_{DS} = 650 , \text{V}, T_C = 125 , ^\circ\text{C}$</td>
<td>300</td>
<td></td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>Gate-body leakage current</td>
<td>$V_{DS} = 0 , \text{V}, V_{GS} = \pm 25 , \text{V}$</td>
<td>±5</td>
<td></td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>Gate threshold voltage</td>
<td>$V_{DS} = V_{GS}, I_D = 250 , \mu\text{A}$</td>
<td>3.25</td>
<td>4</td>
<td>4.75</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>Static drain-source on resistance</td>
<td>$V_{GS} = 10 , \text{V}, I_D = 23 , \text{A}$</td>
<td>35</td>
<td>41</td>
<td></td>
<td>m$\Omega$</td>
</tr>
</tbody>
</table>

1. Defined by design, not subject to production test.

### Table 5. Dynamic characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{iss}$</td>
<td>Input capacitance</td>
<td>$V_{DS} = 100 , \text{V}, f = 1 , \text{MHz}, V_{GS} = 0 , \text{V}$</td>
<td>-</td>
<td>5900</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Output capacitance</td>
<td>$V_{DS} = 100 , \text{V}, f = 1 , \text{MHz}, V_{GS} = 0 , \text{V}$</td>
<td>-</td>
<td>260</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{rss}$</td>
<td>Reverse transfer capacitance</td>
<td>$f = 1 , \text{MHz}, I_D = 0 , \text{A}$</td>
<td>-</td>
<td>1.4</td>
<td>-</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$C_{oss,eq}$</td>
<td>Equivalent output capacitance</td>
<td>$V_{DS} = 0 \text{ to } 520 , \text{V}, V_{GS} = 0 , \text{V}$</td>
<td>-</td>
<td>867</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$R_{G}$</td>
<td>Intrinsic gate resistance</td>
<td>$f = 1 , \text{MHz}, I_D = 0 , \text{A}$</td>
<td>-</td>
<td>1.4</td>
<td>-</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$Q_{g}$</td>
<td>Total gate charge</td>
<td>$V_{DD} = 520 , \text{V}, I_D = 72 , \text{A}, V_{GS} = 0 \text{ to } 10 , \text{V}$</td>
<td>-</td>
<td>116</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gs}$</td>
<td>Gate-source charge</td>
<td>(see Figure 13. Test circuit for gate charge behavior)</td>
<td>-</td>
<td>37</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>Gate-drain charge</td>
<td>(see Figure 13. Test circuit for gate charge behavior)</td>
<td>-</td>
<td>45</td>
<td>-</td>
<td>nC</td>
</tr>
</tbody>
</table>

1. $C_{oss\,eq}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.

### Table 6. Switching characteristics (resistive load)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{d(on)}$</td>
<td>Turn-on delay time</td>
<td>$V_{DD} = 325 , \text{V}, I_D = 36 , \text{A}$,</td>
<td>-</td>
<td>42</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{r}$</td>
<td>Rise time</td>
<td>$R_{G} = 4.7 , \Omega, V_{GS} = 10 , \text{V}$</td>
<td>-</td>
<td>19</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{d(off)}$</td>
<td>Turn-off delay time</td>
<td>(see Figure 12. Switching times test circuit for resistive load and Figure 17. Switching time waveform)</td>
<td>-</td>
<td>108</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Fall time</td>
<td>(see Figure 12. Switching times test circuit for resistive load and Figure 17. Switching time waveform)</td>
<td>-</td>
<td>11</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>
Table 7. Switching characteristics (inductive load)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_d(v)</td>
<td>Voltage delay time</td>
<td>$V_{DD} = 400$ V, $V_{GS} = 0$ to 10 V, $I_D = 72$ A, $R_G = 6.8$ Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 18. Turn-off switching time waveform on inductive load)</td>
<td>-</td>
<td>117</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>t_r(v)</td>
<td>Voltage rise time</td>
<td>$R_G = 6.8$ Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 18. Turn-off switching time waveform on inductive load)</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_f(i)</td>
<td>Current fall time</td>
<td>$R_G = 6.8$ Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 19. Turn-on switching time waveform on inductive load)</td>
<td>-</td>
<td>18</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_c(off)</td>
<td>Crossing time off</td>
<td></td>
<td>-</td>
<td>24</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>t_d(i)</td>
<td>Current delay time</td>
<td>$V_{DD} = 400$ V, $V_{GS} = 0$ to 10 V, $I_D = 72$ A, $R_G = 82$ Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times)</td>
<td>-</td>
<td>354</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_r(i)</td>
<td>Current rise time</td>
<td>$R_G = 82$ Ω (see Figure 14. Test circuit for inductive load switching and diode recovery times and Figure 19. Turn-on switching time waveform on inductive load)</td>
<td>-</td>
<td>140</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_f(v)</td>
<td>Voltage fall time</td>
<td></td>
<td>-</td>
<td>14</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_c(on)</td>
<td>Crossing time on</td>
<td></td>
<td>-</td>
<td>252</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 8. Source-drain diode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{SD}</td>
<td>Source-drain current</td>
<td></td>
<td>-</td>
<td>64</td>
<td>-</td>
<td>A</td>
</tr>
<tr>
<td>I_{SDM}</td>
<td>Source-drain current (pulsed)</td>
<td></td>
<td>-</td>
<td>280</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>V_{SD}</td>
<td>Forward on voltage</td>
<td>$V_{GS} = 0$ V, $I_{SD} = 46$ A</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>t_r</td>
<td>Reverse recovery time</td>
<td>$I_{SD} = 72$ A, $dI/dt = 100$ A/μs, $V_{DD} = 60$ V</td>
<td>-</td>
<td>166</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Q_r</td>
<td>Reverse recovery charge</td>
<td>(see Figure 14. Test circuit for inductive load switching and diode recovery times)</td>
<td>-</td>
<td>1.1</td>
<td>μC</td>
<td></td>
</tr>
<tr>
<td>I_{RRM}</td>
<td>Reverse recovery current</td>
<td></td>
<td>-</td>
<td>11</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>t_r</td>
<td>Reverse recovery time</td>
<td>$I_{SD} = 72$ A, $dI/dt = 100$ A/μs, $V_{DD} = 60$ V, $T_J = 150$ °C</td>
<td>-</td>
<td>336</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Q_r</td>
<td>Reverse recovery charge</td>
<td>$V_{DD} = 60$ V, $T_J = 150$ °C</td>
<td>-</td>
<td>5.1</td>
<td>μC</td>
<td></td>
</tr>
<tr>
<td>I_{RRM}</td>
<td>Reverse recovery current</td>
<td>(see Figure 14. Test circuit for inductive load switching and diode recovery times)</td>
<td>-</td>
<td>26</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs, duty cycle 1.5%.
2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

- Operation in this area is limited by $R_{DS(on)}$.
- $V_{GS} = 10$ V
- $t_{on} = 10$ µs
- $t_{off} = 100$ µs
- $I_D = 72$ A
- $V_{DD} = 520$ V

**Figure 2. Maximum transient thermal impedance**

- $R_{thJC} = 0.33$ °C/W
- Single pulse

**Figure 3. Typical output characteristics**

- $V_{GS} = 9, 10$ V
- $V_{GS} = 8$ V
- $V_{GS} = 7$ V
- $V_{GS} = 6$ V

**Figure 4. Typical transfer characteristics**

- $V_{GS} = 20$ V

**Figure 5. Typical gate charge characteristics**

- $Q_g (nC)$
- $V_{DD} = 520$ V
- $I_D = 72$ A

**Figure 6. Typical drain-source on-resistance**

- $R_{DS(on)} (mΩ)$
- $V_{GS} = 10$ V
Figure 7. Typical capacitance characteristics

Figure 8. Normalized gate threshold vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical reverse diode forward characteristics
Test circuits

Figure 12. Switching times test circuit for resistive load

Figure 13. Test circuit for gate charge behavior

Figure 14. Test circuit for inductive load switching and diode recovery times

Figure 15. Unclamped inductive load test circuit

Figure 16. Unclamped inductive waveform

Figure 17. Switching time waveform
Figure 18. Turn-off switching time waveform on inductive load

Figure 19. Turn-on switching time waveform on inductive load
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 ACEPACK SMIT package information

Figure 20. ACEPACK SMIT package outline
Table 9. ACEPACK SMIT package mechanical data

<table>
<thead>
<tr>
<th>Dim.</th>
<th>mm</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td>19.50</td>
<td>20.00</td>
<td>20.50</td>
</tr>
<tr>
<td>B</td>
<td></td>
<td>21.50</td>
<td>22.00</td>
<td>22.50</td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>22.80</td>
<td>23.00</td>
<td>23.20</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>24.80</td>
<td>25.00</td>
<td>25.20</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>32.20</td>
<td>32.70</td>
<td>33.20</td>
</tr>
<tr>
<td>b</td>
<td>b1</td>
<td></td>
<td>9.00</td>
<td>4.00</td>
</tr>
<tr>
<td>b2</td>
<td></td>
<td>6.75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b3</td>
<td></td>
<td>9.50</td>
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<tr>
<td>c</td>
<td>c1</td>
<td>0.95</td>
<td>1.00</td>
<td>1.10</td>
</tr>
<tr>
<td>d</td>
<td>d1</td>
<td>0.00</td>
<td>0.55</td>
<td>0.65</td>
</tr>
<tr>
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<td>1.50</td>
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<td></td>
<td>3.95</td>
<td>4.00</td>
<td>4.05</td>
</tr>
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<td>m</td>
<td></td>
<td>5.40</td>
<td>5.50</td>
<td>5.60</td>
</tr>
<tr>
<td>m1</td>
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<td>1.80</td>
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<td>V</td>
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<td>1.80</td>
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<tr>
<td>V1</td>
<td></td>
<td>0°</td>
<td>2°</td>
<td>4°</td>
</tr>
<tr>
<td>aaa</td>
<td></td>
<td>0.01</td>
<td>0.05</td>
<td></td>
</tr>
<tr>
<td>bbb</td>
<td></td>
<td>0.00</td>
<td>0.10</td>
<td></td>
</tr>
</tbody>
</table>
**Figure 21. ACEPACK SMIT recommended footprint**

Note: Dimensions in mm.

**Figure 22. ACEPACK SMIT marking orientation vs pinout**
4.2 ACEPACK SMIT packing information

Figure 23. ACEPACK SMIT tape outline

\[
\begin{array}{c}
\text{SECTION A-A} \\
\text{SCALE 1:2} \\
\hline
\end{array}
\]

\[
\begin{array}{c}
\text{DETAIL C} \\
\text{SCALE 2:1} \\
\hline
\end{array}
\]

Note: Dimensions in mm.
## Revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>25-Jul-2022</td>
<td>1</td>
<td>First release.</td>
</tr>
</tbody>
</table>
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