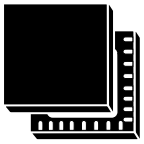
ST25R500

Datasheet

Automotive high performance NFC reader for CCC digital key and car center console



VFQFPN32

(5 x 5 mm)

Product status
ST25R500

Features

AEC-Q100 qualified

Operating modes

- Reader/writer
- Card emulation

RF communication - reader/writer

- EMVCo 3.2a analog- and digital-compliant
- NFC-A/ISO/IEC 14443A up to 848 kbit/s
- NFC-B/ISO/IEC 14443B up to 848 kbit/s
- NFC-V/ISO/IEC 15693 up to 212 kbit/s
- NFC-F/FeliCa™ up to 424 kbit/s
- Low-level modes to implement MIFARE Classic®-compliant and protocols (Kovio BC, CTS, B')

RF communication - card emulation

- NFC-A/ISO/IEC 14443A 106 kbit/s
- NFC-F/FeliCa™ 212/424 kbit/s

Key characteristics

- Passive P2P mode
- NFC Forum universal device
- CCC digital key reader
- USI WLC reader device
- Low-power inductive card detection
- I/Q demodulator with baseband channel summation
- Dynamic power output (DPO) controls the field strength to stay within given limits (software feature)
- Active wave shaping (AWS) reduces both overshoots and undershoots
- Noise suppression receiver (NSR) allows reception in a noisy environment
- Serial peripheral interface (SPI) up to 10 Mbit/s
- Possibility to drive one differential or two independent single-ended antennas

Electrical characteristics

- Wide supply voltage range: 2.7 V to 5.5 V
- Wide peripheral communication supply range: 1.65 to 5.5 V
- Wide ambient temperature range: -40 °C to +125 °C
- Quartz oscillator capable of operating with 27.12 MHz crystal with fast startup

Application

The ST25R500 is suitable for a wide range of applications, among them:

- Automotive access control
- Center console applications and NFC charging
- CCC digital key
- Automotive infrastructure application

1 Description

The ST25R500 is an automotive grade high-performance NFC universal device supporting NFC initiator, NFC target, NFC reader, and NFC card emulation modes. Designed for CCC (Car Connectivity Consortium®) digital key applications, the device enables fast product development for car access/start applications in areas like door handle or center console, and enables additional functionality, like pairing or NFC card protection combined with a Qi charger. Being very robust and noise tolerant while at the same time reducing electromagnetic emission, the device works even under harsh conditions, enabling an easier certification.

The device includes an advanced analog front end (AFE) and a highly integrated data framing system for NFC-A/B (ISO/IEC 14443A/B) reader, including higher bit rates, NFC-F (FeliCa™) reader, NFC-V (ISO/IEC 15693) reader up to 212 kbps, and NFC-A/NFC-F card emulation.

It meets the most demanding requirements set by car and phone OEMs, delivering market-leading performance and ensuring a superior user experience.

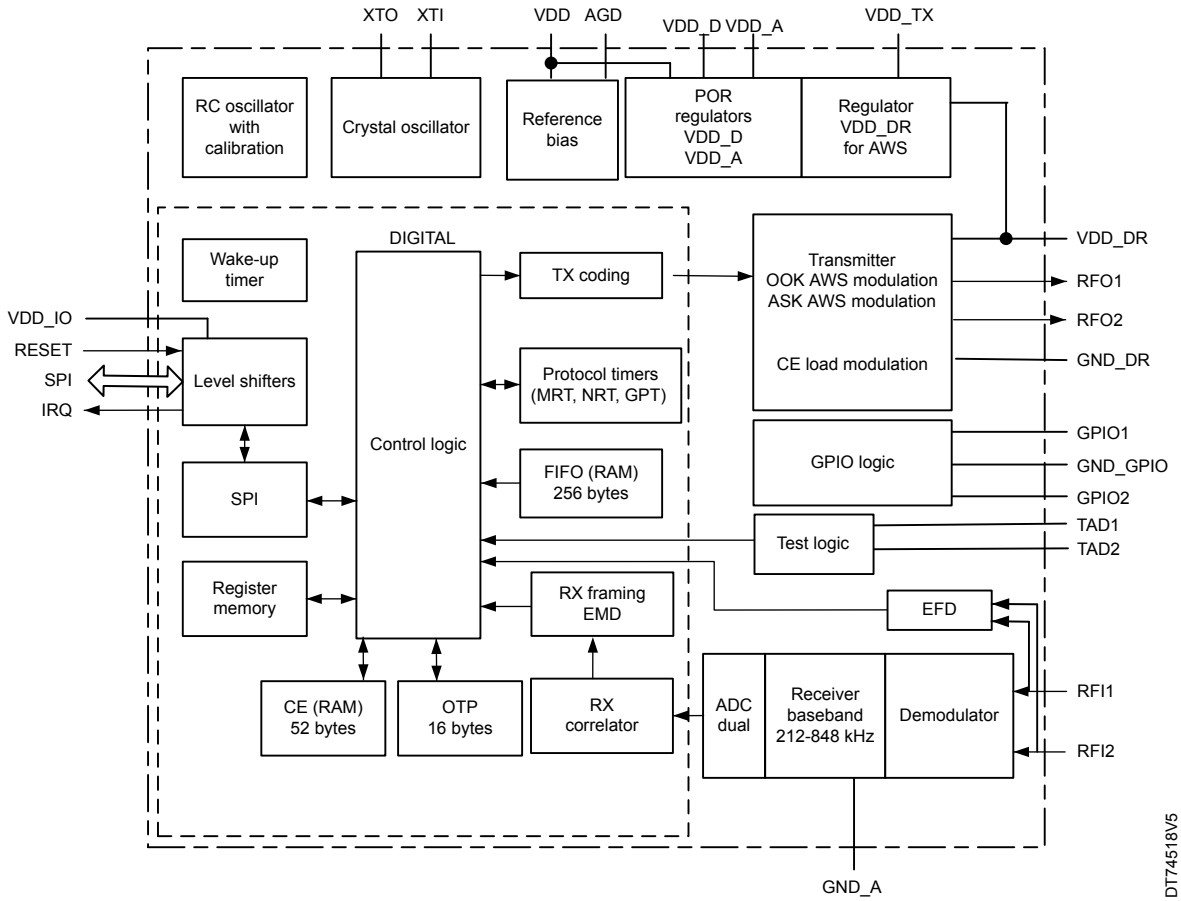
The device features high RF power with dynamic power output to directly drive antennas at high efficiency, achieving large interaction distances even with small antenna sizes common in door handles. The device includes additional features, making it incomparable for low-power applications. It offers low-power card detection by performing a measurement of the I and Q channel, which represent the real and imaginary part of the antenna signal. It is designed to operate from a wide power supply range (from 2.7 to 5.5 V), ambient temperature range from -40 °C to +125 °C, and a wide peripheral I/O voltage range (from 1.65 to 5.5 V). Due to this combination of high RF output power, low-power modes, wide supply range, and AEC-Q100 grade 1 qualification, the device is perfectly suited for automotive applications.

2 Functional overview

2.1 Block diagram

The block diagram is shown in the following figure.

Figure 1. ST25R500 block diagram



2.1.1 Transmitter

The transmitter incorporates the drivers, which drive the external antenna through pins RFO1 and RFO2. Both single-ended and differential antenna configurations are supported. The transmitter block also generates the OOK or AM modulation of the transmitted RF signal during Reader operation and Passive load modulation (PLM) during card emulation (CE) operation.

2.1.2 Receiver

The receiver detects card modulation superimposed on the 13.56 MHz carrier signal. The receiver chain incorporates several features that enable reliable operation in challenging and noisy conditions. The same receiver is also used for card emulation operation.

The receiver is connected to the antenna via the pins RFI1 and RFI2. The output of the receiver is connected to the framing block that decodes the demodulated and digitized subcarrier signal.

2.1.3 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals. At oscillator startup, the transconductance of the oscillator is increased to achieve a fast startup. Since the startup time varies with crystal type, temperature, and other parameters, the oscillator amplitude is monitored, and an I_osc interrupt is sent when stable oscillator operation is reached.

2.1.4 Power supply regulators

Integrated power supply regulators ensure a high-power supply rejection ratio for the complete system. Different voltage regulators supply separate blocks to decouple from noise sources.

2.1.5 POR and bias

This block provides bias currents and reference voltages to all other blocks. It also incorporates a power on reset (POR) circuit, which provides a reset at power-up and at low supply levels.

2.1.6 RC oscillator and wake-up timer

The RC oscillator allows the wake-up timer to run and periodically trigger a measurement of the surroundings for low-power card detection mode.

2.1.7 Tx coding

This block encodes the transmit frames according to the selected RF communication mode and bit rate. It generates the start of frame (SOF), end of frame (EOF), cyclic redundancy check (CRC), and parity bits automatically. The data to be transmitted is taken from the FIFO.

2.1.8 Rx framing

This block decodes received frames according to the selected RF communication mode and bitrate. The SOF, EOF, CRC, and parity bits are automatically checked and removed by this block, except for the CRC. The received data is then placed in the first-in first-out (FIFO) buffer.

2.1.9 Control logic

This block drives all activity of the device based on the commands received through the serial interface and the configurations present on the registers.

2.1.10 FIFO

A 256-byte FIFO is available for exchanging data through the transmitter and receiver. Depending on the mode, it contains either data that has been received or must be transmitted.

2.1.11 SPI

A 4-wire SPI is available for communication between the device and the host.

2.1.12 External field detector (EFD)

The external field detector signals the presence of an external NFC field during card emulation.

2.1.13 RC oscillator

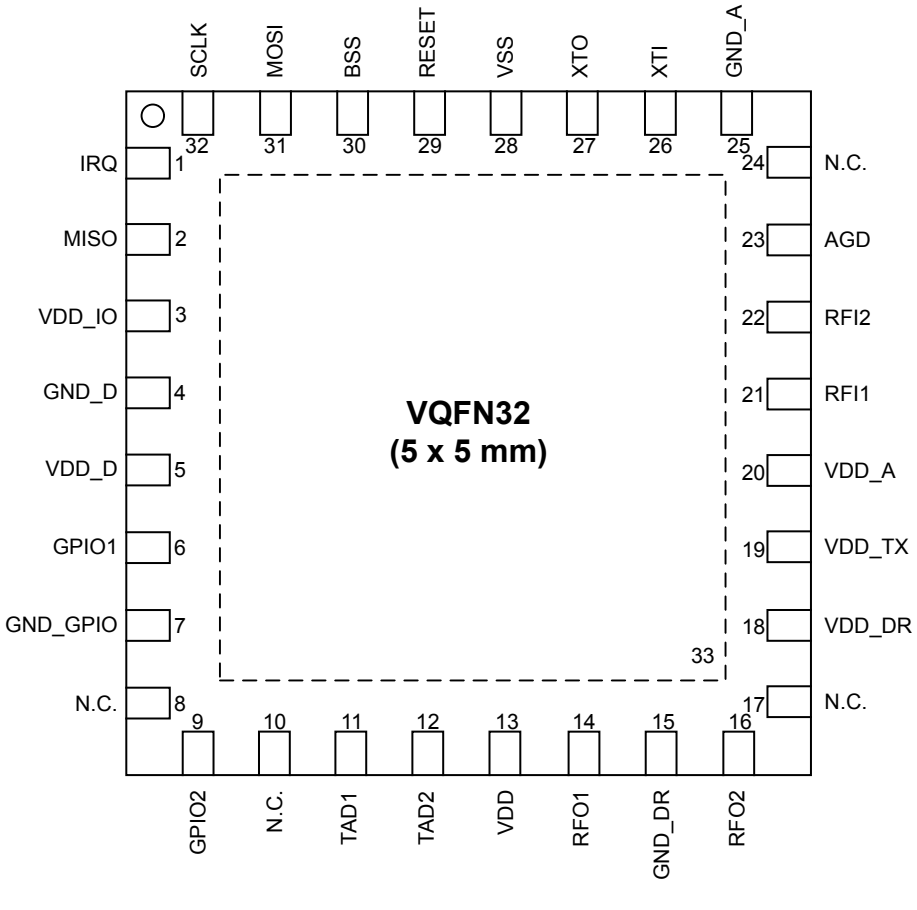
The RC oscillator provides a low frequency clock to the wake-up timer and digital logic block.

2.1.14 Wake-up timer

The wake-up timer periodically transitions the chip from power-down mode to ready mode during wake-up mode.

3 Pin and signal description

Figure 2. **VQFN32 pinout (top view)**



Note: N.C. pins must be connected to PCB ground.

Table 1. VQFN32 pin assignment

Package VQFN32	Pin name	Type(1)	Description
1	IRQ	DO	Interrupt request output
2	MISO	DO_T	Serial peripheral interface data output
3	VDD_IO	S	External peripheral communication supply
4	GND_D	S	Digital ground
5	VDD_D	AOS	Regulated supply for digital block
6	GPIO1	ADO	GPIO to switch between reader operation and CE operation matching network or digital output. When not being used, it must be kept unconnected.
7	GND_GPIO	S	GPIO ground
8	N.C.	-	Not connected internally. Connect to PCB ground.
9	GPIO2	ADO	GPIO to switch between reader operation and CE operation matching network or digital output. When not being used, it must be kept to unconnected.
10	N.C.	-	Not connected internally. Connect to PCB ground.
11	TAD1	ADIO	Analog/Digital test pin. When not being used, it must be kept not connected.
12	TAD2	ADIO	Analog/Digital test pin. When not being used, it must be kept not connected.
13	VDD	S	External main positive supply
14	RFO1	AO	Antenna driver output
15	GND_DR	S	Antenna driver ground, driver V_{SS}. It must be connected to thermal pad via the shortest possible connection.
16	RFO2	AO	Antenna driver output
17	N.C.	-	Not connected internally. Connect to PCB ground.
18	VDD_DR	AOS	Regulated supply for antenna driver
19	VDD_TX	S	External main positive supply for driver
20	VDD_A	AOS	Regulated supply for analog
21	RFI1	AI	Receiver input
22	RFI2	AI	Receiver input
23	AGD	AIO	Analog reference voltage
24	N.C.	-	Not connected internally. Connect to PCB ground.
25	GND_A	S	Analog ground
26	XTI	AI	Crystal oscillator input
27	XTO	AO	Crystal oscillator output
28	VSS	S	Ground, die substrate potential
29	RESET	DI	Reset input
30	BSS	DI	Serial peripheral interface enable (active low)
31	MOSI	DI	Serial peripheral interface data input
32	SCLK	DI	Serial peripheral interface clock
33	VSS	S	Exposed pad, ground, die substrate potential, via exposed die pad

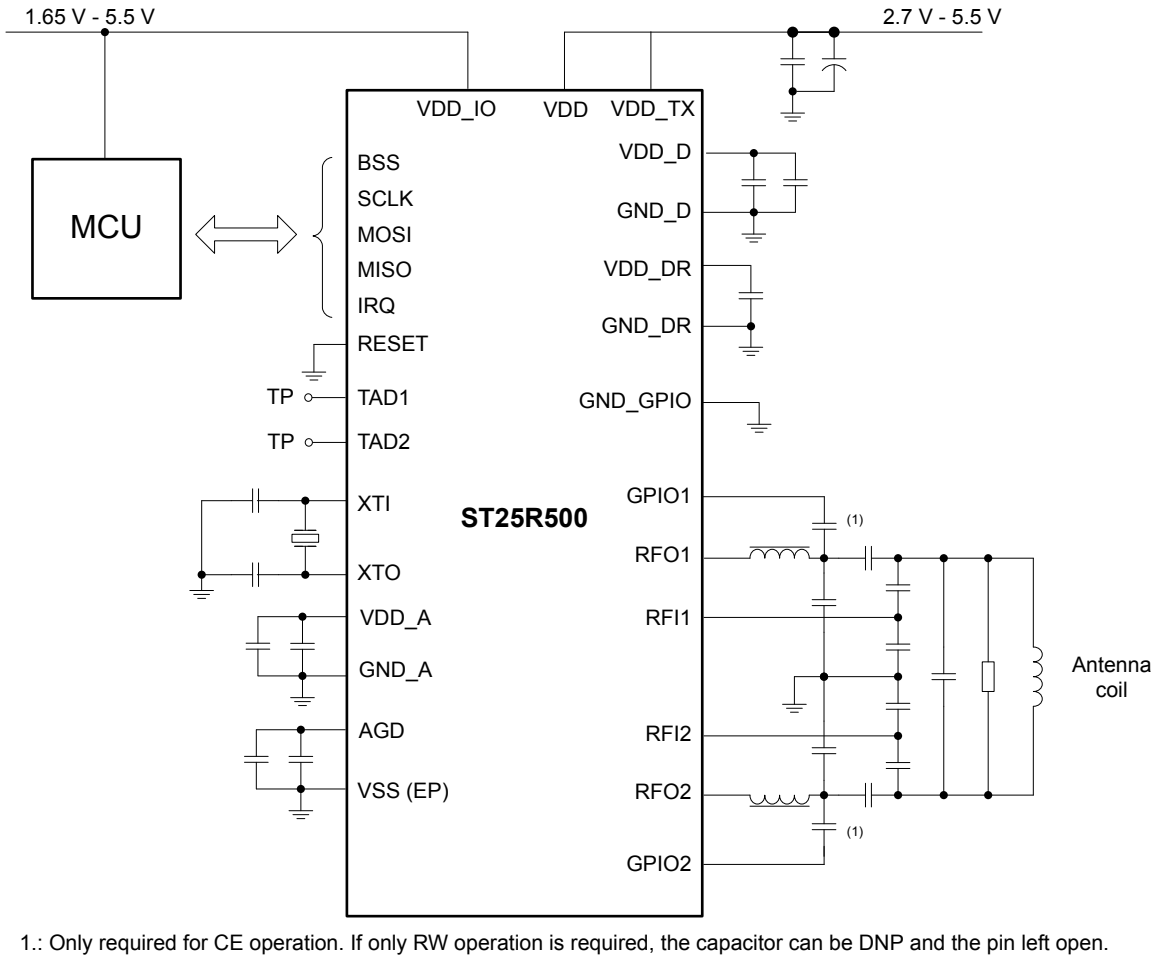
1. *S: power supply pin, AIO: analog I/O, AI: analog input, AO: analog output, ADIO: analog/digital input/output, AOS: analog output/supply input, DI: digital input, DO: digital output, DO_T: digital output/tri-state.*

4 Device description

4.1 System diagram

The minimum system configuration is shown below for a differential antenna configuration.

Figure 3. Minimum system configuration



1.: Only required for CE operation. If only RW operation is required, the capacitor can be DNP and the pin left open.

5 Application information

5.1 Operation modes

The device supports four operating modes.

5.1.1 Reset mode (RESET)

When the device is supplied with VDD, VDD_TX, and VDD_IO, and the RESET pin is high, the device is in reset mode.

All blocks are deactivated, no clock is present, and current consumption is minimized.

5.1.2 Power-down mode (PD)

If the RESET pin is low at power-up or after the RESET pin state changes from high to low, the device enters power-down mode. In this mode, the AFE static power consumption is very low, but SPI communication is possible, in addition to register access to those in the PD domain.

The following blocks are active in PD mode:

- VDD_D regulator (1 V) in low-power mode
- Registers in the PD domain
- SPI block and IRQ logic

5.1.3 Wake-up mode (WU)

Wake-up mode is controlled through the wu_en bit. In this mode, the device senses changes in antenna properties at regular time intervals and triggers an IRQ if a change is detected.

The following blocks are active in WU mode:

- VDD_D regulator (1 V) in low-power mode
- Registers in PD domain
- RC oscillator
- WU timer
- SPI block and IRQ logic

5.1.4 Ready mode (RD)

Ready mode is controlled by the en bit. In this mode the regulators and crystal oscillator are enabled, and the device is ready to transmit or receive.

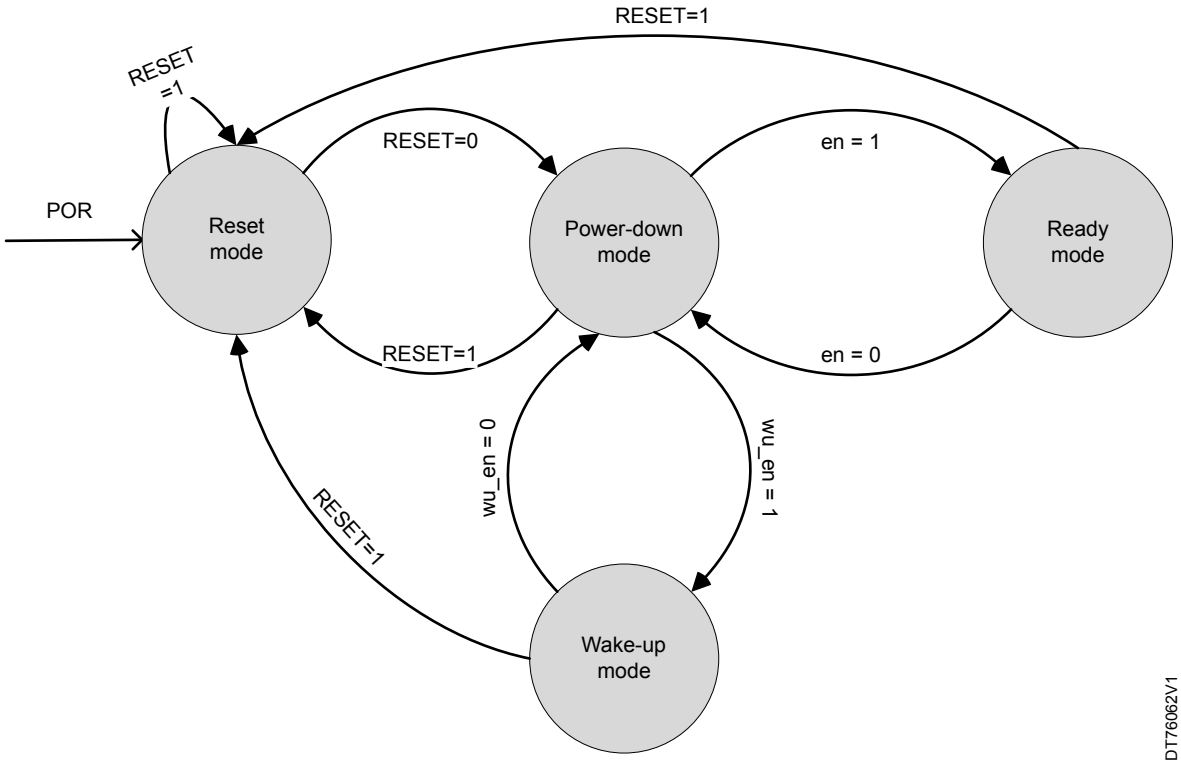
The following blocks are active in RD mode:

- VDD_D regulator (1 V) in normal power mode
- All registers (both in PD and RD domain)
- Main logic
- VDD_A and VDD_DR regulators
- Crystal oscillator
- SPI block and IRQ logic

When RD mode is reached, the device issues an I_osc interrupt.

The following diagram shows the transition from one state to another:

Figure 4. **Transition from one state to another**



5.2 Power-on sequence

Once powered and once the RESET pin is low, the device enters the PD mode. The content of all registers is set to its default state. The device can be set into any other operation mode except RESET by changing the configuration in the Operation register.

Changing from PD mode to RD mode and preparing for communication comprises:

- Apply the appropriate configuration on registers: operation and general configuration registers
- Set en = 1 in the operation register and wait for the device to get ready with the oscillator stabilized (notified by the I_osc interrupt and osc_ok status)
- The adjust regulator direct command should be executed when the carrier is enabled. When coming from RD mode with disabled VDD_DR and disabled field, execute the following:
  - Set vdddr_en to 1
  - Wait at least 10 µs
  - Set tx_en and rx_en to 1
  - Execute adjust regulator direct command
- Additionally, the direct command calibrate RC must be issued.

Once the above-mentioned points are done, the device is ready for communication.

5.3 Transmitter

The transmitter contains two identical push-pull driver blocks connected to the RFO1 and RFO2 pins. These drivers are differentially driving the external antenna LC tank via the antenna matching network. It is also possible to operate only one of the two drivers by setting the single bit in the General configuration register and selecting which RFO/RFI to be used on rfo2 bit.

5.3.1 Output resistance

Each driver is composed of eight segments having binary weighted output resistance. The MSB segment typical ON resistance is 2 x RRFO. When all segments are turned on, the output resistance is defined by RRFO. Usually, all segments are turned on to define the normal transmission (unmodulated) level. It is also possible to switch off certain segments when driving the unmodulated level to drive the circuitry with a higher impedance driver.

The d_res bits in the Tx driver configuration register define the resistance during the normal transmission. The default setting is the minimum available resistance.

When using the single driver mode, the number of external components and therefore the cost of the antenna LC tank components is halved, but also the output power is reduced. In single mode it is possible to connect two antenna LC tanks to the two RFO outputs and multiplex between them by controlling the rfo2 bit in the General configuration register.

To transmit data, the transmitter output level needs to be modulated. AM and OOK modulation principles are supported. The type of modulation is defined by setting the tr_am bit in the Tx modulation register 1.

5.3.2 Driver Tx modulation

During the OOK modulation (for example, NFC-A or NFC-V), the transmitter drivers stop driving the carrier frequency. Therefore, the amplitude of the antenna LC tank oscillation decays. The time constant of the decay is defined by the LC tank Q factor.

AM modulation (for example, NFC-B) is done via a reduction of the VDD_DR regulator-regulated voltage that supplies the drivers during the modulation state.

The AM modulation level is set by the am_mod bits in the Tx modulation register 1.

AM modulation must be enabled and the modulation index must be set correctly for the following protocols:

- NFC-B
- FeliCa

Depending on the applicable standard, the modulation index is set in a range between 8% and 97% in the Tx modulation register 1. The modulation scheme, AM modulation or OOK modulation, can be selected by the tr_am bit in the Tx protocol register 1.

5.3.3 Passive load modulation

The ST25R500 enables passive load modulation using three different methods:

- Internal driver load modulation
- Load modulation with an external NMOS transistor
- Load modulation via the EMI filter switching

The driver load modulation is selected by the lm_dri bit for internal driver load modulation in CE modulation register 2, and the external NMOS modulation is selected by the lm_trim or the lm_gpio option bits.

Normally, the internal driver is used for the generation of the passive load modulation. In case higher load modulation is required, the device also supports external passive load modulation through an NMOS transistor. Advanced antenna tuning (AAT) and the frequency shift circuit (FSC) use NMOS transistors to switch the matching between reader and card emulation operation.

Both the lm_trim or lm_gpio option bits enable the load modulation through an external NMOS transistor and a capacitor. In addition, lm_gpio can be used to perform the load modulation via the EMI capacitor switching.

The following table provides an overview about the passive load modulation capabilities:

Table 2. Modulation scheme

Bit	LM through driver(1)	LM through AAT circuit (1-4 bits)(2)	LM through frequency shift circuit (1-bit)(2)	LM through EMI capacitor switching(2)
lm_dri	Yes	Yes	Yes	Yes
lm_trim	-	-	Yes	-
lm_gpio	-	Yes	Yes	Yes

1. *Main mechanism to fine-tune the passive LMA strength. Based on antenna size and matching, an additional mechanism might be required to pass the ISO 10373-6 loading effect or NFC Forum Delta Vov Ratio (DVR). Also, the ce_res and cem_res bits need to be configured accordingly.*

2. *Additional circuit that can be used for statically switching the matching between reader and card mode or increase/decrease passive LMA in combination with lm_dri.*

Also, the gpio_en, tad_en, trim_ce, gpio_ce, trim_rw and gpio_rw bits need to be configured accordingly. If the antenna has too strong coupling with the reference antenna, one of the three methods (AAT, FSC, EMI capacitor switching) can be implemented to switch between reader operation antenna tuning and card emulation antenna tuning.

5.3.3.1 *LM through driver*

The driver load modulation is based on the change of the driver impedance. The ce_res value depends on the matching and the antenna configuration. It is typically chosen to fulfill the loading effect test. The ce_res bits must be set before entering passive target mode.

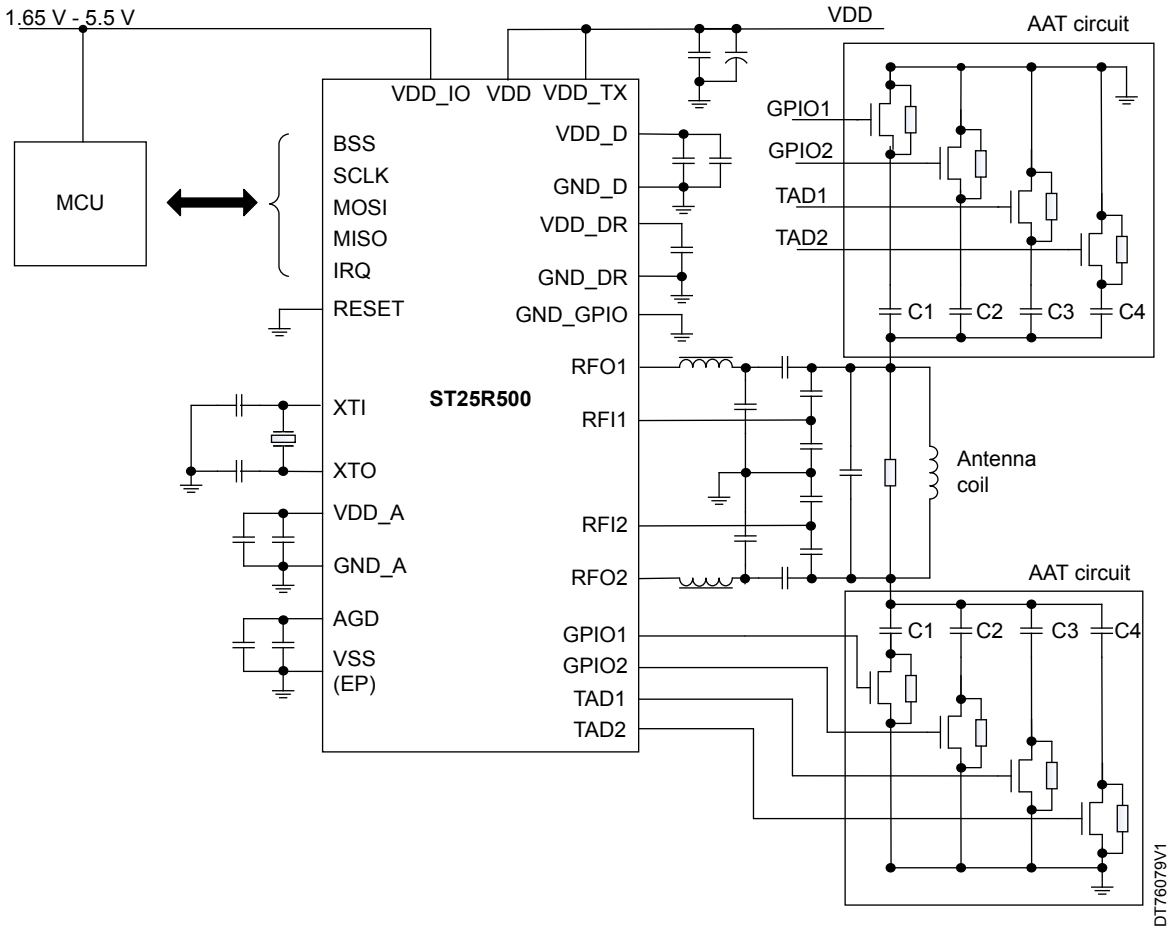
During the non-modulated and the modulated states the driver output impedance is defined, respectively, by the ce_res and the cem_res option bits. During the unmodulated state, the output impedance is defined by ce_res option bits. During modulation the output impedance is defined by the cem_res option bits. Once defined, the ce_res option bits should be kept at the same value during card emulation operation.

Typically, a low driver impedance during the modulated state and a high driver impedance for the non-modulated state is used. It is also possible to reverse the modulation by switching the ce_res and cem_res settings.

5.3.3.2 *LM through AAT*

To increase the load modulation amplitude, the AAT circuit can be used. This circuit may not be only used to switch between reader and card emulation antenna matching, it can also be used to tune the antenna to a certain matching impedance in reader or card emulation operation.

Figure 5. AAT circuit example

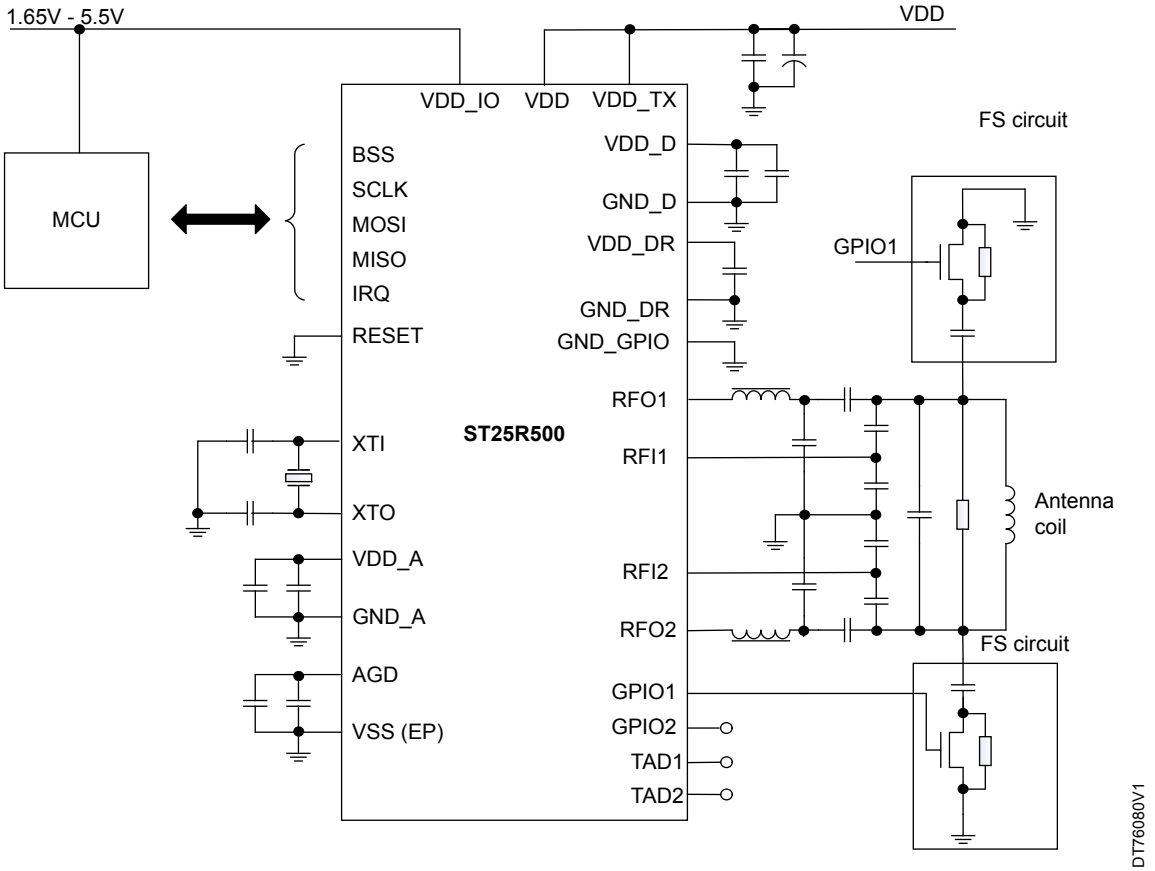


Setting the lm_gpio option bits to ones, the GPIO1 and GPIO2 pins are driven by the digital signal of the load modulation signal. The value of the gpio_ce and gpio_rw bits sets if the polarity is positive or inverse for the external load modulation. The capacitors of the AAT circuit should be binary-weighted; therefore, GPIO1 and GPIO2 can achieve different LMA strengths.

5.3.3.3 *LM through frequency shift circuit*

The frequency shift circuit (FSC) allows switching between reader operation matching and card emulation operation matching to lower the loading effect in card emulation operation. To switch between the two static matchings, the same principle as for AAT can be chosen, but the number of trimming elements can be reduced to one transistor and one capacitor per RFO. It is recommended to connect the FSC to one of the GPIO pins. If the FSC is connected to one GPIO the corresponding lm_gpio bit can be set. If the FSC is connected to one of the TAD pins, the lm_trim should not be used. Using the lm_gpio or the lm_trim bits, the matching switches from card emulation to reader/writer mode matching in or out of phase with the digital signal of the load modulation (848 kHz subcarrier or 424 / 212 kHz modulation signal).

Figure 6. Frequency shift circuit example



5.3.3.4 *LM through EMI capacitor switching*

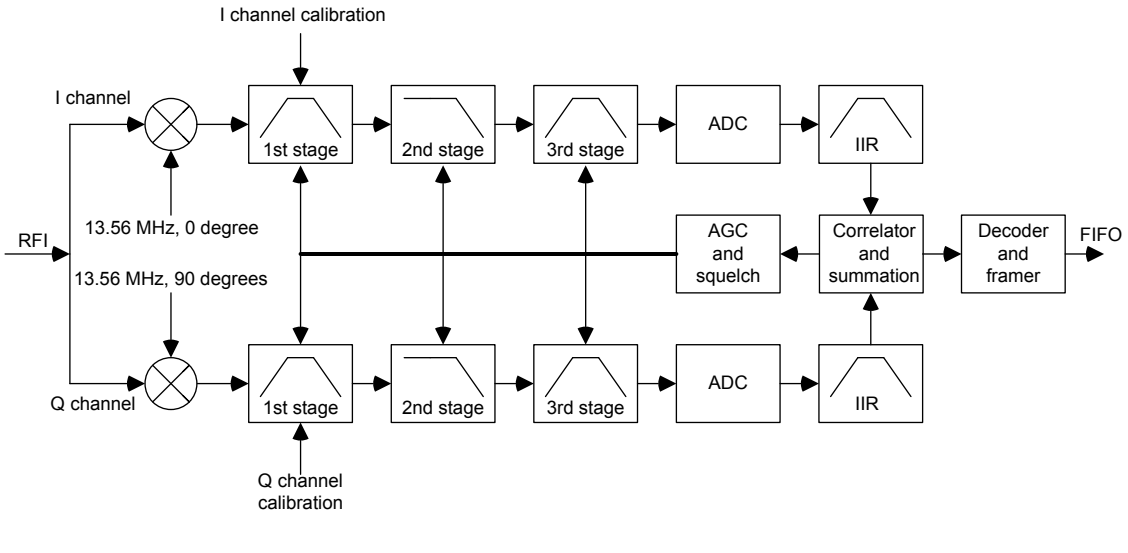
An example of a circuit capable of switching the EMI capacitor can be found in the Figure 3. Minimum system configuration.

The capacitor connected between the EMI filter and GPIO1, and EMI filter and GPIO2 pin is pulled to GND through an internal MOS transistor. Since this capacitor can build a series resonating circuit with parasitic components (bond wires, PCB traces), special care must be taken when selecting the component value. During reader-writer operation, this MOS transistor needs to be enabled (gpio_en = 0x0 and gpio_rw = 0x3), and in card emulation operation, the MOS transistor needs to be disabled (gpio_en = 0x0 and gpio_ce = 0x0). By setting the gpio_en bits to 0, the push-pull driver used for the AAT circuit is disabled, and the internal MOS transistor is selected. By setting the gpio_rw bits to 1 the internal MOS transistor is low ohmic. Setting the lm_gpio option bits to ones, the GPIO1 and GPIO2 pins are driven by the digital signal of the load modulation signal.

5.4 Receiver

The receiver performs the demodulation of the tag subcarrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs an I/Q demodulation, amplification, band-pass filtering, and digitization of the subcarrier signals. It also performs RSSI measurements, automatic gain control (AGC), and squelch functions. The reception chain has two separate channels for the I and Q demodulation. I and Q channels result in mixing the 13.56 MHz carrier signal coming from the antenna with a local 13.56 MHz clock generated by the crystal oscillator. The I and Q mixing clock are 90 degrees phase-shifted. The reception framing is done automatically by the receiver logic. The receiver is switched on when the rx_en bit in the Operation register is set to 1.

Figure 7. Receiver block diagram



5.4.1 Demodulation stage

The I/Q demodulation made up of two mixer circuits, each driven by local oscillator signals that are phase-shifted by 90° relative to each other and derived from the crystal oscillator. The outputs of the two mixers are connected to two equal baseband reception chains and to the decoding logic.

5.4.2 Filter and gain stages

The receiver chain has band pass filtering characteristics. This band pass filter consists of three stages. Each stage has a static gain and an AGC controlled attenuation. The filtering is optimized to pass the subcarrier frequencies while rejecting the carrier frequency, low frequency noise, and DC component. The first and third stages have a selectable first order high pass filter and a fixed first order low pass filter. The high pass filter characteristics of the first and third stages can be controlled via the hpf_ctrl bits in the Rx analog settings register 1. The low pass filter characteristics are fixed for both stages. The second stage consists of a second order fixed low pass filter.

The maximum gain of the first and the second stage is 20 dB and can be reduced in 3 dB steps by the AGC. The gain of the third stage is 6 dB if gain_boost is enabled by setting the gain_boost bit to 1 in the Rx analog settings register 1, which increases the max gain by an additional 3 dB. The total gain of the filter and gain stage is 49 dB including the gain boost. A default gain reduction for the AGC can be configured via the afe_gain_rw bits in the Rx analog settings register 2.

The same filter blocks can also be used for other operation modes. In all modes, the starting gain is set through the corresponding gain reduction. The gain in wake-up mode can be configured by the afe_gain_td in Rx analog settings 2 register. The gain in card emulation operation can be configured by the afe_gain_ce bits in the Rx analog settings register 3.

The chip features a secondary filter stage after the analog to digital converter. It consists of an infinite impulse response (IIR) low pass filter and an IIR high pass filter. Its coefficient can be configured in the Rx digital settings register 1 by setting the lpf_coef and hpf_coef bits.

5.4.3 Analog-to-digital converter

The analog-to-digital converter digitizes the signal coming from the filter and the gain stages. In wake-up mode, the ADC output is stored in the I-channel WU ADC display register and the Q-channel WU ADC display register.

5.4.4 Correlator system

The correlation system is designed to maximize the receiver sensitivity and the selectivity to the subcarrier frequencies found in a tag's reply. To achieve this, the subcarrier signal coming from the tag is compared to a local subcarrier clock. The best signal to noise ratio is achieved if these two signals match. I and Q channel signals are combined via the summation block to remove the need for a channel selection while simultaneously improving the performance. The same topology is used to achieve NFC-A and NFC-B 106-848 kbit/s, FeliCa 212 kbit/s and 424 kbit/s, and NFC-V single subcarrier 26 kbit/s, 52 kbit/s 106 kbit/s and 212 kbit/s demodulation.

The correlator has two main modes of operation - Manchester and BPSK (binary phase shift keying). Manchester refers to the Manchester code subcarrier modulation used in NFC-A 106 kbit/s and NFC-V single subcarrier protocols. BPSK refers to the subcarrier modulation used in the remaining protocols and data rates. In BPSK mode, the local subcarrier clock follows the phase of the input subcarrier signal. The bit information is coded into the phase of the input subcarrier, so a comparison between the input phase and clock phase returns the bit data. In Manchester mode, the local subcarrier clock does not follow the phase of the input subcarrier signal as the bit information is coded into subcarrier presence (amplitude). The correlator comprises an additional circuitry, used by both modes, for symbol recognition and subcarrier presence detection.

The iir_coef1 and iir_coef2 bits in the Correlator settings register 2 adjust the correlator internal filter.

5.4.5 Automatic gain control

The automatic gain control configures the gain reduction in the filter and gain stage to input an optimal signal into the correlator. It can be enabled in the Rx digital settings register 1 by setting the agc_en bit to 1. As long as the input signal is larger than the threshold defined by the agc_thr bits in the Correlator settings register 2, the gain is reduced in 3 dB steps. In reader operation, the AGC is only active at the start of reception. In card emulation operation, the AGC is operating during the reception when activated via the agc_en bit set to 1. There are two special cases where the AGC is behaving differently. In NFC-F CE reception, the AGC freezes after the subcarrier has been detected. In NFC-A reception, the AGC freezes when the bit ce_agc_freeze is set to 1. The result of the gain reduction after the AGC is complete can be read in the afe_gain bits of the Analog display register 2. It displays the actual gain reduction during the last reception.

5.4.6 Squelch

The squelch is reducing the receiver gain based on the noise level. Due to the high starting gain of the receiver, noise could be decoded and corrupt the communication between reader and card. The squelch enables the reception in noisy environments if the signal level is above the noise level.

Automatic squelch is enabled by the sq_en option bit in the Mask receive timer configuration register 1. It is activated automatically after the end of the transmission. The delay can be configured in the Mask receive timer configuration register 1 by setting the sq_del bits. The squelch is terminated when the mask receive timer (MRT) reaches the value defined in the Mask receive timer configuration register 2 or the squelch timer defined in the Squelch timer configuration register is expired.

This mode is primarily intended to suppress the noise generated by the tag processing before the tag response (covered by MRT) and environmental noise.

After the squelch time is expired, the determined gain setting is applied for the next reception.

The gain setting acquired by the squelch is cleared by sending a direct command clear Rx gain.

If the card response starts during the squelch, the gain is reduced to ignore the modulation. Such scenarios are happening, for example, during the ISO10373-6 EMD recovery tests.

5.4.7 RSSI

The RSSI is an indication of the estimated signal level at the input of the IC. It is used for diagnostic and observational purposes. The RSSI is calculated from the amplitude of the signal at the input of the correlator. The measurements take place in intervals that start when the receiver is enabled and end when the receiver is disabled. The information about the I and Q RSSI measurements is reset only when the receiver is opened for a valid reception (when issuing the rx_start interrupt) or when a direct command to clear the Rx gain is issued. The RSSI information can be read after a tag reply without any timing constraints. The result takes the AGC gain reduction into account. The result of the measurement can be read from the RSSI display register 1 and the RSSI display register 2.

5.4.8 Digitizing stage

The digitizing stage produces a digital representation of the subcarrier signal from the receiver. This digital signal is processed by the receiver framing logic.

5.4.9 ADC to CE memory recording

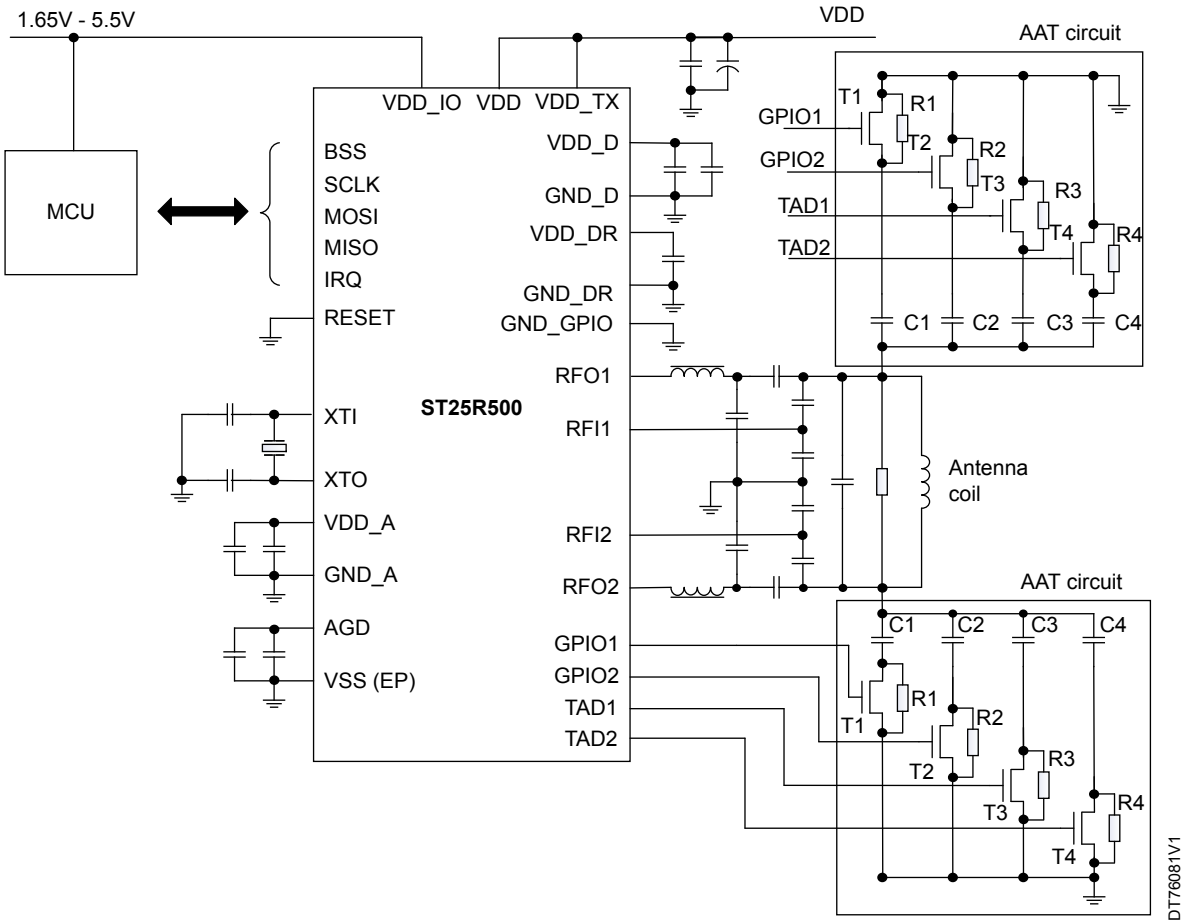
The envelope of the carrier signal can be sampled and stored in the card emulation memory. This feature can be used to measure the rising and falling edge of the modulation signal in reader operation. The feature can be enabled by setting the trigger to falling, rising, or both edges using the adc_cemem bit in the test register ADC to CE memory. The sampling rate can be selected by setting the bit adc_cemem_rate to 13.56 MHz or 6.78 MHz, which allows recording 3.83 µs or 7.67 µs.

The input source can be selected by setting the bit adc_cemem_src to ADC or correlator input. The input source ADC returns a 6-bit result which is saturated to a value of 63. The input source correlator returns an 8-bit result which is saturated to a value of 250. The input gain can be configured by the bits afe_gain_ce in the Rx analog settings register 3.

5.5 Antenna tuning

The ST25R500 supports antenna tuning through an external NMOS transistor and external multilayer ceramic capacitor (MLCC). The following figure shows the minimum configuration when using four tuning capacitors for each RFO channel. Per channel four NMOS transistor, four MLCC capacitor and four resistors are used.

Figure 8. Antenna tuning schematic



The external MLCC capacitors should be connected to the parallel capacitor on one side and to the drain of the NMOS transistor on the other side. The source of the NMOS transistor is connected to GND. Both the capacitor and the NMOS transistor are connected in parallel to the parallel capacitor of the matching network. By driving the gate of the transistor T1 to high the capacitor C1 is added in parallel to the parallel capacitor of the matching network. This causes a change of the resonance frequency of the NFC antenna. The R1 resistor is discharging the capacitor slowly if the NMOS transistor is high ohmic. The value of the resistor can be very high (~1 MΩ). The capacitors C1 to C4 are binary weighted. Typical values are 5.6 pF, 12 pF, 27 pF, and 56 pF, which allow increasing the parallel capacitor by 0pF to 100.6 pF in 16 steps. The values of C1 to C4 may be adapted based on the desired tuning range of AAT.

The gates of the NMOS transistors can be connected to the GPIO1, GPIO2, TAD1, and TAD2 pins. The pins need to be configured to push-pull configuration. By setting the gpio_en and tad_en bits to 1 in the CE modulation register 2, the push-pull mode is enabled.

The state of the push-pull output can be defined in the GPIO control register for reader operation and the card emulation operation. The outputs are automatically changed based on the GPIO control register content depending on if the reader is in for reader operation and card emulation operation.

5.6 RC oscillator

The RC oscillator is used to support the low-power WU mode and it runs at a nominal frequency of 26.48 kHz. It is enabled when the device enters the WU mode, and disabled when the device goes to PD or RD mode. Additionally, it may be enabled by executing the direct command to start the wake-up timer.

5.7 Quartz crystal oscillator

The quartz crystal oscillator operates at 27.12 MHz. This operation is enabled when the option bit en is set to 1.

An I_osc interrupt is sent to inform the microcontroller when the oscillator amplitude is sufficiently high, meaning that the frequency is stable. The oscillator is based on an inverter stage supplied by a controlled current source. A feedback loop controls the bias current to regulate the amplitude on XTI pin to approximately 1 V_{PP}. The amplitude of the XTI signal depends on the parameters of the crystal. Depending on these parameters, the XTI signal can be greater than 1 V_{PP} at the lowest possible drive level. It must be ensured that V_{OSC_PP} in the operating conditions table is not exceeded.

Division by two ensures that the 13.56 MHz signal has a duty cycle of 50%.

The oscillator is additionally enabled when the transition to RD mode is triggered in card emulation operation by detecting an external magnetic field or when the wake-up timer expires and a wake-up measurement is performed.

The status of the oscillator can be observed by checking the bit osc_ok. This bit is set to one when the oscillator frequency is stable.

5.8 Timers

The ST25R500 contains several timers, which eliminate the need to run counters in the controller, thus reducing the effort of the controller's code implementation and improve the portability of the code to different controllers.

Every timer has one or more associated configuration registers in which the timeout duration and different operating modes are defined. These configuration registers must be set while the corresponding timer is not running. Any modification of timer configuration while the timer is active may result in unpredictable behavior. All timers are stopped by the direct command stop all activities.

5.8.1 Mask receive timer (MRT)

In reader operation, this timer blocks the receiver and the reception process in the framing logic by keeping the rx_on signal low after the end of the Tx during the time the tag reply is not expected. While the mask receive timer is running, the squelch is automatically turned on when enabled. The MRT does not produce an IRQ.

The MRT timeout is configured in the Mask receive timer configuration register 2 and is automatically started at the end of the data transmission (at the end of EOF). The MRT can be triggered by the start mask receive timer direct command. In this case, the squelch is enabled according to the Squelch timer configuration register. The MRT also starts in the PD mode when card emulation operation is enabled. After the initiator field has been detected, the regulator, the crystal oscillator, the receiver, and the MRT are enabled. After the MRT expires, the receiver starts to detect the start of the initiator message.

5.8.2 No-response timer (NRT)

The purpose of this timer is to observe whether a response is detected during a configured time starting at the by end of the transmission. The I_nre flag in the IRQ status register 2 is signaling an interrupt event resulting from this timer timeout. The NRT value is defined by writing the NRT and GPT configuration register 2 and the NRT and GPT configuration register 3. Operation options are defined by setting the nrt_emv and nrt_step bits in the NRT and GPT configuration register 1. The NRT is automatically started at the end of the transmission. The nrt_step bit configures the time step of the no-response timer. Two steps are available, $64/f_C$ (4.72 µs) and $4096/f_C$ covering, respectively, the range up to 309 ms and up to 19.8 s. The nrt_emv bit controls the timer operation mode.

When this bit is set to 0 (default mode), the I_nre interrupt is produced if the NRT expires before a start of a response is detected. The rx_on bit is set low to disable the receiver. In the opposite case, when the start of a tag reply is detected before the timeout, the timer is stopped, and no IRQ is produced.

When this bit is set to 1, the timer unconditionally produces an IRQ when it expires. This means that the IRQ is independent from whether or not a tag reply was detected. When a tag reply is processed during a timeout, no other action is taken and the reply is normally received. In the opposite case, when no tag response is processed, the receiver is disabled.

The NRT can also be started using a start no-response timer direct command. The purpose of this command is to extend the no-response timer timeout beyond the range defined in the no-response timer control registers. If this command is sent while the timer is running, it is reset and restarted.

The NRT can be terminated using stop no-response timer or stop all activities direct command. The timer is terminated and no IRQ is sent. It is expected to be used in the nrt_emv mode, when the incoming reception does not stop the no-response timer.

5.8.3 General-purpose timer (GPT)

The GPT value is defined by writing the NRT and GPT configuration register 4 and the NRT and GPT configuration register 5. It can be used to survey the duration of the reception process (triggered by the start of reception, after SOF) or to time out the PCD to PICC response time (triggered by the end of reception, after EOF). The trigger source can be configured through the gptc bit in the NRT and GPT configuration register 1. The possible trigger configurations can be seen in Table 56. General purpose timer trigger source.

The GP timer can also be started by sending the start general-purpose timer direct command. If this command is sent while the timer is running, it is reset and restarted.

5.8.4 Wake-up timer (WUT)

This timer is primarily used in the wake-up mode.

It can also be triggered by sending the start WUT direct command. When this command is sent, the RC oscillator, which is used as the clock source for the wake-up timer, is started. When the timer expires, an IRQ with the I_wut flag is sent.

As the RC oscillator is the clock source for the WUT, it can run during PD mode. The other timers, which are based on the crystal oscillator, cannot be used in PD or WU mode.

Note: The tolerance of WUT is defined by the tolerance of the RC oscillator. During WU mode, a calibration mechanism can be enabled to compensate the RC inaccuracies, as detailed in Section 5.9.5: Wake-up timer calibration.

5.9 Wake-up mode

Once in PD mode, the wu_en bit sets the ST25R500 into wake-up mode (WU), which is used to perform low-power card detection. An integrated low-power 26.48 kHz RC oscillator and configurable wake-up timer (WUT) are used to trigger periodic measurements.

Usually, the presence of a card is detected by the RF/NFC polling. In this process, the reader field is periodically turned on, and the host checks whether a card is present using RF commands. This procedure consumes considerable energy since the reader emits a field for long periods before a command can be issued due to guard time fulfillment.

Low-power detection of card presence is performed by detecting a change in the reader environment, produced by an approaching detuning element. When a change is detected, an interrupt is sent to the host. The host can then perform the regular RF/NFC polling afterward.

In wake-up mode, the ST25R500 performs periodic measurements and sends an IRQ to the host when a difference to the configured reference value is detected.

The device monitors the I and Q channels to assess a variation in the antenna surroundings.

The latest measurement value is shown in i_adc and q_adc, and the current reference is defined on i_ref and q_ref. ADC values are provided in 8-bit signed values using two's complement representation. The delta/difference to the reference that triggers a wake-up interrupt is defined in i_diff and q_diff.

Besides periodic execution via the wake-up timer, the measurement and processing of the measured data can be triggered by the trigger wake-up event direct command. This mechanism allows synchronization with external events.

5.9.1 Card detection

The presence of a card close to the reader antenna coil produces a change of the antenna LC tank signal. The reader field activation time required to perform the measurement is extremely short, compared to the activation time required to send a protocol activation command.

The power level during the measurement can be lower than that during normal operation as the card does not have to be powered to produce a coupling effect. The emitted power can be configured by changing the RFO driver resistance.

An IRQ is sent when the difference between a measured value and reference value is larger than the configured delta/diff value. There are two possibilities how to define the reference value, controlled by the bit iq_aaref:

- The ST25R500 can automatically calculate the reference based on previous measurements (auto-averaging)
- The host determines the reference value and sets it on i_ref and q_ref

5.9.2 Automatic averaging

In case auto-averaging is enabled (iq_aaref = 1) the reference value is recalculated after every measurement. The last measurement value, the old reference value, and the weight are used in this calculation.

The following formula is used to calculate the new reference value:

new_reference = old_reference - (old_reference - measured_value) / weight

The i_iirqm and q_iirqm bits define whether a measurement that causes an interrupt is taken into account for the average value calculation.

The influence that the new measurement has over the reference can be configured by a weight defined in i_aaw and q_aaw bits.

5.9.3 Calibration

The wake-up mode has an additional calibration step that can be executed manually or automatically. The skip_cal and skip_recal bits control the automatic calibration behavior.

When starting the wake-up mode, if skip_cal = 0, a calibration step is performed automatically on the first WUT timeout.

While the wake-up mode is running and skip_recal = 0, if reference ± delta/diff is larger than 63, a recalibration is performed.

5.9.4 Wake-up IRQ

The device allows configuring the conditions when a wake-up IRQ is sent to the host.

This behavior is defined by i_tdi_en and q_tdi_en bits and the following three conditions can be used:

- I_wui/q IRQ when the latest measurement is above the upper limit: i/q_adc > i/q_ref + i/q_diff
- I_wui/q IRQ when the latest measurement is in between the upper and lower limit: i/q_ref – i/q_diff ≤ i/q_adc ≤ i/q_ref + i/q_diff
- I_wui/q IRQ when the latest measurement is below the lower limit: i/q_adc < i/q_ref - i/q_diff

If the bits i_tdi_en = 0, the I channel is not used during WU, and the same applies for the Q channel when q_tdi_en = 0.

During WU mode the ST25R500 produces additional IRQs that may be masked, or used for diagnostics:

- I_wut IRQ when the WUT timer expires, indicating that the device temporarily enables itself in RD mode and performs a measurement
- I_wutme IRQ when the device has concluded the WU measurement event, and goes back to WU mode

5.9.5 Wake-up timer calibration

The WUT uses the RC oscillator as its clock source. The RC oscillator is process and temperature dependent, which may result in a deviated WU period from the target defined by the wut bits. A wake-up timer duration of 100 ms ± 5ms can only be guaranteed with a wake-up timer calibration.

In applications where an accurate WU period is required, a calibration mechanism can be enabled to minimize the RC variations. It is not recommended to use the wake-up timer calibration on a wake-up timer period of less than 100 ms. When the WU mode is started, and WUT calibration is enabled by setting wut_cal = 1, the wake-up timer is calibrated based on the crystal oscillator.

Therefore, the crystal oscillator is kept enabled for a certain calibration duration. The calibration is executed in wake-up mode whenever the wake-up timer expires and the chip transitions from PD to RD mode. A longer calibration duration results in increased accuracy of the WUT period.

The calibration duration of the WUT calibration step is defined by the wut_cal_len bits.

The below table shows the calibration time and the achieved target accuracy based on the selected wut_cal_len.

Wut_cal_len <1:0>	Calibration duration (ms)	Target accuracy (%)
0	0.781	3.33
1	1.562	1.67
2	3.125	0.83
3	6.248	0.43

As an example, using a wut_cal_len = 0 and a wake-up timer period of 100 ms, the expected timer period is between 96.7 ms and 103.33 ms. Since this calibration is performed every time the wake-up timer expires, temperature and other effects are neglected. The calibration is based on the crystal quartz oscillator and is therefore dependent on its frequency. An accurate and stable oscillator frequency is mandatory for the calibration.

5.10 NFC WLC WPT monitor

NFC devices can transfer power via their magnetic field to other listener devices. NFC wireless charging (WLC) foresees two modes where the power transfer may take place: Static mode or negotiated mode.

In negotiated mode, during the wireless power transfer (WPT) phase, the wireless charging poller monitors the transfer and reacts upon certain events.

These events, defined by NFC Forum, include a foreign object detection (FOD) and WPT stop request.

ST25R500 supports WLC WPT monitoring and reports to the host when a FOD or stop pattern has been detected.

WPT monitoring shall take place after the negotiated power has been set, and for the time defined by the WPT duration.

While in RD mode (en = 1) and Tx enabled (tx_en = 1), the WLC WPT monitoring can be enabled by setting the wpt_en bit to 1 in the Operation register.

During this operation, periodic measurements are taken to monitor the WPT phase, and the sampling period is defined by the wut bits in the Wake-up control register 1.

Whenever the ST25R500 detects an impedance change (FOD) or the WPT-Stop condition, it informs the host via I_wpt_fod and I_ wpt_stop respectively.

The WPT monitoring operation is terminated by setting wpt_en = 0.

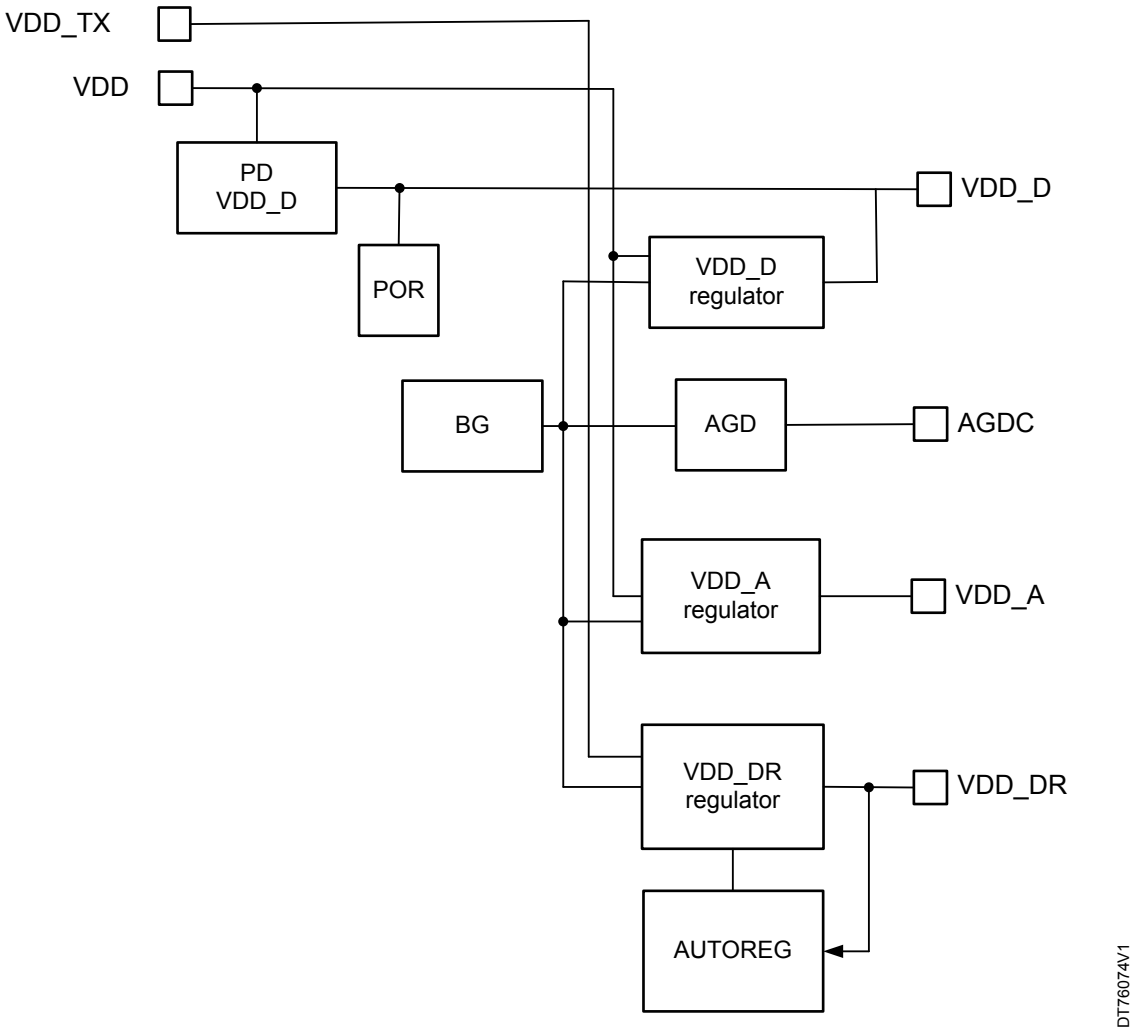
5.11 Power supply system

The ST25R500 features three positive supply pins, VDD, VDD_TX and VDD_IO:

- VDD is the main power supply pin. It supplies the ST25R500 blocks through two regulators (VDD_A, VDD_D)
- VDD_TX is the transmitter supply pin. It supplies the transmitter via the VDD_DR regulator. VDD / VDD_TX range from 2.7 to 5.5 V is supported. VDD and VDD_TX must be connected to the same power supply.
- VDD_IO is used to define supply level for the digital communication pins (BSS, MISO, MOSI, SCLK, IRQ, MCU_CLK). Digital communication pins interface to the ST25R500 logic through level shifters, therefore the internal supply voltage can be lower than VDD_IO. VDD_IO range from 1.65 to 5.5 V is supported.

The following figure details the building blocks of the ST25R500 power supply system.

Figure 9. Power supply system



Note:
- *BG: Bandgap reference*
- *AUTOREG: Automatic regulator adjustment*

The power supply system contains three regulators, a power-down support block (POR), a block generating the analog reference voltage (AGD) and a block performing the automatic power supply adjustment procedure. The three regulators provide supply to the analog (VDD_A), logic (VDD_D), and the transmitter (VDD_DR) blocks. VDD_D, VDD_DR, and VDD_A pins are not intended for supplying power to the chip. The VDD_A, VDD_D, and VDD_DR regulators must be used for supplying power to the chip.

A decoupling capacitor pair of 10 nF in parallel with 2.2 µF must be connected to the V_{DD} and V_{DD_TX} supply, shown in Figure 3. Minimum system configuration.

The decoupling capacitors should be placed close to the VDD_TX pin. The PCB trace between the VDD_TX pin and the decoupling capacitor should not be longer than 3 mm, with no vias in between. The trace width should be wider than 0.25 mm. Another decoupling capacitor pair is recommended to be placed at the VDD pin.

5.11.1 Power-down block

In the power-down mode, the regulators are disabled to save power. In this mode, a low-power power-down support block maintains the VDD_D voltage level.

5.11.2 VDD_A regulator

The VDD_A regulator supplies the analog part of the receiver and the crystal oscillator. Its nominal voltage is 3.0 V. Below 3.0 V output voltage, the VDD_A regulator follows the VDD_DR voltage setting. A decoupling capacitor pair of 10 nF in parallel with 2.2 µF must be connected and placed close to the IC with good connectivity to the positive and negative supply pins of VDD_A. The 10nF decoupling capacitor should be placed as close as possible to the positive and negative supply pins.

5.11.3 VDD_D regulator

The VDD_D regulator supplies the digital logic. Its nominal voltage is 1.15 V. A decoupling capacitor pair of 10 nF in parallel with 2.2 µF must be connected and placed close to the IC with good connectivity to the positive and negative supply pins of VDD_D. The 10nF decoupling capacitor should be placed as close as possible to the positive and negative supply pins.

5.11.4 VDD_DR regulator

The VDD_DR regulator is supplying the TX driver via the VDD_TX pin. The decoupling capacitor connected to the VDD_DR pin should be 47 nF. The decoupling capacitor should be placed as close as possible to the positive and negative supply pins. To avoid oscillations on the output this decoupling capacitor should be directly connected with the shortest possible traces to the VDD_DR and GND_DR pin. Its LDO dropout voltage can be configured between 200 mV and 550 mV using the regd bits in the Tx driver configuration register. The LDO drop is based on the IC internal measurement thus the VDD_DR voltage measured outside of the IC, at its pins, can vary.

The regulator can also be configured to an absolute voltage. The reg_s bit in the VDD_DR regulator configuration register switches between the automatic adjustment based on the configured LDO drop (reg_s = 0) and the manual one defined by an absolute voltage. The absolute voltage can be configured by setting reg_s bit set to one and configuring rege bits according to Table 13. Regulated voltages.

The regulator features an internal current limiter. The limiter threshold is set above the 500mA current limit. Its threshold is dependent on internal mechanisms to achieve the maximum output current without damaging the ST25R500. When the current limiter is operating, the i_lim bit in the Analog display register 1 is set. Although the limiter is active, the ST25R500 can still operate normally for a short period of time. As a result of the limiter being active, the VDD_DR voltage is being reduced. Nevertheless, the device should be designed not to exceed the limits specified in the absolute maximum ratings section.

Besides the definition of a static voltage in unmodulated state, the VDD_DR regulator is used to generate AM modulation and shaping of the OOK modulation in modulated state.

Further details about the shaping of the modulation signal can be found in Section 5.12: Active wave shaping.

5.12 Active wave shaping

The ST25R500 supports active wave shaping of the modulation signal. The supported modes of operations are

- Field on and off transitions
- OOK modulation
- AM modulation

During the OOK modulation, the driver is stopped during the modulated state (also called pause). When in AM modulation operation, the driver switches between two voltage levels.

The device supports two AM modulation methods which can be combined with each other:

- Resistance am modulation (res_am)
- Regulator shaped modulation (rgs_am)

Both can be enabled in the Tx modulation register 1. When using the regulator shape modulation, the VDD_DR voltage level changes between the modulated and the unmodulated voltage level (modulation state change). The unmodulated voltage level is defined by the am_mod bits. The transition between the modulated and the unmodulated voltage level follows an exponential filter curve. The time constant of this filter curve can be modified for the falling and rising edge of the modulation signal individually. The filter can be modified in the AWS configuration register 2 by setting the am_fall and am_rise bits. The value of the filter should be in conjunction with the Q-factor of the reader antenna. A too high value can cause non-standard compliant wave shape timings. For example ISO/IEC 14443-2 t3 and t4 could be too slow. A too low value could cause over- or undershoots. The filter curve defined by am_fall and am_rise bits is generated by an RC network inside of the ST25R500. By enabling the dig_aws_en bit, the same signal is generated by a digital logic, reducing the device to device variation.

The resistive am modulation (res_am) allows switching between the unmodulated driver resistance (d_res) and the modulated driver resistance (md_res). The switch between d_res to md_res is occurring at the modulation state change after a certain number of carrier clock cycles defined in the tdres1 (falling edge) and tdres2 (rising edge) bits. The tdres1 bits can be configured in the AWS timing register 1, the tdres2 bits can be configured in the AWS timing register 3.

When res_am is used in combination with OOK modulation (tr_am=0), then the driver is being stopped after a certain number of carrier cycles defined in tentx1 bits. The tentx1 bits can be configured in the AWS timing register 1. The usage of tentx1 different from 0 can be beneficial when enabling also rgs_am in the OOK modulation scheme.

The ST25R500 also features two voltage sinking mechanisms.

- Dynamic passive sink
- Active sink

The voltage sink is used to reduce the energy stored in the VDD_DR decoupling capacitor while transitioning from the modulated state to the unmodulated state. The sinks can only be enabled when the regulator is used for shaping (rgs_am = 1).

The dynamic passive sink is enabled during the modulated state. It is drawing an additional continuous current during the modulation. This sink can be activated in combination with very high ohmic matchings to reduce the energy stored in the VDD_DR capacitor. It can be delayed by a certain number of carrier cycles by setting the tpasssinkx1 (falling edge modulation signal) and tpasssinkx2 (rising edge of the modulation signal) bits. The tpasssinkx1 bits can be configured in the AWS timing register 2 and the tpasssinkx2 bits can be configured in the AWS timing register 4.

The active sink can be enabled by setting the act_sink_en bit to 1 in the AWS configuration register 1. In addition, the offset measurement must be enabled by setting the sink_offset_en and dyn_sink_offset bits in the AWS configuration register 1 to 1. This configuration enables the active sink during the modulation pulse. It is only drawing additional current out of the VDD_DR capacitor, if the VDD_DR voltage is above the offset. The offset is following the reference signal defined by am_fall and am_rise. Using the bits tsinkoff1 in AWS timing register 2 and tsinkoff2 in the AWS timing register 4 can delay the operation of the active sink after the modulation state change. It is recommended to keep tsinkoff1 and tsinkoff2 at a value of 0 for accurate shaping of the modulation pulse during the complete modulation pulse.

The internal current limiter can be temporarily disabled during the modulation by setting the bit dyn_ilim_aws = 1. Due to the active and passive sink, the current consumption could increase during the modulation of the carrier. It is recommended to activate the internal short circuit protection by setting the sc_prot_en bit to 1. Both bits can be found in the AWS configuration register 1.

Additional overshoots or undershoots can be reduces by configuring the over- and undershoot protection. The bit pattern can be defined using the bits ov_pattern defined in the Overshoot protection register and un_pattern defined in the undershoot protection register. To enable the over- and undershoot protection both bits, ov_pattern and un_pattern must be different from 0 and res_am = 1. The driver then switches from d_res to md_res during the configured carrier cycles after the modulation state change.

5.13 Reader operation

The ready mode must be entered by setting the en bit in the Operation register. In this mode the oscillator is started and the regulators are enabled. When the oscillator operation is stable, the I_osc interrupt is sent, and the osc_ok bit indicates it.

The operation mode and data rate must then be configured by writing to the Tx protocol register 1 and the Tx protocol register 2. The receiver and transmitter operation options related to operation mode must be defined too. If the selected operation mode uses AM modulation for the reader-to-tag communication, the modulation depth must be configured.

Before sending any command to a card, the VDD_DR regulator must be enabled by setting the vdddr_en bit and waiting 10 µs. Then, the transmitter and the receiver must be enabled by setting the rx_en and tx_en bits. A guard time for each technology is defined by the NFC standards (for example 5 ms for ISO/IEC 14443) requiring that the reader field must be turned on for some time before the first command is sent. A general-purpose timer can be used to count this time or NFC field on command with a defined time by the NFC field on guard timer register.

Preparation and execution of a transceiver sequence:

- Execute the stop all activities direct command
- Execute the Clear Rx gain direct command
- Configure the timers accordingly

- Define the number of transmitted bytes in the Tx frame configuration register 1 and Tx frame configuration register 2
- Write the bytes to be transmitted in the FIFO
- Send the transmit data or the transmit next slot (NFC-V) direct command

When all the data is transmitted, the I_txe interrupt is generated to inform the microcontroller that the transmission is finished (IRQ due to the end of transmission)

After the transmission is executed, the ST25R500 receiver automatically starts to observe the RFI inputs to detect a card response. The RSSI monitoring and AGC (if enabled) are started. The framing block processes the subcarrier signal from the receiver and fills the FIFO with data. When the reception is finished, and all the data is in the FIFO, the I_rxe interrupt is sent to the microcontroller (IRQ due to end of receive), and the FIFO status register 1 and FIFO status register 2 display the number of bytes in the FIFO so the microcontroller can proceed with the data download.

If an error or a collision bit are detected during reception, the I_rxe interrupt with the appropriate flag is sent, and the microcontroller can take appropriate action.

When the data packet is longer than the FIFO size, the above mentioned procedure changes.

The FIFO is prepared with the data before the transmission starts. The I_wl interrupt is sent during the transmission to signal when the remaining number of bytes is lower than the water level (IRQ due to FIFO water level). The microcontroller then adds more data in the FIFO. When all the data are transmitted the I_txe interrupt is sent to inform the microcontroller that the transmission is finished.

The situation during the reception is similar. When the FIFO is loaded with more data than the received water level, the I_wl interrupt is sent, and the microcontroller reads the data from the FIFO. When the reception is finished, the I_txe interrupt is sent to the microcontroller (IRQ due to end of receive) the FIFO status register 1 and FIFO status register 2 display the number of the bytes in the FIFO still to be read.

5.14 Card emulation operation

The ST25R500 CE operation is activated by setting the ce_en bit in the Operation register. There are various target or listening modes implemented depending on the setting of the om bits, refer to Table 40. Operation modes.

The device supports:

- PICC type A according to ISO/IEC 14443.
- NFCIP-1 passive target in bitrates $f_C/128$, $f_C/64$, and $f_C/32$
- NFC Forum listen mode NFC-A and NFC-F

Active target and active communication mode are not supported.

There are various options available, including bitrate detection, automatic responses, and power savings, which are described below.

5.14.1 Low-power field detection

The external field detector is enabled by setting ce_en = 1. The power consumption of the application can be optimized by starting the card emulation from the PD mode (en = 0) while waiting for an external field from a peer/reader.

Upon detection of an external field (I_eon), the ST25R500 temporarily enables the oscillator and the receiver. The host can confirm it by setting the en and rx_en option bits in Table 37. Protocol register 1. From this point on, either bit rate detection or fixed CE communication can be performed.

This temporary enable of the oscillator can be observed with the tmp_on bit in Table 90. Static status register 1. Oscillator gets disabled on field off (I_eof) and tmp_on goes to 0.

The external field detector (EFD) is automatically enabled when in CE mode (ce_en = 1) and during the execution of the NFC field on command. The status of the EFD can be observed through the bit efd_on, and when the EFD is active (efd_on = 1), its output can be monitored by the bit efd_out. EFD activation (efd_at<3:0>) and deactivation (efd_dt<3:0>) thresholds can be configured individually in the external field detector register.

5.14.2 Fixed card emulation

Fixed communication mode is active when one of the target modes with om = 1 or om=3 is selected. ST25R500 only receives and answers in the selected technology.

5.14.3 Bit rate detection

The card emulation can also be started from the bit rate detection mode. There are three different modes selectable by om in protocol register 1.

In these modes, the ST25R500 accepts frames in different technologies for at least the first frame.

Once the reception of the first frame starts, the bit rate detection mode signals an I_nfct interrupt, indicating that the bit rate has been identified and the host can retrieve the related information by reading nfc_rate on card emulation status register 1.

When the first frame has been fully received, the host can exit the bit rate detection mode by setting the corresponding mode on om bits in the protocol definition register to the corresponding fixed listen communication mode.

The difference between the om = 0xD, 0xE, and 0xF is the conditions when it gets rearmed:

- All modes re-arm bit rate detection on setting om to 0x0 and back to a bit rate mode.
- Singe bit rate detection (0xE) rearms additionally on field reset.
- Normal bit rate detection (0xF) rearms additionally on field reset and when bit ce_state moves to the IDLE state.

5.14.4 CE communication

Communication can be performed by the host (through FIFO) or by using automatic responses as detailed in the CE configuration register 1.

These automatic responses can include for NFC-A, the complete collision resolution including SEL_RES and SAK.

For NFC-F, only the SENSF_REQ is handled by sending SENSF_RES.

To enable slow hosts to perform emulation of T4T, handling of higher commands such as RATS, SLP_REQ, and S(DESELECT) can be enabled (not fully standard compliant, CID = 15 handling).

When receiving automatically handled frames, the ST25R500 signals this by sending I_rxe_cea instead of normal I_rxe interrupts.

While in card emulation, the state machine moves through a limited set of states corresponding to NFC Forum activity. These states can be observed in the Card emulation status register 1.

The ce_state in the same register can also be written by the host to move the state machine to for example SLEEP_A mode after the reception of a directly received SLP_REQ.

The content of the automatic responses is defined by the content of CE memory.

5.14.5 CE memory

The CE memory is used to store data for NFC-A (0x58) and NFC-F (0x5A) automatic card responses.

Table 3. CE memory address space

Location	Description	Data usage	Comment
0-6	NFCID1(4/7)	4 bytes: locations 0-3 7 bytes: locations 0-6	NFC-A
7,8	SENS_RES2:1	SENS_RES (ATQA)	
9	SEL_RES CL1	Response to SEL_REQ(SAK) CL1	
10	SEL_RES CL2	Response to SEL_REQ(SAK) CL2	
11-30	ATS	Response to RATS, first byte is length (TL)	
31,32	NFC_SC	Additional System code (SC) besides FFFFh in SENSF_REQ to which the device answers	NFC-F
33-51	SENSF_RES	Response to SENSF_REQ, last two bytes may not be transmitted based on RC in SENSF_REQ	

5.15 Host interface

5.15.1 Communication with an external microcontroller

The device communicates with a microcontroller through SPI where it acts as a target device, relying on the microcontroller to initiate all communication.

To notify the microcontroller of completed commands or external events, the device signals an interrupt on the IRQ pin.

A RESET pin is available to reset the device logic and put the device registers to the default state.

5.15.2 Interrupt interface

There are three interrupt registers implemented in the device. When an interrupt condition is met, the source of the interrupt bit is set and the IRQ pin transitions to high.

The microcontroller can read the interrupt registers to distinguish between different interrupt sources. After a particular interrupt register is read, its content is reset to 0.

Note: There can be more than one interrupt bit set if the microcontroller does not immediately read the interrupt registers after the IRQ signal is set and another event causing an interrupt occurs. In this case, the IRQ pin transitions to low after the last bit causing the interrupt is read.

If an interrupt from a certain source is not required, it can be disabled by setting the corresponding bit in the mask interrupt registers. In the case of masking a certain interrupt source the IRQ line is not set high, but the interrupt status bit is still set in the IRQ status registers.

By reading the IRQ status registers the masked interrupt bits are also retrieved and cleared.

In case an interrupt is masked and set to high due to a previous IRQ event and then the host unmasks this IRQ source, the IRQ line is immediately set to high. This notifies the host system that there are some interrupt events not yet read out.

5.15.2.1 *Serial peripheral interface (SPI)*

The device has a standard SPI with clock polarity of 0, a clock phase of 1, and an active low target select signal. SPI speeds up to 10 Mbit/s are supported. The communication starts with the controller pulling BSS low. The MOSI pin is sampled on the falling edge of SCLK, and the state of the MISO pin is updated on the rising edge of the SCLK signal. Data is transferred byte-wise, the most significant bit first. Read and write commands support an address auto increment to reduce communication time.

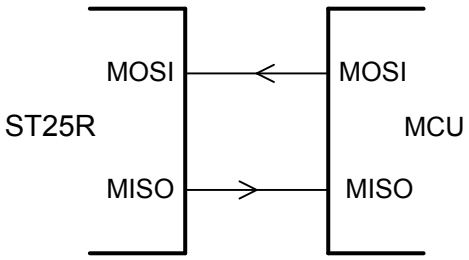
Table 4. SPI signal lines

Name	Signal	Signal Level	Description
BSS	Digital input	CMOS	SPI enable (active low)
MOSI	Digital input	CMOS	Serial data input
SCLK	Digital input	CMOS	Clock for serial communication
MISO	Digital output with tristate	CMOS	Serial data output

MISO output is mostly in a tristate condition and is only driven when output data is available.

While the MISO output is in a tristate condition, it is possible to switch on a 10 kΩ internal pull-down resistor by activating the option bits miso_pd1 and miso_pd2 in the General configuration register.

Figure 10. SPI data signals with a host



The following addressing scheme is used:

- Bit 7 indicates the direction of the operation (0-Write /1-Read)
- 88 addressable registers (0x00 - 0x57)
- 32 command codes (0x60 - 0xF9)
- FIFO access (0x5F)
- Test register access (0xFC)
- CE memory access (0x58)

Table 5. SPI operation modes

Mode	Mode pattern (com. bits)								Related data
	R/W	B6	B5	B4	B3	B2	B1	B0	
Register write	0	A6	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing) A<6:0> = 0x57 max
Register read	1	A6	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing) A<6:0> = 0x57 max
Commands	C7	1	1	C4	C3	C2	C1	C0	-
Test	1	1	1	1	1	1	0	0	Address and data byte (or more bytes in case of auto incrementing)
CE memory write	0	1	0	1	1	0	0	0	Write CE memory
CE memory read	1	1	0	1	1	0	0	0	Read CE memory

Mode	Mode pattern (com. bits)								Related data
	R/W	B6	B5	B4	B3	B2	B1	B0	
FIFO write	0	1	0	1	1	1	1	1	One or more bytes of FIFO data
FIFO read	1	1	0	1	1	1	1	1	One or more bytes of FIFO data

5.15.2.2 *Writing of data to addressable registers (write mode)*

The following figures show cases of writing a single byte and writing multiple bytes with an auto-incrementing address. After the SPI operation direction bit, the address of the register to be written is provided. Then one or more data bytes are transferred from the SPI, always from the MSB to the LSB. The data byte is written in a register on falling edge of its last clock.

Figure 11. SPI communication: writing of single byte

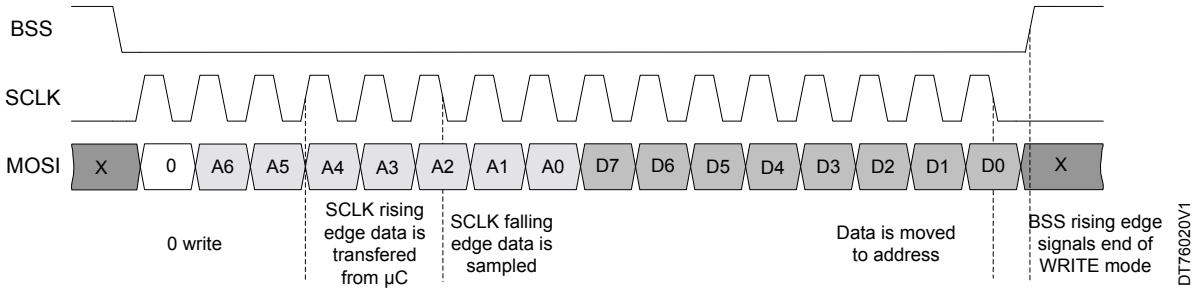
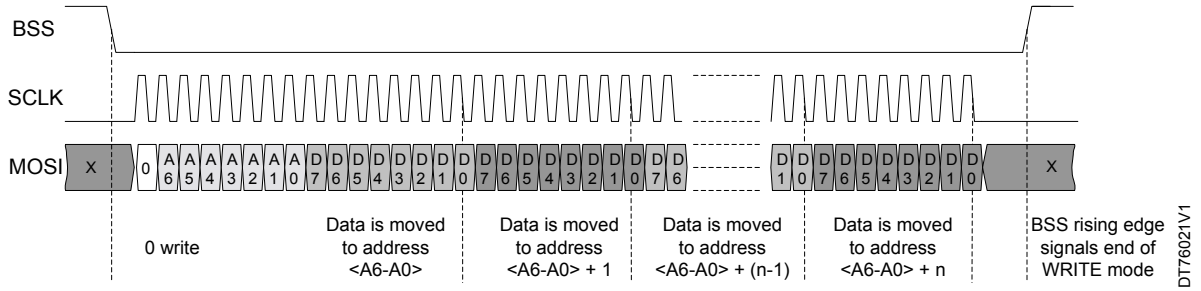


Figure 12. SPI communication: writing of multiple bytes



5.15.2.3 *Reading of data from addressable registers (read mode)*

After the SPI operation direction bit, the address of the register to be read must be provided from the MSB to the LSB. Then one or more data bytes are transferred to the MISO output, always from the MSB to the LSB. Analogous to the write mode, also the read mode supports auto-incrementing address.

MOSI is sampled at the falling edge of SCLK (as shown in Figure 13 and Figure 14), data to be read from the device internal register is driven to MISO pin on the rising edge of SCLK and is sampled by the controller at the falling edge of SCLK.

Figure 13. SPI communication: reading of single byte

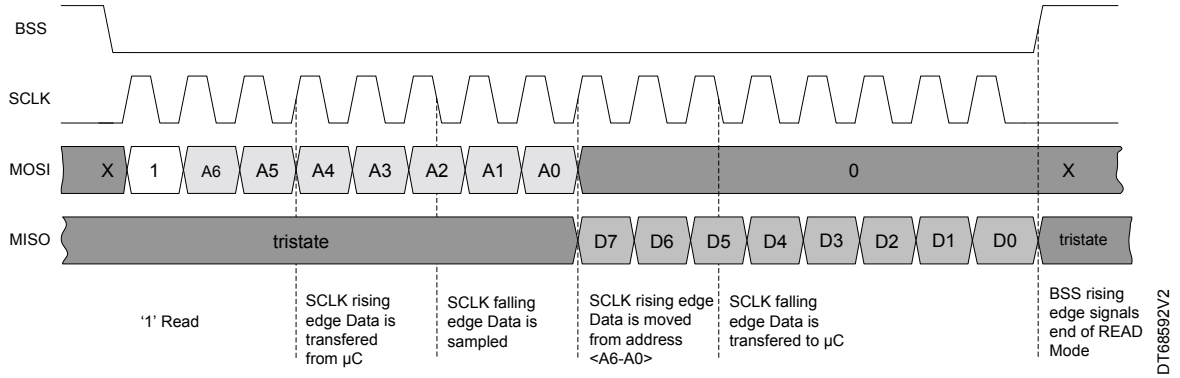
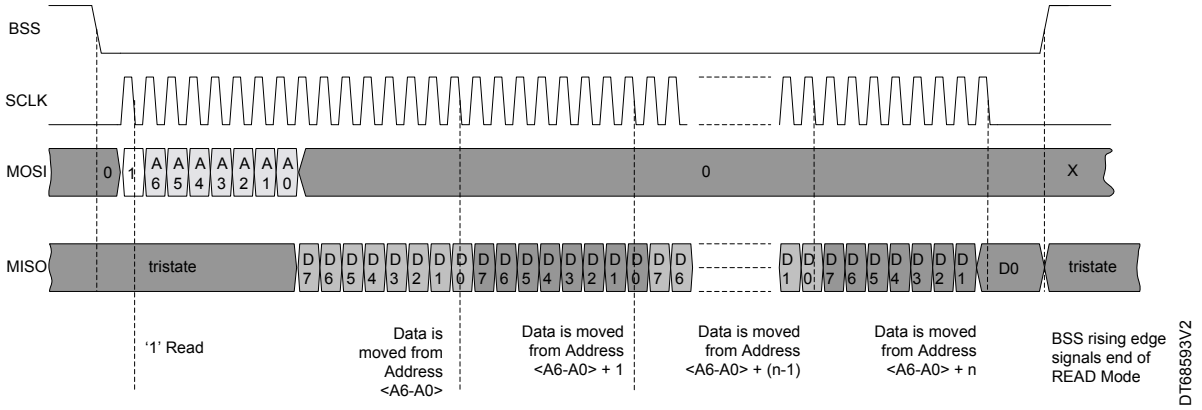


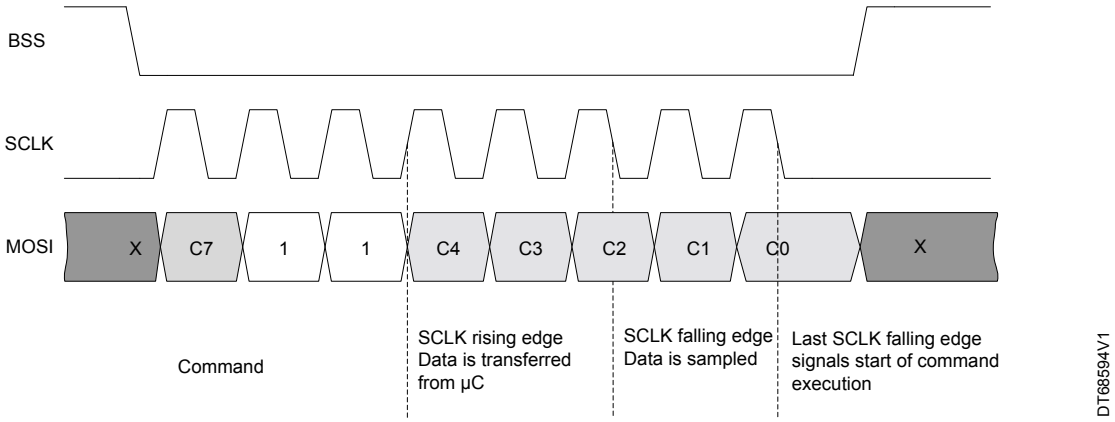
Figure 14. SPI communication: reading of multiple bytes



5.15.2.4 *Direct command mode*

The direct command mode has no additional data apart from the command code itself, therefore a single byte is sent MSB first. Execution of the direct command starts after the last clock.

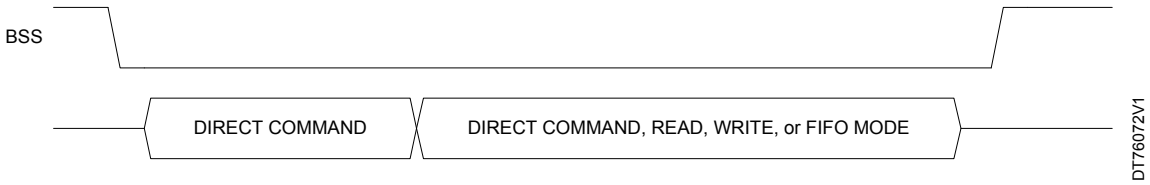
Figure 15. SPI communication: direct command



While the execution of some direct commands is immediate, others start a process of a certain duration, for example, calibration or measurements. During the execution of such commands, it is not allowed to start another activity over the SPI. An IRQ is sent when the execution has terminated.

Direct commands with immediate execution can be followed by another SPI mode (direct command, read, write, or FIFO) without deactivating the BSS signal in between.

Figure 16. SPI communication: direct command chaining



5.15.2.5 *FIFO mode*

Reading the received data from the FIFO is similar to reading the data from the addressable registers. Read and write operations are performed by accessing the address 0x5F.

Figure 17. SPI communication: writing bytes into FIFO

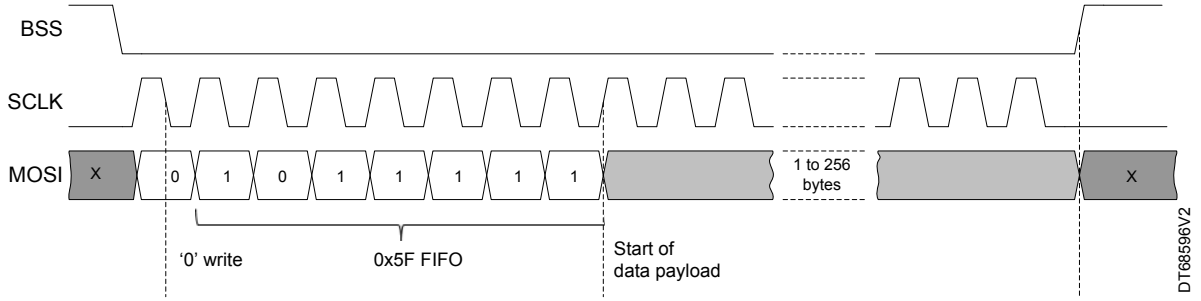
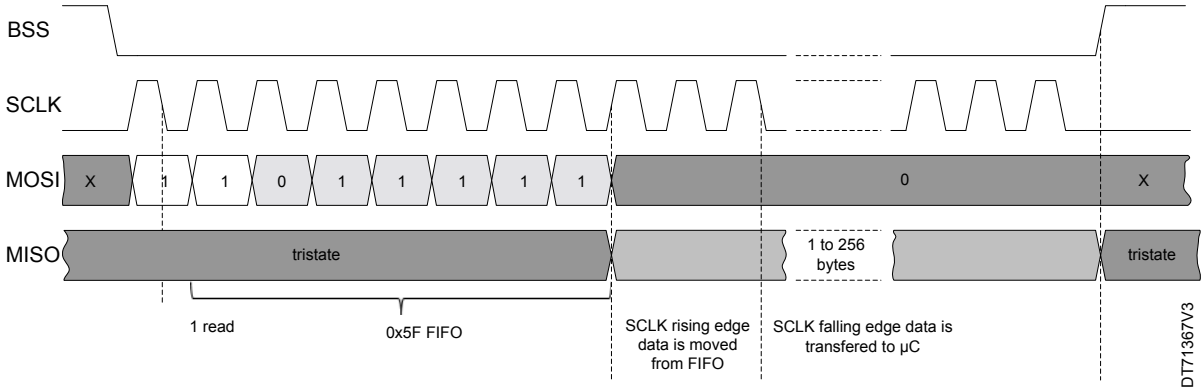


Figure 18. SPI communication: reading bytes from FIFO



5.16 Direct commands

Table 6. Direct commands

Code (hex)[1]	Command	Comments	Operation mode	I_dct after termination
60, 61	Set default	Puts the device into a power-up state	RD or PD	No
62, 63	Stop all activities	Stops all activities: transmission, reception, direct commands execution, timers, clears FIFO, collision, and IRQ status	RD	No
64, 65	Clear FIFO	Clears FIFO and collision status	RD	No
66, 67	Clear Rx Gain	Clears the current squelch setting and loads the manual gain reduction from the register	RD	No
68, 69	Adjust regulators	Adjusts supply regulators according to the current supply voltage level	RD	Yes
6A, 6B	Transmit data	Starts a data transmit sequence	RD	No
6C, 6D	Transmit next slot	Transmits an ISO15693 EOF; Single modulation pulse	RD	No
6E, 6F	NFC field on	Performs initial RF collision avoidance and field-on	RD	Yes
70, 71	Mask receive data	Masks the receiver; Incoming data after this command is ignored	RD	No
72, 73	Unmask receive data	Unmasks the receiver; Incoming data after this command is normally processed	RD	No
74, 75	Calibrate WU measurement	Calibrates the WU measurement	RD or PD	Yes
76, 77	Clear WU calibration	Clears previous calibration data	RD or PD	No
78, 79	WU measurement	The I and Q components of the RFI signal are measured similarly as in WU mode	RD or PD	Yes
7A, 7B	I/Q measurement	The I and Q components of the RFI signal are measured, with or without the transmitter enabled	RD	Yes
7C, 7D	Sense RF	Senses RF signal presence on RFI inputs, with or without the transmitter enabled	RD	Yes
7E, 7F	Trigger wake-up event	Triggers event that is normally triggered by WU timer in WU mode	PD	Yes
E2, E3	Start GPT	Manually starts the general-purpose timer	RD	No
E4, E5	Start WUT	Manually starts the wake-up timer	PD or RD	No
E6, E7	Start MRT	Manually starts the mask receive timer	RD	No
E8, E9	Start NRT	Manually starts the no response timer	RD	No
EA, EB	Stop NRT	Manually stops the no response timer	RD	No
EE, EF	Calibrate RC	Calibrate AWS time constant	RD	No
F8, F9	Trigger diagnostic measurement	-	RD	Yes
FC	Test register access	Enable access to test registers	PD or RD	No

1. *The command codes not explicitly listed in this table can't be used.*

5.16.1 Set default

This direct command puts the device in the same state as power-up initialization:

- Performs stop all activities direct command
- Sets all registers to default state
- Clears IRQ line and IRQ status bits
- Clears collision bits

5.16.2 Stop all activities

This direct command:

- Performs a Clear FIFO command direct command
- Stops data transmission and reception
- Stops all timers
- Clears IRQ line and IRQ status bits
- Terminates NFC Field on command (but does not switch off the field, if already on, due to command or earlier)

The command does not switch off the field in reader writer operation.

In CE operation, the reception is interrupted and re-enabled. This command is accepted in RD mode when the en bit is set and the oscillator frequency is stable osc_ok=1.

Direct command chaining can be used with this command.

5.16.3 Clear FIFO

This direct command clears the FIFO and the FIFO status registers. It does not clear the IRQ line or IRQ status bits. To prepare a transmission, send this command first before writing data into the FIFO. If a clear FIFO command is sent during an ongoing data transmission, then the data transmission is aborted, and FIFO status registers are cleared.

Direct command chaining can be used with this command.

5.16.4 Clear Rx gain

This command initializes the AGC and squelch. Sending this command stops squelch operation, in case it is going on, and clears the current squelch setting and loads the manual gain reduction as in afe_gain_rw

Direct command chaining can be used with this command.

5.16.5 Adjust regulators

The system can adjust the VDD_DR and VDD_A regulator voltage drop as defined in the regd bits. Using this method, the power supply rejection is optimized and the maximum available driver supply is used.

The command starts with the maximal target voltage setting and decreases the target until the configured voltage drop in the regulator is reached.

Before the command is triggered, the tx_en and rx_en bits should be enabled, to perform the adjustment at realistic load conditions.

Command is accepted in PD or RD mode when reg_s = 0.

5.16.6 Transmit data

Transmit data command is accepted if the transmitter is enabled (the tx_en bit is set) or the device is in card emulation operation (the ce_en bit is set).

Before sending the transmit data command, the clear FIFO direct command must be sent, followed by the definition of the number of transmitted bytes and by writing data to be transmitted in the FIFO.

The a_tx_par, tx_crc, f_tx_len, b_tx_sof_0, b_tx_sof_1, b_tx_eof and b_tx_half bits have an impact on the transmitted data. For example, CRC or parity bits are added.

The I_txe IRQ is signaled after the transmit command has been finished.

5.16.7 Transmit next slot

Transmit next slot command is accepted in case the transmitter is enabled (tx_en bit is set).

For the transmit next slot direct command, the ISO 15693 mode is set and it is not necessary to send the clear FIFO direct command before as the FIFO is not used.

At the end of the transmission an I_txe interrupt is produced, and the device moves into the reception mode.

5.16.8 NFC field on

The NFC field on direct command is used to perform the RF collision avoidance. The external field detector is activated (efd_on = 1) for this commands to work correctly. The collision avoidance threshold defined in the efd_at bits is used to observe the RFI input voltage and to determine whether there is some other device, which is emitting the 13.56 MHz field, close to the antenna.

If no external field is detected, then the ST25R500 transmitter is switched on automatically (the tx_en bit in the Operation register is set) and an I_dct IRQ is signaled. After the RF, the guard time (t_{IRFG}) defined in the GP timer register (gptc) has passed an I_gpe IRQ is signaled. At this point the controller can initiate a data transmission using a transmit command.

Figure 19. Direct command NFC field on (no RF collision)

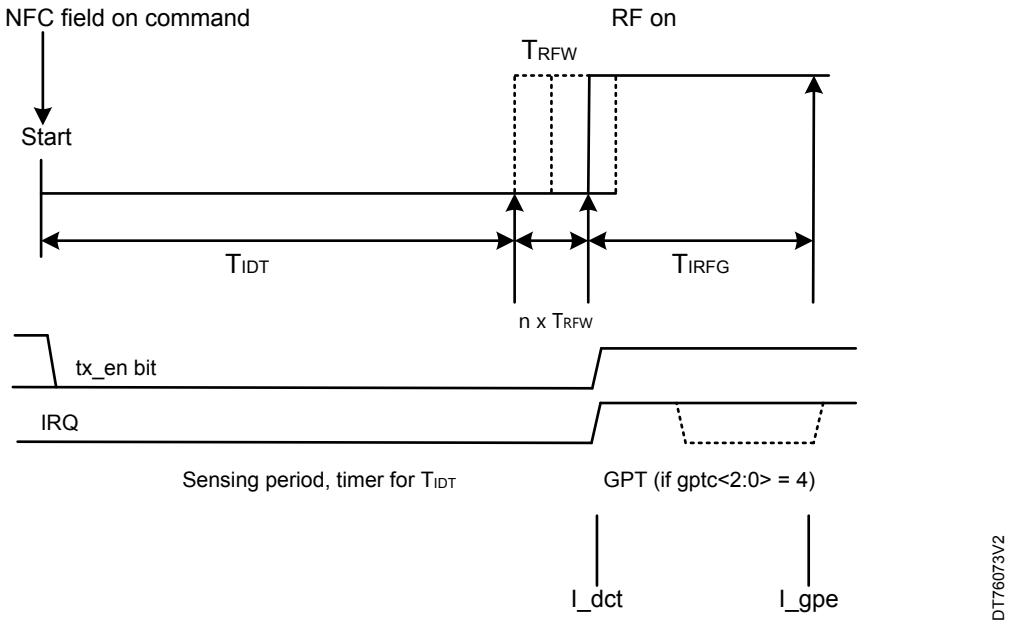


Table 7. Timing parameters of NFC field on commands

Parameter	Symbol	Value	Unit	Note
Initial delay time	T_{IDT}	4096	$1/f_C$	NFC initial field ON (302 µs)
RF waiting time	T_{RFW}	512	$1/f_C$	n = 0…3 (0...3 x 37.8 µs)
Initial guard time	T_{IRFG}	GPT	N/A	GPT timer

If the external field is detected the field is not switched on automatically (bit tx_en = 0) and IRQ with I_dct is sent. In such a case a transmission cannot be performed, the NFC Field on command must be repeated as long as the collision is not detected anymore.

The NFC initial field on command performs initial collision avoidance according to the NFCIP-1 standard. The number n is defined by bits nfc_n in the General configuration register.

5.16.9 Mask receive data

After the mask receive data direct command, the receiver output and the receive data framing block are disabled. This command is useful to mask the receiver and receive framing from processing the data when there is no input signal expected and only noise would be processed (for example in cases where a card processing time after receiving a command from the reader is long).

Direct command chaining can be used with this command.

5.16.10 Unmask receive data

The unmask receive data direct command is enabling normal processing of the received data by enabling the received data framing block. A common use of this command is to enable again the receiver operation after it was masked by the mask receive data command. In case the mask receive timer is running while the unmask receive data command is received, the reception is enabled, the mask receive timer is reset.

Direct command chaining can be used with this command.

5.16.11 Calibrate WU measurement

The command calibrates the wake-up mechanism to optimize the ADC input signal. The calibration value is visible in the I-channel WU calibration register and the Q-channel WU calibration register.

The command is automatically executed when enabling wake-up operation or if the input signal of the ADC drifts too far from the optimal area.

If the ST25R500 is in PD mode, it first temporarily enables the oscillator. After the oscillator is stable, the field is temporarily turned on, and the calibration is executed.

5.16.12 Clear WU calibration

The clear WU calibration direct command clears the previously obtained calibration data. The ADC calibration is reset to the default value.

This command must be used prior to the I/Q measurement or the amplitude measurement in case one wants to do the measurement without previous calibration. This enables approximate absolute measurement, but for a decreased resolution.

5.16.13 WU measurement

This command performs the wake-up measurement. It is automatically executed at each wake-up timer expiration in wake-up mode.

It can be triggered manually and is accepted from RD and PD mode.

If the IC is in PD mode, it first temporarily enables the oscillator and waits for the oscillator to be stable. Afterward, the field is temporarily enabled, and the measurement is performed.

If the IC is in RD mode, it only temporarily enables the field and then performs the measurement.

5.16.14 I/Q measurement and sense RF

These commands allow the user to measure the I and Q components of the RFI signal, whether it is measured at an external or self-emitted field.

The measurements are similar to the WU measurement but they can only be triggered once in RD mode and the state of the transmitter is kept. Depending on tx_en it measures its own field or checks for the presence of an external field.

Before executing the measurement, a clear WU calibration command is executed.

The measurement result is available at:

- I/Q measurement: i_adc in the I-channel WU ADC display register and q_adc in the Q-channel WU ADC display register
- Sense RF: sense_adc as a combination of I and Q in the Sense RF display register

5.16.15 Trigger wake-up event

The trigger wake-up event direct command triggers a wake-up measurement and the processing of the measurement data, the same as the normal wake-up mechanism. The following activities are executed if enabled:

- Wake-up calibration
- Reference measurement
- Wake-up measurement
- IRQ generation
- Recalibration
- Auto averaging

Instead of the wake-up timer, the MCU can trigger the execution of the single wake-up measurements. This mechanism allows the MCU to synchronize the wake-up measurements with other external events. The direct command is accepted when the wu_en bit is set to 1 and the wake-up timer is configured to 0xf which is an infinite wake-up timer period.

5.16.16 Start GPT

This command manually starts the general-purpose timer.

5.16.17 Start WUT

This command manually starts the wake-up timer.

5.16.18 Start MRT

This command manually starts the mask receive timer. Along with the MRT, Start MRT command starts the NRT if nrt<15:0> ≠ 0.

5.16.19 Start NRT

This command manually starts the no response timer.

5.16.20 Stop NRT

This command manually stops the no response timer.

5.16.21 Calibrate RC

The AWS filter curve is defined by an internal RC network if the dig_aws_en bit is set to 0. This command calibrates the RC network to show less spread over process, voltage, and temperature to maintain a constant time constant.

The command is accepted in RD mode only.

5.16.22 Trigger diagnostic measurement

Internal signals can be routed in the receiver block. The receiver can execute a DC level measurement to estimate those signals. The measurement can only be performed in ready mode when the receiver is enabled. Up to 52 measurements can be defined and scheduled in the CE memory. The completion of the execution is signaled via the I_dct interrupt. The estimation result is stored in the FIFO. There are 4 bytes produced per measurement: Command byte, calibration MSB, calibration LSB and one RFU byte. Calibration data is 9 bits unsigned and can be converted to mV/mA by multiplying with the conversion factor.

The following steps are an example to execute such a measurement:

1. Enable ready mode and enable the receiver (rx_en = 1)
2. Clear CE RAM and FIFO
3. Specify the measurement to be executed in the CE memory (for example, write 0x11 0x00 into CE memory to perform one measurement of VDD).
4. Execute the direct command trigger diagnostic measurement
5. Retrieve the result from the FIFO, (for example, read the 4 bytes 0x11 0x01 0xAB 0x41. Calibration value 0x1AB corresponds to 5 V).

The following commands can be specified in the CE memory:

Table 8. Diagnostic measurement

Command byte	Function	Comment	Conversion factor
00h	Terminate diagnostic measurement mode	-	-
01h	I_VDD_DR(1)	current through the VDD_DR regulator	3.2 (mA)
02h	VDD_TX	VDD_TX	11.7 (mV)
03h	VDD_DR(1)	VDD_DR	11.7 (mV)
04h	VDD_IO	VDD_IO	11.7 (mV)
0Ch	VDD_D	VDD_D	5.9 (mV)
0Dh	VDD_A	VDD_A	11.7 (mV)
11h	VDD	VDD	11.7 (mV)
12h	AGD	AGD	5.9 (mV)

1. *The measurements performed at rege/regc settings below 3.3 V are inaccurate and should not be used.*

5.16.23 Test register access

This command allows access to the device's test registers.

Test registers are not part of the normal register address space. After sending the direct command, test registers can be accessed using the normal read/write register operation.

Access to test registers is possible in a chained command sequence where the command test register access is sent first, followed by the read/write operation to test registers. The test registers are set to the default state at power-up.

5.17 Registers

The 7-bit register addresses below are defined in hexadecimal notation. The possible addresses range from 00h to 57h.

There are two types of registers available in this device:

- Configuration registers
- Display registers

Configuration registers can be read and written (RW) through the SPI and hold the device configuration.

Display registers are read only (RO) and contain information about the device's internal state.

Additionally, registers are grouped in two different power domains:

- Power down (PD)
- Ready (RD)

When the device is not in Ready mode, only the register belonging to the PD domain can be accessed. In ready mode all registers can be accessed.

The registers are set to their default state at power-up, and reset after execution of the direct command set default.

Table 9. Registers

Type	Address(hex)	Register name	Type, power domain
Operation	0	Operation register	RW, PD
Configuration	1	General configuration register	RW, PD
	2	VDD_DR regulator configuration register	RW, PD
	3	Tx driver configuration register	RW, PD
	4	Tx modulation register 1	RW, PD
	5	Tx modulation register 2	RW, PD
	6	CE modulation register 1	RW, PD
	7	CE modulation register 2	RW, PD
	8	GPIO control register	RW, PD
	9	Rx analog settings register 1	RW, PD
	A	Rx analog settings register 2	RW, PD
	B	Rx analog settings register 3	RW, PD
	C	Rx analog settings register 4	RW, RD
	D	Rx digital settings register 1	RW, RD
	E	Correlator settings register 1	RW, RD
	F	Correlator settings register 2	RW, RD
	10	Correlator settings register 3	RW, RD
	11	Correlator settings register 4	RW, RD
	12	Correlator settings register 5	RW, RD
	13	Correlator settings register 6	RW, RD
Protocol	14	Protocol register 1	RW, RD
	15	Tx protocol register 1	RW, RD
	16	Tx protocol register 2	RW, RD
	17	Rx protocol register 1	RW, RD
	18	Rx protocol register 2	RW, RD
	19	Rx protocol register 3	RW, RD
EMD	1A	EMD configuration register	RW, RD

Type	Address(hex)	Register name	Type, power domain
EMD	1B	EMD configuration register 2	RW, RD
CE	1C	CE configuration register	RW, PD
	1D	CE configuration register 2	RW, PD
	1E	CE configuration register 3	RW, PD
Timers	1F	Mask receive timer configuration register	RW, PD
	20	Mask receive timer configuration register 2	RW, PD
	21	Squelch timer configuration register	RW, RD
	22	NRT and GPT configuration register 1	RW, RD
	23	NRT and GPT configuration register 2	RW, RD
	24	NRT and GPT configuration register 3	RW, RD
	25	NRT and GPT configuration register 4	RW, RD
	26	NRT and GPT configuration register 5	RW, RD
Wake-up	27	Wake-up control register 1	RW, PD
	28	Wake-up control register 2	RW, PD
	29	Wake-up control register 3	RW, PD
	2A	I-channel WU configuration	RW, PD
	2B	I-channel WU difference	RW, PD
	2C	I-channel WU calibration	RO, PD
	2D	I-channel WU ADC display register	RO, PD
	2E	I-channel WU reference register	RO, PD
	2F	Q-channel WU configuration	RW, PD
	30	Q-channel WU difference	RW, PD
	31	Q-channel WU calibration	RO, PD
	32	Q-channel WU ADC display register	RO, PD
	33	Q-channel WU reference register	RO, PD
Tx/Rx frame	34	Tx frame configuration register 1	RW, RD
	35	Tx frame configuration register 2	RW, RD
	36	FIFO register status 1	RO, RD
	37	FIFO register status 2	RO, RD
	38	Rx collision display register	RO, RD
IRQ mask	39	IRQ mask register 1	RW, RD
	3A	IRQ mask register 2	RW, RD
	3B	IRQ mask register 3	RW, RD
IRQ status	3C	IRQ status register 1	RO, RD
	3D	IRQ status register 2	PD, RD
	3E	IRQ status register 3	RO, PD
Identity	3F	IC identity	RO, PD
Status	40	Status register 1	RO, PD
	41	Status register 2	RO, RD
	42	Static status register 1	RO, PD
	43	Static status register 2	RO, RD

Type	Address(hex)	Register name	Type, power domain
Status	44	Static status register 3	RO, RD
	45	Card emulation status register 1	RO/RW, RD
	46	Card emulation status register 2	RO, RD
	47	Wake up status register	RO, PD
Display	48	Analog display register 1	RO, PD
	49	Analog display register 2	RO, RD
	4A	RSSI display register 1	RO, RD
	4B	RSSI display register 2	RO, RD
	4C	Sense RF display register	RO, PD
AWS	4D	AWS configuration register 1	RW, RD
	4E	AWS configuration register 2	RW, RD
	4F	AWS timing register 1	RW, RD
	50	AWS timing register 2	RW, RD
	51	AWS timing register 3	RW, RD
	52	AWS timing register 4	RW, RD
	53	Overshoot protection register	RW, RD
	54	Undershoot protection register	RW, RD
EFD	57	External field detector	RW, PD

5.17.1 Operation register

Address: 00h

Type: RW

Table 10. Operation register

Bit	Name	Default	Function	Comment
7	wpt_en	0	1: Enables NFC WLC WPT operation	-
6	tx_en	0	1: Enables TX operation	-
5	rx_en	0	1: Enables RX operation	-
4	vdddr_en	0	1: Enables VDD_DR regulator	vdddr_en should be enabled at least 10 µs ahead of tx_en
3	en	0	1: Enables ready mode (RD)	Enables oscillator and V_{DD_A}/V_{DD_D} regulator
2	ce_en	0	1: Enables CE operation	Includes field detector operation
1	RFU	0	RFU	-
0	wu_en	0	1: Enables WU operation	Wake-up operation

5.17.2 General configuration register

Address: 01h

Type: RW

Table 11. General configuration register

Bit	Name	Default	Function	Comment
7:6	RFU<1:0>	0	RFU	-
5	Single	0	0: Differential antenna operation 1: Single ended antenna operation	Choose between differential and single driving of antenna.
4	rfo2	0	0: RFO1, RFI1 1: RFO2, RFI2, and field detector sense at RFI2	Chose which output driver and which input will be used in case of single driving
3	miso_pd2	0	1: Pull down on MISO, when BSS is low and MISO is not driven	-
2	miso_pd1	0	1: Pull down on MISO when BSS is high	-
1:0	nfc_n<1:0>	0	Definition of n for NFC field on command	-

5.17.3 VDD_DR regulator configuration register

Address: 02h

Type: RW

Table 12. VDD_DR regulator configuration register

Bit	Name	Default	Function	Comment
7	reg_s	0	0: regulated voltages are defined by result of *Adjust Regulators* command 1: regulated voltages are defined by rege<6:0> bits	-
6:0	rege<6:0>	0x7F	Regulator target voltage Used when manual voltage setting is used (reg_s =1)	-

The following table shows the VDD_DR regulated voltage inside the integrated circuit (IC). Voltages at the decoupling capacitors might be slightly higher due to the voltage drop across the bond wire and package contacts.

Table 13. Regulated voltages

rege <6:0>	Typical regulated voltage (V)	rege <6:0>	Typical regulated voltage (V)	rege <6:0>	Typical regulated voltage (V)
0x32	2.39	0x4C	3.61	0x66	4.83
0x33	2.44	0x4D	3.66	0x67	4.88
0x34	2.48	0x4E	3.70	0x68	4.92
0x35	2.53	0x4F	3.75	0x69	4.97
0x36	2.58	0x50	3.80	0x6A	5.02
0x37	2.63	0x51	3.84	0x6B	5.06
0x38	2.67	0x52	3.89	0x6C	5.11
0x39	2.72	0x53	3.94	0x6D	5.16
0x3A	2.77	0x54	3.98	0x6E	5.20
0x3B	2.81	0x55	4.03	0x6F	5.25
0x3C	2.86	0x56	4.08	0x70	5.30
0x3D	2.91	0x57	4.13	0x71	5.34
0x3E	2.95	0x58	4.17	0x72	5.39
0x3F	3.00	0x59	4.22	0x73	5.44
0x40	3.05	0x5A	4.27	0x74	5.48
0x41	3.09	0x5B	4.31	0x75	5.53
0x42	3.14	0x5C	4.36	0x76	5.58
0x43	3.19	0x5D	4.41	0x77	5.63
0x44	3.23	0x5E	4.45	0x78	5.67
0x45	3.28	0x5F	4.50	0x79	5.72
0x46	3.33	0x60	4.55	0x7A	5.77
0x47	3.38	0x61	4.59	0x7B	5.81
0x48	3.42	0x62	4.64	0x7C	5.86
0x49	3.47	0x63	4.69	0x7D	5.91
0x4A	3.52	0x64	4.73	0x7E	5.95
0x4B	3.56	0x65	4.78	0x7F	6.00

5.17.4 Tx driver configuration register

Address: 03h

Type: RW

Table 14. Tx driver configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:4	regd<2:0>	2	Regulator target drop Used in adjust regulators command (reg_s = 0)	-
3:0	d_res<3:0>	0	RFO driver resistance, during active transmission	-

Table 15. VDD_DR Regulator Drop

Regd<2:0>	Target drop (mV)	Regd<2:0>	Target drop (mV)
0x0	200	0x4	400
0x1	250	0x5	450
0x2	300	0x6	500
0x3	350	0x7	550

Table 16. Driver resistance multiplier

d_res<3:0>	d_res3	d_res2	d_res1	d_res0	Driver output resistance (normalized)(1)
0x0	0	0	0	0	1.01
0x1	0	0	0	1	1.12
0x2	0	0	1	0	1.24
0x3	0	0	1	1	1.38
0x4	0	1	0	0	1.51
0x5	0	1	0	1	1.67
0x6	0	1	1	0	1.86
0x7	0	1	1	1	2.21
0x8	1	0	0	0	2.56
0x9	1	0	0	1	3.05
0xA	1	0	1	0	4.09
0xB	1	0	1	1	6.19
0xC	1	1	0	0	12.8
0xD	1	1	0	1	27.4
0xE	1	1	1	0	64.0
0xF	1	1	1	1	High Z

1. *The value must be multiplied by the RFO resistance from Section 6: Electrical characteristics to obtain the driver output resistance for the corresponding d_res setting.*

5.17.5 Tx modulation register 1

Address: 04h

Type: RW

Table 17. Tx modulation register 1

Bit	Name	Default	Function	Comment
7:4	am_mod<3:0>	0x07	AM modulation index	-
3	mod_state	0	0: Unmodulated state 1: Modulated state	Switch RFO output between modulated and unmodulated AM voltage
2	rgs_am	0	0: disable regulator shape modulation 1: enable Regulator shape modulation	Can be combined with res_am
1	res_am	0	0: disable Resistive AM modulation 1: enable Resistive AM modulation	Can be combined with tr_am = 0
0	RFU	0	RFU	-

Table 18. AM modulation index

am_mod<3:0>	am_mod3	am_mod 2	am_mod 1	am_mod 0	Modulation index target
0x0	0	0	0	0	8%
0x1	0	0	0	1	10%
0x2	0	0	1	0	11%
0x3	0	0	1	1	12%
0x4	0	1	0	0	13%
0x5	0	1	0	1	14%
0x6	0	1	1	0	15%
0x7	0	1	1	1	20%
0x8	1	0	0	0	30%
0x9	1	0	0	1	40%
0xA	1	0	1	0	50%
0xB	1	0	1	1	60%
0xC	1	1	0	0	70%
0xD	1	1	0	1	80%
0xE	1	1	1	0	88%
0xF	1	1	1	1	97%

5.17.6 Tx modulation register 2

Address: 05h

Type: RW

Table 19. Tx modulation register 2

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:0	md_res<6:0>	0	Resistive modulation	-

Table 20. md_res setting

md_res	Driver output resistance (normalized)(1)	md_res	Driver output resistance (normalized)(1)	md_res	Driver output resistance (normalized)(1)	md_res	Driver output resistance (normalized)(1)
0x00	1.005	0x20	1.561	0x40	3.050	0x60	6.190
0x01	1.016	0x21	1.600	0x41	3.100	0x61	6.400
0x02	1.027	0x22	1.641	0x42	3.150	0x62	6.620
0x03	1.038	0x23	1.684	0x43	3.200	0x63	6.860
0x04	1.049	0x24	1.730	0x44	3.250	0x64	7.110
0x05	1.061	0x25	1.761	0x45	3.310	0x65	7.380
0x06	1.073	0x26	1.794	0x46	3.370	0x66	7.680
0x07	1.085	0x27	1.829	0x47	3.430	0x67	8.000
0x08	1.097	0x28	1.864	0x48	3.490	0x68	8.350
0x09	1.110	0x29	1.901	0x49	3.560	0x69	8.730
0x0A	1.123	0x2A	1.939	0x4A	3.620	0x6A	9.140
0x0B	1.136	0x2B	1.979	0x4B	3.690	0x6B	9.600
0x0C	1.150	0x2C	2.021	0x4C	3.760	0x6C	10.100
0x0D	1.164	0x2D	2.065	0x4D	3.840	0x6D	10.700
0x0E	1.178	0x2E	2.110	0x4E	3.920	0x6E	11.300
0x0F	1.193	0x2F	2.157	0x4F	4.000	0x6F	12.000
0x10	1.208	0x30	2.207	0x50	4.090	0x70	12.800
0x11	1.223	0x31	2.259	0x51	4.170	0x71	13.700
0x12	1.239	0x32	2.313	0x52	4.270	0x72	14.800
0x13	1.255	0x33	2.370	0x53	4.360	0x73	16.000
0x14	1.272	0x34	2.430	0x54	4.470	0x74	17.500
0x15	1.289	0x35	2.494	0x55	4.570	0x75	19.200
0x16	1.306	0x36	2.560	0x56	4.680	0x76	21.300
0x17	1.324	0x37	2.630	0x57	4.800	0x77	24.000
0x18	1.343	0x38	2.704	0x58	4.920	0x78	27.400
0x19	1.362	0x39	2.743	0x59	5.050	0x79	32.000
0x1A	1.381	0x3A	2.783	0x5A	5.190	0x7A	38.400
0x1B	1.401	0x3B	2.824	0x5B	5.330	0x7B	48.000
0x1C	1.422	0x3C	2.866	0x5C	5.490	0x7C	64.000
0x1D	1.455	0x3D	2.909	0x5D	5.650	0x7D	96.000

md_res	Driver output resistance (normalized)(1)	md_res	Driver output resistance (normalized)(1)	md_res	Driver output resistance (normalized)(1)	md_res	Driver output resistance (normalized)(1)
0x1E	1.488	0x3E	2.954	0x5E	5.820	0x7E	192.000
0x1F	1.512	0x3F	3.000	0x5F	6.000	0x7F	High Z

1. *The value must be multiplied by the RFO resistance from Section 6: Electrical characteristics to obtain the driver output resistance for the corresponding md_res setting.*

5.17.7 CE modulation register 1

Address: 06h

Type: RW

Table 21. CE modulation register 1

Bit	Name	Default	Function	Comment
7:4	cem_res<3:0>	8	RFO resistance during CE modulation in modulated state	Bits to be set before entering CE operation
3:0	ce_res<3:0>	0	RFO resistance during CE modulation in unmodulated state	Bits to be set before entering CE operation

Table 22. Driver resistance in unmodulated (CE_RES) and modulated (CEM_RES) state

cem_res3:0 ce_res3:0	R-RFO-Normalized (1)
0x0	1.01
0x1	1.51
0x2	3.05
0x3	6.19
0x4	9.14
0x5	12.8
0x6	19.2
0x7	24.0
0x8	27.4
0x9	32.0
0xA	38.4
0xB	48.0
0xC	64.0
0xD	96.0
0xE	192
0xF	High Z

1. *The value must be multiplied by the RFO resistance from Electrical specification to obtain the driver output resistance for the corresponding d_res setting.*

5.17.8 CE modulation register 2

Address: 07h
Type: RW

Table 23. CE modulation register 2

Bit	Name	Default	Function	Comment
7:6	gpio_en<1:0>	0	0: Push-pull disabled, NMOS enabled 1: Push-pull output on gpio1, gpio2	Gpio2/1 can be used as TRIM 2/1 for antenna tuning via external HV MOS, MSB: GPIO2, and LSB: GPIO1
5	RFU	0	RFU	-
4	tad_en	0	0: Push-pull disabled 1: Push-pull output on tad1, tad2	Tad2/1 can be used as TRIM 4/3 for antenna tuning via external HV MOS
3:2	lm_gpio<1:0>	0	CE modulation via gpio2, gpio1 (en_ce=1)	MSB: GPIO2 and LSB: GPIO1
1	lm_trim	0	CE modulation via tad2/1 (en_ce=1)	-
0	lm_dri	1	CE modulation via Driver resistance	-

5.17.9 GPIO control register

Address: 08h
Type: RW

Table 24. GPIO control register

Bit	Name	Default	Function	Comment
7:6	trim_ce<1:0>	0	Defines TAD2/1 value in CE operation (en_ce=1)	TAD2/1 can be used as TRIM 4/3 for antenna tuning in CE operations, MSB: TAD2, and LSB: TAD1
5:4	gpio_ce<1:0>	0	Defines GPIO2/1 value in CE operation (en_ce=1)	GPIO2/1 can be used as TRIM 2/1 for antenna tuning in CE operations (gpio_en = 1), MSB: GPIO2, and LSB: GPIO1
3:2	trim_rw<1:0>	0	Defines TAD2/1 value in read operation (en_ce = 0)	TAD2/1 can be used as TRIM 4/3 for antenna tuning in reader operation, MSB: TAD2, and LSB: TAD1
1:0	gpio_rw<1:0>	0	Defines GPIO2/1 value in read operation (en_ce = 0)	GPIO2/1 can be used as TRIM 2/1 for antenna tuning in reader operation (gpio_en = 1), MSB: GPIO2, and LSB: GPIO1

5.17.10 Rx analog settings register 1

Address: 09h
Type: RW

Table 25. Rx analog settings register 1

Bit	Name	Default	Function	Comment
7:4	dig_clk_dly<3:0>	0x5	Digital clock delay	Recommended value: 0x7
3	RFU	0	RFU	-
2	gain_boost	0	1: Increased gain in Rx path by 3 dB	Can be used in read operation, CE operation and wake-up operation
1:0	hpf_ctrl<1:0>	0x3	00: 80kHz, 01: 160kHz 10: 240kHz, 11: 380kHz	Analogue 1 and 3rd stage HPF setting (2nd stage: LPF, 2nd order, 2MHz) For WU: 0x11

5.17.11 Rx analog settings register 2

Address: 0Ah
Type: RW

Table 26. Rx analog settings register 2

Bit	Name	Default	Function	Comment
7:4	afe_gain_rw<3:0>(1)	0x0	3dB start gain reduction in read operation	-
3:0	afe_gain_td<3:0> (2)	0x8	3dB start gain reduction in WU mode	-

1. *Choosing a gain different from 0x0 requires dis_agc_noise_meas = 1.*
2. *For applications used at V_{DD_A} ≤ 2.7 V and at -40 °C, a minimum afe_gain_td of ≥ 0x5 must be used. The gain_boost can be set to either 0x0 or 0x1.*

5.17.12 Rx analog settings register 3

Address: 0Bh
Type: RW

Table 27. Rx analog settings register 3

Bit	Name	Default	Function	Comment
7:4	afe_gain_ce<3:0>	0x8	3dB gain reduction in CE operation	Maximum reduction: 3 dB * 0xB = 33 dB
3:2	ook_thr_hi<1:0>	1	Data threshold for envelope falling	Signal level: 00 : 0.375 01 : 0.5 10 : 0.675 11 : 0.75
1:0	ook_thr_lo<1:0>	1	Data threshold for envelope rising	Signal level: 00: 0.125 01: 0.25 10: 0.375 11: 0.5

5.17.13 Rx analog settings register 4

Address: 0Ch
Type: RW

Table 28. Rx analog settings register 4

Bit	Name	Default	Function	Comment
7	en_phase_deadzone	0	1: Enable dead zone for BPSK phase correction during phase changes (to be used in NFC-F CE operation)	-
6	en_rect_cor	0	1: Enable rectifier correction after subcarrier start	-
5:0	RFU<5:0>	0x0	RFU	-

5.17.14 Rx digital settings register 1

Address: 0Dh
Type: RW

Table 29. **Rx digital settings register 1**

Bit	Name	Default	Function	Comment
7	agc_en	1	0: AGC disabled 1: AGC enabled	-
6:4	lpf_coef<2:0>	4	1st-order IIR coefficient	-
3:2	hpf_coef<1:0>	3	1st-order IIR coefficient	-
1	ce_agc_freeze	0	Freeze AGC in CE operation during reception	-
0	RFU	0	RFU	-

5.17.15 Correlator settings register 1

Address: 0Eh
Type: RW

Table 30. **Correlator settings register 1**

Bit	Name	Default	Function	Comment
7:4	iir_coef2<3:0>	0xC	1st-order IIR coefficient	-
3:0	iir_coef1<3:0>	0x1	1st-order IIR coefficient	-

5.17.16 Correlator settings register 2

Address: 0Fh
Type: RW

Table 31. **Correlator settings register 2**

Bit	Name	Default	Function	Comment
7:4	agc_thr_squelch<3:0>	0x5	Read operation: Squelch threshold CE operation: Low AGC limit	CE: increase gain
3:0	agc_thr<3:0>	0xA	Read operation: AGC threshold CE operation: High AGC limit	CE: decrease gain

5.17.17 Correlator settings register 3

Address: 10h
Type: RW

Table 32. **Correlator settings register 3**

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	en_subc_end	0	BPSK only 0: No subcarrier end detection (reception stops with valid EOF or timeout) 1: Fast subcarrier end detection	-
5:0	start_wait<5:0>	0x7	Wait time for subcarrier detection	-

5.17.18 Correlator settings register 4

Address: 11h
Type: RW

Table 33. Correlator settings register 4

Bit	Name	Default	Function	Comment
7:4	coll_lvl<3:0>	0xA	Manchester: collision level ratio collision level ratio	-
5:0	data_lvl<3:0>	0xA	Manchester: data level ratio BPSK: Subcarrier end detection level	-

5.17.19 Correlator settings register 5

Address: 12h
Type: RW

Table 34. Correlator settings register 5

Bit	Name	Default	Function	Comment
7	dis_noise_leak	0	0: Automatic noise level adjustment when no signal 1: disabled	-
6	dis_noise_meas	0	0: Noise level adjustment 1: disabled	-
5	dis_soft_sq	0	0: noise measurement after start of reception 1: disabled	-
4	dis_agc_noise_meas	0	0: AGC effect on internally used noise level 1: disabled	-
3	no_phase	0	1: Disables phase correction after signal start detection (BPSK only)	-
2:0	dec_f<2:0>	3	Decimation factor for IIR filters	-

5.17.20 Correlator settings register 6

Address: 13h
Type: RW

Table 35. Correlator settings register 6

Bit	Name	Default	Function	Comment
7:4	init_noise_lvl<3:0>	0x3	I and Q correlator initial noise level setting	-
5:0	agc_freeze_cnt<3:0>	0x0	AGC freeze before the subcarrier start is detected	BPSK protocols in reader operation (NFC-A HBR, NFC-B, NFC_F) Step size: 1/(2 * bitrate)

Table 36. Initial correlator noise level

init_noise_lvl3:0	init_noise_lvl3	init_noise_lvl2	init_noise_lvl1	init_noise_lvl0	Correlator initial Noise level
0x0	0	0	0	0	5
0x1	0	0	0	1	10
0x2	0	0	1	0	15

init_noise_lvl3:0	init_noise_lvl3	init_noise_lvl2	init_noise_lvl1	init_noise_lvl0	Correlator initial Noise level
0x3	0	0	1	1	20
0x4	0	1	0	0	25
0x5	0	1	0	1	30
0x6	0	1	1	0	35
0x7	0	1	1	1	40
0x8	1	0	0	0	50
0x9	1	0	0	1	60
0xA	1	0	1	0	70
0xB	1	0	1	1	80
0xC	1	1	0	0	90
0xD	1	1	0	1	100
0xE	1	1	1	0	110
0xF	1	1	1	1	120

5.17.21 Protocol register 1

Address: 14h
Type: RW

Table 37. **Protocol register 1**

Bit	Name	Default	Function	Comment
7:6	rx_rate<1:0>	00	Set rx bit rate according to technology: NFC-A, NFC-B, NFC-F or NFC-V	Selects bit rate for Rx
5:4	tx_rate<1:0>	00	Set tx bit rate according to technology: NFC-A, NFC-B, NFC-F or NFC-V	Selects bit rate for Tx
3:0	om<3:0>	0x1	Operation mode (protocol)	-

Table 38. **rx_rate**

rx_rate 1	rx_rate 0	NFC-A	NFC-B	NFC-F	NFC-V
0	0	106 kbps	106 kbps	-	26kbps
0	1	212 kbps	212 kbps	212 kbps	53 kbps
1	0	424 kbps	424 kbps	424 kbps	106 kbps
1	1	848 kbps	848 kbps	-	212 kbps

Table 39. **tx_rate**

tx_rate 1	tx_rate 0	NFC-A	NFC-B	NFC-F	NFC-V
0	0	106 kbps	106 kbps	-	26kbps
0	1	212 kbps	212 kbps	212 kbps	-
1	0	424 kbps	424 kbps	424 kbps	-
1	1	848 kbps	848 kbps	-	-

Table 40. **Operation modes**

om3	om2	om1	om0	Reader operation (ce_en = 0)	CE operation (ce_en = 1)
0	0	0	0	N/A	N/A
0	0	0	1	ISO14443-A/NFC-A	ISO14443-A/NFC-A (106k)
0	0	1	0	ISO14443-B/NFC-B	N/A
0	0	1	1	NFC-F	NFC-F (212k/424k)
0	1	0	0	Topaz	N/A
0	1	0	1	ISO15693/NFC-V	N/A
1	1	0	1	N/A	Single bit rate detection mode with lock
1	1	1	0	N/A	Single bit rate detection mode
1	1	1	1	N/A	Normal bit rate detection mode

5.17.22 Tx protocol register 1

Address: 15h

Type: RW

Table 41. **Tx protocol register 1**

Bit	Name	Default	Function	Comment
7	a_nfc_f0	0	1: support of NFCIP-1 transport frame format	Add SB (F0) and LEN bytes during Tx and skip SB(F0) byte during Rx – Not to be used in Bit Rate detection operation.
6	a_tx_par	1	1: parity bit is generated during Tx	Parity and CRC is generated and transmitted
5	tx_crc	1	1: CRC is generated during Tx	CRC is generated and transmitted
4	tr_am	0	0: OOK 1: AM	Tx modulation type in digital control
3:0	p_len<3:0>	0x0	OOK modulation duration	Modulation pulse width NFC-A/ NFC-V. Defined in number of 13.56 MHz clock periods

Table 42. **OOK modulation pulse width**

p_len	p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1/f_C for different bit rates NFC-A and NFC-V				
					f_C/512	f_C/128	f_C/64	f_C/32	f_C/16
0x7	0	1	1	1	128	42	-	-	-
0x6	0	1	1	0	124	41	24	-	-
0x5	0	1	0	1	120	40	23	-	-
0x4	0	1	0	0	116	39	22	13	-
0x3	0	0	1	1	112	38	21	12	8
0x2	0	0	1	0	108	37	20	11	7
0x1	0	0	0	1	104	36	19	10	6
0x0	0	0	0	0	100	35	18	9	5
0xF	1	1	1	1	96	34	17	8	4
0xE	1	1	1	0	92	33	16	7	3
0xD	1	1	0	1	88	32	15	6	2
0xC	1	1	0	0	84	31	14	5	-
0xB	1	0	1	1	80	30	13	-	-
0xA	1	0	1	0	76	29	12	-	-
0x9	1	0	0	1	72	28	-	-	-
0x8	1	0	0	0	68	27	-	-	-

5.17.23 Tx protocol register 2

Address: 16h

Type: RW

Table 43. **Tx protocol register 2**

Bit	Name	Default	Function	Comment
7:5	RFU<7:5>	0	RFU	-
4	f_tx_len	1	1: NFC-F, length byte is generated and transmitted	LEN byte is generated and transmitted RW and CE operation
3	b_tx_sof_0	0	0: 10 etu,1: 11 etu	SOF, number of etu with logic 0 (10 or 11)
2	b_tx_sof_1	0	0: 2 etu, 1: 3 etu	SOF, number of etu with logic 1 (2 or 3)
1	b_tx_eof	0	0: 10 etu, 1: 11 etu	EOF, number of etu with logic 0 (10 or 11)
0	b_tx_half	0	1: SOF 10.5, 2.5, EOF: 10.5	Sets SOF and EOF settings in middle of specification

5.17.24 Rx protocol register 1

Address: 17h
Type: RW

Table 44. Rx protocol register 1

Bit	Name	Default	Function	Comment
7:6	RFU<7:6>	0	RFU	-
5	b_rx_sof	1	1: Expects SOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Support of B' (no SOF)
4	b_rx_eof	1	1: Expects EOF PICC to PCD	According to ISO 14443-3 chapter 7.10.3.3
3	a_rx_par	1	1: Receive with parity check	When set to 1, parity check is performed
2	rx_crc	1	1: Receive with CRC check	When set to 1, CRC check is performed
1	rx_nbtx	0	1: Received bits are positioned according to nbtx<2:0> setting	The nbtx<2:0> bits define position of the first bit in the first byte in consecutive reception. To be used for SDD_REQ.
0	antcl	0	1: NFC-A/V: Anti-collision frame	Has to be set to 1 when NFC-A/ NFC-V bit oriented anti-collision frame is expected. • coll_lvl is used to detect colliding bits • The first parity bit is ignored in case the split happens within the byte

5.17.25 Rx protocol register 2

Address: 18h
Type: RW

Table 45. Rx protocol register 2

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:0	tr1_min_len<6:0>	0x3A	Minimum remaining TR1 length (Type B) in subcarrier periods (0-127)	If received TR1 is shorter than the minimum specified length, a soft error interrupt is generated. TR1 in this register starts after the subcarrier is detected (see start_wait<5:0> setting)

5.17.26 Rx protocol register 3

Address: 19h
Type: RW

Table 46. Rx protocol register 3

Bit	Name	Default	Function	Comment
7:0	tr1_max_len<7:0>	0xC0	Maximum remaining TR1 length (Type B) in subcarrier periods (1-255). 0x00: No check	If received TR1 is longer than the maximum specified length, a soft error interrupt is generated. TR1 in this register starts after the subcarrier is detected (see start_wait<5:0> setting)

5.17.27 EMD configuration register 1

Address: 1Ah
Type: RW

Table 47. EMD configuration register 1

Bit	Name	Default	Function	Comment
7:4	emd_thld<3:0>	0x4	EMD threshold definition in number of received bytes	If the received message length is less than the number of bytes defined by emd_thld then EMD suppression is triggered.
3	emd_thld_ff	1	0: emd thld applies for the error limit 1: emd_thld applies for the full frame size	When disabled the emd_thld applies to the error location independently of the full frame length
2:1	RFU<1:0>	0	RFU	-
0	emd_en	0	0: Disable HW EMD Suppression 1: Enable HW EMD Suppression	-

5.17.28 EMD configuration register 2

Address: 1Bh
Type: RW

Table 48. EMD configuration register 2

Bit	Name	Default	Function	Comment
7:0	RFU<7:0>	0x0	RFU	-

5.17.29 CE configuration register 1

Address: 1Ch
Type: RW

Table 49. CE configuration register 1

Bit	Name	Default	Function	Comment
7:6	RFU<7:6>	0	RFU	-
5	ce_signal_all	0	0: Interrupt I_ce_sc is triggered only on CARD_EMU_4A and CE_F being entered. 1: all state machine changes (ce_state) trigger I_ce_sc	Define whether all state machine changes performed by HW trigger an interrupt
4	en_other_idle	1	handling of OTHER frames in IDLE mode: 0: Put in FIFO and wait for MCU to decide action (answer/ goto state). 1: OTHER frames are handled automatically (ignored)	Other according to NFC Forum activity specification
3	en_dsl_a	1	Enable automatic responses to S(DESELECT) while in CARD_EMU_4A state	CID and NAD
2	en_ce4a	1	Enable automatic responses to RATS, SLP_REQ and OTHER frames in ACTIVE_A[*] state. Automatic move to CARD_EMU_4A state on reception of RATS. From CARD_EMU4A state the HW can handle SELECT or DESELECT.	All RATS (2 byte frame with E0 and correct CRC) are accepted. 2nd byte of RATS is put into rats_param register to be read by MCU.
1	en_212/424_1r	0	Enable automatic SENSF_RES in NFC-F 212/424 kbps	-
0	en_106_ac_a	1	Enable automatic anti-collision in NFC-A 106 kbps	-

5.17.30 CE configuration register 2

Address: 1Dh
Type: RW

Table 50. CE configuration register 2

Bit	Name	Default	Function	Comment
7:4	fdel<3:0>	0	PCD to PICC FDT compensation. Frame compensation defined as fdel*1/f_C	Valid for NFC-A CE operation fdel=0: Nominal FDT time produced in logic. fdel>0: Shortens the FDT provided by logic.
3:1	RFU<2:0>	0	RFU	-
0	nfc_id	0	0: 4 bytes NFCID; Address 0-4 in CE memory 1: 7 bytes NFCID; Address 0-7 in CE memory	4/7 byte NFCID support

5.17.31 CE configuration register 3

Address: 1Eh
Type: RW

Table 51. CE configuration register 3

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:0	tsn<6:0>	0	Pseudo random number generator for TSN (slot numbers in NFC-F)	Sending SENSF_RES uses the topmost 4 bits from the register, and afterwards, it produces 4 new bits by shifting/calculating Software can set these bits to re-seed / set the next to be used slot number

5.17.32 Mask receive timer configuration register 1

Address: 1Fh
Type: RW

Table 52. Mask receive timer configuration register 1

Bit	Name	Default	Function	Comment
7:6	sq_del<1:0>	0	00: 18.88us 01: 2x18.88us = 37.76us 10: 4x18.88us = 75.52us 11: 8x18.88us = 151.04us	Defines the delay of the squelch enable, with respect to end of Tx
5:4	mrt_step<1:0>	2	00: 16/f_C (1.18us) 01: 32/f_C (2.36us) 10: 64/f_C (4.72us) 11: 512/f_C (37.8us)	Selects the Mask-receive timer step
3:1	RFU<2:0>	0	RFU	-
0	sq_en	1	1: Automatic squelch activation after end of Tx	Activated 18.88us after end of Tx, terminated with Mask Receive timer expiration

5.17.33 Mask receive timer configuration register 2

Address: 20h

Type: RW

Table 53. Mask receive timer configuration register 2

Bit	Name	Default	Function	Comment
7:0	mrt<7:0>	0x0B	Defined in mrt_step<1:0> (16/f_C…512/f_C). Timeout = mrt<7:0> * mrt_step<1:0> Range: 16/f_C (1.18us) at 16/f_C to 130560/fc (~9.6 ms) at 512/f_C)	Defines time after end of Tx during which receiver output is masked (ignored). In case mrt < sq_del, rx_on goes high at sq_del

5.17.34 Squelch timer configuration register

Address: 21h

Type: RW

Table 54. Squelch timer configuration register

Bit	Name	Default	Function	Comment
7:0	sqt<7:0>	0x0B	In steps equal to the mask receive timer (mrt_step).	Squelch is enabled 18.88us-151us after the end of reader data transmission, as defined in sq_del<1:0>. Squelch is enabled till the time defined by sqt<7:0>. In case sqt < sq_del, there is no squelch period (and Gain reduction from previous reception is used as Starting point for AGC). In case sqt > mrt, squelch is enabled until the mrt expires. Setting in afe_gain_rw is a starting point for squelch. Gain reduction due to squelch is locked and used as a starting point for AGC.

5.17.35 NRT and GPT configuration register 1

Address: 22h
Type: RW

Table 55. NRT and GPT configuration register 1

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:4	gptc<2:0>	0x0	Defines the GP timer trigger source	-
3:2	RFU<1:0>	0	RFU	-
1	nrt_emv	0	1: EMV mode of no-response timer	-
0	nrt_step	0	0: 64/f_C 1: 4096/f_C	No-response timer step

Table 56. General purpose timer trigger source

gptc2	gptc1	gptc0	Trigger source
x	x	x	The timer starts always with direct command start general purpose timer
0	0	0	No additional trigger source
0	0	1	Additionally starts at End of Rx (after EOF)
0	1	0	Additionally starts at Start of Rx
0	1	1	Additionally starts at end of Tx frame
1	0	0	Additionally starts at Field on (en_tx 0 to 1 transition) – To be used at NFC field on command to mark ‘Guard time expire’
1	x	x	RFU

5.17.36 NRT and GPT configuration register 2

Address: 23h
Type: RW

Table 57. NRT and GPT configuration register 2

Bit	Name	Default	Function	Comment
7:0	nrt<15:8>	0x00	No-response timer definition MSB bits Defined in steps of 64/f_C (4.72 µs), range from 0 to 309ms In case the bit nrt_step is set the step is changed to 4096/f_C (302 µs), range 19.8 s.	Defines timeout after end of Tx. In case this timeout expires without detecting a response a No-response interrupt is sent. All 0: No-response timer is not started. No-response timer can also be reset and restarted with start no-response timer direct command.

5.17.37 NRT and GPT configuration register 3

Address: 24h
Type: RW

Table 58. NRT and GPT configuration register 3

Bit	Name	Default	Function	Comment
7:0	nrt<7:0>	0x00	No-response timer definition LSB bits	-

5.17.38 NRT and GPT configuration register 4

Address: 25h
Type: RW

Table 59. NRT and GPT configuration register 4

Bit	Name	Default	Function	Comment
7:0	gpt<15:8>	0x00	General purpose timeout definition MSB bits. Defined in steps of $8/f_C$ (590 ns) Range from 590 ns to 38.7 ms	-

5.17.39 NRT and GPT configuration register 5

Address: 26h
Type: RW

Table 60. NRT and GPT configuration register 5

Bit	Name	Default	Function	Comment
7:0	gpt<7:0>	0x00	General purpose timeout definition LSB bits.	-

5.17.40 Wake-up control register 1

Address: 27h
Type: RW

Table 61. Wake-up control register 1

Bit	Name	Default	Function	Comment
7:4	wut<3:0>	0	Wake-up timer timeout value (wu_en = 1) (in WU mode) or Measure Sampling period (wpt_en=1) (in RD mode)	See the following table
3:1	RFU<2:0>	0	RFU	-
0	fast_efd_irq	0	0: Efd IRQs generated by 26.24 kHz clk 1: Efd IRQs generated by 262.4 kHz clk	-

Table 62. **Wake- up timer periode / WPT measure sampling period (wut/wpt)**

wut<3:0>	WU time (wu_en=1) nominal (ms)	Measure sampling period (wpt_en=1) (µs)
0x0	12.5	RFU
0x1	25	RFU
0x2	50	RFU
0x3	75	RFU
0x4	100	RFU
0x5	125	RFU
0x6	150	RFU
0x7	200	151.0(1)
0x8	250	RFU
0x9	300	RFU
0xA	350	RFU
0xB	400	RFU
0xC	500	RFU
0xD	800	RFU
0xE	1000	RFU
0xF	Inf.	RFU

1. *Required setting for WLC WPT operation.*

5.17.41 Wake-up control register 2

Address: 28h

Type: RW

Table 63. **Wake-up control register 2**

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	wut_cal	0	0: No WU timer calibration 1: Calibrate WU period during WU event (valid for wut > 3)	higher WU period accuracy at increased RD time (wut_cal_len)
5:4	wut_cal_len<1:0>	0	WU timer calibration length	0: 0.781ms 1: 1.562ms 2: 3.125ms 3: 6.248ms
3	weak_disch	0	0: AGD and VDD_A discharged in PD mode and WU operation 1: Only weak / self discharge on AGD and VDD_A in PD mode and WU operations	1: Weak discharge allows capacitors to remain mainly charged between WU events, decreasing overall wake-up consumption.
2	RFU	0	RFU	-

Bit	Name	Default	Function	Comment
1:0	tagdet_len<1:0>	0	Field-on time fixed to 00: td_mt setting 01: 36 * 16/f_C (42.5 us) 10: 44 * 16/f_C (51.9 us) 11: 52 * 16/f_C (61.4 us)	Real measurement at the second half of available field-on duration

5.17.42 Wake-up control register 3

Address: 29h

Type: RW

Table 64. Wake-up control register 3

Bit	Name	Default	Function	Comment
7	skip_recal	0	1: Disable automatic recalibration	-
6	skip_cal	0	1: Disable automatic calibration	-
5	skip_twcal	0	1: Disable calibration delay at start	-
4	skip_twref	0	1: Disable reference delay at start	-
3	iq_aaref	0	0: Manually defined reference for both I and Q channel 1: Enable auto average reference for both I and Q channel	-
2	td_mf	0	Wake-up measure time	-
1:0	td_mt<1:0>	0	Wake-up measure time	-

Table 65. Wake-up measurement time

td_mt	td_mf	Measurement pulse µs
0x0	0x0	26.0
0x1	0x0	29.5
0x2	0x0	34.2
0x3	0x0	43.7
0x0	0x1	10.6
0x1	0x1	14.2
0x2	0x1	18.9
0x3	0x1	28.3

5.17.43 I-channel WU configuration register

Address: 2Ah
Type: RW

Table 66. **I-channel WU configuration register**

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	i_iirqm	0	0: exclude the IRQ measurement 1: include all measurements	-
5:3	i_aaw<2:0>	0	000: 4 001: 8 010: 16 011: 32 100: 50 101: 64 110: 100 111: 128	Define weight of last measurement result for auto-averaging
2	i_tdi_en2	0	1: IRQ if i_adc > i_ref + i_diff	All 0: I-channel wake-up measurement, disabled, including receiver circuitry and correlator clock (to minimize consumption)
1	i_tdi_en1	0	1: IRQ if i_ref - i_diff ≤ i_adc ≤ i_ref + i_diff	
0	i_tdi_en0	0	1: IRQ if i_adc < i_ref - i_diff	

5.17.44 I-channel WU difference register

Address: 2Bh
Type: RW

Table 67. **I-channel WU difference register**

Bit	Name	Default	Function	Comment
7	i_cal<8>	1	MSB unsigned calibration result (Unsigned)	-
6	RFU	0	RFU	-
5:0	i_diff<5:0>	0x0A	ADC to reference difference that triggers IRQ	Unsigned

5.17.45 I-channel WU calibration register

Address: 2Ch
Type: RW

Table 68. **I-channel WU calibration register**

Bit	Name	Default	Function	Comment
7:0	i_cal<7:0>	0x00	8-bit unsigned calibration result (unsigned)	-

5.17.46 I-channel WU ADC display register

Address: 2Dh
Type: RW

Table 69. I-channel WU ADC display register

Bit	Name	Default	Function	Comment
7:0	i_adc<7:0>	0	8-bit signed ADC part Range: -128 to 127	-

5.17.47 I-channel WU reference register

Address: 2Eh
Type: RW

Table 70. I-channel WU reference register

Bit	Name	Default	Function	Comment
7:0	i_ref<7:0>	0	8-bit signed reference Range: -128 to 127	If iq_aaref = 1 the reference is automatically calculated, and this register is RO. When iq_aaref = 0 the reference shall be set manually, and this register becomes RW

5.17.48 Q-channel WU configuration register

Address: 2Fh
Type: RW

Table 71. Q-channel WU configuration register

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	q_iirqm	0	0: exclude the IRQ measurement 1: include all measurements	-
5:3	q_aaw<2:0>	0	000: 4 001: 8 010: 16 011: 32 100: 50 101: 64 110: 100 111: 128	Define weight of last measurement result for auto-averaging
2	q_tdi_en2	0	1: IRQ if q_adc > q_ref + q_diff	All 0: Q-channel wake-up measurement disabled, including receiver circuitry and correlator clock (to minimize consumption)
1	q_tdi_en1	0	1: IRQ if q_ref - q_diff ≤ q_adc ≤ q_ref + q_diff	
0	q_tdi_en0	0	1: IRQ if q_adc < q_ref - q_diff	

5.17.49 Q-channel WU difference register

Address: 30h
Type: RW

Table 72. **Q-channel WU difference register**

Bit	Name	Default	Function	Comment
7	q_cal<8>	1	MSB unsigned calibration result (Unsigned)	-
6	RFU	0	RFU	-
5:0	q_diff<5:0>	0x0A	ADC to reference difference that triggers IRQ	Unsigned

5.17.50 Q-channel WU calibration register

Address: 31h
Type: RW

Table 73. **Q-channel WU calibration register**

Bit	Name	Default	Function	Comment
7:0	q_cal<7:0>	0x00	8-bit unsigned calibration result (Unsigned)	-

5.17.51 Q-channel WU ADC display register

Address: 32h
Type: RW

Table 74. **Q-channel WU ADC display register**

Bit	Name	Default	Function	Comment
7:0	q_adc<7:0>	0	8-bit signed ADC part Range: -128 to 127	-

5.17.52 Q-channel WU reference register

Address: 33h
Type: RW

Table 75. **Q-channel WU reference register**

Bit	Name	Default	Function	Comment
7:0	q_ref<7:0>	0	8-bit signed reference Range: -128 to 127	If iq_aaref = 1 the reference is automatically calculated, and this register is RO. When iq_aaref = 0 the reference shall be set manually, and this register becomes RW

5.17.53 Tx frame configuration register 1

Address: 34h
Type: RW

Table 76. Tx frame configuration register 1

Bit	Name	Default	Function	Comment
7:0	ntx<12:5>	0x000	Number of full bytes to be transmitted	Maximum supported number of bytes is 8191

5.17.54 Tx frame configuration register 2

Address: 35h
Type: RW

Table 77. Tx frame configuration register 2

Bit	Name	Default	Function	Comment
7:3	ntx<4:0>	0x000	Number of full bytes to be transmitted	Maximum supported number of bytes is 8191
2:0	nbtx<2:0>	0x0	Number of bits transmitted after the last full byte. Nbtx<2:0> = 0 only full bytes to be transmitted	The valid bits are in the LSB part. Applicable for NFC-A: • bit oriented anti-collision frame in case last byte is split byte • Tx is done without parity bit generation • CE: 4-bit ACK, NACK for NFC-A T2T

5.17.55 FIFO status register 1

Address: 36h
Type: RO

Table 78. FIFO status register 1

Bit	Name	Default	Function	Comment
7:0	fifo_b<7:0>	0x00	Number of bytes currently in the FIFO (LSB part)	Valid range: 0 to 255

Note: At power-up, at start of data reception, and after the direct commands set default and clear FIFO, the content of this register is set to 0.

5.17.56 FIFO status register 2

Address: 37h

Type: RO

Table 79. **FIFO status register 2**

Bit	Name	Default	Function	Comment
7	RFU	0	-	-
6	fifo_b<8>	0	Number of bytes currently in the FIFO (MSB part)	-
5	fifo_unf	0	FIFO underflow	Readout from an empty FIFO or FIFO or too fast FIFO read (>10 Mb/s)
4	fifo_ovr	0	FIFO overflow	Write into a full FIFO or too fast FIFO write (>10 Mb/s)
3:1	fifo_lb<2:0>	0	Number of bits in last FIFO byte in case it was not complete	In case of incomplete byte the LSB part is valid In case of I_hfe the bits may be invalid
0	np_lb	0	Parity bit is missing in last byte	The bit is set if the last byte was complete with 8 data bits and only the parity bit is missing. This is a framing error. In case of I_hfe the bit may be invalid

Note: At power-up, at start of data reception, and after the direct commands set default and clear FIFO, the content of this register is set to 0.

5.17.57 Rx collision display register

Address: 38h

Type: RO

Table 80. **Rx collision display register**

Bit	Name	Default	Function	Comment
7:4	c_byte<3:0>	0x0	Position of the first bit collision (number of bytes and bits)	The Collision display register range covers NFC-A bit oriented anti-collision frame. In case collision (or framing error which is interpreted as collision) happens in a longer frame, the collision register is not set. In case of I_hfe the bits may be invalid.
3:1	c_bit<2:0>	0x0		
0	c_pb	0	Collision in parity bit	Error, reported in case it is the first collision detected In case of I_hfe the bit may be invalid.

5.17.58 IRQ mask register 1

Address: 39h
Type: RW

Table 81. **IRQ mask register 1**

Bit	Name	Default	Function	Comment
7	M_subc_start	0	Mask IRQ due to subcarrier start	-
6	M_col	0	Mask IRQ due to bit collision	-
5	M_wl	0	Mask IRQ due to FIFO water level	-
4	M_rx_rest	0	Mask IRQ due to automatic reception restart	-
3	M_rxe	0	Mask IRQ due to end of receive	-
2	M_rxs	0	Mask IRQ due to start of receive	-
1	M_txe	0	Mask IRQ due to end of transmission	-
0	M_rx_err	0	Mask IRQ due to Reception error	-

5.17.59 IRQ mask register 2

Address: 3Ah
Type: RW

Table 82. **IRQ mask register 2**

Bit	Name	Default	Function	Comment
7	M_gpe	0	Mask IRQ due to general purpose timer expire	-
6	M_nre	0	Mask IRQ due to No-response timer expire	-
5	M_wpt_stop	0	Mask IRQ due to WPT Stop detection	-
4	M_wpt_fod	0	Mask IRQ due to WPT Foreign object detection	-
3	RFU	0	RFU	-
2	M_ce_sc	0	Mask IRQ due to CE state change	-
1	M_rxe_cea	0	Mask IRQ due to end of receive, device is handling the response	-
0	M_nfct	0	Mask IRQ when bit rate was recognized	-

5.17.60 IRQ mask register 3

Address: 3Bh
Type: RW

Table 83. **IRQ mask register 3**

Bit	Name	Default	Function	Comment
7	M_wutme	0	Mask IRQ after each WU measurement event (Calibration, wake-up measurement, Recal.)	-
6	M_eof	0	Mask IRQ due to detection of external field drop below Target activation level	-
5	M_eon	0	Mask IRQ due to detection of external field higher than Target activation level	-
4	M_dct	0	Mask IRQ due to termination of direct command	-
3	M_wuq	0	Mask IRQ due to WU Q-channel Measurement	-
2	M_wui	0	Mask IRQ due to WU I-channel Measurement	-
1	M_wut	0	Mask IRQ due to wake-up timer	-

Bit	Name	Default	Function	Comment
0	M_osc	0	Mask IRQ when oscillator is ready	-

5.17.61 IRQ status register 1

Address: 3Ch
Type: RO

Table 84. IRQ status register 1

Bit	Name	Default	Function	Comment
7	I_subc_start	0	IRQ due to subcarrier start	-
6	I_col	0	IRQ due to bit collision	-
5	I_wl	0	IRQ due to FIFO water level	-
4	I_rx_rest	0	IRQ due to automatic reception restart	-
3	I_rxe	0	IRQ due to end of receive	-
2	I_rxs	0	IRQ due to start of receive	-
1	I_txe	0	IRQ due to end of transmission	-
0	I_rx_err	0	IRQ due to Reception error	-

5.17.62 IRQ status register 2

Address: 3Dh
Type: RO

Table 85. IRQ status register 2

Bit	Name	Default	Function	Comment
7	I_gpe	0	IRQ due to general purpose timer expire	-
6	I_nre	0	IRQ due to No-response timer expire	-
5	I_wpt_stop	0	IRQ due to WPT Stop detection	-
4	I_wpt_fod	0	IRQ due to WPT Foreign object detection	-
3	RFU	0	RFU	-
2	I_ce_sc	0	IRQ due to CE state change	-
1	I_rxe_cea	0	IRQ due to end of receive, device is handling the response	-
0	I_nfct	0	IRQ when bit rate was recognized	-

5.17.63 IRQ status register 3

Address: 3Eh
Type: RO

Table 86. IRQ status register 3

Bit	Name	Default	Function	Comment
7	I_wutme	0	IRQ after each WU measurement event (Calibration, wake-up measurement, Recalibration)	-
6	I_eof	0	IRQ due to detection of external field drop below Target activation level	-
5	I_eon	0	IRQ due to detection of external field higher than Target activation level	-
4	I_dct	0	IRQ due to termination of direct command	-

Bit	Name	Default	Function	Comment
3	I_wuq	0	IRQ due to WU Q-channel Measurement	-
2	I_wui	0	IRQ due to WU I-channel Measurement	-
1	I_wut	0	IRQ due to wake-up timer	-
0	I_osc	0	IRQ when oscillator is ready (represents all_ok-including agd_ok and wait_ok)	-

5.17.64 IC identify register

Address: 3Fh
Type: RO

Table 87. IC identify register

Bit	Name	Default	Function	Comment
7:3	ic_type<4:0>	0x16 10110b	5-bit IC type code Code for ST25R500: 10110	5-bit IC type code
2:0	ic_rev<2:0>	0	IC revision code 001: rev 1.1	3-bit IC revision code

5.17.65 Status register 1

Address: 40h
Type: RO

Table 88. Status register 1

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	wut_on	0	1: WU timer is running	-
5	agd_ok	0	1: AGD stable	-
4	osc_ok	0	1: Oscillator stable	-
3	RFU	0	RFU	-
2	tmp_on	0	1: Oscillator temporary enabled in ce operation due to external field	-
1	efd_out	0	1: External field above the threshold	Only valid if efd_on = 1
0	efd_on	0	1: External field detector active	-

5.17.66 Status register 2

Address: 41h
Type: RO

Table 89. Status register 2

Bit	Name	Default	Function	Comment
7	subc_on	0	1: Subcarrier detected	-
6	gpt_on	0	1: General purpose timer is running	-
5	nrt_on	0	1: No-response timer is running	-
4	mrt_on	0	1: Mask receive timer is running	-
3	rx_act	0	1: Receive is receiving a message	-
2	rx_on	0	1: Receive decoder is enabled	-
1	tx_on	0	1: Transmission is active (data)	-
0	RFU	**0**	RFU	-

5.17.67 Static status register 1

Address: 42h
Type: RO

Table 90. Static status register 1

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	s_eof	0	External field below efd_th	-
5	s_eon	0	External field above efd_th	-
4	s_dct	0	Command terminated	-
3	RFU	0	RFU	-
2	RFU	0	RFU	-
1	RFU	0	RFU	-
0	RFU	0	RFU	-

Note: Each bit can be individually cleared by setting it to 1.

5.17.68 Static status register 2

Address: 43h
Type: RO

Table 91. Static status register 2

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	RFU	0	RFU	-
5	s_rx_err	0	Reception error detected	-
4	s_rxe	0	Reception ended	-
3	s_rx_rest	0	Reception restarted	-
2	s_col	0	Collision detected	-

Bit	Name	Default	Function	Comment
1	s_rxs	0	Data reception started	-
0	RFU	**0**	RFU	-

Note: Each bit can be individually cleared by setting it to 1.

5.17.69 Static status register 3

Address: 44h
Type: RO

Table 92. Static status register 3

Bit	Name	Default	Function	Comment
7	s_crc	0	CRC error	-
6	s_par	0	Parity error	-
5	s_hfe	0	Hard framing error	-
4	s_sfe	0	Soft framing error	-
3:0	RFU<3:0>	0	RFU	-

Note: Status bits are cleared at the start of reception.
Each bit can be individually cleared by setting it to 1

5.17.70 Card emulation status register 1

Address: 45h

Type: RO

Table 93. Card emulation status register 1

Bit	Name	Default	Function	Comment
7:6	nfc_rate_lock<1:0>	0	00: Bit rate detection not locked 01: Rx is locked to NFC_A 10: Rx is locked to NFC_F	-
5:4	nfc_rate<1:0>	0	Detected bit rate	Result of automatic bit rate detection in the bit rate detection operation
3:0	ce_state<3:0>	0	States according to NFC Forum Activity	NFC_A CE states (NFC-A states) After entering ACTIVE or ACTIVE* state, the MCU handles all commands, The NFC212/424 kb CE is always in idle state; It responses to SENSF_REQ anytime it is received and NFC212/424-kb CE operation is enabled. Register is writable and user can use it to advance the states based on received frames (valid for normal NFC-A and NFC-F - om = 1 or om = 3)

Table 94. Card emulation states

CE_state<3:0>	WU time (wu_en=1) nominal (ms)
0x0	POWER OFF
0x1	IDLE
0x2	READY_A
0x3	READY_A’
0x5	ACTIVE_A
0x6	CARD_EMU_4A
0x9	SLEEP_A
0xA	READY_A*
0xB	READY_A’*
0xD	ACTIVE_A*
0xF	CE_F (1)
Others	RFU

1. *READY_F is combined with CARD_EMULATOR_3*

5.17.71 Card emulation status register 2

Address: 46h
Type: RO

Table 95. Card emulation status register 2

Bit	Name	Default	Function	Comment
7:0	rats_param<7:0>	0	Content of PARAM of RATS command as previously received.	-

5.17.72 Wake up status register

Address: 47h
Type: RO

Table 96. Wake up status register

Bit	Name	Default	Function	Comment
7	RFU	1	RFU	-
6	q_tdi2	0	1 in case q_adc is above q_ref + q_diff	-
5	q_tdi1	0	1 in case q_adc is between or equals q_ref - q_diff, q_ref + q_diff	-
4	q_tdi0	0	1 in case q_adc is below q_ref - q_diff	-
3	RFU	0	RFU	-
2	i_tdi2	0	1 in case i_adc is above i_ref + i_diff	-
1	i_tdi1	0	1 in case i_adc is between or equals i_ref - i_diff, i_ref + i_diff	-
0	i_tdi0	0	1 in case i_adc is below i_ref - i_diff	-

5.17.73 Analog display register 1

Address: 48h
Type: RO

Table 97. Analog display register 1

Bit	Name	Default	Function	Comment
7	i_lim	0	1: VDD_DR regulator in current limit mode	-
6:0	regc<6:0>	0x7F	Actual regulator control setting	-

5.17.74 Analog display register 2

Address: 49h
Type: RO

Table 98. Analog display register 2

Bit	Name	Default	Function	Comment
7:4	RFU<3:0>	0	RFU	-
3:0	afe_gain<3:0>	0	Read operation and wake-up operation: Actual AFE Rx gain CE operation: AFE Preamplifier gain	-

5.17.75 RSSI display register 1

Address: 4Ah
Type: RO

Table 99. RSSI display register 1

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:0	rssi_i<6:0>	0	Reader operation: I channel RSSI (7 bit) CE operation: Envelope after AGC, valid 150 µs after field on event (I_eon) when the device is in ready mode, or oscillator stable (I_osc) when the device is in PD mode.	-

5.17.76 RSSI display register 2

Address: 4Bh
Type: RO

Table 100. RSSI display register 2

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6:0	rssi_q<6:0>	0	Reader operation: Q Channel RSSI	-

5.17.77 Sense RF display register

Address: 4Ch
Type: RO

Table 101. Sense RF display register

Bit	Name	Default	Function	Comment
7:0	sense_adc<7:0>	0	Result of sense RF direct command	-

5.17.78 AWS configuration register 1

Address: 4Dh
Type: RW

Table 102. AWS configuration register 1

Bit	Name	Default	Function	Comment
7	dig_aws_en	0	1: Digital filter in AWS path	-
6	dyn_ilim_aws	1	1: Dynamic limiter for AWS mode	-
5	dyn_sink_offset	1	1: Dynamic offset in Act. sink	-
4	dyn_pass_sink	1	1: Dynamic passive sink	-
3	sc_prot_en	1	1: Enable short circuit protection	-
2	sink_offset_en	1	1: Enable Active Sink offset	-
1	act_sink_en	1	1: Enable Active sink	-
0	RFU	0	RFU	-

5.17.79 AWS configuration register 2

Address: 4Eh
Type: RW

Table 103. **AWS configuration register 2**

Bit	Name	Default	Function	Comment
7:4	am_fall<3:0>	0x7	Filter for AM reference (AWS) fall time	-
3:0	am_rise<3:0>	0x7	Filter for AM reference (AWS) rise time	-

5.17.80 AWS timing register 1

Address: 4Fh
Type: RW

Table 104. **AWS timing register 1**

Bit	Name	Default	Function	Comment
7:4	tentx1<3:0>	3	Time	In f_C periods
3:0	tdres1<3:0>	3	Time	In f_C periods

5.17.81 AWS timing register 2

Address: 50h
Type: RW

Table 105. **AWS timing register 2**

Bit	Name	Default	Function	Comment
7:4	tpasssinkx1<3:0>	0	Time	In f_C periods
3:0	tsinkoff1<3:0>	0	Time	In f_C periods

5.17.82 AWS timing register 3

Address: 51h
Type: RW

Table 106. **AWS timing register 3**

Bit	Name	Default	Function	Comment
7:4	tilim2<3:0>	0xF	Time	In f_C periods
3:0	tdres2<3:0>	3	Time	In f_C periods

5.17.83 AWS timing register 4

Address: 52h
Type: RW

Table 107. **AWS timing register 4**

Bit	Name	Default	Function	Comment
7:4	tpasssinkx2<3:0>	0	Time	In f_C periods
3:0	tsinkoff2<3:0>	0	Time	In f_C periods

5.17.84 Overshoot protection register

Address: 53h
Type: RW

Table 108. Overshoot protection register

Bit	Name	Default	Function	Comment
7:0	ov_pattern<7:0>	0	Bit pattern controlling low to high transition	Bit Value 0: Drive with d_res impedance Bit Value 1: Drive using md_res impedance LSB is transmitted first Pattern applies only if res_am=1

5.17.85 Undershoot protection register

Address: 54h
Type: RW

Table 109. Undershoot protection register

Bit	Name	Default	Function	Comment
7:0	un_pattern<7:0>	0	Bit pattern controlling high to low transition	Bit value 0: Drive with md_res impedance Bit value 1: Drive using d_res impedance LSB is transmitted first Pattern applies only if res_am=1

5.17.86 External field detector

Address: 57h
Type: RW

Table 110. External field detector

Bit	Name	Default	Function	Comment
7:4	efd_dt<3:0>	2	Deactivation threshold	-
3:0	efd_at<3:0>	3	Activation threshold	-

Table 111. External field detector threshold

efd_dt<3:0> efd_at<3:0>	efd_dt3 efd_at3	efd_dt2 efd_at2	efd_dt1 efd_at1	efd_dt0 efd_at0	V_RFI1/2 (mVp)
0x0	0	0	0	0	50
0x1	0	0	0	1	100
0x2	0	0	1	0	150
0x3	0	0	1	1	200
0x4	0	1	0	0	250
0x5	0	1	0	1	300
0x6	0	1	1	0	350
0x7	0	1	1	1	400
0x8	1	0	0	0	12.5
0x9	1	0	0	1	25

efd_dt<3:0> efd_at<3:0>	efd_dt3 efd_at3	efd_dt2 efd_at2	efd_dt1 efd_at1	efd_dt0 efd_at0	V_RFI1/2 (mVp)
0xA	1	0	1	0	37.5
0xB	1	0	1	1	50
0xC	1	1	0	0	62.5
0xD	1	1	0	1	75
0xE	1	1	1	0	87.5
0xF	1	1	1	1	100

Note: efd_dt3 or efd_at3 = 1: Additional pre-amplifier enabled, which causes increased current consumption during power-down mode when card emulation is enabled (CE).

5.18 Test registers

Table 112. Test registers

Type	Address(hex)	Register name	Type , , power domain
Test register	08	ADC to CE memory register	RW, PD
	0E	Oscillator timing control register	RW, PD
	13	Manual timing register	RW, PD
	14	Diagnostic measurement register	RW, PD
	1E	Overlap control register	RW, PD
	30	Receive start timer display register 1	RO, RD
	31	Receive start timer display register 2	RO, RD
	32	Receive end timer display register 1	RO, RD
	33	Receive end timer display register 2	RO, RD

5.18.1 ADC to CE Memory register

Address: Test register 08h

Type: RW

Table 113. ADC to CE memory register

Bit	Name	Default	Function	Comment
7:4	RFU<3:0>	0	RFU	-
3	adc_cemem_src	0	0: ADC I-channel (6 bit) 1: Correlator input I-channel (8 bit)	Input source selection
2	adc_cemem_rate<1:0>	0	0: 13.56 MHz 1: 6.78 MHz	Sampling rate selection
1:0	adc_cemem	0	00: sampling disabled 01: sampling falling edge 10: sampling rising edge 11: sampling falling and rising edge	Select sampling of the modulation signal

5.18.2 Oscillator timing control register

Address: Test register 0Eh
Type: RW

Table 114. Oscillator timing control register

Bit	Name	Default	Function	Comment
7:6	RFU<1:0>	0	RFU	-
5:0	wait_ok_count_set <5:0>	0	Additional oscillator startup delay in 38.11 µs steps	-

5.18.3 Manual timing register

Address: Test register 13h
Type: RW

Table 115. Manual timing register

Bit	Name	Default	Function	Comment
7	RFU	0	RFU	-
6	man_wait_ok	0	0: disable delay 1: enable delay	Additional oscillator startup delay (man_wait_count_set)
3:0	RFU<3:0>	0	RFU	-

5.18.4 Diagnostic measurement register

Address: Test register 14h
Type: RW

Table 116. Diagnostic measurement register

Bit	Name	Default	Function	Comment
7:3	RFU<4:0>	0	RFU	-
2	discon_tad_out	0	1: TAD1 and TAD2 pad output is disconnected during diagnostic measurement	To be set to 1 during diagnostic measurements
1:0	RFU<1:0>	0	RFU	-

5.18.5 Overlap control register

Address: Test register 1Eh
Type: RW

Table 117. Overlap control register

Bit	Name	Default	Function	Comment
7:3	RFU<4:0>	0	RFU	-
2:1	rfo_non_mode<1:0>	0x00	RFO1/2 non-overlap mode	01: Both RFO low when Tx stop 10: Both RFO high when Tx stop 00: RFU 11: RFU
0	rfo_non_en	0	1: Enable non-overlapping between RFO1 and RFO2	-

5.18.6 Receive start timer display register 1

Address: Test register 30h
Type: RO

Table 118. Receive start timer display register 1

Bit	Name	Default	Function	Comment
7:0	t_rxs <15:8>	0x00	Time (based on NRT setting) between transmission end (I_txe) to start of reception (I_rxs)	msb part

Note: t_rxs is displayed for each reception without error.

5.18.7 Receive start timer display register 2

Address: Test register 31h
Type: RO

Table 119. Receive start timer display register 2

Bit	Name	Default	Function	Comment
7:0	t_rxs <7:0>	0x00	Time (based on NRT setting) between transmission end (I_txe) to start of reception (I_rxs)	lsb part

Note: t_rxs is displayed for each reception without error.

5.18.8 Receive end timer display register 1

Address: Test register 32h
Type: RO

Table 120. Receive end timer display register 1

Bit	Name	Default	Function	Comment
7:0	t_rxe <15:8>	0x00	Time (based on NRT setting) between transmission end (I_txe) to end of reception (I_rxe)	msb part

Note: t_rxe is displayed for each reception without error.

5.18.9 Receive end timer display register 2

Address: Test register 33h
Type: RO

Table 121. Receive end timer display register 2

Bit	Name	Default	Function	Comment
7:0	t_rxe <7:0>	0x00	Time (based on NRT setting) between transmission end (I_txe) to end of reception (I_rxe)	lsb part

Note: t_rxe is displayed for each reception without error.

6 Electrical characteristics

6.1 Absolute maximum ratings

Any stress beyond the limits listed in the following table may permanently damage it. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in following table is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 122. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{DD}(1)	Positive supply voltage	-0.3	6.5	V	Pin numbers: 13 and 19
V_{DD_IO}(1)	Peripheral communication supply voltage	-0.3	6.5		Pin number: 3
$\Delta(V_{DD} - V_{DD\_TX})$(1)	V_{DD_DIFF}	-0.3	0.3		Pin numbers: 13 and 19
V_{GND}(1)	Negative supply voltage	-0.3	0.3		Pin number: 4, 7, 15, 25, and 33
V_{PIO}(1)	Voltage for peripheral I/O communication pins	-0.3	6.5		Pin number: 1, 2, and 29-32
V_{P5V}(1)	Pin voltage other pins in the 5 V domain	-0.3	6.5		Pin numbers: 6, 9, 11, 12, 14, 16, 18
V_{P3V}(1)	Pin voltage other pins in the 3 V domain	-0.3	4.6		Pin numbers: 20-23, 26, and 27
V_{P1V}(1)	Pin voltage other pins in the 1 V domain	-0.3	2.0		Pin number: 5
V_{RFO}(1)	Maximum voltage on RFO1 and RFO2	-	6.6	V_P	-
T_{Jun}(2)	Junction temperature	-40	135	°C	-
I_{SCR}	LU immunity	-200	200	mA	Norm: JESD78F
HBM(3)	ESD immunity	-2000	2000	V	Norm: JS-001-2024
CDM	ESD immunity	-500	500	V	Norm: JS-002-2022
T_{strg}	Storage temperature	-40	135	°C	-
T_{bod}(4)	Package body temperature	-	260	°C	Norm: IPC/JEDEC J-STD-020F
-	Humidity non-condensing	5	85	%	-
I_{VDD}	Maximum driver current using internal voltage regulator	-	500	mA	-

1. *Referenced to V_{SS}(EP).*
2. *Provide good thermal management to ensure that junction temperature remains below the specified value.*
3. *Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with ANSI/ESDA/JEDEC JS-001 standard, C1 = 100 pF, R1 = 1500 Ω).*
4. *Reflow peak soldering temperature (body temperature) is specified according to the IPC/JEDEC J-STD-020 “Moisture/ Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”.*

6.2 Operating conditions

Table 123. Operating condition

Symbol	Parameter	Min	Max	Unit	Note
V_{DD} (1)	Positive supply voltage	2.7	5.5	V	Pin number 13, 19
V_{DD_IO} (1)(2)	Peripheral communication supply voltage	1.65	5.5		Pin number 3
$\Delta(V_{DD} - V_{DD\_TX})$	V_{DD_DIFF}	-0.2	0.2		Pin numbers: 13 and 19
V_{PIO} (1)	Voltage for peripheral IO communication pins	0	5.5		Pin number 1, 2, 29-32
V_{P5V} (1)	Pin voltage other pins in the 5 V domain	0	5.5		Pin number 6, 9, 11, 12, 14, 16, 18
V_{P3V} (1)	Pin voltage other pins in the 3 V domain	0	3.6		Pin number 20-23, 26, 27
V_{P1V} (1)	Pin voltage other pins in the 1 V domain	0	1.4		Pin number 5
V_{RFI_A}	RFI input amplitude	0.15	3	V_{PP}	The maximum value must not exceed V_{DD_A} voltage.
T_{Jun}	Junction temperature	-40	135	°C	-
V_{OSC_PP} (1)	Oscillator amplitude in steady state	1	3	V_{PP}	-

1. *Referenced to V_{SS}*
2. *$V_{DD\_IO} \leq V_{DD}$*

6.3 Electrical specification

Table 124. ST25R500 electrical characteristics (V_{DD} = V_{DD_TX} = 5.5 V, V_{DD_IO} = 5.5 V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{RESET}	Supply current in hold RESET: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C(1)	-	0.03	2	µA
		T_{Jun} = 25 °C(1)	-	0.2	2	
		T_{Jun} = 85 °C(1)(2)	-	1.5	15	
		T_{Jun} = 125 °C(1)(2)	-	8.5	40	
I_{PD}	Supply current in power-down mode: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C(3)	-	1.3	3	
		T_{Jun} = 25 °C(3)	-	2.2	7	
		T_{Jun} = 85 °C(2)(3)	-	8.2	35	
		T_{Jun} = 125 °C(2)(3)	-	35	110	
I_{WU}	Supply current in wake-up mode: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C(4)	-	2.0	8	
		T_{Jun} = 25 °C(4)	-	2.9	8	
		T_{Jun} = 85 °C(2)(4)	-	9	35	
		T_{Jun} = 125 °C(2)(4)	-	36.1	110	
I_{CE}	Supply current in card emulation mode during power-down: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(5)	-	5	12	
		T_{Jun} = 25 °C(5)	-	5.7	12	
		T_{Jun} = 85 °C(2)(5)	-	12.4	40	
		T_{Jun} = 125 °C(2)(5)	-	42.6	126	
I_{CE}	Supply current in card emulation mode during power down with high field detector gain: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(6)	-	41.5	100	
		T_{Jun} = 25 °C(6)	-	45	100	
		T_{Jun} = 85 °C(2)(6)	-	55.7	110	
		T_{Jun} = 125 °C(2)(6)	-	90	190	
I_{RD}	Supply current in ready mode: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C (7)	-	2.7	4	mA
		T_{Jun} = 25 °C(7)	-	3	4	
		T_{Jun} = 85 °C(2)(7)	-	3.2	8	
		T_{Jun} = 125 °C(2)(7)	-	3.5	8	
		T_{Jun} = 135 °C(2)(7)	-	3.6	8	
I_{ALL}	Supply current all active: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(8)	-	11.7	20	
		T_{Jun} = 25 °C(8)	-	12	20	
		T_{Jun} = 85 °C(2)(8)	-	12.5	20	
		T_{Jun} = 125 °C(2)(8)	-	13	20	
		T_{Jun} = 135 °C(2)(8)	-	13.5	20	
R_{RFO}	RFO1 and RFO2 driver output resistance	T_{Jun} = -40 °C to 135 °C(9)(10)(11)	-	0.63	1.5	Ω
R_{RFI}	RFI input resistance	T_{Jun} = -40 °C to 135 °C(9)(12)	-	11.1	15	kΩ
V_{POR}	Power on reset voltage	T_{Jun} = -40 °C to 135 °C(9)(12)	-	0.8	1.3	V
V_{AGD}	AGD voltage	T_{Jun} = -40 °C to 135 °C(9)(12)	1.44	1.5	1.56	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{RESET}	Minimal duration of RESET in high state	T_{Jun} = -40 °C to 135 °C[9][12]	10	-	-	us
t_{BOOT}	Time between power On/reset high-to-low transition and first SPI operation	T_{Jun} = -40 °C to 135 °C[9][12]	70	140	900	us
R_{TAD}	Test output pin and GPIO pin resistance in push-pull configuration	T_{Jun} = -40 °C to 135 °C[9][12][13]	-	54	90	Ω
R_{GPIO}	GPIO pin output resistance in pull-down configuration	T_{Jun} = -40 °C to 135 °C GPIO_p = 0x0 [9][10][14]	-	0.3	1.1	Ω

1. *Reset pin set to high level.*
2. *Evaluated by characterization - not tested in production.*
3. *Registers are at default state.*
4. *Register 00h set to 01h, while other registers are in their default state.*
5. *Register 00h set to 04h, while other registers are in their default state.*
6. *Register 00h set to 04h and register 57h set to FFh, while other registers are in their default state.*
7. *Register 00h set to 08h, while other registers are in their default state.*
8. *Register 00h set to 78h and register 03h set to 0Fh, while other registers are in their default state.*
9. *V_{DD} = 6 V instead of 5.5 V.*
10. *Tested at T_{Junc} = 25 °C in production. Other temperatures are evaluated by characterization - not tested in production.*
11. *Register 00h set to 78h and register 03h to 20h, while other registers are at default state, and XTI pin is forced to GND.*
12. *Tested in production at T_{Junc} = -40 °C and 25 °C . Other temperatures are evaluated by characterization - not tested in production.*
13. *Register 00h set to 08h, register 07h set to D1h register 08h set either to 00h or 0fh, while other registers are set at default state.*
14. *Register 00h set to 08h, register 08h set to 03h while other registers are at default state.*

Table 125. ST25R500 electrical characteristics (V_{DD} = V_{DD_TX} = 3.3 V, V_{DD_IO} = 3.3 V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{RESET}	Supply current in hold RESET: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C[1]	-	0.02	1	µA
		T_{Jun} = 25 °C[1]	-	0.07	1	
		T_{Jun} = 85 °C[1][2]	-	0.8	8	
		T_{Jun} = 125 °C[1][2]	-	5	30	
I_{PD}	Supply current in power-down mode: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C[3]	-	0.8	2	
		T_{Jun} = 25 °C[3]	-	1.4	5	
		T_{Jun} = 85 °C[2][3]	-	6.6	30	
		T_{Jun} = 125 °C[2][3]	-	30.5	90	
I_{WU}	Supply current in wake-up mode: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C[4]	-	1.5	3	
		T_{Jun} = 25 °C[4]	-	2	6	
		T_{Jun} = 85 °C[2][4]	-	7.3	30	
		T_{Jun} = 125 °C[2][4]	-	31.1	90	
I_{CE}	Supply current in card emulation mode during power-down: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C[5]	-	4.2	7	
		T_{Jun} = 25 °C[5]	-	4.6	10	
		T_{Jun} = 85 °C[2][5]	-	10	35	
		T_{Jun} = 125 °C[2][5]	-	35.7	100	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CE}	Supply current in card emulation mode during power-down with high field detector gain: $V_{DD} + V_{DD\_TX} + V_{DD\_IO}$	T_{Jun} = -40 °C[6]	-	34.7	75	µA
		T_{Jun} = 25 °C[6]	-	37.7	75	
		T_{Jun} = 85 °C[2][6]	-	46.5	90	
		T_{Jun} = 125 °C[2][6]	-	75.8	153	
I_{RD}	Supply current in ready mode: $V_{DD} + V_{DD\_TX} + V_{DD\_IO}$	T_{Jun} = -40 °C[7]	-	2.5	4	mA
		T_{Jun} = 25 °C[7]	-	2.8	4	
		T_{Jun} = 85 °C[2][7]	-	3	6	
		T_{Jun} = 125 °C[2][7]	-	3.3	7	
		T_{Jun} = 135 °C[2][7]	-	3.3	7	
I_{ALL}	Supply current all active: $V_{DD} + V_{DD\_TX} + V_{DD\_IO}$	T_{Jun} = -40 °C[8]	-	10.9	15	
		T_{Jun} = 25 °C[8]	-	11.3	15	
		T_{Jun} = 85 °C[2][8]	-	11.7	17	
		T_{Jun} = 125 °C[2][8]	-	12	17	
		T_{Jun} = 135 °C[2][8]	-	12.2	17	
R_{RFO}	RFO1 and RFO2 driver output resistance	T_{Jun} = -40 °C to 135 °C[2][9]	-	1	2	Ω
R_{RFI}	RFI input resistance	T_{Jun} = -40 °C to 135 °C[2]	-	11.1	15	kΩ
V_{POR}	Power on reset voltage	T_{Jun} = -40 °C to 135 °C[10]	-	0.8	1.3	V
V_{AGD}	AGD voltage	T_{Jun} = -40 °C to 135 °C[10]	1.44	1.5	1.56	V
t_{RESET}	Minimal duration of RESET in high state	T_{Jun} = -40 °C to 135 °C[2]	10	-	-	us
t_{BOOT}	Time between Power On/RESET high-to-low transition and first SPI operation	T_{Jun} = -40 °C to 135 °C[2]	70	140	900	us
R_{TAD}	Test output pin and GPIO pin resistance in Push-Pull configuration	T_{Jun} = -40 °C to 135°C[2][11]	-	64	110	Ohm
R_{GPIO}	GPIO pin output resistance in pull-down configuration	T_{Jun} = -40 °C to 135 °C GPIO_p = 0x0 [2][12]	-	0.3	1.1	Ohm

1. *Reset pin set to high level.*
2. *Evaluated by characterization - not tested in production.*
3. *Registers set at their default state.*
4. *Register 00h set to 01h, while other registers are set at default state.*
5. *Register 00h set to 04h, while other registers are set at default state.*
6. *Register 00h set to 04h and Register 57h to FFh, while other registers are set at default state.*
7. *Register 00h set to 08h, while other registers are set at default state.*
8. *Register 00h set to 78h and Register 03h to 0Fh, while other registers are set at default state.*
9. *Register 00h set to 78h and Register 03h to 20h, , while other registers are set at default state,and XTI pin is forced to GND.*
10. *Tested at T_{Junc} = -40° C and 25 °C in production. Other temperatures are evaluated by characterization - not tested in production.*
11. *Register 00h set to 08h, register 07h set to D1h, register 08h set to either 00h or 0Fh, while other registers are at their default state.*
12. *Register 00h set to 08h, register 08h set to 03h, while other registers are at their default state*

Table 126. ST25R500 electrical characteristics (V_{DD} = V_{DD_TX} = 2.7 V, V_{DD_IO} = 2.7 V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{RESET}	Supply current in hold RESET: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C(1)	-	0.02	1	µA
		T_{Jun} = 25 °C(1)	-	0.06	1	
		T_{Jun} = 85 °C(1)(2)	-	0.7	6	
		T_{Jun} = 125 °C(1)(2)	-	4.5	25	
I_{PD}	Supply current in power-down mode: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °(3)	-	0.7	2	
		T_{Jun} = 25 °C(3)	-	1.2	5	
		T_{Jun} = 85 °C(2)(3)	-	6.3	30	
		T_{Jun} = 125 °C(2)(3)	-	29.3	85	
I_{WU}	Supply current in wake-up mode: V_{DD} + V_{DD_TX}	T_{Jun} = -40 °C (4)	-	1.3	3	
		T_{Jun} = 25 °C(4)	-	1.8	6	
		T_{Jun} = 85 °C(2)(4)	-	6.9	30	
		T_{Jun} = 125 °C(2)(4)	-	29.9	85	
I_{CE}	Supply current in card emulation mode during power-down: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(5)	-	4	7	
		T_{Jun} = 25 °C(5)	-	4.3	8	
		T_{Jun} = 85 °C(2)(5)	-	9.5	35	
		T_{Jun} = 125 °C(2)(5)	-	34.2	100	
I_{CE}	Supply current in card emulation mode during power-down with high field detector gain: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(6)	-	33.1	70	
		T_{Jun} = 25 °C(6)	-	36.1	70	
		T_{Jun} = 85 °C(2)(6)	-	44.7	90	
		T_{Jun} = 125 °C(2)(6)	-	72.7	146	
I_{RD}	Supply current in ready mode: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(7)	-	2.2	3	mA
		T_{Jun} = 25 °C(7)	-	2.4	3	
		T_{Jun} = 85 °C(2)(7)	-	2.6	6	
		T_{Jun} = 125 °C(2)(7)	-	3	6	
		T_{Jun} = 135 °C(2)(7)	-	3	6	
I_{ALL}	Supply current all active: V_{DD} + V_{DD_TX} + V_{DD_IO}	T_{Jun} = -40 °C(8)	-	10.4	15	
		T_{Jun} = 25 °C(8)	-	10.9	15	
		T_{Jun} = 85 °C(2)(8)	-	11.3	17	
		T_{Jun} = 125 °C(2)(8)	-	11.6	17	
		T_{Jun} = 135 °C(2)(8)	-	11.7	17	
R_{RFO}	RFO1 and RFO2 driver output resistance	T_{Jun} = -40 °C to 135 °C(2)(9)	-	1.2	2.5	Ω
R_{RFI}	RFI input resistance	T_{Jun} = -40 °C to 135 °C(2)	-	11.1	15	kΩ
V_{POR}	Power on reset voltage	T_{Jun} = -40 °C to 135 °C(10)	-	0.8	1.3	V
V_{AGD}	AGD voltage	T_{Jun} = -40 °C to 135 °C(10)	1.44	1.5	1.56	V
t_{RESET}	Minimal duration of RESET in high state	$_{Jun}$ = -40 °C to 135 °C(2)	10	-	-	us

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{BOOT}	Time between Power On/RESET high-to-low transition and first SPI operation	T_{Jun} = -40 °C to 135°C(2)	70	140	900	us
R_{TAD}	Test output pin and GPIO pin resistance in push-pull configuration	T_{Jun} = -40 °C to 135 °C(2)(11)	-	64	110	Ω
R_{GPIO}	GPIO pin output resistance in pull-down configuration	T_{Jun} = -40 °C to 135 °C GPIO_p = 0x0 (2)(12)	-	0.37	1.1	Ohm

1. *Reset pin set to high level.*
2. *Evaluated by characterization - not tested in production.*
3. *Registers are at default state.*
4. *Register 00h set to 01h, while other registers are at their default state.*
5. *Register 00h set to 04h, while other registers are at their default state.*
6. *Register 00h set to 04h and Register 57h to FFh, while other registers are at their default state.*
7. *Register 00h set to 08h, while other registers are at their default state.*
8. *Register 00h set to 78h and Register 03h to 0Fh, while other registers are at their default state.*
9. *Register 00h set to 78h and Register 03h to 20h, while other registers are at their default state,and XTI pin forced to GND.*
10. *Tested at T_{Junc} = -40 °C and 25 °C in production. Other temperatures are evaluated by characterization - not tested in production.*
11. *Register 00h set to 08h, register 07h set to D1h, register 08h set to either 00h or 0Fh, while other registers are at their default state.*
12. *Register 00h set to 08h, register 08h set to 03h, other registers are at their default state.*

Table 127. V_{DD_IO} supply current

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VDD_IO}	Supply current in reset mode	T_{Jun} = -40 °C(1)	-	0.0008	1	uA
		T_{Jun} = 25 °C(1)	-	0.0041	1	
		T_{Jun} = 85 °C(1)(2)	-	0.082	5	
		T_{Jun} = 125 °C(1)(2)	-	0.8	6	
		T_{Jun} = 135 °C(1)(2)	-	1.4	10	
I_{VDD_IO}	Supply current in ready mode	T_{Jun} = -40 °C(1)	-	0.5	2	
		T_{Jun} = 25 °C(1)	-	0.6	2	
		T_{Jun} = 85 °C(1)(2)	-	0.75	4	
		T_{Jun} = 125 °C(1)(2)	-	1.52	8	
		T_{Jun} = 135 °C(1)(2)	-	2	10	
I_{VDD_IO}	Supply current in reset mode	T_{Jun} = -40 °C(3)	-	0	1	
		T_{Jun} = 25 °C(3)	-	0.001	1	
		T_{Jun} = 85 °C (2)(3)	-	0.06	2	
		T_{Jun} = 125 °C(2)(3)	-	0.61	3	
		T_{Jun} = 135 °C(2)(3)	-	1.1	10	
I_{VDD_IO}	Supply current in ready mode	T_{Jun} = -40 °C(3)	-	0.25	2	
		T_{Jun} = 25 °C(3)	-	0.3	2	
		T_{Jun} = 85 °C(2)(3)	-	0.41	3	
		T_{Jun} = 125 °C(2)(3)	-	1	6	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VDD_IO}	Supply current in ready mode	T_{Jun} = 135 °C(2)(3)	-	1.44	10	uA
I_{VDD_IO}	Supply current in reset mode	T_{Jun} = -40 °C(4)	-	0	1	
		T_{Jun} = 25 °C(4)	-	0.0015	1	
		T_{Jun} = 85 °C(2)(4)	-	0.053	2	
		T_{Jun} = 125 °C(2)(4)	-	0.6	3	
		T_{Jun} = 135 °C(2)(4)	-	1.04	10	
I_{VDD_IO}	Supply current in ready mode	T_{Jun} = -40 °C(4)	-	0.2	1	
		T_{Jun} = 25 °C(4)	-	0.23	1	
		T_{Jun} = 85 °C(2)(4)	-	0.32	2	
		T_{Jun} = 125 °C(2)(4)	-	0.9	3	
		T_{Jun} = 135 °C(2)(4)	-	1.3	10	
I_{VDD_IO}	Supply current in reset mode	T_{Jun} = -40 °C(5)	-	0	1	
		T_{Jun} = 25 °C(5)	-	0	1	
		T_{Jun} = 85 °C(2)(5)	-	0.02	2	
		T_{Jun} = 125 °C(2)(5)	-	0.14	3	
		T_{Jun} = 135 °C(2)(5)	-	0.22	10	
I_{VDD_IO}	Supply current in ready mode(5)	T_{Jun} = -40 °C(5)	-	0.09	1	
		T_{Jun} = 25 °C(5)	-	0.11	1	
		T_{Jun} = 85 °C(2)(5)	-	0.14	2	
		T_{Jun} = 125 °C(2)(5)	-	0.28	3	
		T_{Jun} = 135 °C(2)(5)	-	0.36	10	

1. *V_{DD} = V_{DD_TX} = V_{DD_IO} = 5.5 V*
2. *Evaluated by characterization - not tested in production.*
3. *V_{DD} = V_{DD_TX} = V_{DD_IO} = 3.3 V*
4. *V_{DD} = V_{DD_TX} = V_{DD_IO} = 2.7 V*
5. *V_{DD} = V_{DD_TX} = V_{DD_IO} = 1.65 V*

6.4 DC/AC characteristics for digital inputs and outputs

Table 128. Table 7: Characteristics of CMOS I/Os

Type	Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input	V_{IH}	High level input	See note (1)	0.8 x V_{DD_IO}	-	-	V
	V_{IL}	Low level input voltage	See note (1)	-	-	0.2 x V_{DD_IO}	
	I_{LEAK}	Input leakage current	V_{DD_IO} = 1.65 - 5.5 V	-	-	10	µA
Output	V_{OH}	High level output voltage	See note (1) I_{SOURCE}=1 mA(2)	0.9 x V_{DD_IO}	-	-	V
	V_{OL}	Low level output voltage	See note (1) I_{SOURCE} = 1 mA(2)	-	-	0.1 x V_{DD_IO}	
	$C_{L\text{-}SPI}$	Capacitive load	See note (1)	-	-	50	pF
	R_O	Output resistance	See note (1)	-	60	260	Ω
	R_{PD}	Pull-down resistance pin MISO	See note (1)	7	10	15	kΩ

1. *V_{DD} = 2.7 - 5.5 V and V_{DD_IO} = 1.65 - 5.5 V*
2. *I_{SOURCE} = 0.5 mA when V_{DD_IO} < 2.7 V*

6.5 SPI characteristics

Table 129. SPI characteristics (up to 10 MHz)

Operation	Symbol	Parameter	Condition	Min	Typ	Max	Unit
General[1]	T_{SCLK}	SCLK period	$T_{SCLK} = T_{SCLKL} + T_{SCLKH}$	100	-	-	ns
	T_{SCLKL}	SCLK low	-	45	-	-	
	T_{SCLKH}	SCLK high	-	45	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}	Data in setup time	-	10	-	-	
	T_{DIH}	Data in hold time	-	10	-	-	
	T_{DOD}	Data out delay	C_{Load} < 50 pF	-	20	45	
	T_{DOHZ}	Data out to high impedance delay	C_{Load} < 50 pF	-	20	-	
Read[1]	T_{DOD}	Data out delay	C_{Load} < 50 pF	-	20	45	
	T_{DOHZ}	Data out to high impedance delay	C_{Load} < 50 pF	-	20	-	

1. *V_{DD_IO} = 2.7 V to 5.5 V, V_{DD} = 2.7 V to 5.5 V, with $V_{DD\_IO} \leq V_{DD}$.*

Table 130. SPI characteristics (up to 5 MHz)

Operation	Symbol	Parameter	Condition	Min	Typ	Max	Unit
General[1]	T_{SCLK}	SCLK period	TSCLK = TSCLKL + TSCLKH	200	-	-	ns
	T_{SCLKL}	SCLK low	-	90	-	-	
	T_{SCLKH}	SCLK high	-	90	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}	Data in setup time	-	10	-	-	
	T_{DIH}	Data in hold time	-	10	-	-	
	T_{DOD}	Data out delay	C_{Load} < 50 pF	-	30	90	
	T_{DOHZ}	Data out to high impedance delay	C_{Load} < 50 pF	-	20	-	
Read[1]	T_{DOD}	Data out delay	C_{Load} < 50 pF	-	30	90	
	T_{DOHZ}	Data out to high impedance delay	C_{Load} < 50 pF	-	20	-	

1. *V_{DD_IO} = 1.65 V to 2.7 V, V_{DD} = 2.7 V to 5.5 V, with $V_{DD\_IO} \leq V_{DD}$.*

Figure 20. **SPI timing diagram - General operation**

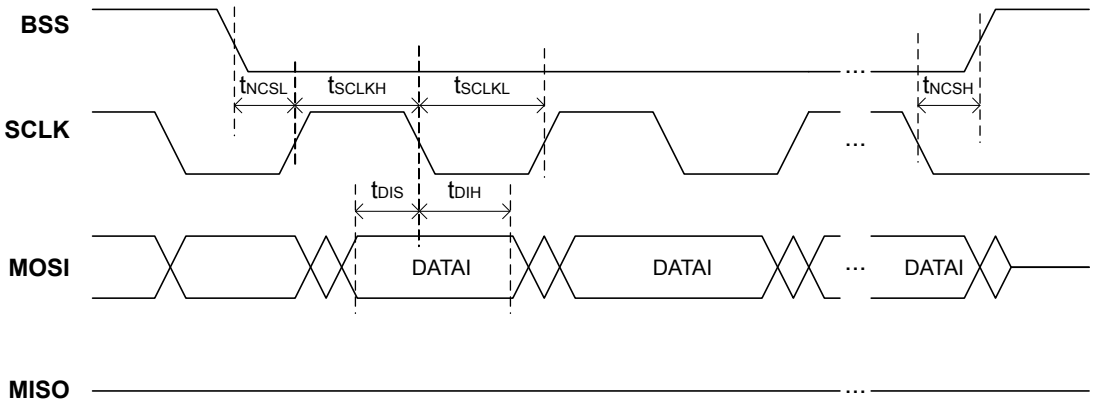
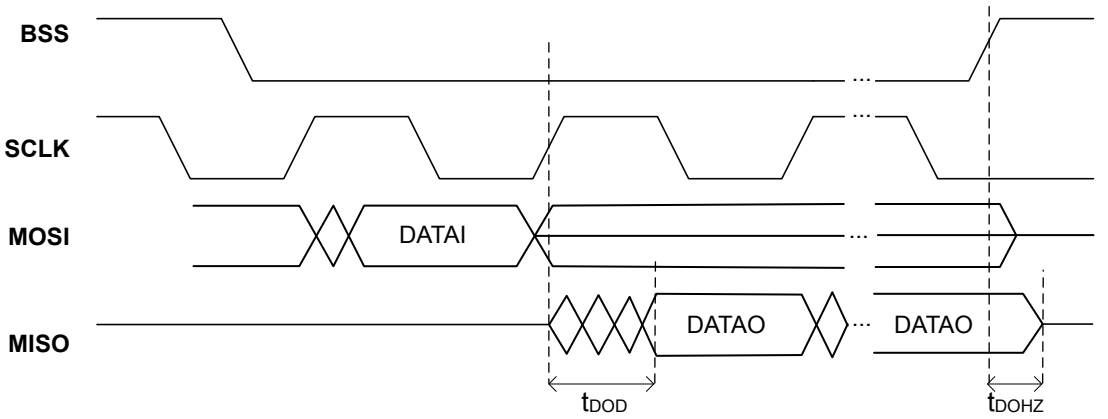


Figure 21. **SPI timing diagram - Read operation**



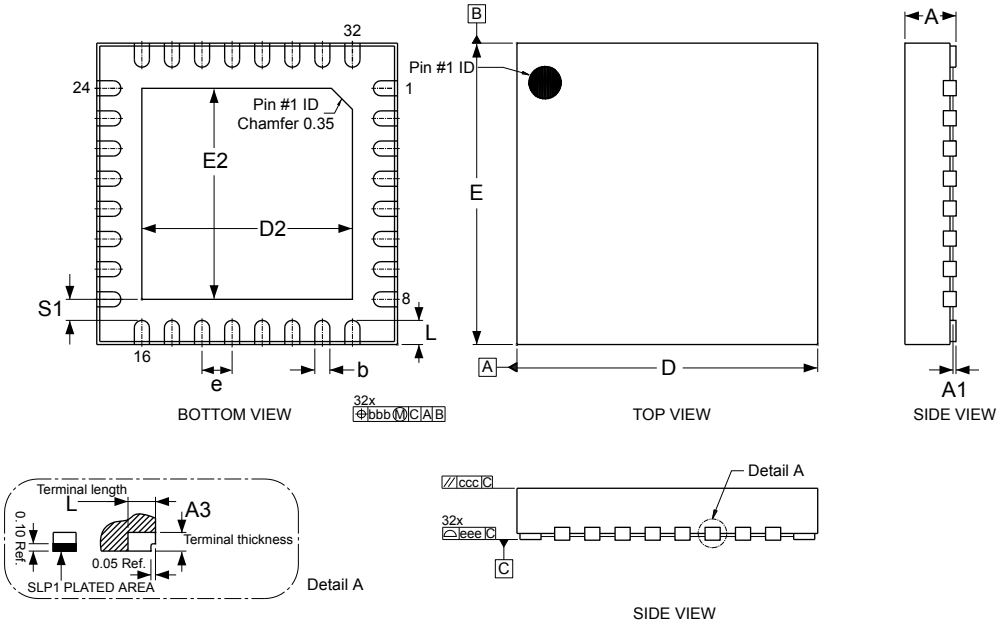
7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at www.st.com. ECOPACK is an ST trademark.

7.1 VFQFPN32 package information (B04R)

VFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead package.

Figure 22. VFQFPN32 - Outline



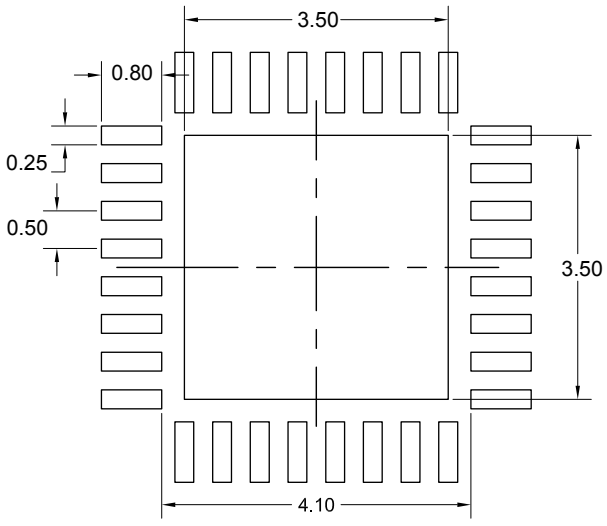
1. *Drawing is not to scale.*
2. *Coplanarity applies to the exposed heat slug as well as to the terminal.*

Table 131. **VFQFPN32 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0	-	0.050	0	-	0.0020
A3		0.200			0.0079	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D		5.000			0.1969	
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E		5.000			0.1969	
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e		0.500			0.0197	
S1		0.350			0.0138	
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
eee	-	0.080	-	-	0.0031	-

1. *Values in inches are converted from mm and rounded to four decimal digits.*

Figure 23. **VFQFPN32 - Recommended footprint**



1. *Dimension are expressed in millimeters.*

8 Ordering information

Table 132. Ordering information scheme

Example:	ST25	R	500	-	H	QW	T

Device type

ST25 = NFC/RFID tags and readers

Product type

R = NFC/HF reader

Product feature

500 = Automotive NFC reader for CCC DK and center console with the need for continuous high power

Ambient temperature range

H = - 40 to 125 °C

Package/Packaging

QW = Wetable flank QFN-32 (5 x 5 mm)

Tape and reel

T = 4000 pcs/reel

Revision history

Table 133. **Document revision history**

Date	Revision	Changes
06-May-2025	1	Initial release.

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