

Automotive N-channel 650 V, 0.042 Ω typ., 60 A Power MOSFET MDmesh™ DM2 in a D³PAK package

Datasheet - preliminary data

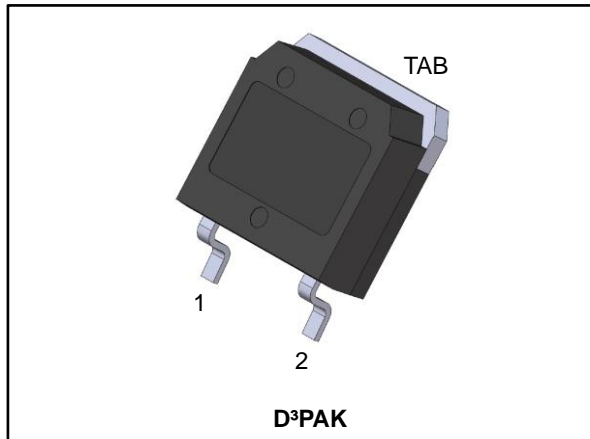
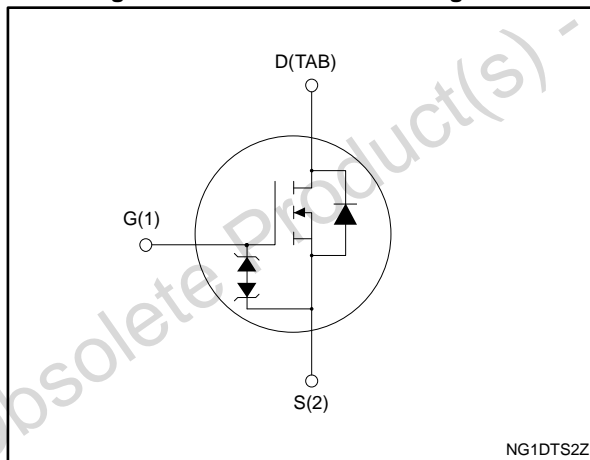


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STA65N65DM2AG	650 V	0.050 Ω	60 A	446 W



- Designed for automotive applications
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected
- SMD package D³PAK to improve creepage and thermal dissipation

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STA65N65DM2AG	65N65DM2	D ³ PAK	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	60	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	38	
$I_{DM}^{(1)}$	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	446	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) $I_{SD} \leq 60\text{ A}$, $di/dt=800\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

(3) $V_{DS} \leq 520\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.28	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	

Notes:

(1) When mounted on 1 inch² FR-4 board, 2 oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive	8	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	1100	mJ

Notes:

(1) starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$			10	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 30\text{ A}$		0.042	0.050	Ω

Notes:

⁽¹⁾ Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	5500	-	pF
C_{oss}	Output capacitance		-	210	-	
C_{riss}	Reverse transfer capacitance		-	3	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }520\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	456	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	3.3	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 520\text{ V}$, $I_{\text{D}} = 60\text{ A}$, $V_{\text{GS}} = 0$ to 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	120	-	nC
Q_{gs}	Gate-source charge		-	27	-	
Q_{gd}	Gate-drain charge		-	58	-	

Notes:

⁽¹⁾ $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 325\text{ V}$, $I_{\text{D}} = 30\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	33	-	ns
t_{r}	Rise time		-	13.5	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	114	-	
t_{f}	Fall time		-	11.5	-	

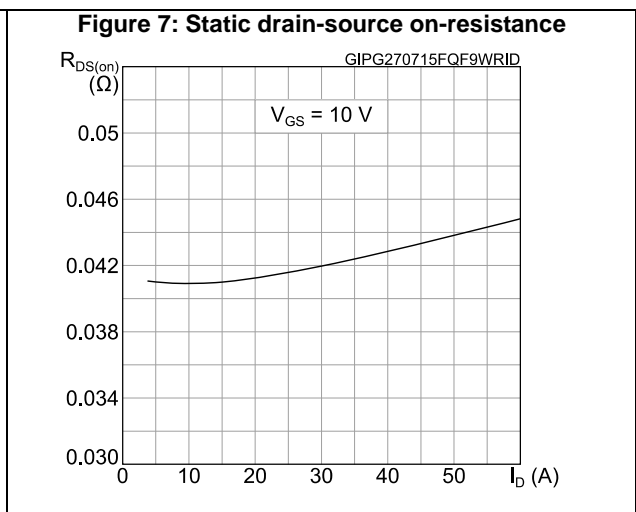
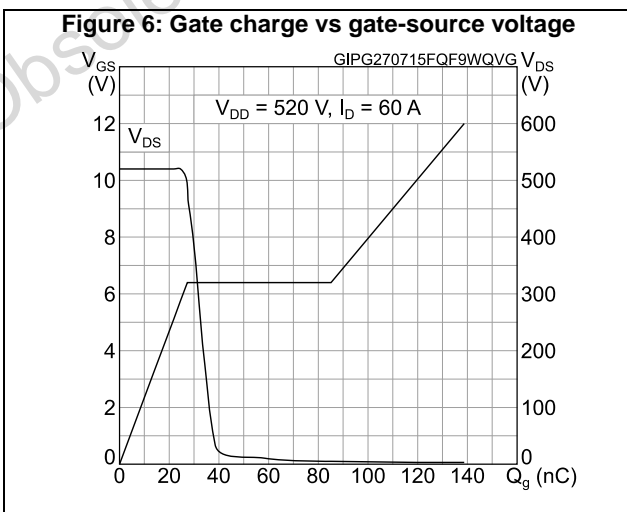
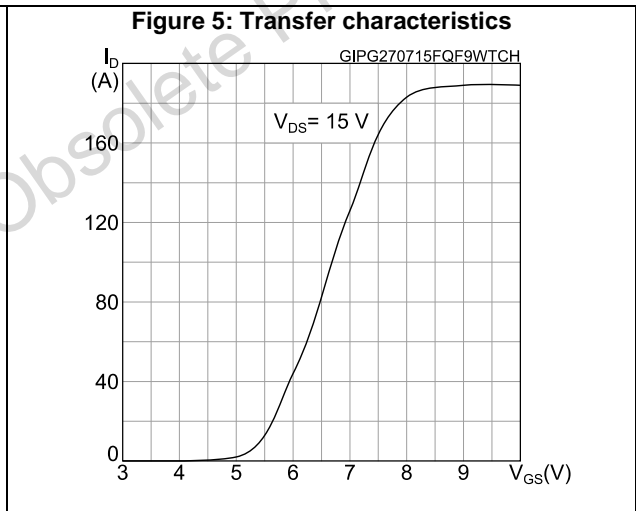
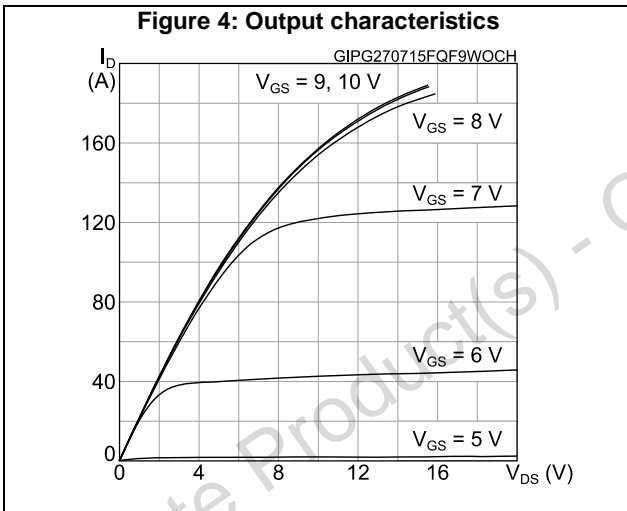
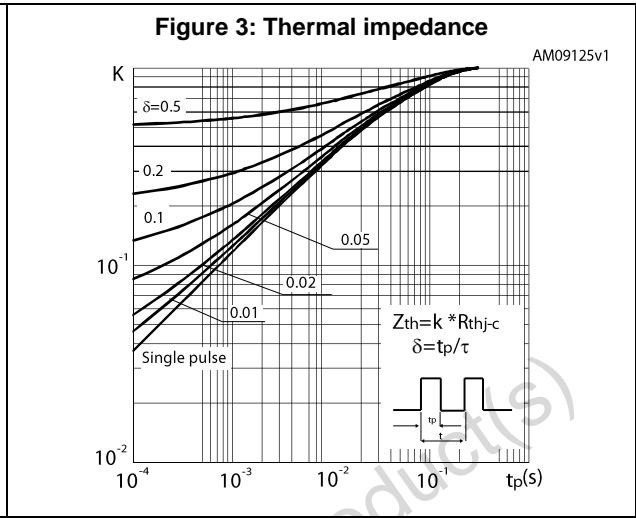
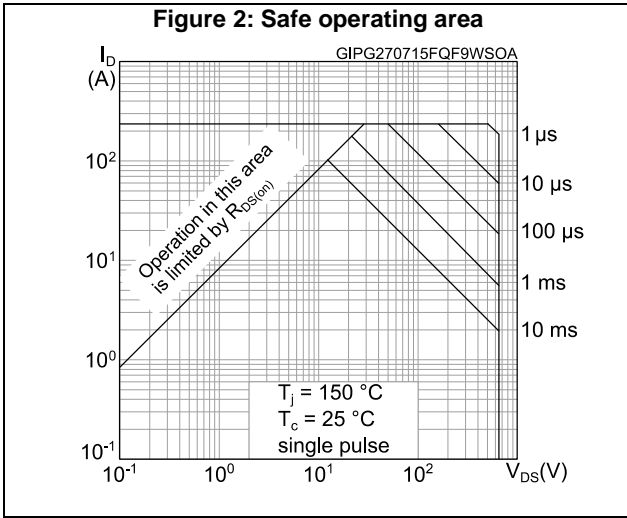
Table 8: Source-drain diode

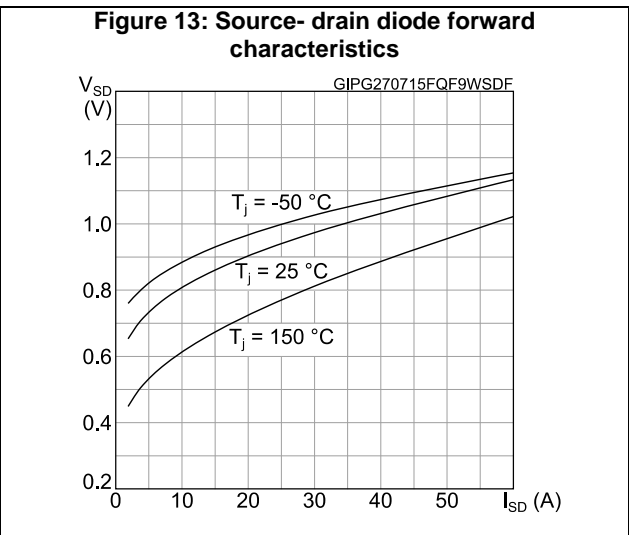
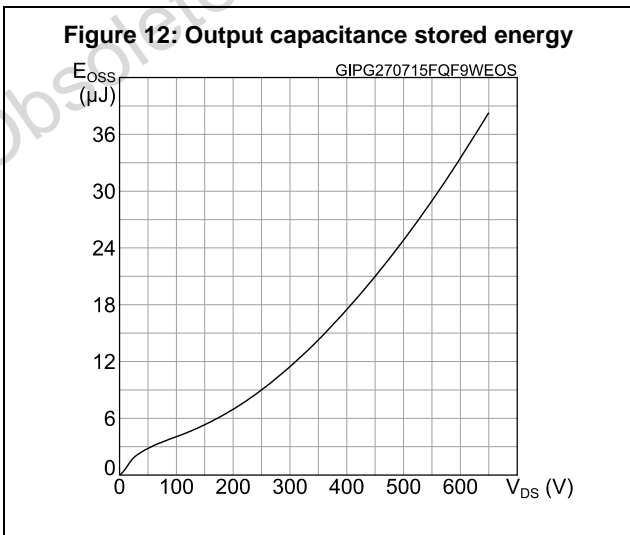
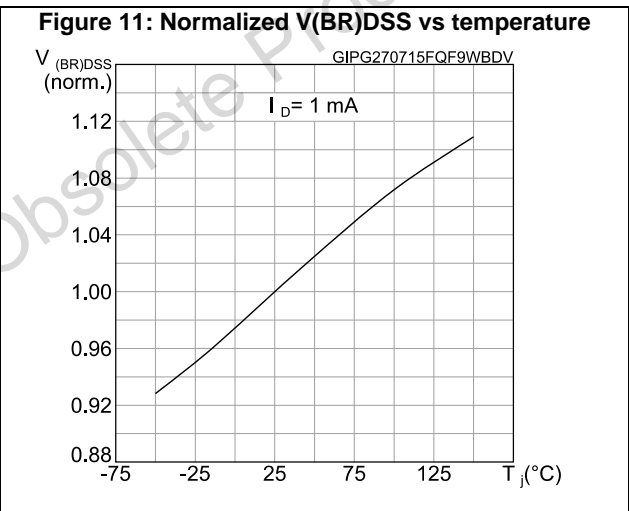
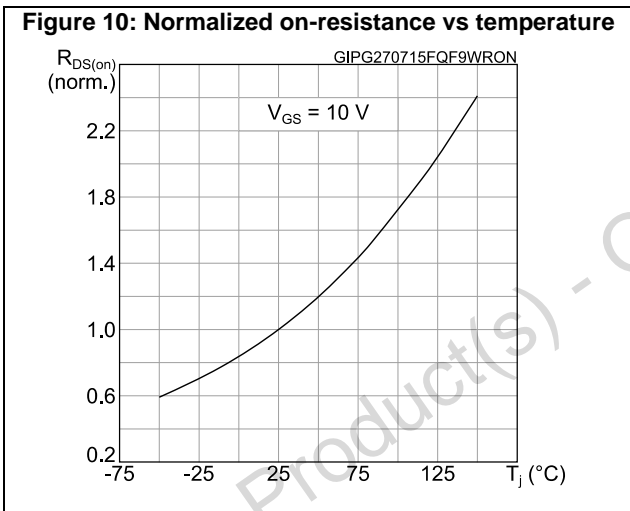
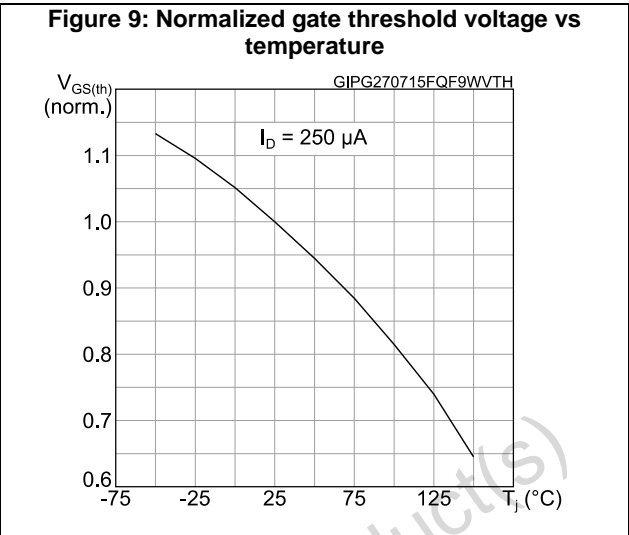
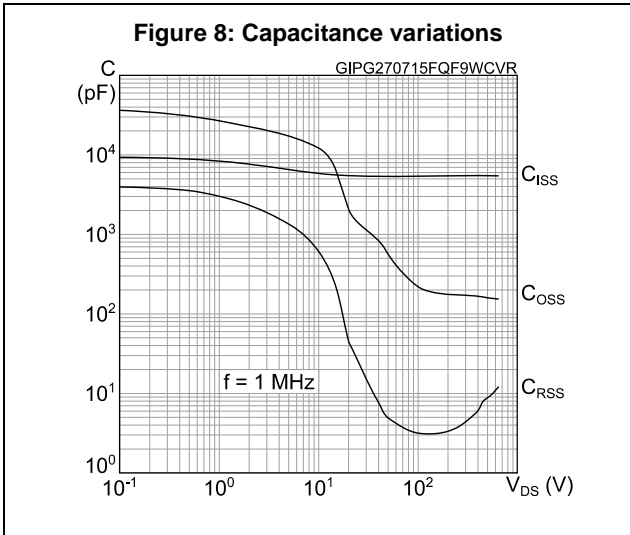
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		60	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		240	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 60\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 60\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	154		ns
Q_{rr}	Reverse recovery charge		-	0.94		μC
I_{RRM}	Reverse recovery current		-	12.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 60\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	288		ns
Q_{rr}	Reverse recovery charge		-	3.65		μC
I_{RRM}	Reverse recovery current		-	25.4		A

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





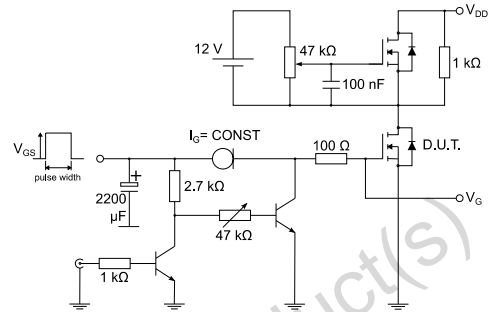
3 Test circuits

Figure 14: Test circuit for resistive load switching times



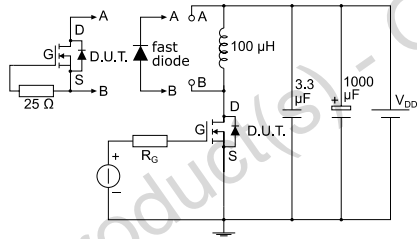
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Figure 15: Test circuit for gate charge behavior



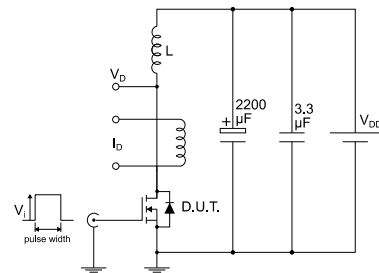
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Figure 16: Test circuit for inductive load switching and diode recovery times



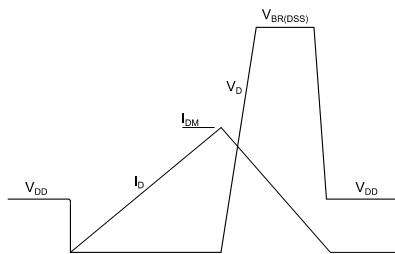
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Figure 17: Unclamped inductive load test circuit



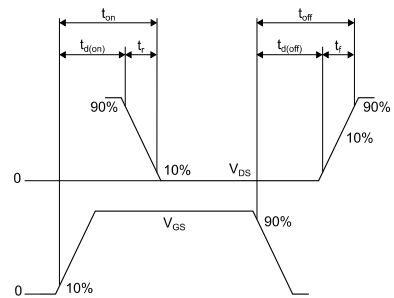
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D³PAK package information

Figure 20: D³PAK package outline

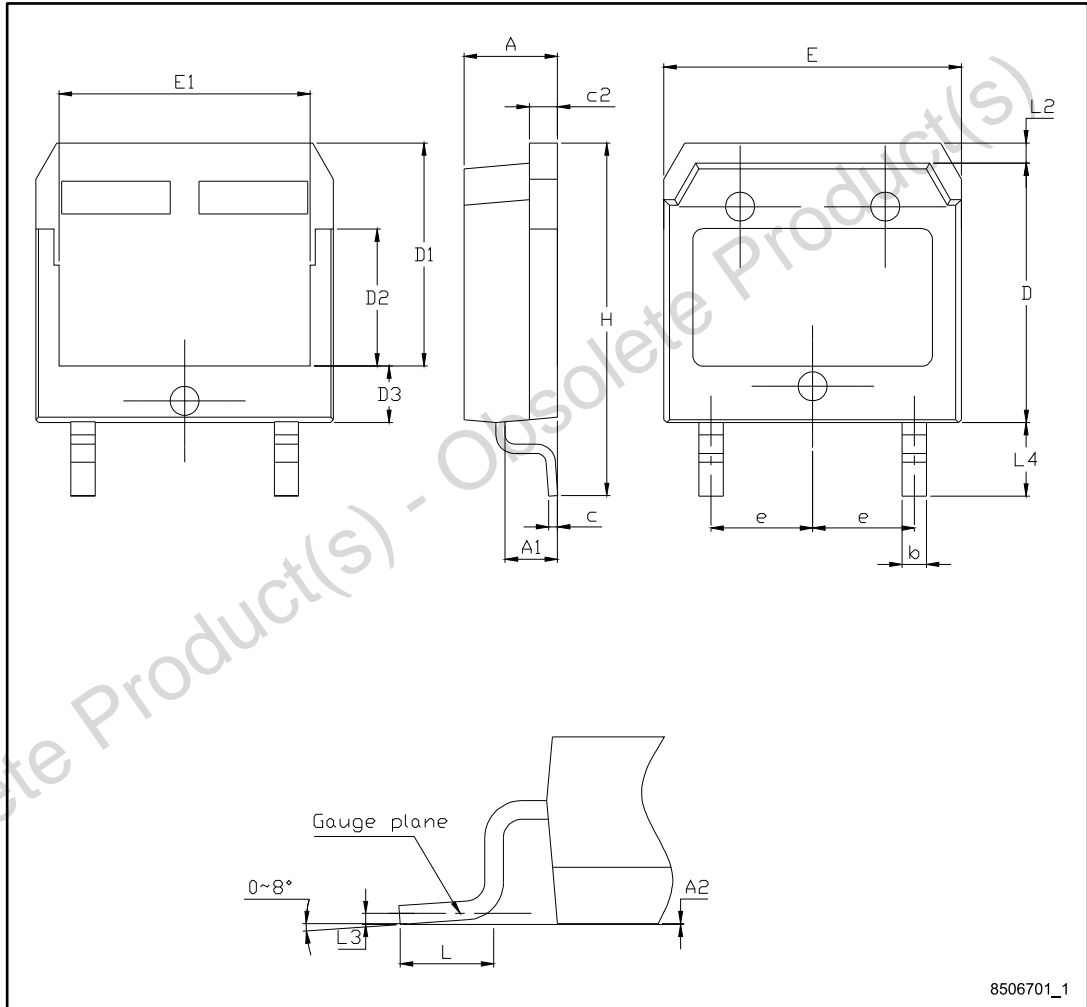
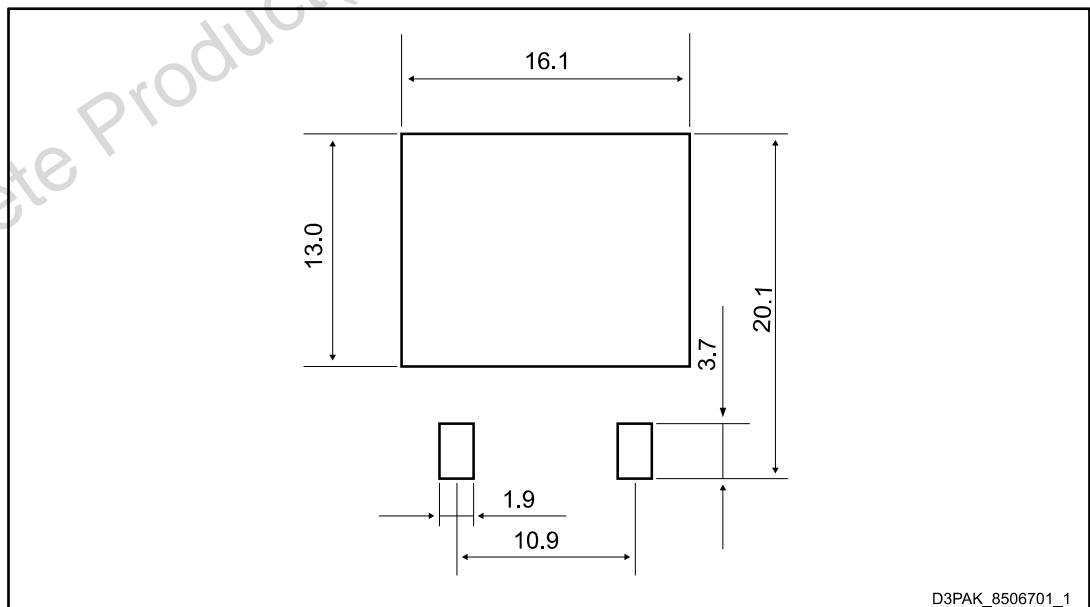


Table 9: D³PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.10
A1	2.70		2.90
A2	0.02		0.25
b	1.15		1.45
C	0.40		0.65
C2	1.45		1.61
D	13.80		14.00
D1	11.80		12.10
D2	7.50		7.80
D3	2.90		3.20
E	15.85		16.05
E1	13.30		13.60
e		5.45	
H	18.70		19.10
L	1.70		2.00
L2	1.00		1.15
L3		0.25	
L4	3.80		4.10

Figure 21: D³PAK recommended footprint (dimensions are in mm)



4.2 D³PAK packing information

Figure 22: D³PAK (TO-268) tape outline (dimensions are in mm)

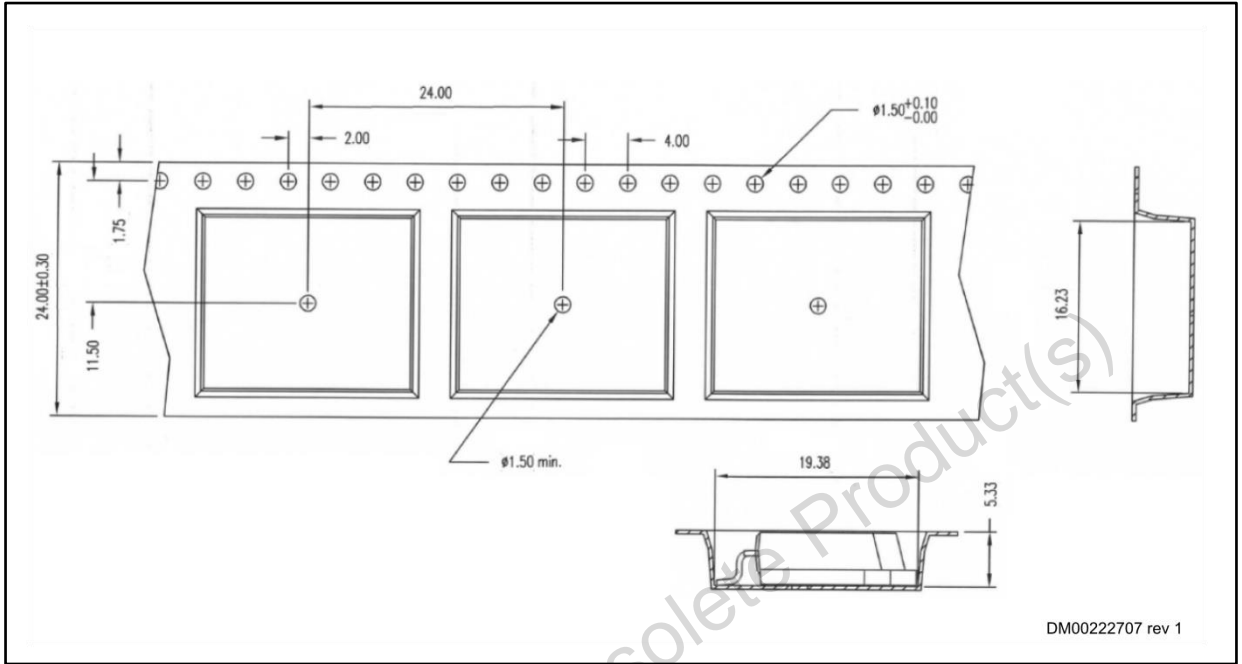
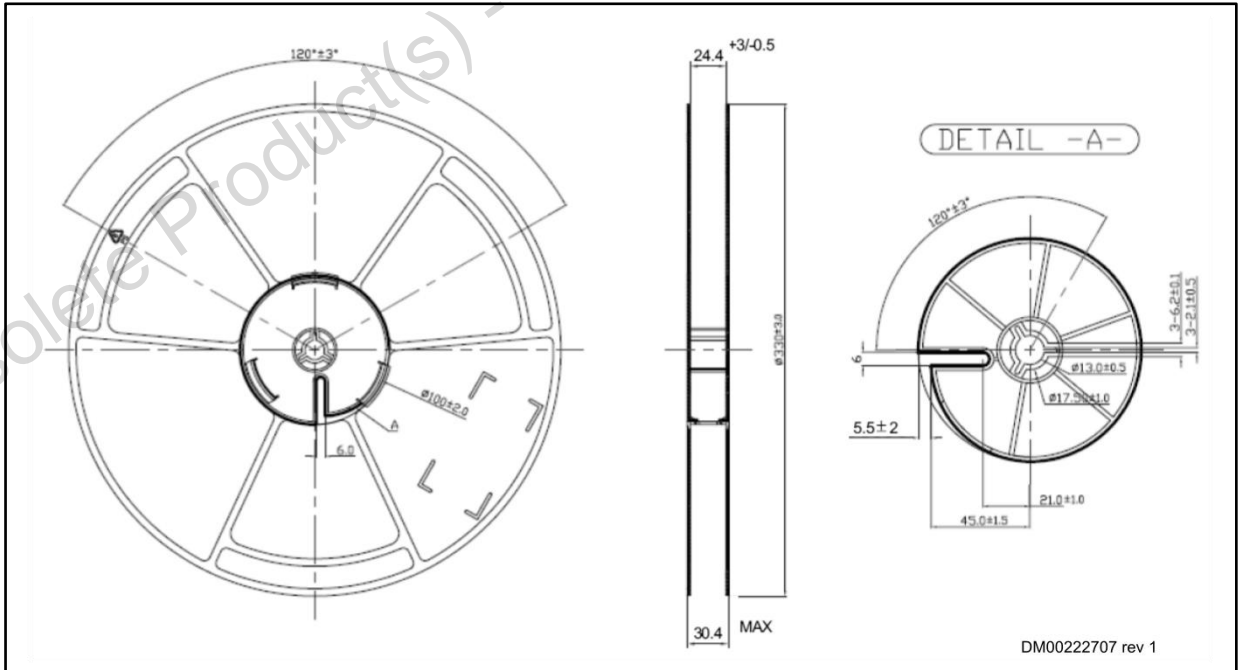


Figure 23: D³PAK (TO-268) reel outline (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
23-Jun-2017	1	Initial release.

Obsolete Product(s) - Obsolete Product(s)

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