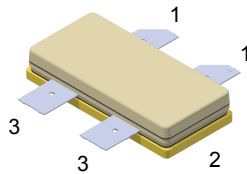


350 W, 50 V, 1200 to 1400 MHz RF power LDMOS transistor


STAC780-4F
Pin connection

Pin	Connection
1	Drain
2	Source
3	Gate

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
STAC1214-350	1200 to 1400 MHz	50 V	350 W	14 dB	55%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internal input matching for ease of use
- Large positive and negative gate/source voltage range for improved class C operation
- In compliance with the European Directive 2002/95/EC

Applications

- L-band radars

Description

The STAC1214-350 is a 50 V common-source N-channel enhancement-mode lateral field-effect RF power transistor designed for L-band radar applications.


Product status link
[STAC1214-350](#)
Product summary

Order code	STAC1214-350
Marking	1214-350
Package	STAC780-4F
Packing	Box

1 Electrical ratings

Table 1. Absolute maximum ratings (T_{CASE} = 25°C)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	115	V
V _{GS}	Gate-source voltage	-8/+10	V
V _{DD}	Drain supply voltage	55	V
T _{STG}	Storage temperature range	-65 to +150	°C
T _J	Junction temperature	+200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Junction-case thermal resistance T _{CASE} = +85 °C , T _J = +200 °C, DC test	0.28	°C/W

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to JESD22-A114)	2

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	115			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 6\text{ V}$			1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 50\text{ V}, I_D = 50\text{ mA}$		2.9		V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		2.3		V
C_{RSS}	Common source feedback capacitance	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V},$ $f = 1\text{ MHz}$		2		pF
C_{OSS}	Common source output capacitance			44		pF

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency	$P_{in} = 14\text{ W}, f = 1300\text{ MHz}$	1200	-	1400	MHz
P_{OUT}	Output power		-	350	-	W
Gain	Power gain		-	14	-	dB
Efficiency	Drain efficiency		-	55	-	%
VSWR	Load mismatch	$P_{OUT} = 350\text{ W}, \text{all phases}$	-	-	10:1	

Table 6. Impedance data

Frequency (in MHz)	Input impedance (Z_{IN})	Drain load impedance (Z_{DL})
1200	0.12-0.72	3.07+1.82
1300	0.17-0.96	3.18+0.97
1400	0.28-1.3	2.81+0.35

Note: $V_{DD} = 50\text{ V}, I_{DQ} = 30\text{ mA}, \text{pulsed CW}, PW = 10\text{ }\mu\text{s}, DC = 1\%$.

2.1 Typical performance

Figure 1. Gain vs output power (1200 – 1400 MHz frequency band)

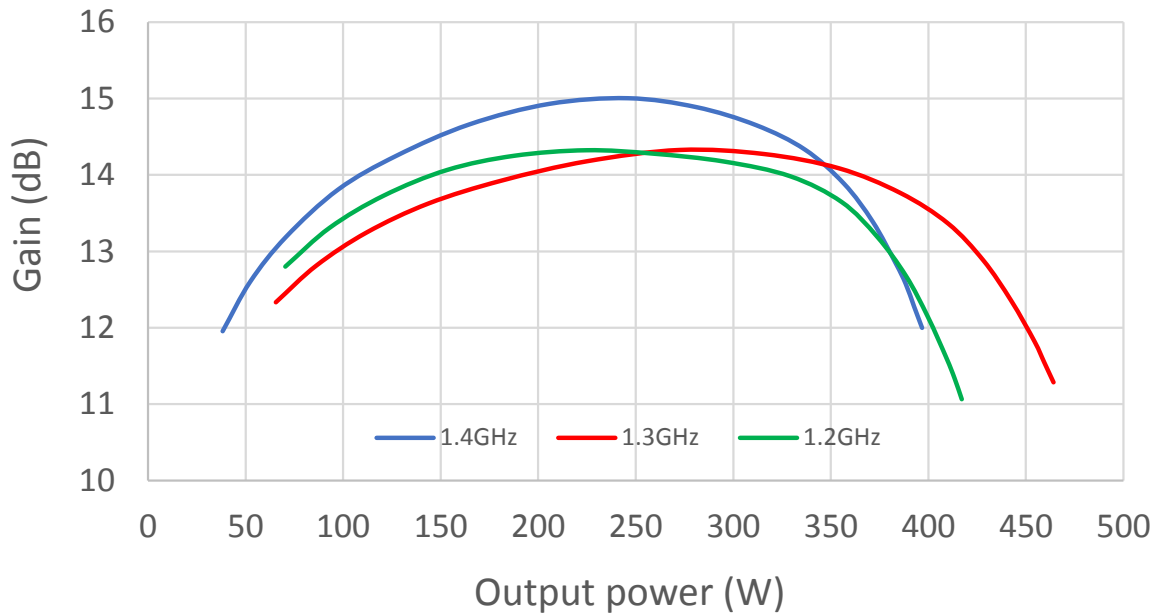


Figure 2. Efficiency vs output power (1200 – 1400 MHz frequency band)

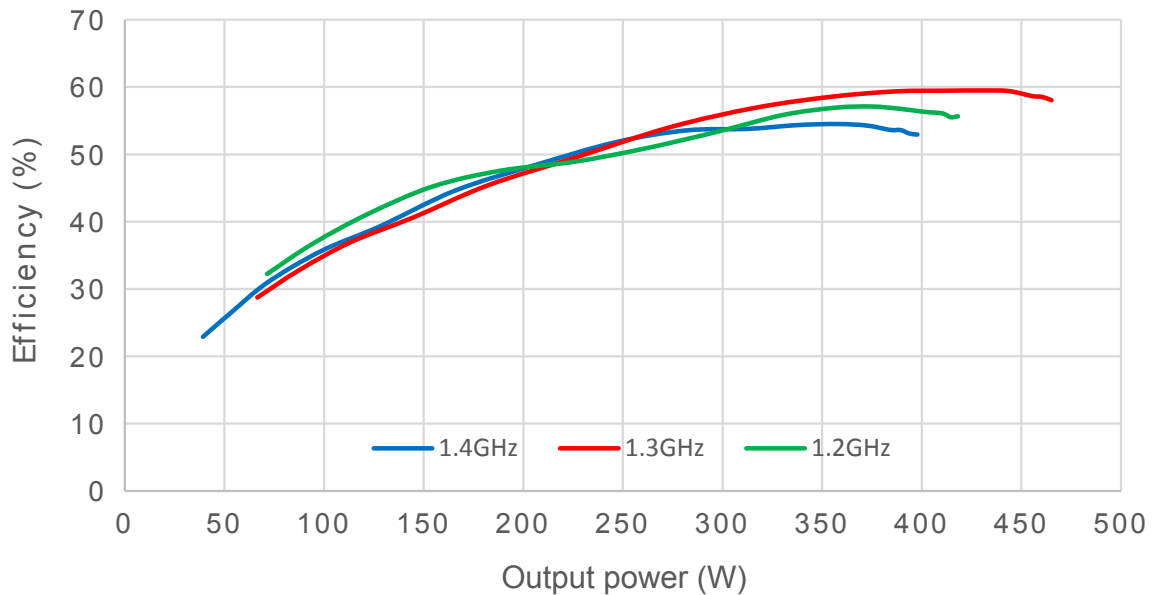
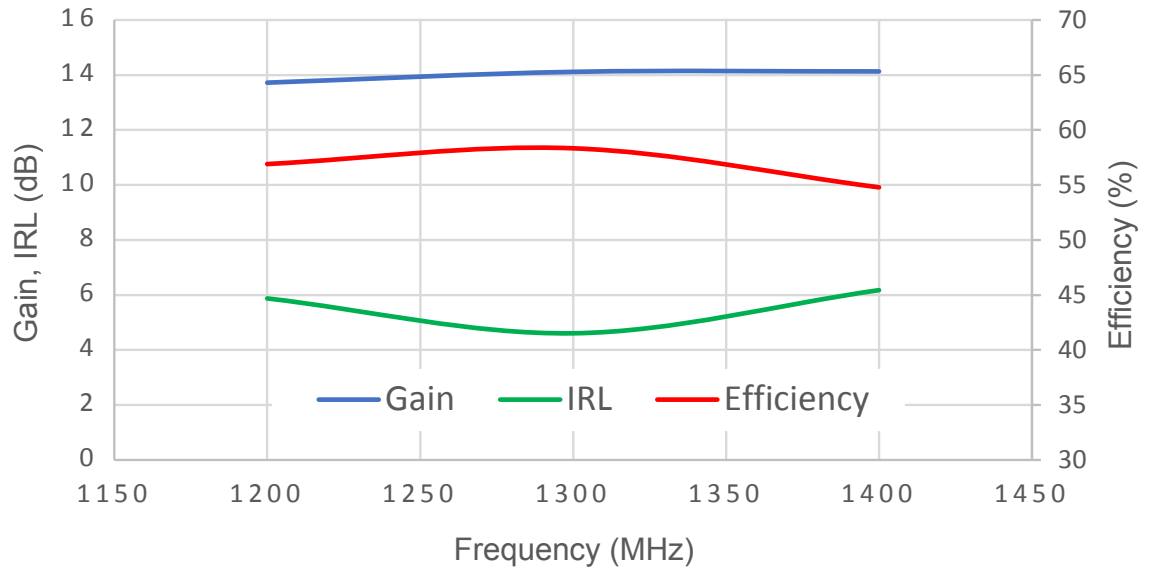
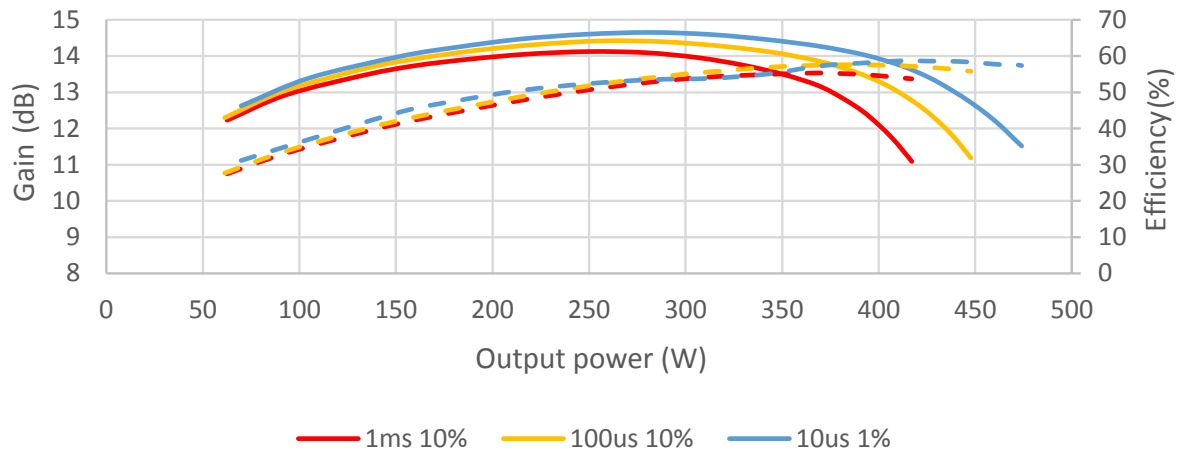


Figure 3. Gain, IRL and efficiency vs frequency ($P_{OUT} = 350\text{ W}$)



Note: $V_{DD} = 50\text{ V}$, $I_{DQ} = 30\text{ mA}$, Pulsed CW, $PW = 10\ \mu\text{s}$, $DC = 1\%$.

Figure 4. Gain and efficiency vs output power at different PW and DC ($f = 1300\text{ MHz}$)



Note: $V_{DD} = 50\text{ V}$, $I_{DQ} = 30\text{ mA}$

3 Test circuits

Figure 5. Test circuit schematic

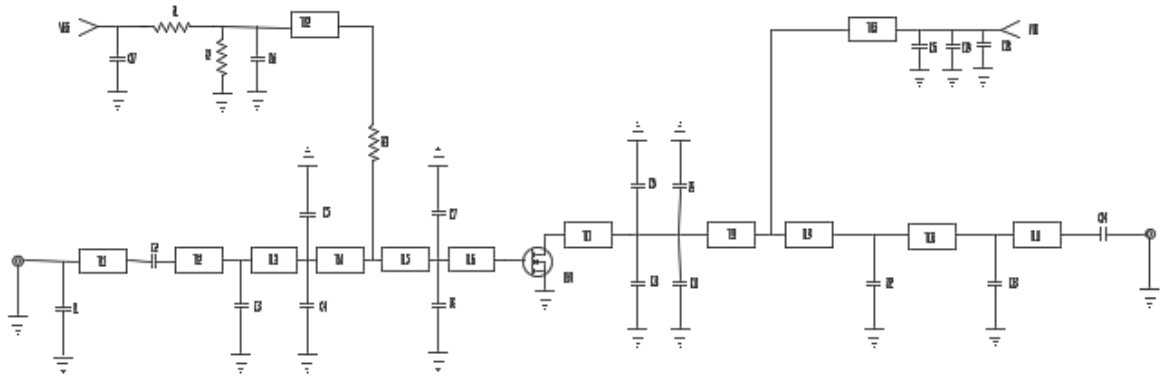


Figure 6. Test circuit layout

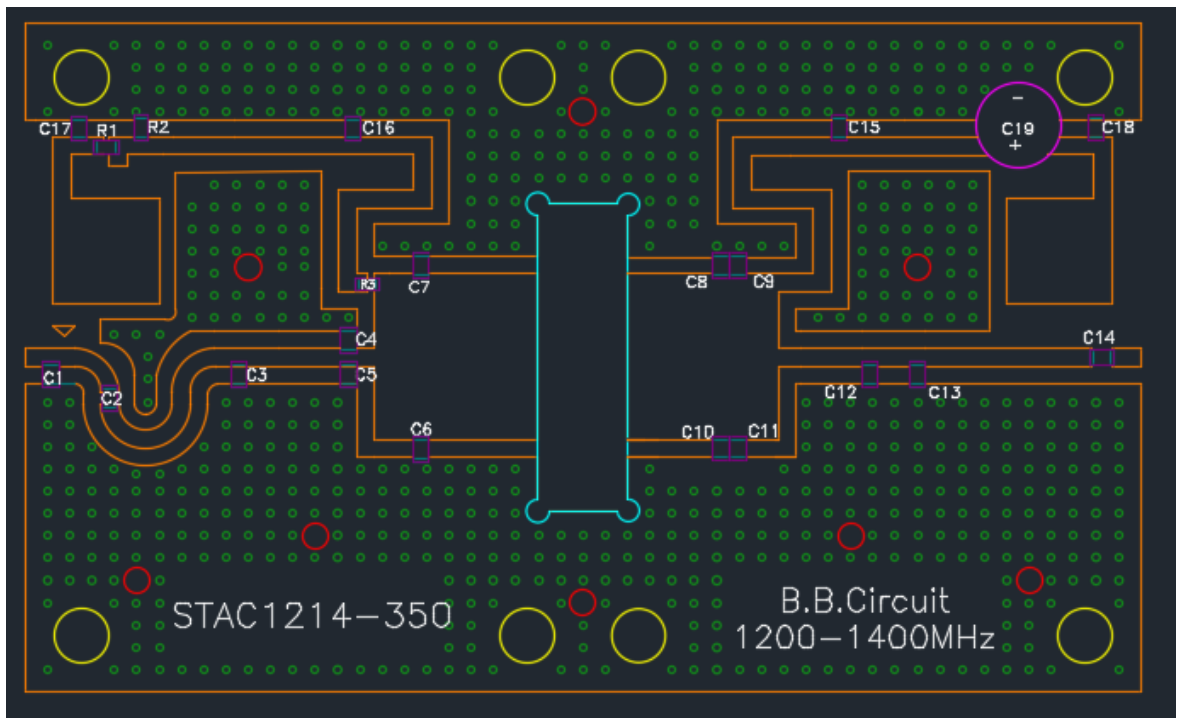


Table 7. Component list

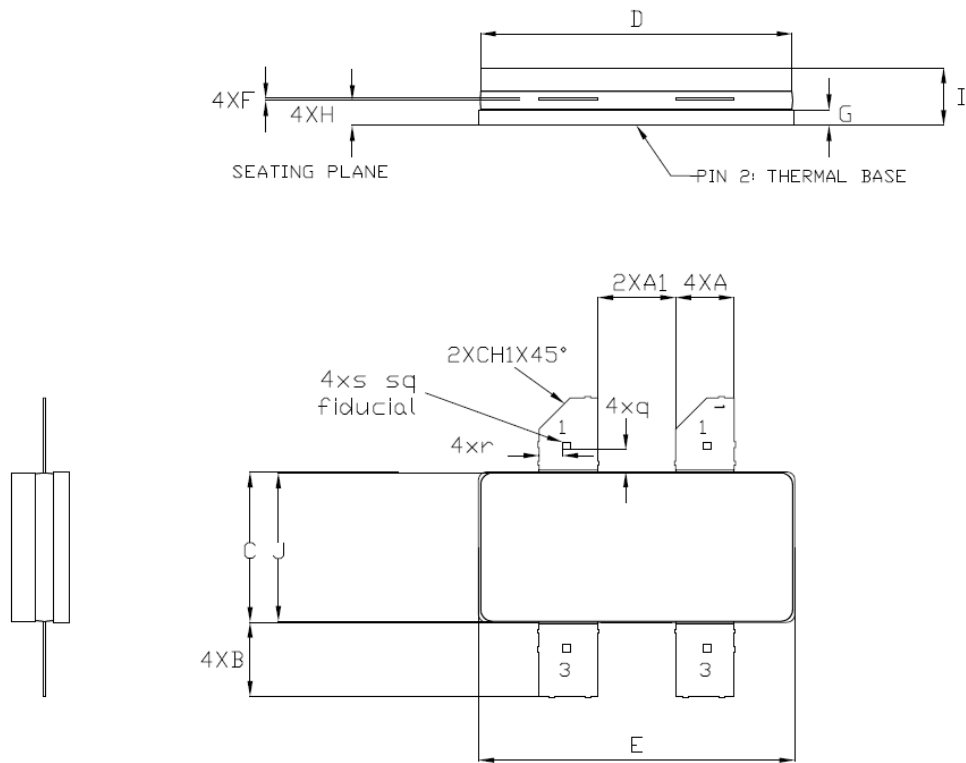
Item	Qty	Part number	Vendor	Description, dimension (x, y)
C2, C14,C15,C16	4	1111C360G501X	Passive Plus Inc.	36 pF chip ceramic capacitor
C1	1	1111C2R0G501X	Passive Plus Inc.	2 pF chip ceramic capacitor
C3,C8,C10	1	1111C3R3G501X	Passive Plus Inc.	3.3 pF chip ceramic capacitor
C4,C5	3	1111C1R3G501X	Passive Plus Inc.	1.3 pF chip ceramic capacitor
C6,C7	2	1111C2R7G501X	Passive Plus Inc.	2.7 pF chip ceramic capacitor
C9,C11	2	1111C0R2G501X	Passive Plus Inc.	0.2 pF chip ceramic capacitor
C12,C13	1	1111C1R2G501X	Passive Plus Inc.	1.2 pF chip ceramic capacitor
C17, C18	2	ATC200B103JT50X	ATC	10000 pF chip ceramic capacitor
C19	1	TVX1J102MCD	Nichicon	1000 μ F, 63 V electrolytic capacitor
R1	1	CR1206-4W-1001JB	Venkel	1 k Ω surface mount resistor
R2	1	CR1206-4W-474JB	Venkel	4.74 M Ω surface mount resistor
R3	1	CR1206-4W-270JB	Venkel	27 Ω surface mount resistor
T1				L = 0.320 in W = 0.082 in
T2				L = 0.850 in W = 0.082 in
T3				L = 0.500 in W = 0.082 in
T4				L = 0.110 in W = 0.082 in
T5				L = 0.210 in W = 0.748 in
T6				L = 0.525 in W = 0.748 in
T7				L = 0.554 in W = 0.748 in
T8				L = 0.220 in W = 0.748i n
T9				L = 0.411 in W = 0.082 in
T10				L = 0.210 in W = 0.082 in
T11				L = 0.781 in W = 0.082 in
T12				L = 1.35 in W = 0.082 in
T13				L = 1.6 in W = 0.082 in
Board 3X5	1		Rogers corp	0.030 THK , Er = 2.5, 2Oz Cu both sides

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 STAC780-4F package information

Figure 7. STAC780-4F package outline



PIN	CONNECTIO N
1	DRAIN
2	SOURCE
3	GATE

DM00481940-1

Table 8. STAC780-4F mechanical data

Ref.	Millimeters		
	Min.	Typ.	Max.
A	3.76		3.86
A1	5.03		5.13
B	4.57		5.08
C	9.65		9.91
D	20.17		20.37
E	20.45		20.70
F	0.11		0.17
G	0.97		1.14
H	1.52		1.70
I	3.18		4.32
J	9.52		9.78
q		1.37	
r		1.52	
s		0.51	
CH1		2.03	

Revision history

Table 9. Document revision history

Date	Version	Changes
05-Sep-2018	1	Initial release
04-Aug-2020	2	Updated product summary in cover page. Added Pin connection in cover page. Updated Table 2. Thermal data and Section 2 Electrical characteristics . Added Section 2.1 Typical performance and Section 3 Test circuits . Minor text changes.

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