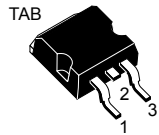
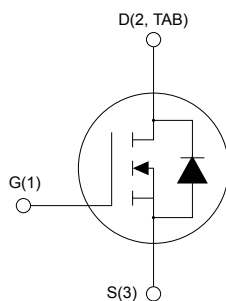


N-channel 500 V, 285 mΩ typ., 12 A MDmesh II Power MOSFET in a D²PAK package


D²PAK


AM01475v1_noZen


Product status link
[STB14NM50N](#)
Product summary

Order code	STB14NM50N
Marking	14NM50N
Package	D ² PAK
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB14NM50N	500 V	320 mΩ	12 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	12	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	90	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.39	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	172	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	500			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 500 V			1	μA
		V _{GS} = 0 V, V _{DS} = 500 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 6 A		285	320	mΩ

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	816	-	pF
C _{oss}	Output capacitance		-	60	-	pF
C _{rss}	Reverse transfer capacitance		-	3	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 400 V, V _{GS} = 0 V	-	308	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.5	-	Ω
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 12 A, V _{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	27	-	nC
Q _{gs}	Gate-source charge		-	5	-	nC
Q _{gd}	Gate-drain charge		-	15	-	nC

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 400 V, I _D = 12 A, R _G = 4.7 Ω V _{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	12	-	ns
t _r	Rise time		-	16	-	ns
t _{d(off)}	Turn-off delay time		-	42	-	ns
t _f	Fall time		-	22	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 12\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	252		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	300		ns
Q_{rr}	Reverse recovery charge		-	3.3		μC
I_{RRM}	Reverse recovery current		-	22.2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

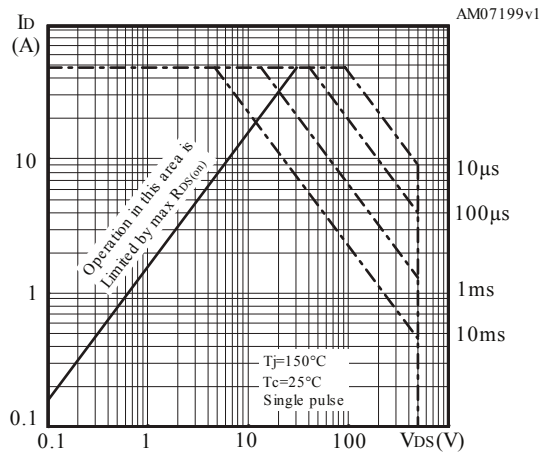
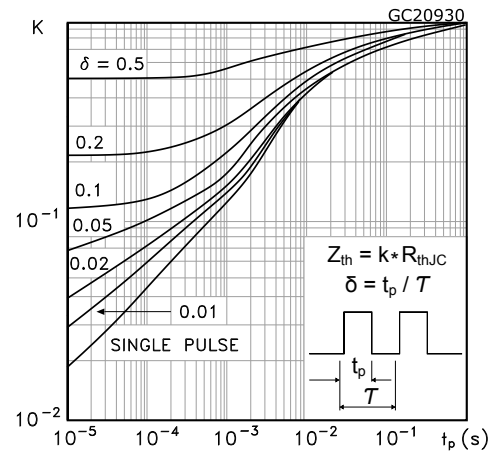
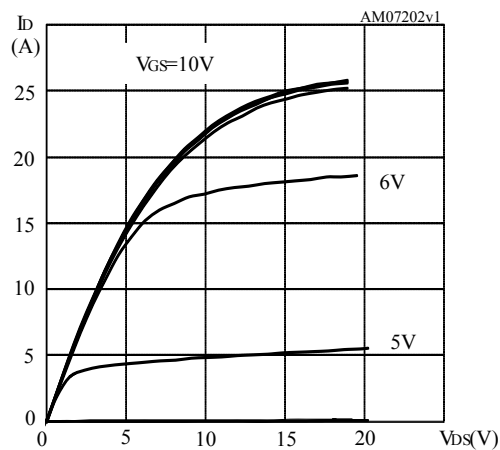
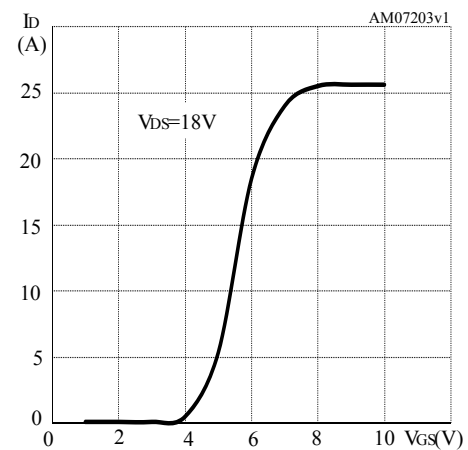
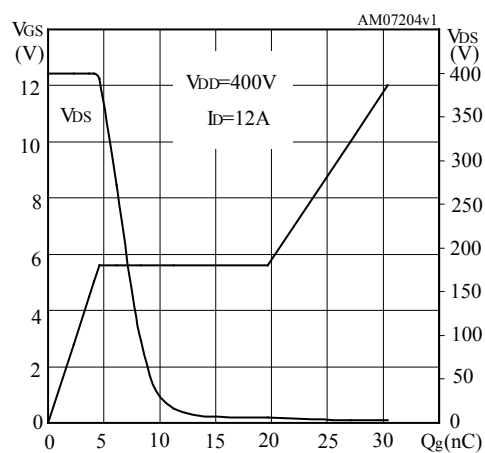
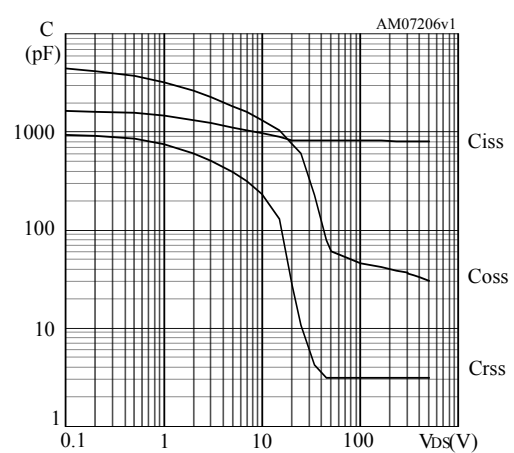
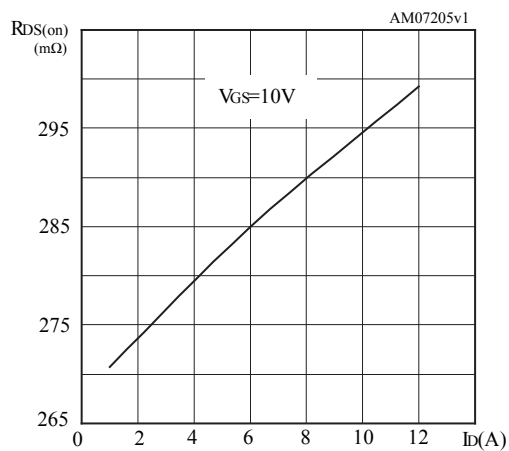
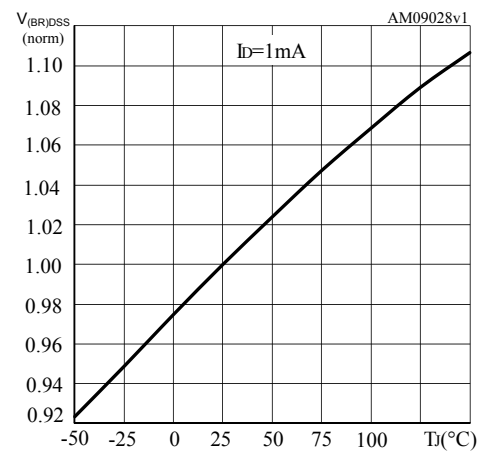
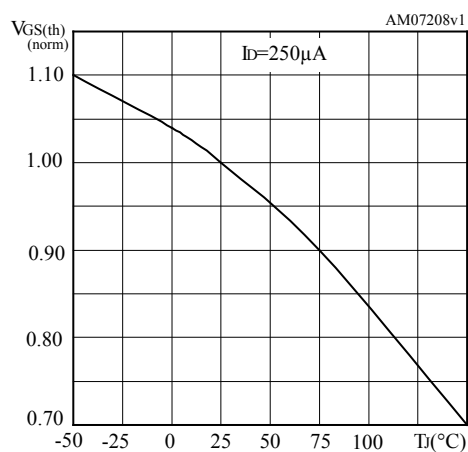
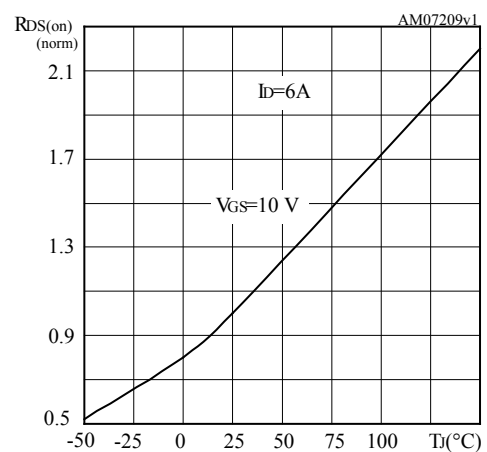
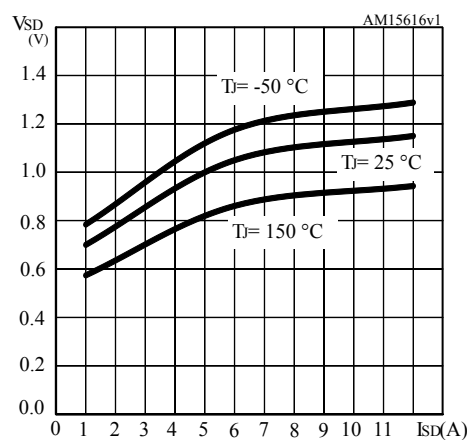
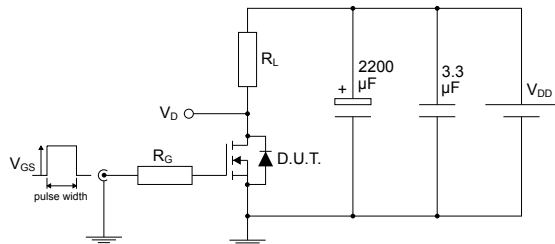
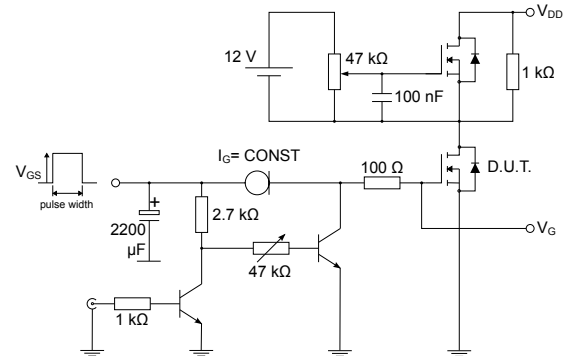
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical capacitance characteristics


Figure 7. Typical drain-source on-resistance

Figure 8. Normalized breakdown voltage vs temperature

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Typical reverse diode forward characteristics


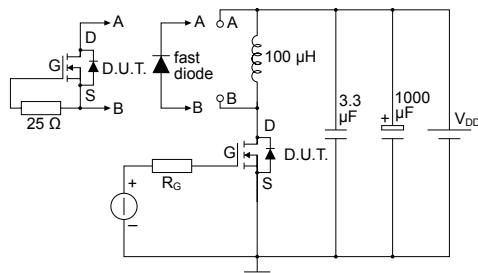
3 Test circuits

Figure 12. Test circuit for resistive load switching times


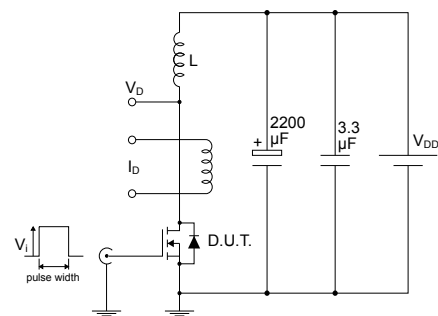
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Figure 13. Test circuit for gate charge behavior


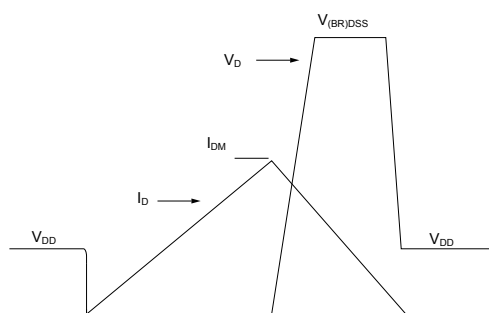
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Figure 14. Test circuit for inductive load switching and diode recovery times


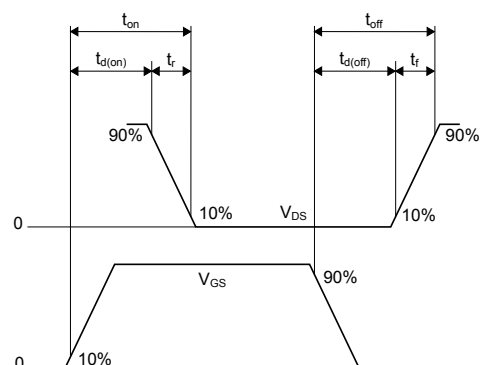
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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


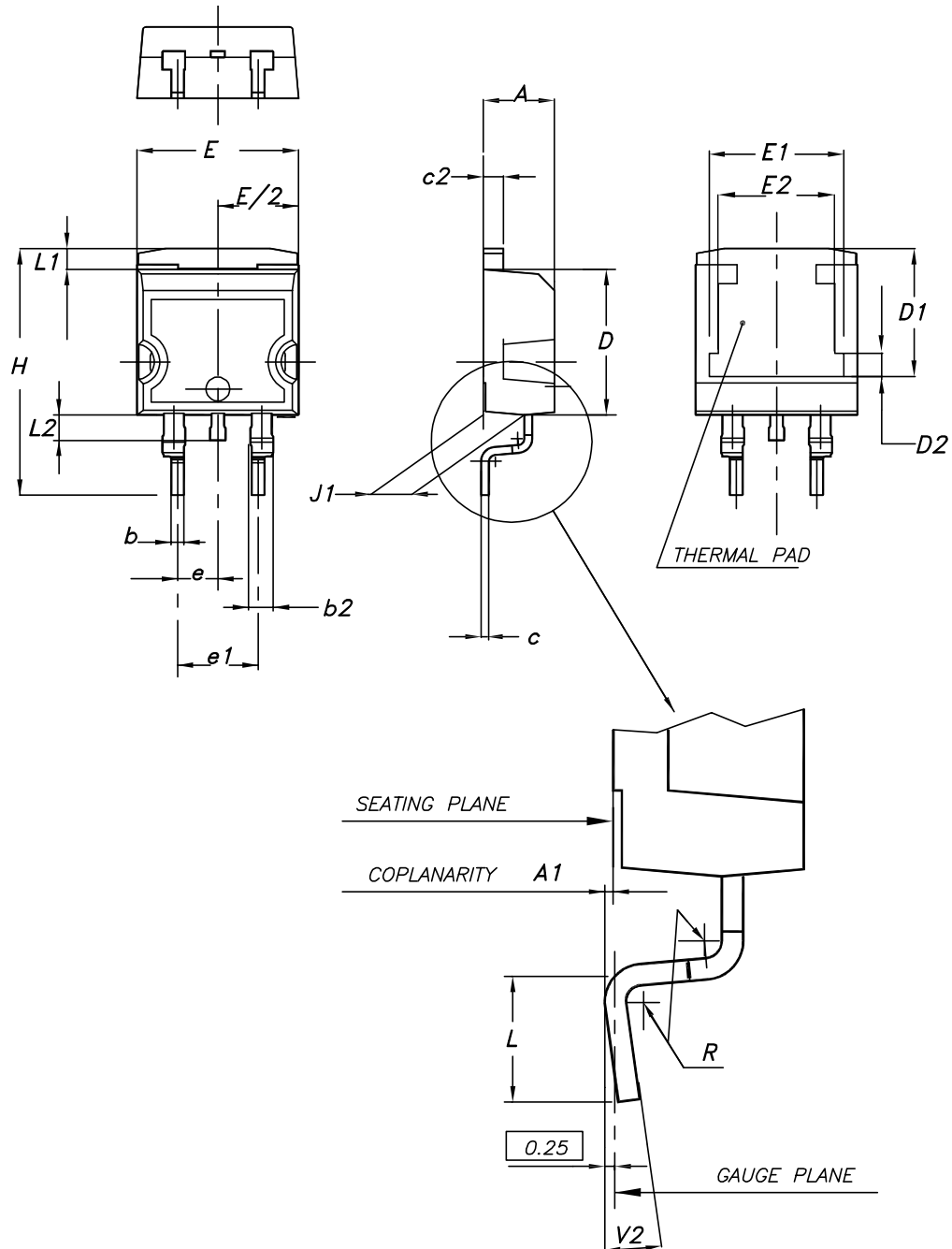
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 18. D²PAK (TO-263) type A package outline

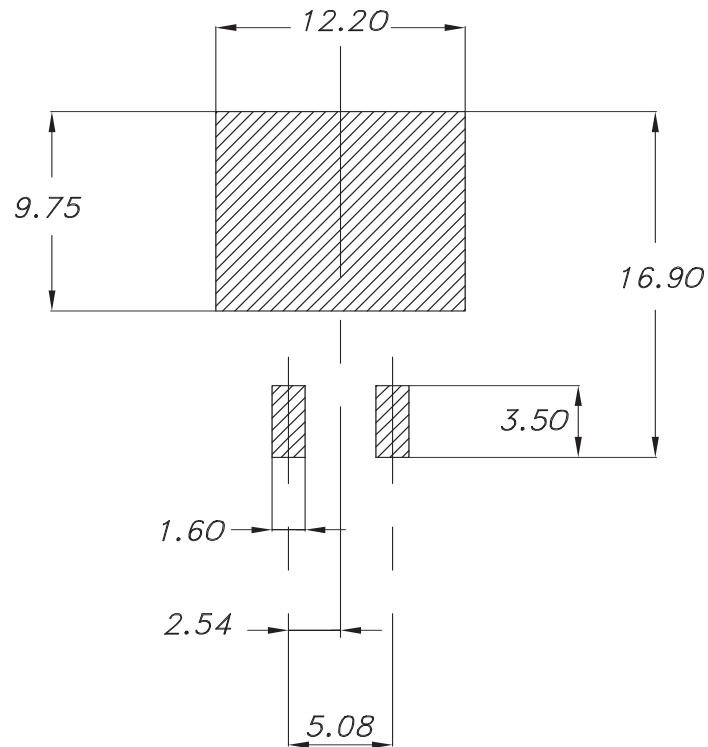


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Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

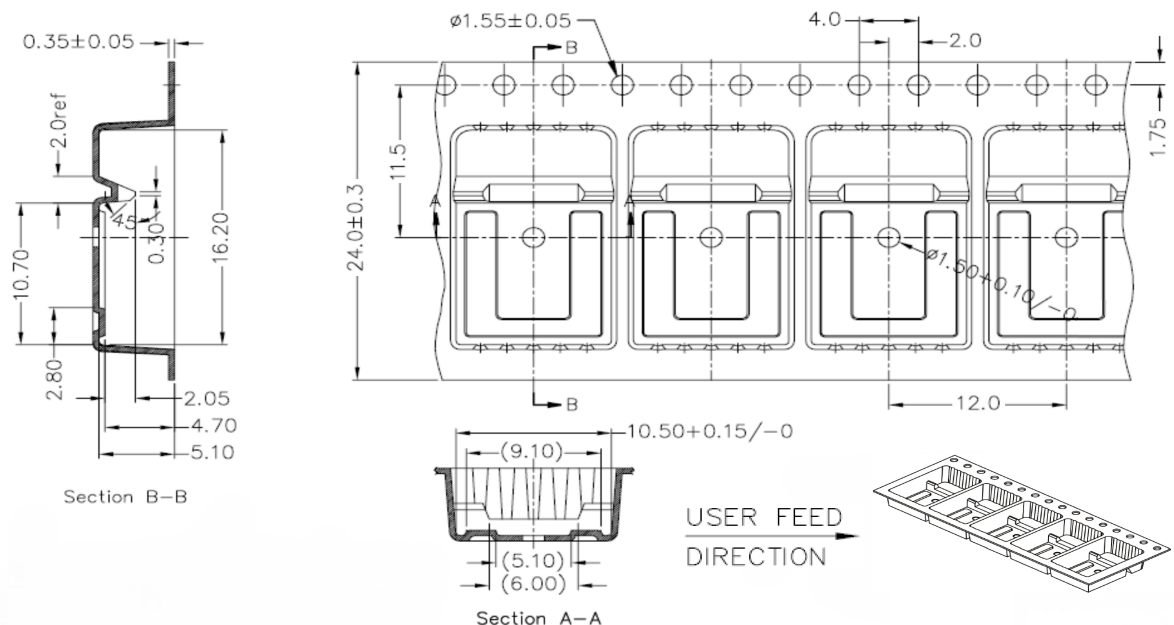
Figure 19. D²PAK (TO-263) recommended footprint (dimensions are in mm)



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4.2 D²PAK packing information

Figure 20. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. Document revision history

Date	Revision	Changes
27-Jun-2014	1	First release.
22-Jul-2025	2	Updated Table 4. On/off states and Table 5. Dynamic . Updated Section 4: Package information . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	D ² PAK (TO-263) type A package information	8
4.2	D ² PAK packing information	10
	Revision history	11

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