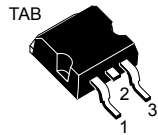
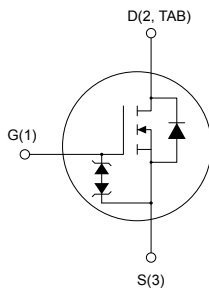


## N-channel 600 V, 255 mΩ typ., 13 A MDmesh M2 Power MOSFET in a D<sup>2</sup>PAK package


**D<sup>2</sup>PAK**


AM01476v1\_tab


**Product status link**
[STB18N60M2](#)
**Product summary**

<b>Order code</b>	STB18N60M2
<b>Marking</b>	18N60M2
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB18N60M2	600 V	280 mΩ	13 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC resonant, converters

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	13	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8	
$I_{DM}^{(1)}$	Drain current (pulsed)	52	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 13\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ .
3.  $V_{DS} \leq 480\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C}/\text{W}$

1. When mounted on a standard 1 inch<sup>2</sup> area of FR-4 PCB with 2-oz copper.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	3	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	135	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	100	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6.5\text{ A}$	-	255	280	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	791	-	pF
$C_{oss}$	Output capacitance		-	40	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1.3	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	164.5	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 13\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	21.5	-	nC
$Q_{gs}$	Gate-source charge		-	3.2	-	nC
$Q_{gd}$	Gate-drain charge		-	11.3	-	nC

1.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 6.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	12	-	ns
$t_r$	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	47	-	ns
$t_f$	Fall time		-	10.6	-	ns

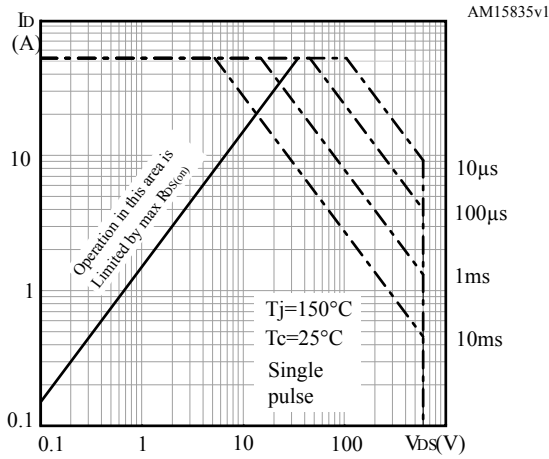
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	52	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 13\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	305	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	3.3	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	22	-	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	417	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	4.6	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	22	-	A

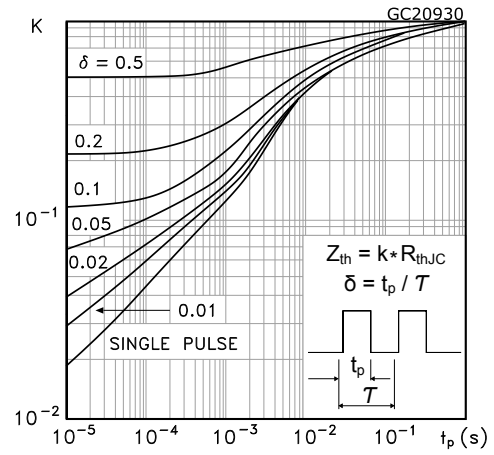
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

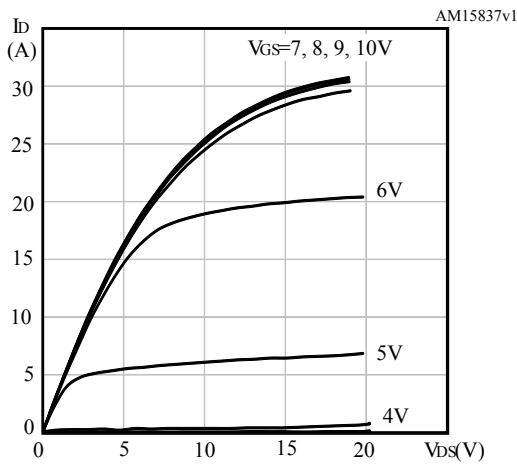
**Figure 1. Safe operating area**



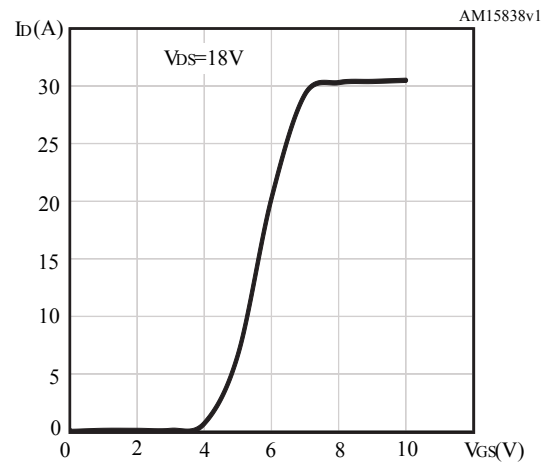
**Figure 2. Normalized transient thermal impedance**



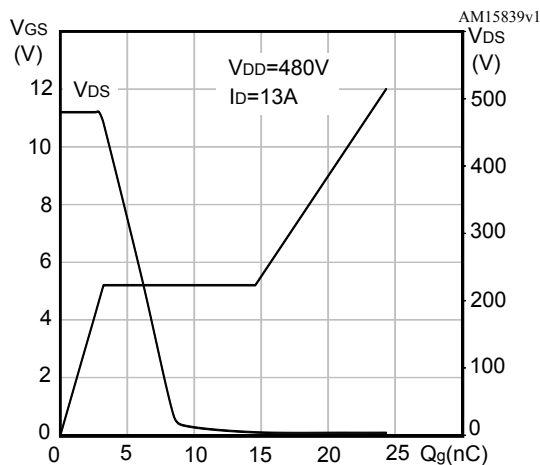
**Figure 3. Typical output characteristics**



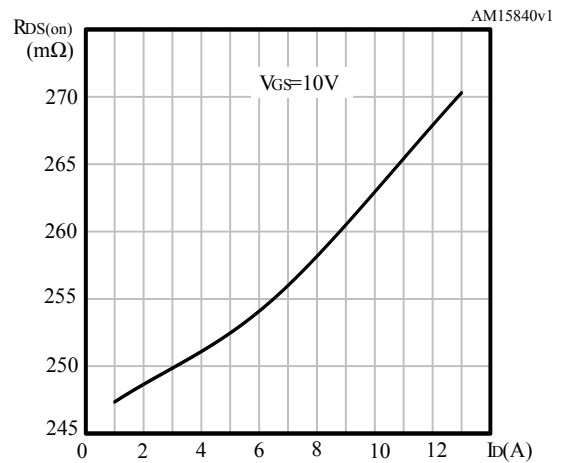
**Figure 4. Typical transfer characteristics**



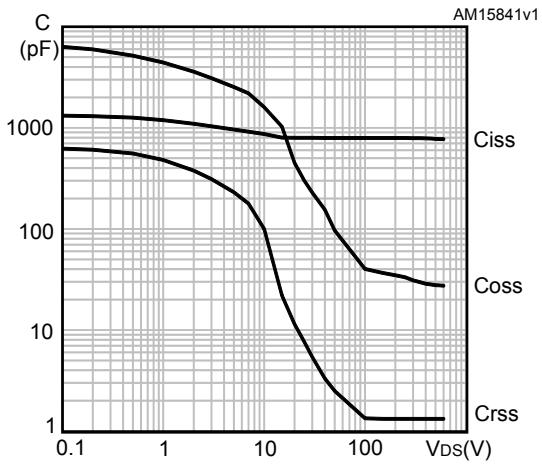
**Figure 5. Typical gate charge characteristics**



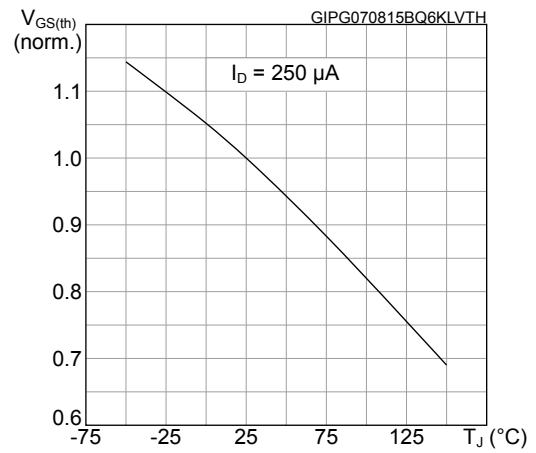
**Figure 6. Typical drain-source on-resistance**



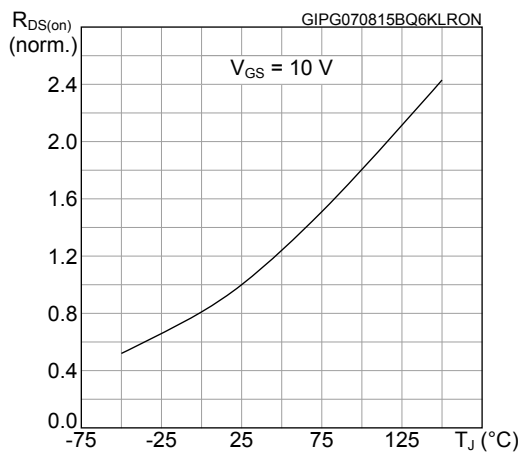
**Figure 7. Typical capacitance characteristics**



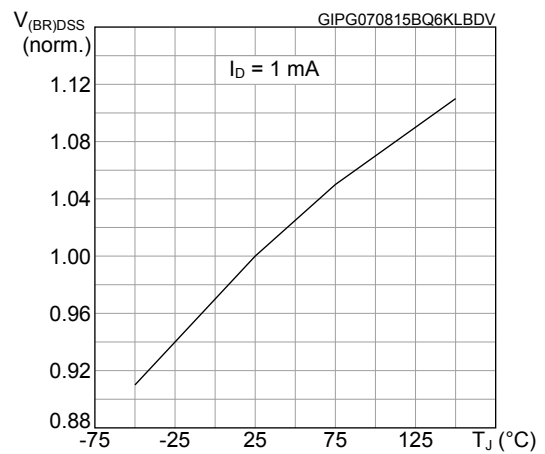
**Figure 8. Normalized gate threshold vs temperature**



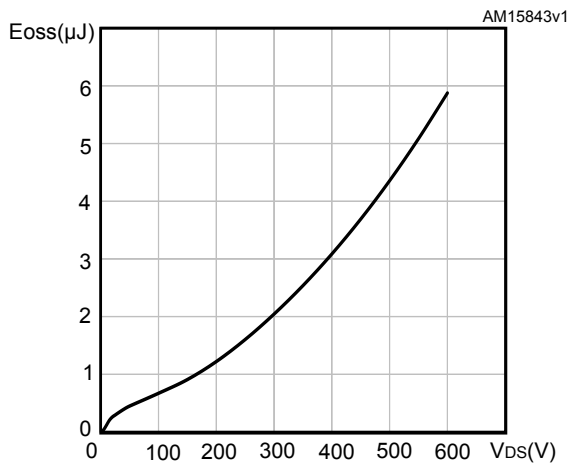
**Figure 9. Normalized on-resistance vs temperature**



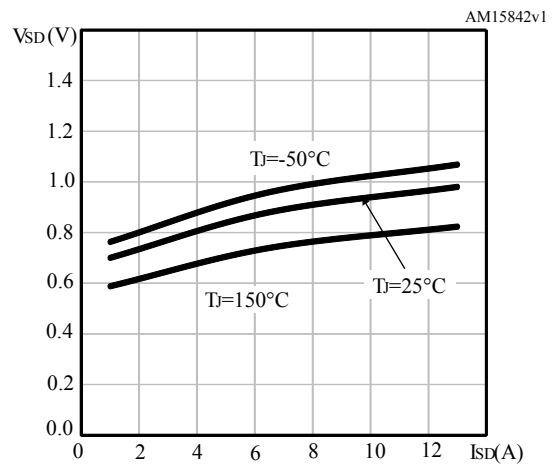
**Figure 10. Normalized breakdown voltage vs temperature**



**Figure 11. Typical output capacitance stored energy**



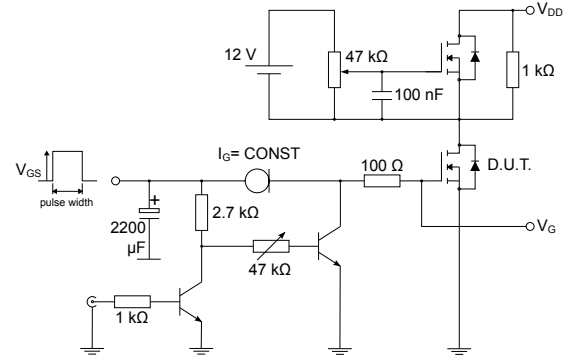
**Figure 12. Typical reverse diode forward characteristics**



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

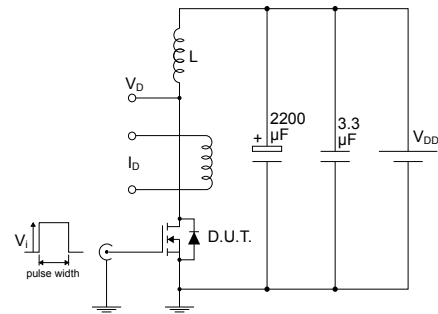

AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**

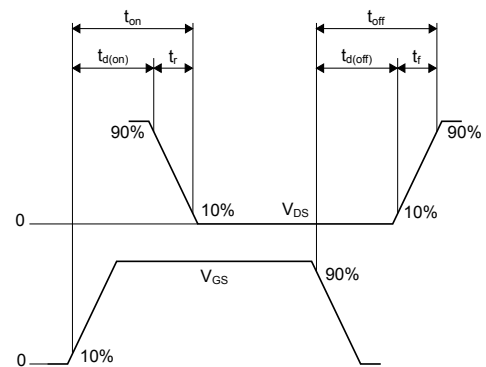

AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


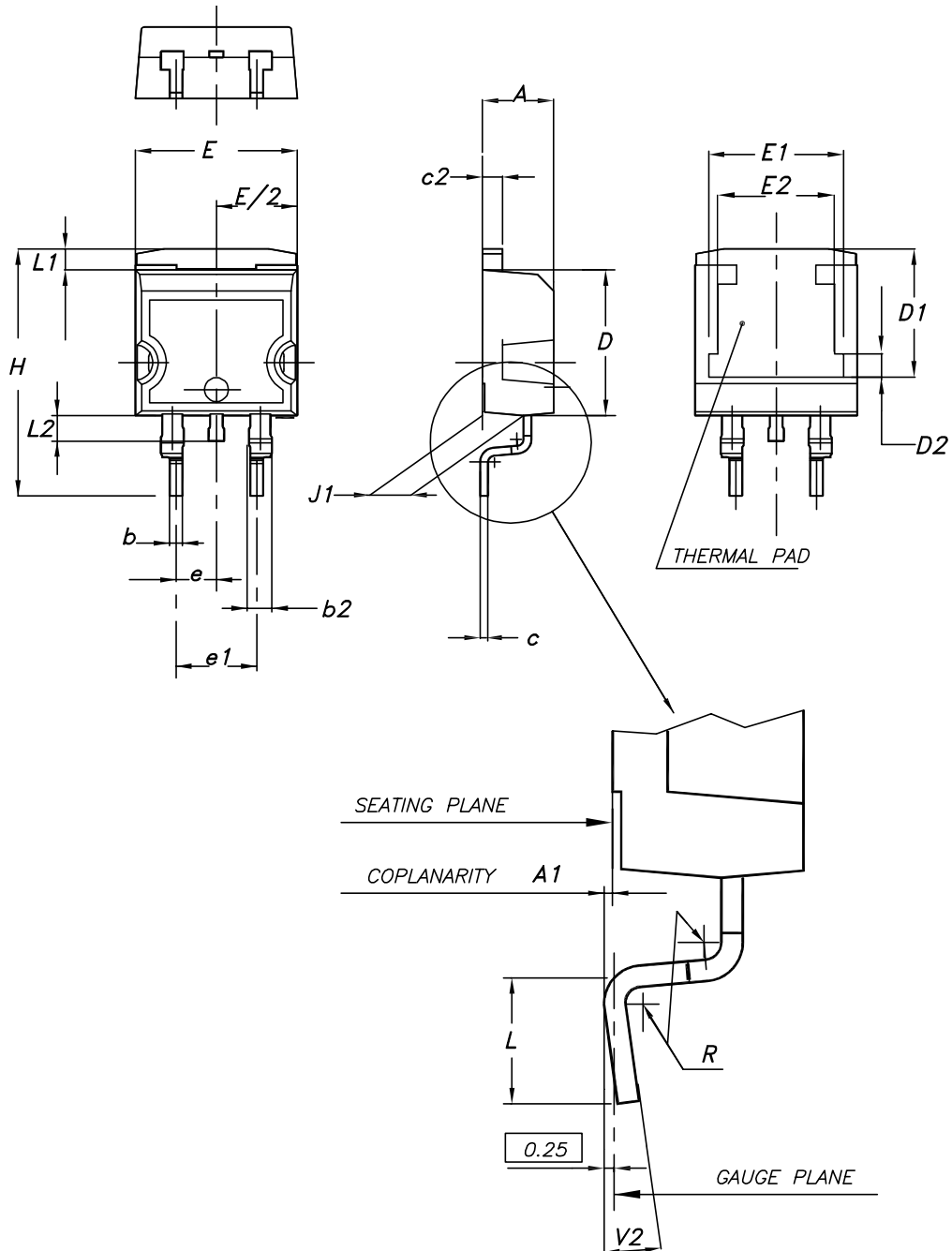
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 19. D<sup>2</sup>PAK (TO-263) type A package outline



0079457\_27

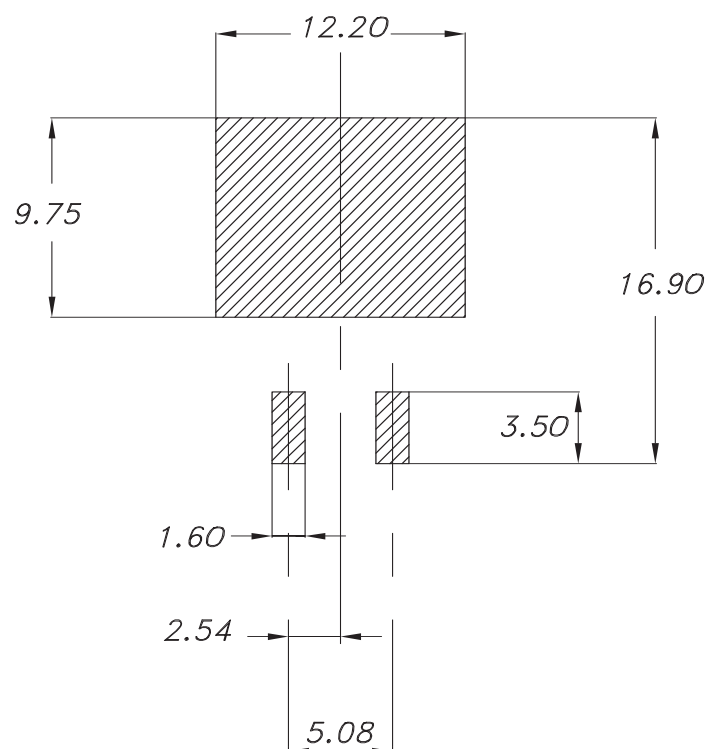
**Table 8. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°



**Table 9. D<sup>2</sup>PAK (TO-263) type B mechanical data**

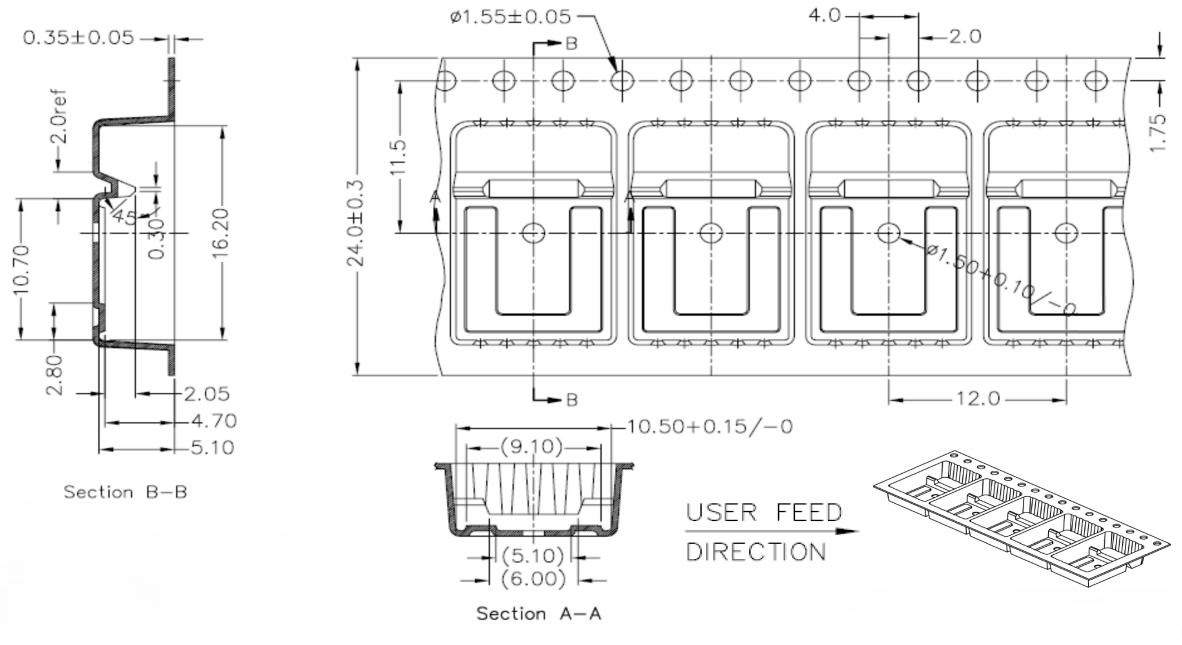
Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

**Figure 21. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**


0079457\_Rev27\_footprint

### 4.3 D<sup>2</sup>PAK packing information

**Figure 22. D<sup>2</sup>PAK tape drawing (dimensions are in mm)**



DM01095771\_2

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
16-Apr-2024	1	First release. Part number STB18N60M2 previously included in datasheet DS9714.
08-Jul-2025	2	Updated <a href="#">Section 4: Package information</a> .
02-Apr-2026	3	Updated <a href="#">Section 4: Package information</a> .

---

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	D <sup>2</sup> PAK (TO-263) type A package information .....	<b>8</b>
<b>4.2</b>	D <sup>2</sup> PAK (TO-263) type B package information .....	<b>10</b>
<b>4.3</b>	D <sup>2</sup> PAK packing information .....	<b>12</b>
	<b>Revision history</b> .....	<b>13</b>

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers’ market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved