STB20N95DK5

N-channel 950 V, 0.275 Ω typ., 18 A, MDmesh™ DK5 Power MOSFET in a D²PAK package

Datasheet - preliminary data

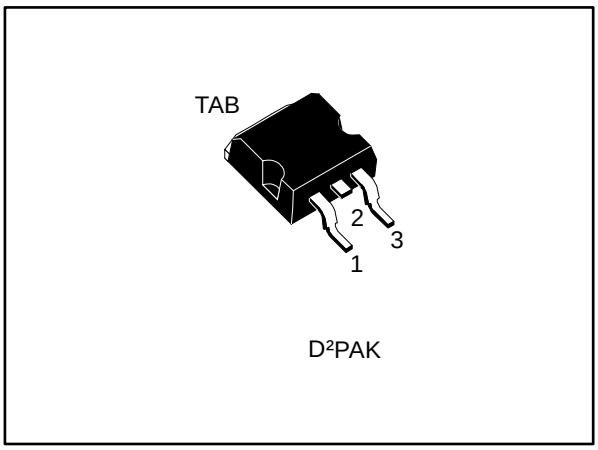
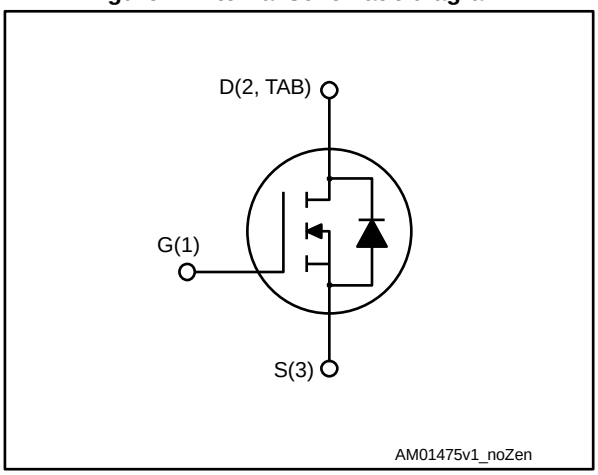


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB20N95DK5	950 V	0.330 Ω	18 A

- Fast-recovery body diode
- Best $R_{DS(on)}$ x area
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is part of the MDmesh™ DK5 fast recovery diode series. The MDmesh™ DK5 combines very low recovery charge (Q_{rr}) and recovery time (t_{rr}) with an excellent improvement in $R_{DS(on)}$ * area and one of the most effective switching behaviors, ideal for half bridge and full bridge converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB20N95DK5	20N95DK5	D²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	18	V
I_D	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM}(1)	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 8.5 A, di/dt ≤ 400 A/µs, V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD} = 475 V

(3)V_{DS} ≤ 760 V

Table 3: Avalanche characteristics

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	30	°C/W

Notes:

(1)When mounted on 1 inch² FR-4 board, 2 Oz Cu.

Table 4: Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Maximum current during repetitive or single pulse avalanche	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR} ,V_{DD} = 50 V)	520	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0 V	950			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 950 V			1	µA
		V_{GS} = 0 V, V_{DS} = 950 V, T_C= 125 °C (1)			100	µA
I_{GSS}	Gate source leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DD} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		0.275	0.330	Ω

Notes:

(1)Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS}= 0 V	-	1600	-	pF
C_{oss}	Output capacitance		-	76	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
$C_{o(tr)}$(1)	Time- related equivalent capacitance	V_{GS} = 0 V, V_{DS}= 0 to 760 V	-	169	-	pF
$C_{o(er)}$(2)	Energy-related equivalent capacitance		-	60	-	pF
R_g	Intrinsic gate resistance	f =1 MHz, I_D= 0 A	-	4	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 18 A, V_{GS} = 0 to 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	50.7	-	nC
Q_{gs}	Gate source charge		-	7.8	-	nC
Q_{gd}	Gate drain charge		-	34.2	-	nC

Notes:

(1)$C_{o(tr)}$ is defined as the constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is defined as the constant equivalent capacitance giving the same stored energy as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DS} = 475 V, I_D= 9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15: "Test circuit for resistive load switching times"* and *Figure 20: "Switching time waveform"*)	-	23	-	ns
t_r	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time		-	74	-	ns
t_f	Fall time		-	25.4	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM}(1)	Source-drain current (pulsed)		-		72	A
V_{SD}(2)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	150		ns
Q_{rr}	Reverse recovery charge		-	1		µC
I_{RRM}	Reverse recovery current		-	13.5		A
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	264		ns
Q_{rr}	Reverse recovery charge		-	2.9		µC
I_{RRM}	Reverse recovery current		-	22		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

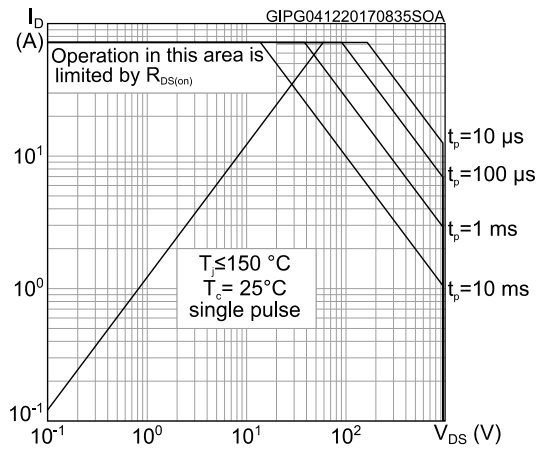


Figure 3: Thermal impedance

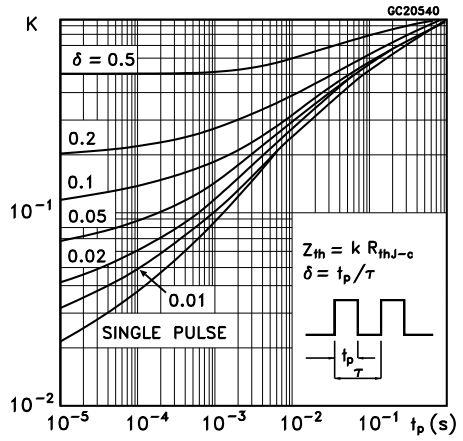


Figure 4: Output characteristics

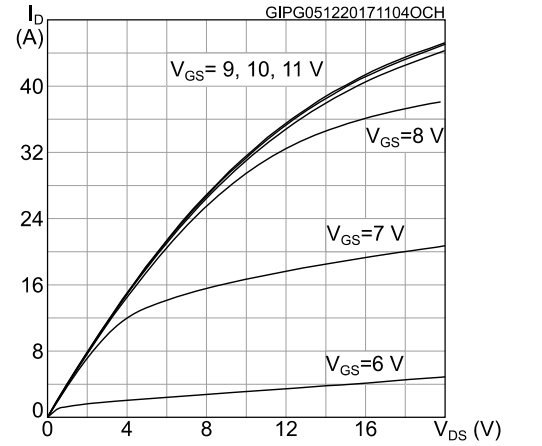


Figure 5: Transfer characteristics

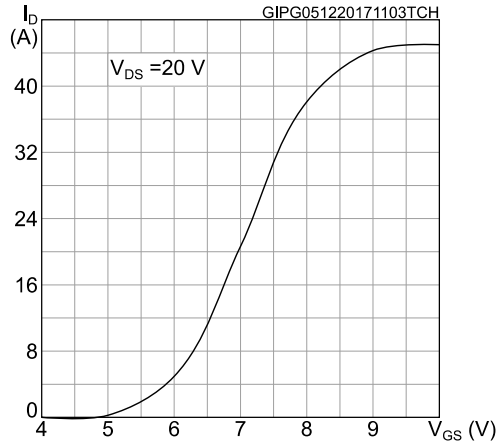


Figure 6: Gate charge vs gate-source voltage

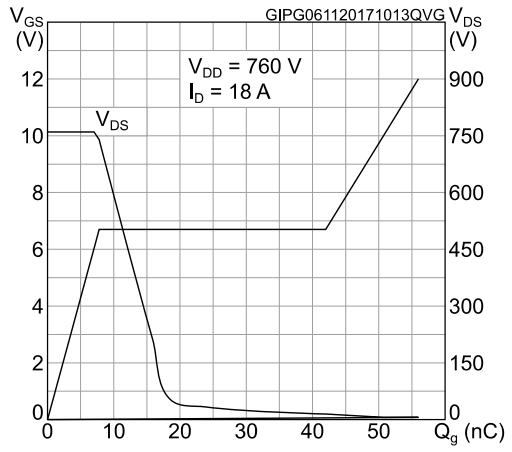


Figure 7: Static drain-source on-resistance

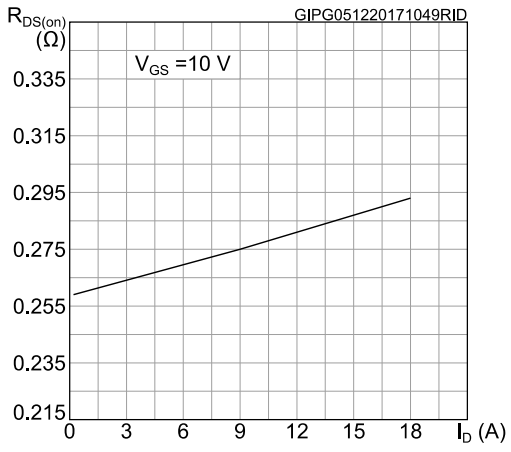


Figure 8: Capacitance variations

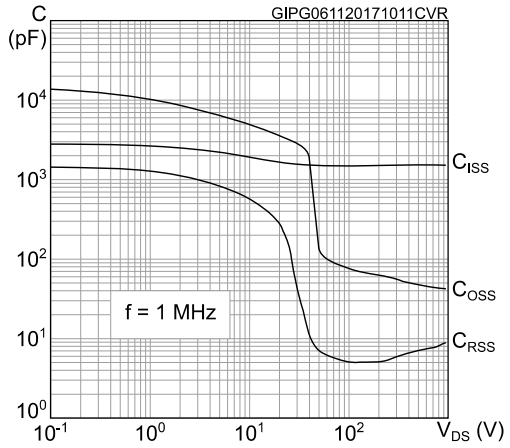


Figure 9: Output capacitance stored energy

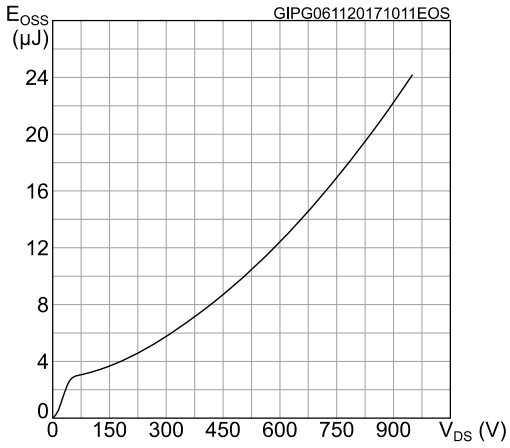


Figure 10: Normalized gate threshold voltage vs temperature

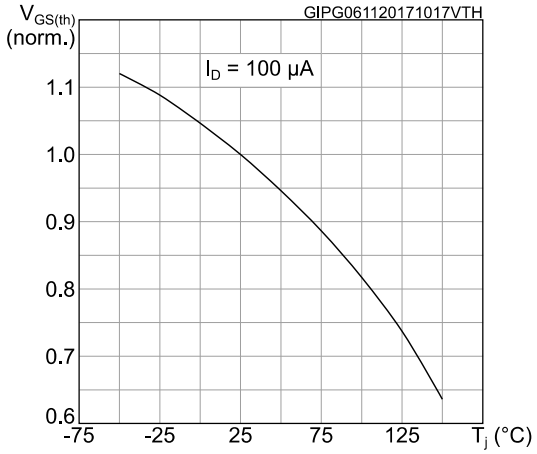


Figure 11: Normalized on-resistance vs temperature

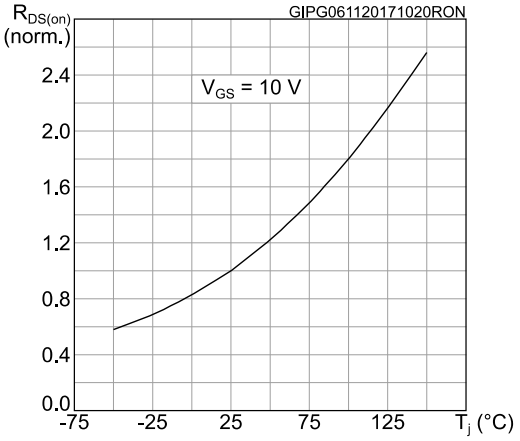


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

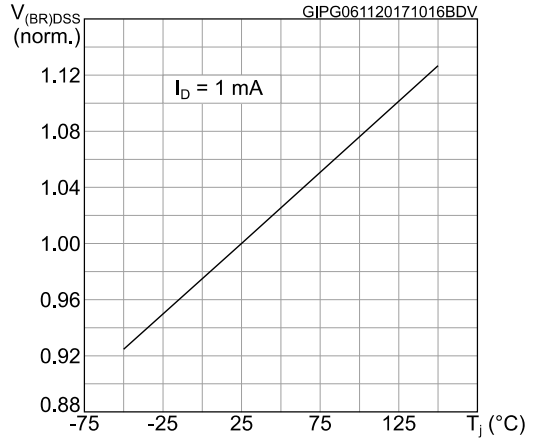


Figure 13: Source-drain diode forward characteristics

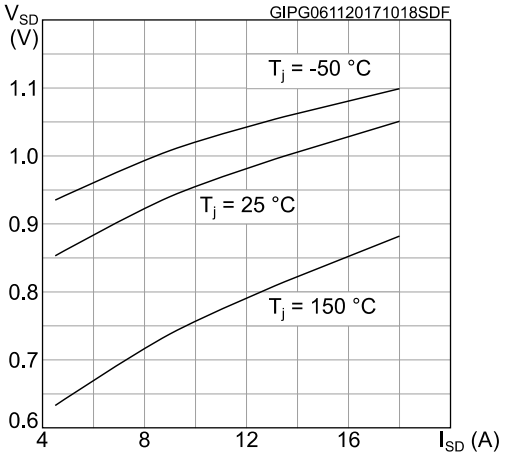
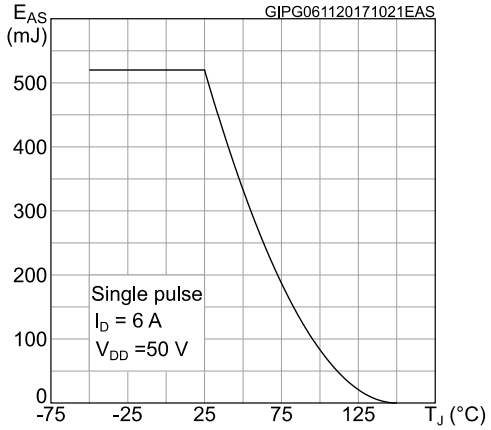


Figure 14: Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 15: Test circuit for resistive load switching times

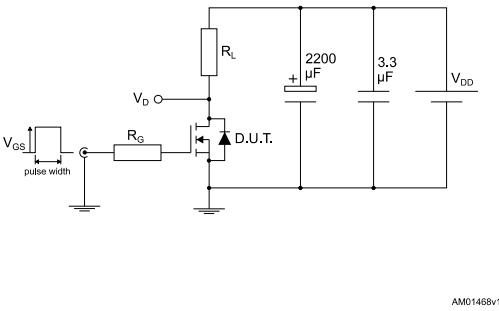


Figure 16: Test circuit for gate charge behavior

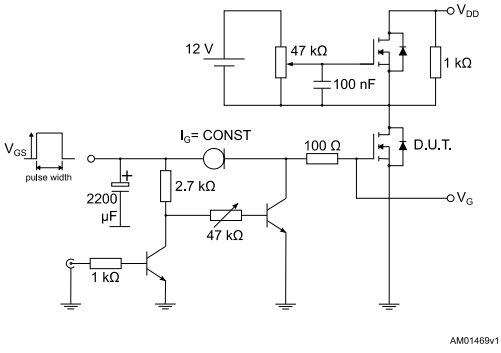


Figure 17: Test circuit for inductive load switching and diode recovery times

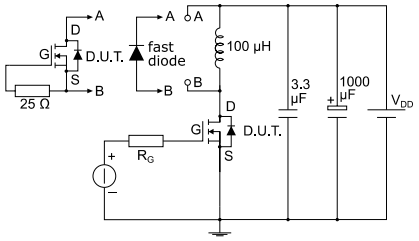


Figure 18: Unclamped inductive load test circuit

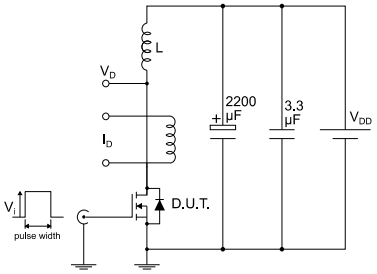


Figure 19: Unclamped inductive waveform

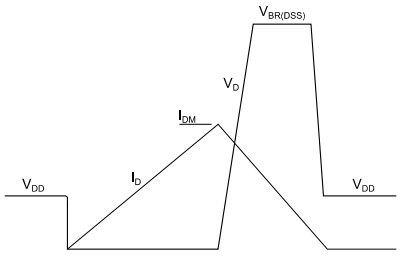
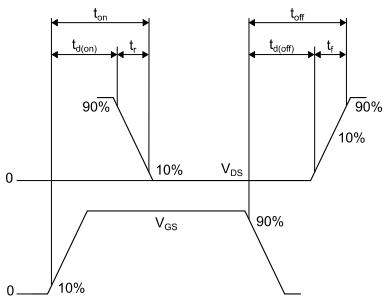


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 21: D²PAK (TO-263) type A2 package outline

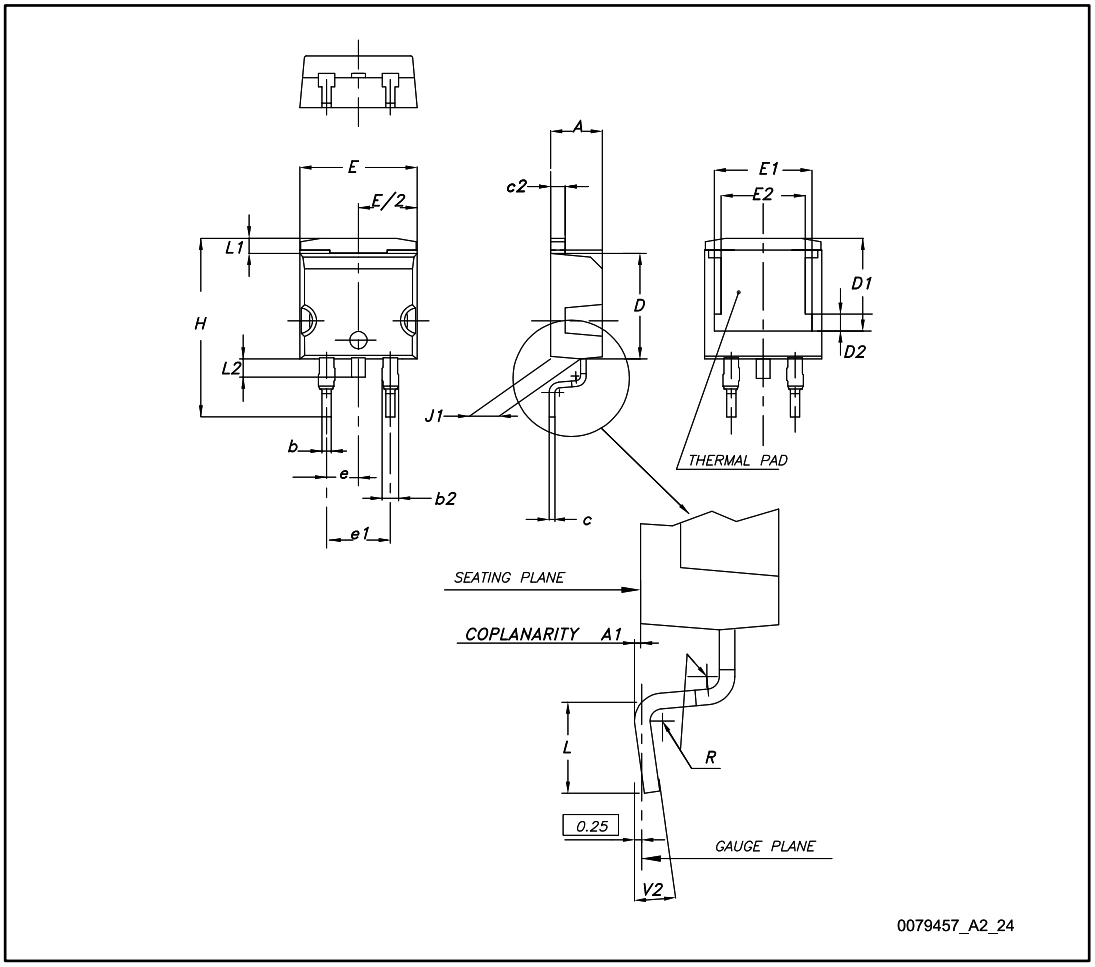
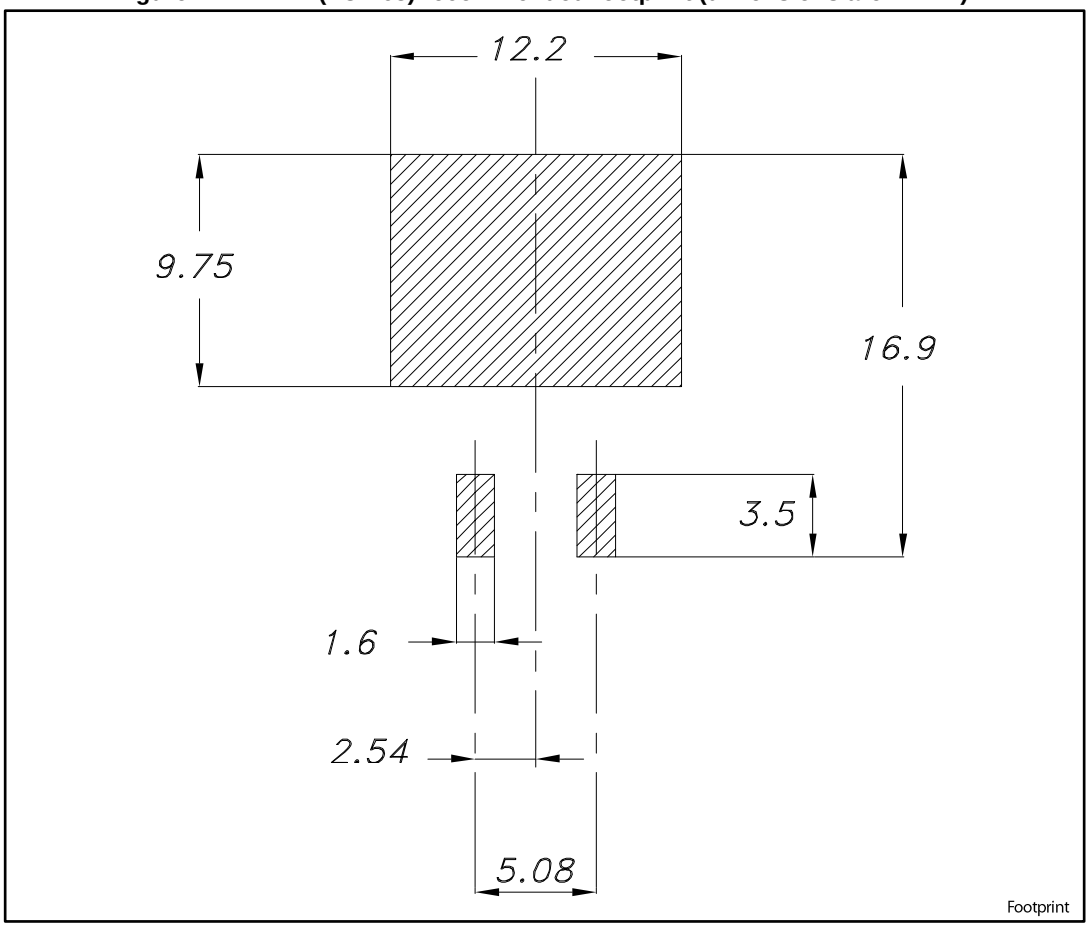


Table 9: D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 22: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 D²PAK (TO-263) packing information

Figure 23: D²PAK tape outline

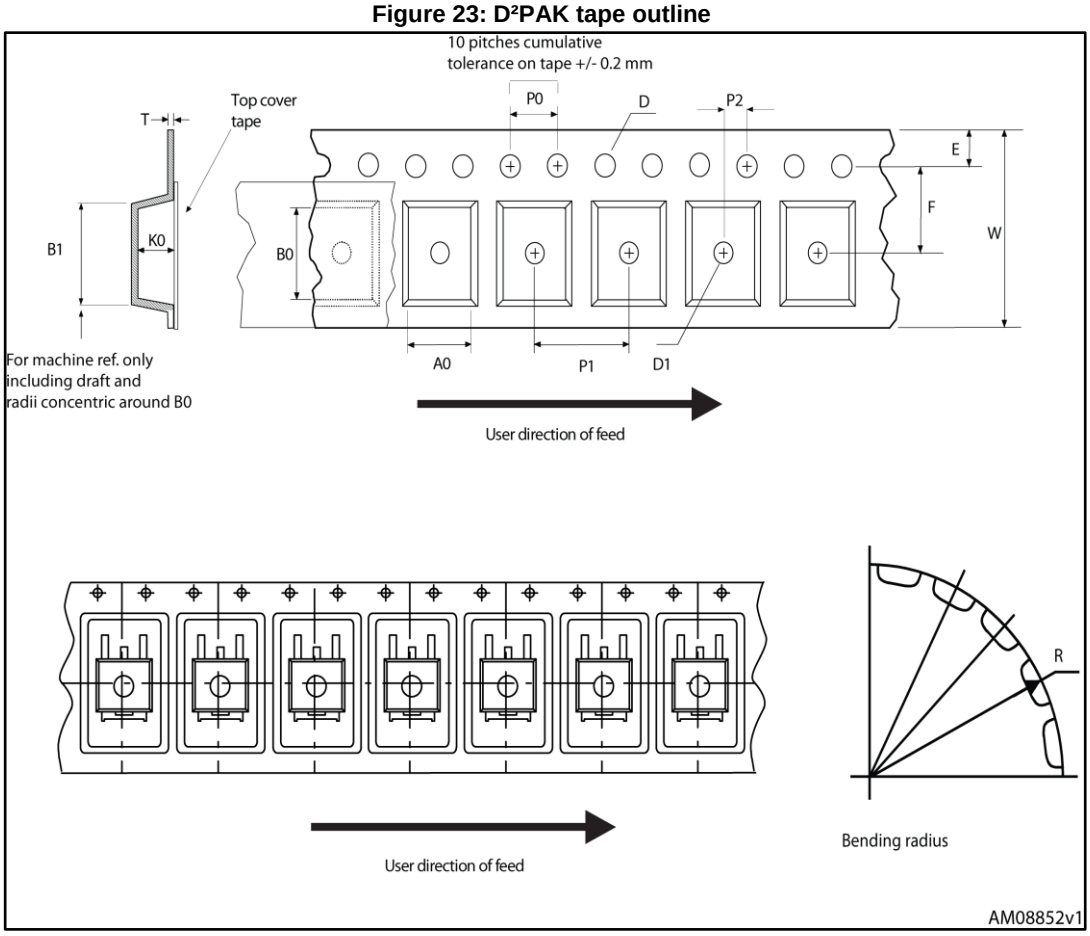


Figure 24: D²PAK reel outline

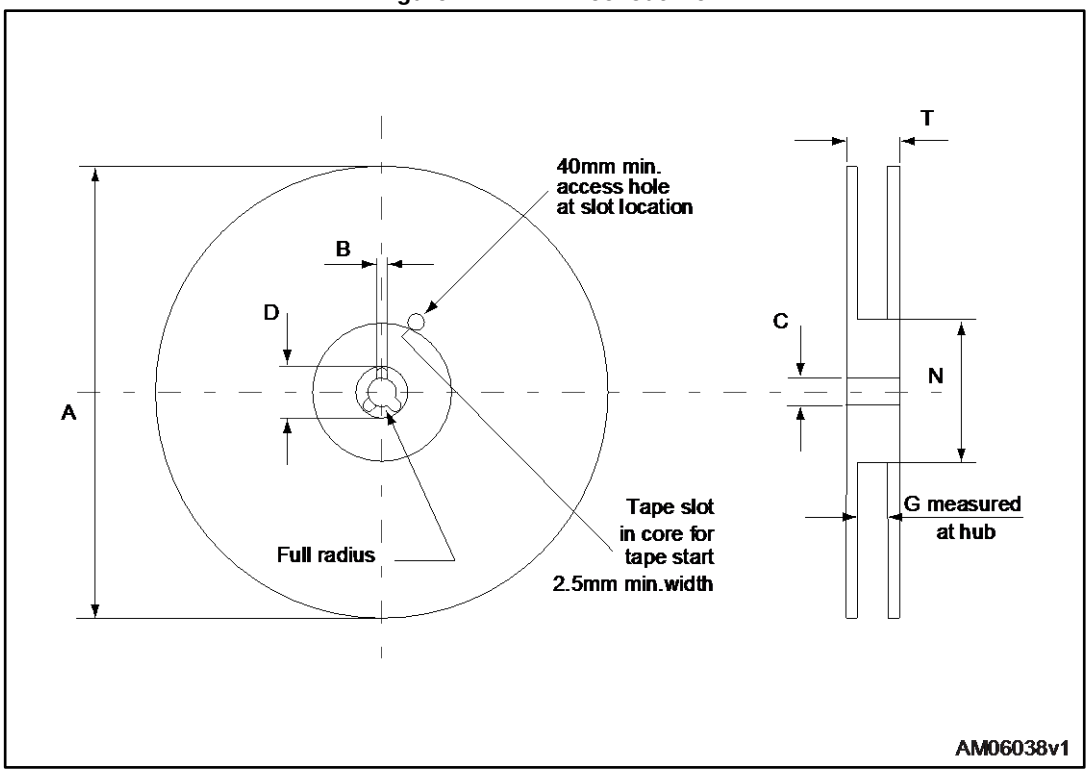


Table 10: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Dec-2017	1	Initial release

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