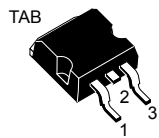
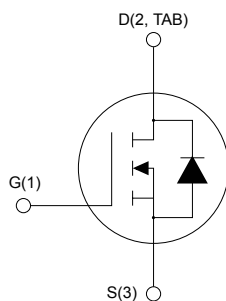


N-channel 650 V, 95 mΩ typ., 24 A MDmesh M5 Power MOSFET in a D²PAK package


D²PAK


AM01475v1_noZen


Product status link
[STB32N65M5](#)
Product summary

Order code	STB32N65M5
Marking	32N65M5
Package	D ² PAK
Packing	Tape and reel

Features

Order code	V _{DS} at T _J max.	R _{DS(on)} max.	I _D
STB32N65M5	710 V	119 mΩ	24 A

- 100% avalanche tested
- Excellent switching performance
- Extremely low R_{DS(on)}
- Low gate charge and input capacitance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	24	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	15	A
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 24\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-to-case	0.83	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance junction-to-ambient	30	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	8	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	650	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$,			1	μA
		$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$		95	119	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3320	-	pF
C_{oss}	Output capacitance			75		
C_{rss}	Reverse transfer capacitance			5		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }520\text{ V}$	-	210	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	70	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	72	-	nC
Q_{gs}	Gate-source charge			17		
Q_{gd}	Gate-drain charge			29		

1. $C_{o(tr)}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$, $I_D = 15\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	53	-	ns
t_r	Rise time			12		
t_c	Cross time			29		
t_f	Fall time			16		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				96	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	375		ns
Q_{rr}	Reverse recovery charge			6		μC
I_{RRM}	Reverse recovery current			33		A
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	440		ns
Q_{rr}	Reverse recovery charge			8		μC
I_{RRM}	Reverse recovery current			36		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

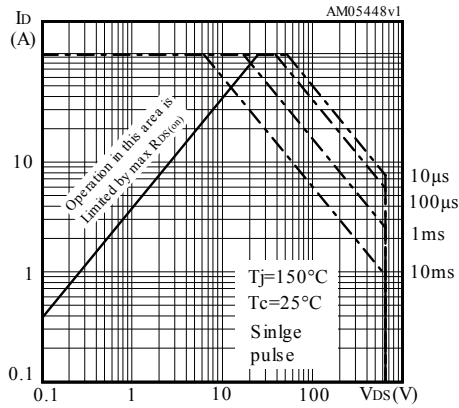
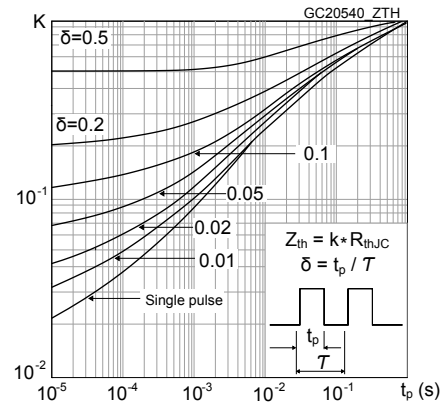
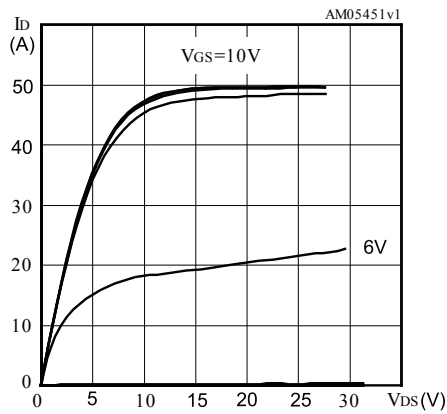
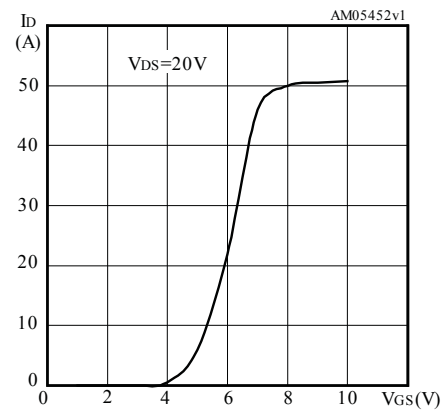
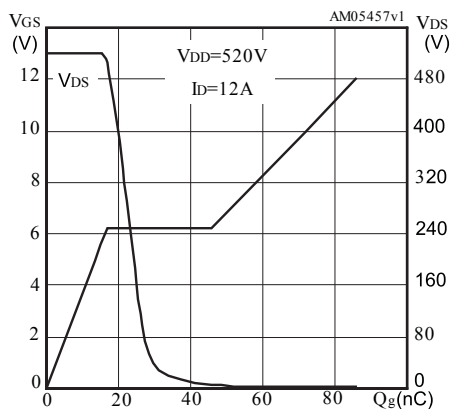
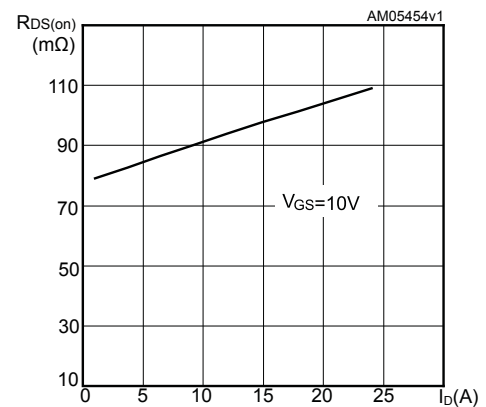
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on resistance


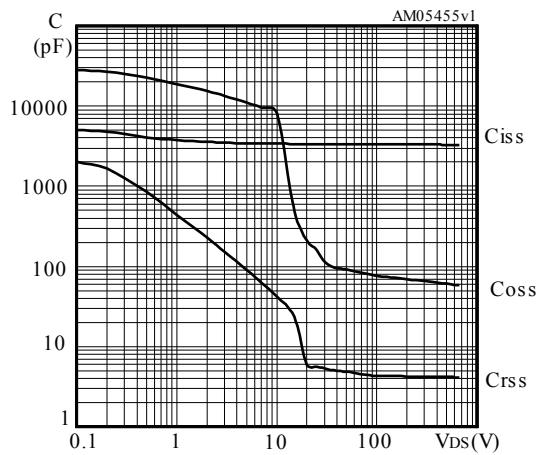
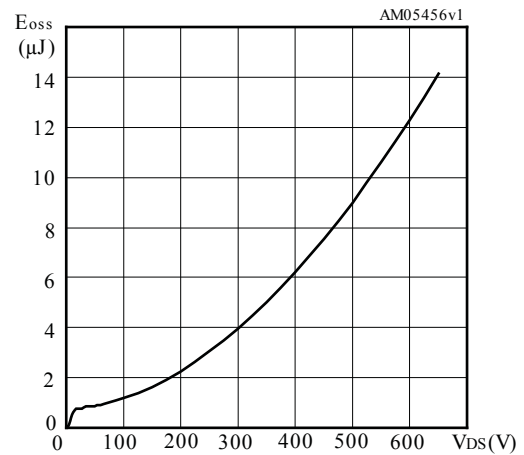
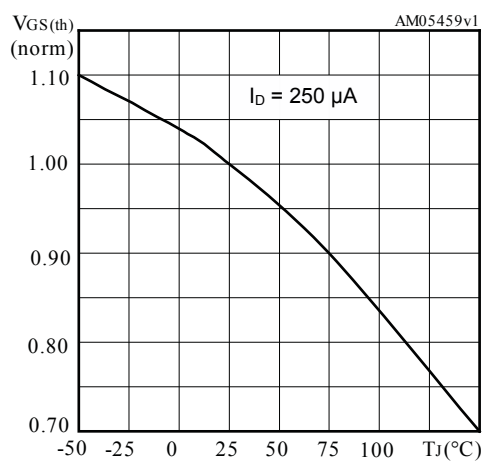
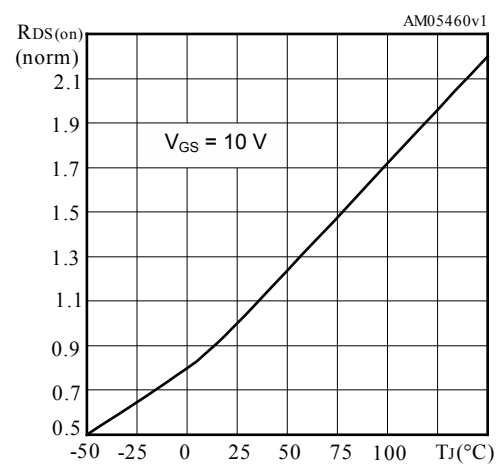
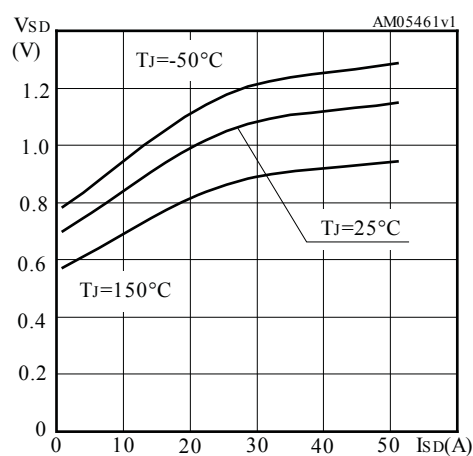
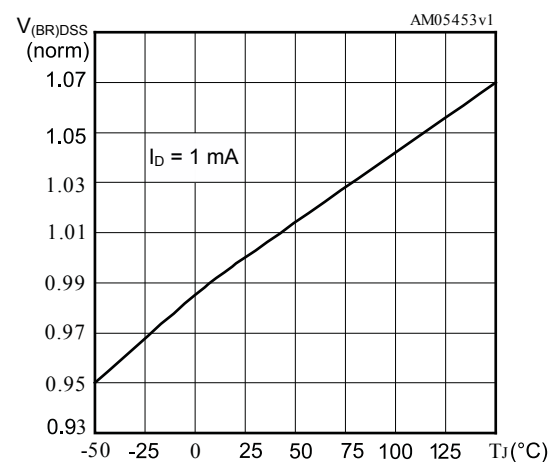
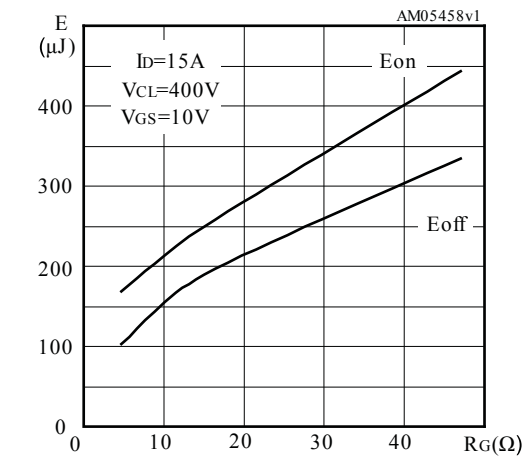
Figure 7. Capacitance variations

Figure 8. Output capacitance stored energy

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on resistance vs temperature

Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized V(BR)DSS vs temperature


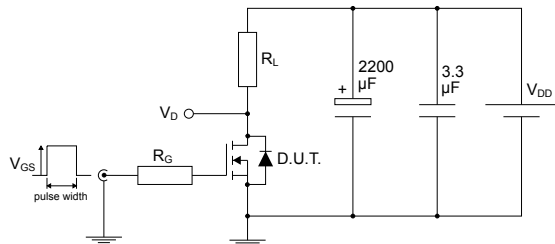
Figure 13. Switching energy vs gate resistance



* Eon including reverse recovery of a SiC diode.

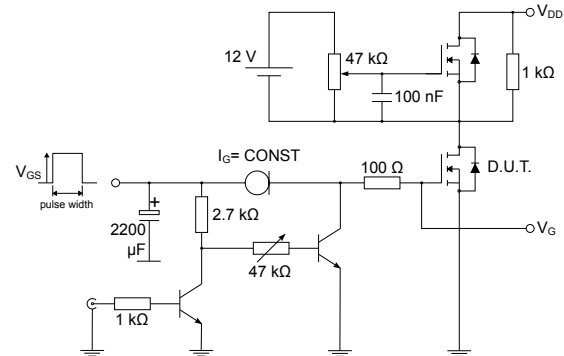
3 Test circuits

Figure 14. Test circuit for resistive load switching times



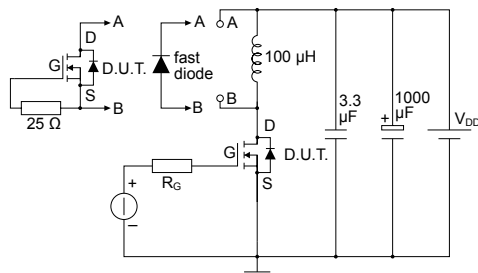
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Figure 15. Test circuit for gate charge behavior



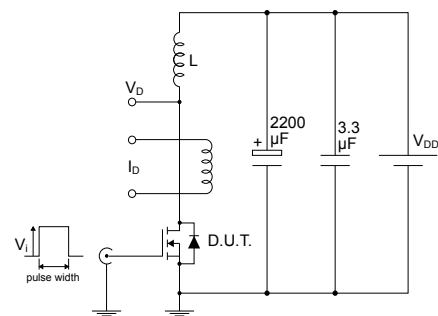
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Figure 16. Test circuit for inductive load switching and diode recovery times



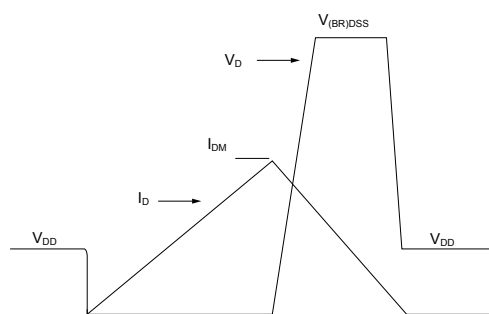
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Figure 17. Unclamped inductive load test circuit



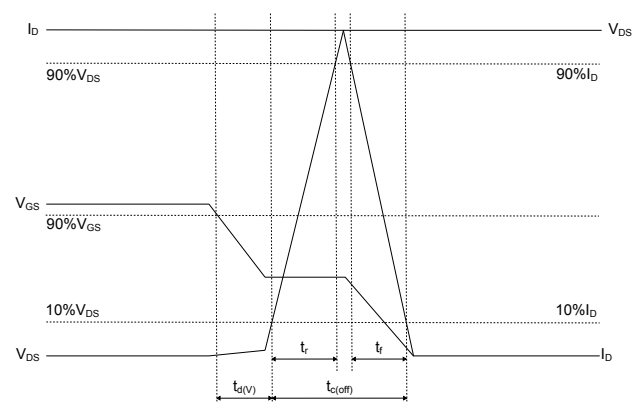
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



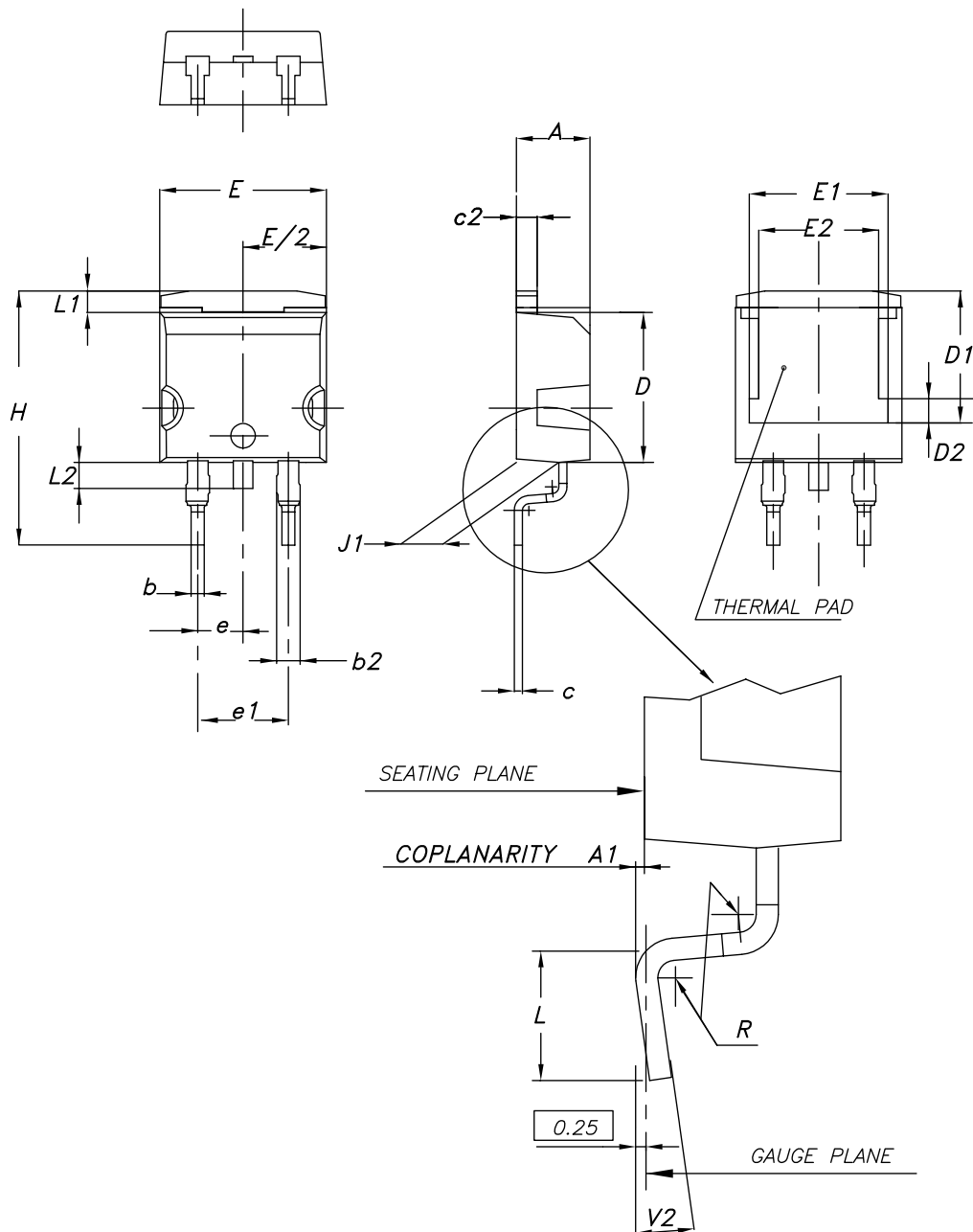
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 20. D²PAK (TO-263) type A2 package outline

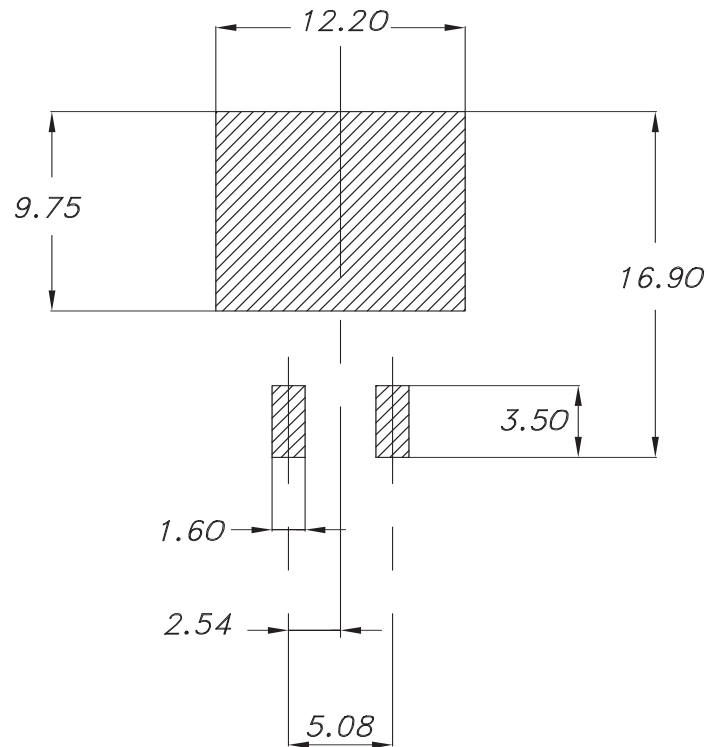


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Table 8. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

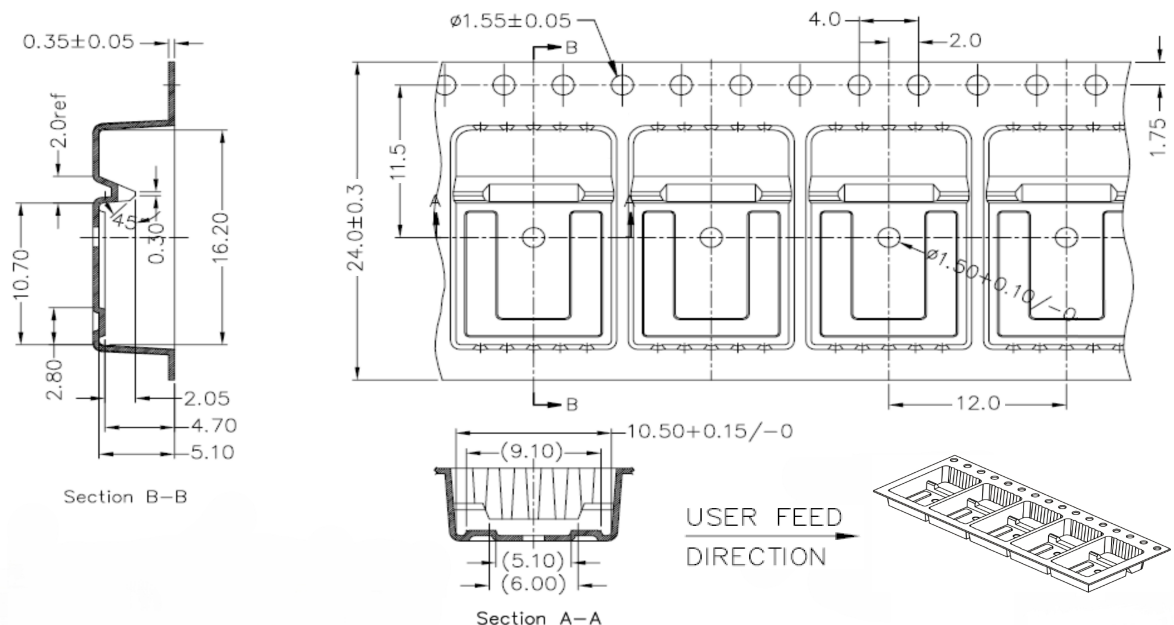
Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)



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4.2 D²PAK packing information

Figure 22. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. Document revision history

Date	Version	Changes
16-Jan-2009	1	First release
01-Sep-2009	2	Document status promoted from preliminary data to datasheet.
30-Sep-2009	3	Corrected V_{GS} value on Table 2: Absolute maximum ratings
06-Oct-2011	4	$C_{o(er)}$ and $C_{o(tr)}$ values changed in <i>Table 5: Dynamic</i> <i>Table 6: Switching times</i> parameters updates <i>Figure 24: Switching time waveform</i> has been corrected Minor text changes <i>Section 4: Package mechanical data</i> has been modified. Added: – <i>Table 8: D²PAK (TO-263) mechanical data</i>, <i>Figure 25: D²PAK (TO-263) drawing</i> and <i>Figure 26: D²PAK footprint</i>; – <i>Table 9: TO-220FP mechanical data</i>, and <i>Figure 27: TO-220FP drawing</i>; – <i>Table 10: I²PAK (TO-262) mechanical data</i>, and <i>Figure 28: I²PAK (TO-262) drawing</i>; – <i>Table 11: TO-220 type A mechanical data</i>, and <i>Figure 29: TO-220 type A drawing</i>; – <i>Table 12: TO-247 mechanical data</i>, and <i>Figure 30: TO-247 drawing</i>; <i>Section 5: Packaging mechanical data</i> has been modified. Added: – <i>Table 13: D²PAK (TO-263) tape and reel mechanical data</i>, <i>Figure 31: Tape</i> and <i>Figure 32: Reel</i>;
02-Nov-2018	5	The part numbers STF32N65M5, STI32N65M5, STP32N65M5, STW32N65M5 have been moved to a separate datasheet. Content reworked to improve readability, no technical changes.
04-Aug-2025	6	Updated Section 4.1: D²PAK (TO-263) type A2 package information. Updated Figure 6. Static drain-source on resistance. Minor text changes.

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