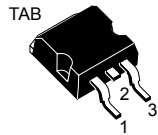
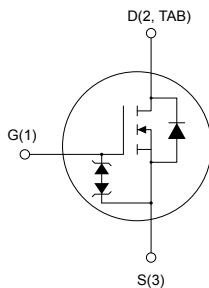


N-channel 650 V, 93 mΩ typ., 32 A MDmesh DM2 Power MOSFET in a D²PAK package


D²PAK


AM01476v1_tab


Maturity status link
[STB35N65DM2](#)
Device summary

| | |
|-------------------|--------------------|
| Order code | STB35N65DM2 |
| Marking | 35N65DM2 |
| Package | D ² PAK |
| Packing | Tape and reel |

Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|-------------|-----------------|--------------------------|----------------|
| STB35N65DM2 | 650 V | 110 mΩ | 32 A |

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 32 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 20 | |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 90 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 250 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 100 | V/ns |
| $di/dt^{(2)}$ | Peak diode recovery current slope | 1000 | A/ μs |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 100 | V/ns |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature | | $^\circ\text{C}$ |

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 32\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
3. $V_{DS} \leq 520\text{ V}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------------|---|-------|--------------------|
| R_{thJC} | Thermal resistance, junction-to-case | 0.5 | $^\circ\text{C/W}$ |
| $R_{thJA}^{(1)}$ | Thermal resistance, junction-to-ambient | 30 | $^\circ\text{C/W}$ |

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.) | 4 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 1150 | mJ |

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|---------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 650 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}^{(1)}$ | | | 100 | |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$ | | | ± 5 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 16\text{ A}$ | | 93 | 110 | m Ω |

1. Specified by design, not tested in production.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 2540 | - | pF |
| C_{oss} | Output capacitance | | - | 115 | - | pF |
| C_{rSS} | Reverse transfer capacitance | | - | 2.5 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$ | - | 204 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 4.2 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 520\text{ V}$, $I_D = 32\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior) | - | 56.3 | - | nC |
| Q_{gs} | Gate-source charge | | - | 12.7 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 27.6 | - | nC |

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 325\text{ V}$, $I_D = 16\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 23.4 | - | ns |
| t_r | Rise time | | - | 23 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 72 | - | ns |
| t_f | Fall time | | - | 10.4 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 32 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 90 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 32\text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 32\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 100 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 0.42 | | μC |
| I_{RRM} | Reverse recovery current | | - | 8.4 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 32\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 205 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1.8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 17.6 | | A |

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%

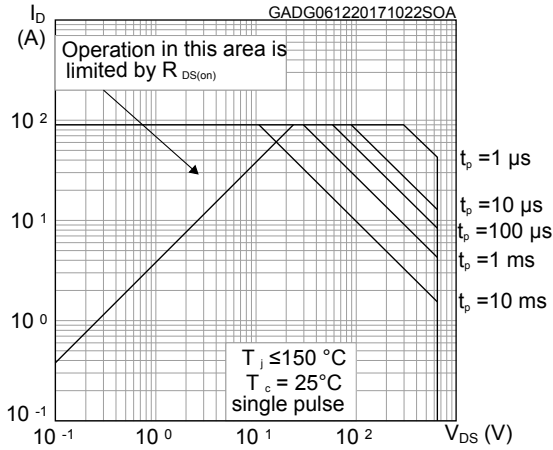
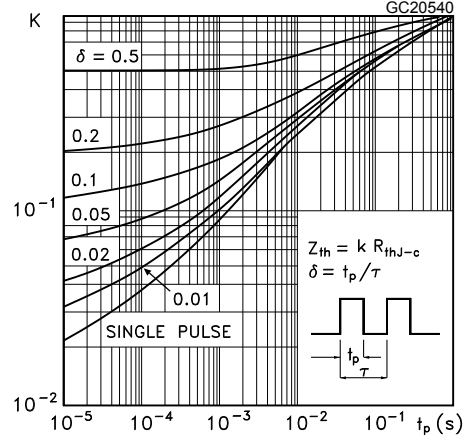
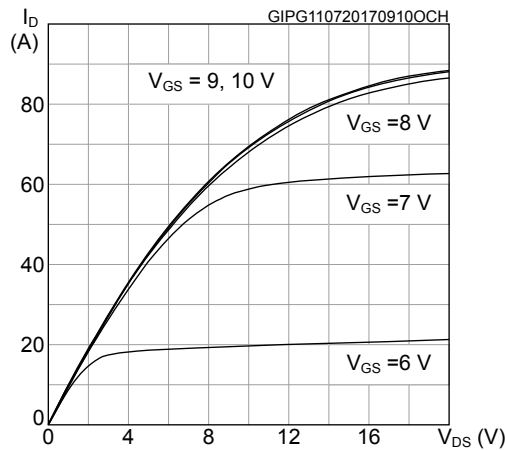
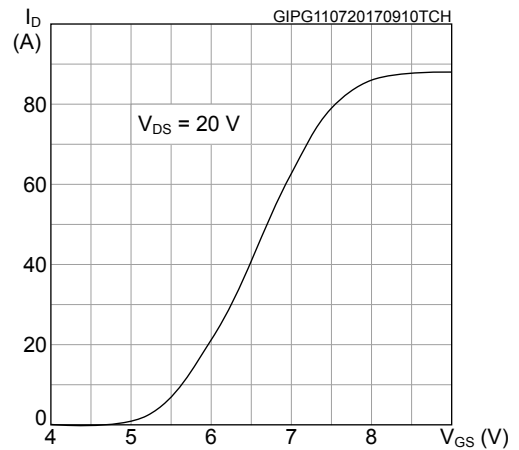
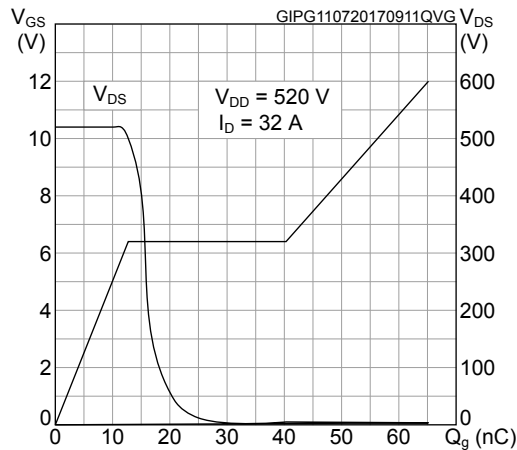
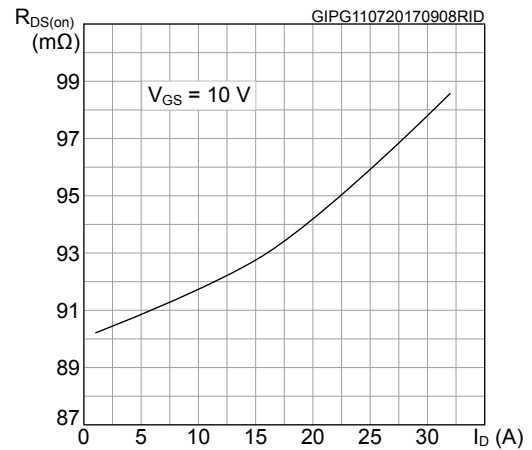
2.1 Electrical characteristics curves
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

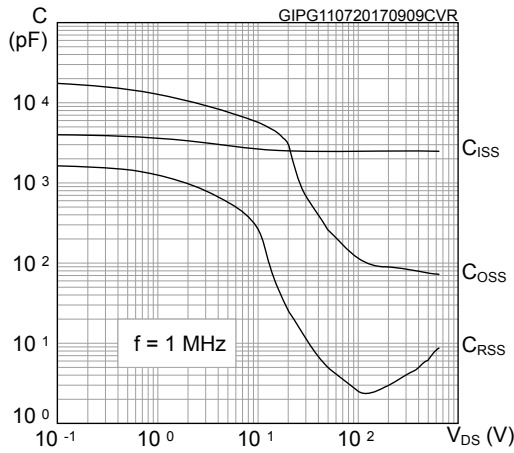


Figure 8. Normalized gate threshold voltage vs temperature

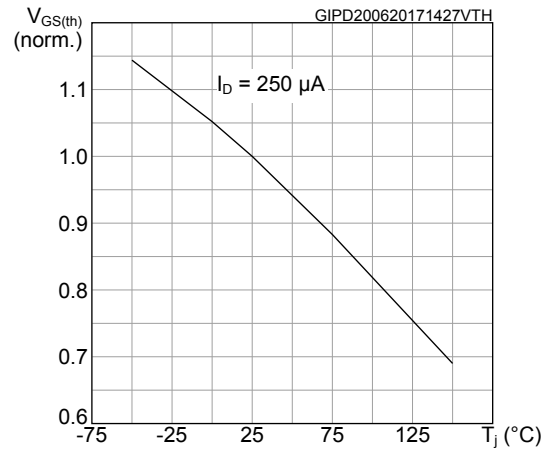


Figure 9. Normalized on-resistance vs temperature

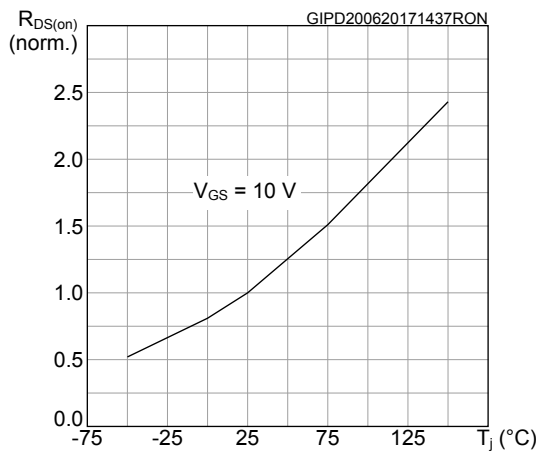


Figure 10. Normalized V_(BR)DSS vs temperature

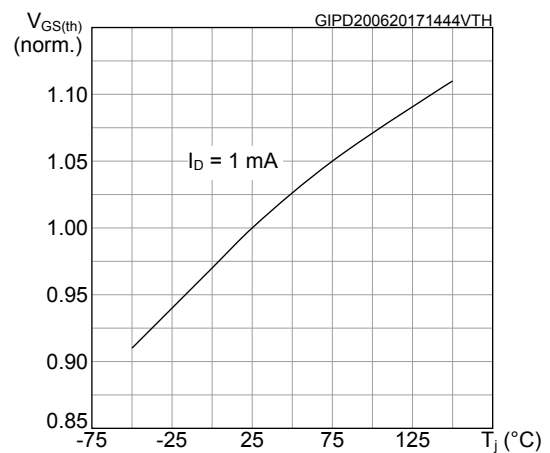


Figure 11. Output capacitance stored energy

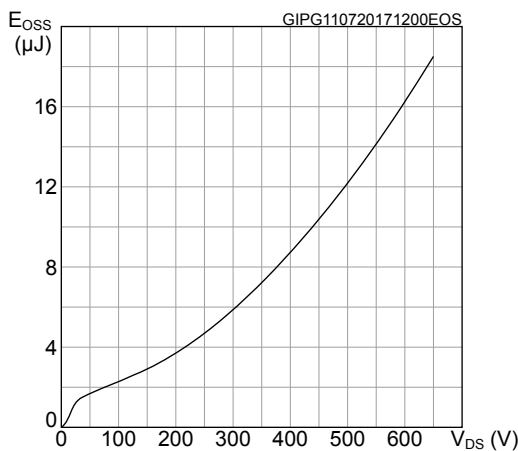
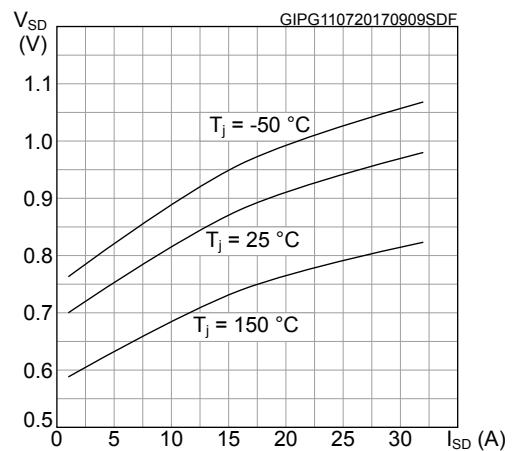
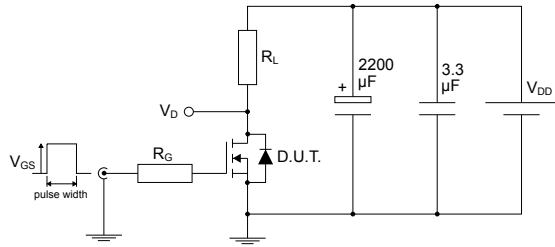


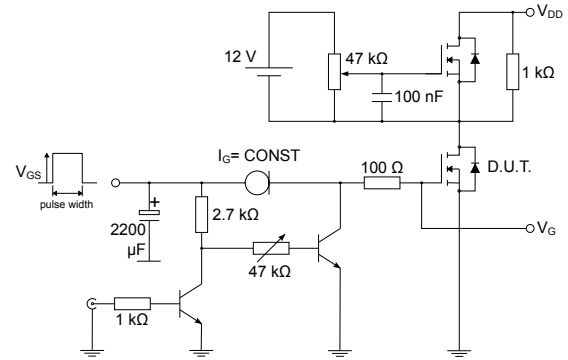
Figure 12. Source- drain diode forward characteristics



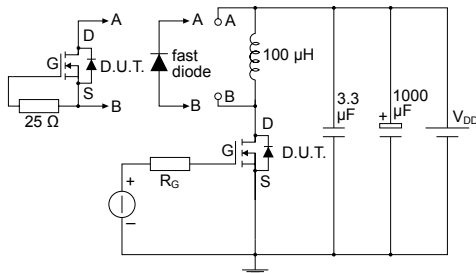
3 Test circuits

Figure 13. Test circuit for resistive load switching times


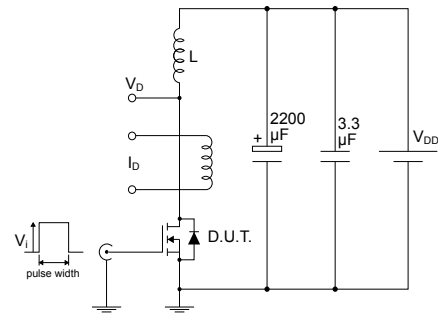
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Figure 14. Test circuit for gate charge behavior


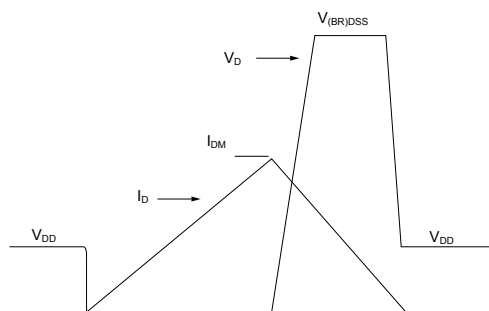
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Figure 15. Test circuit for inductive load switching and diode recovery times


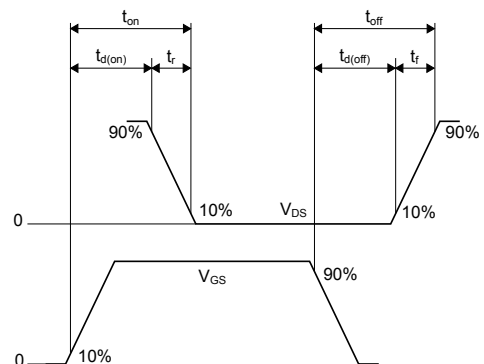
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


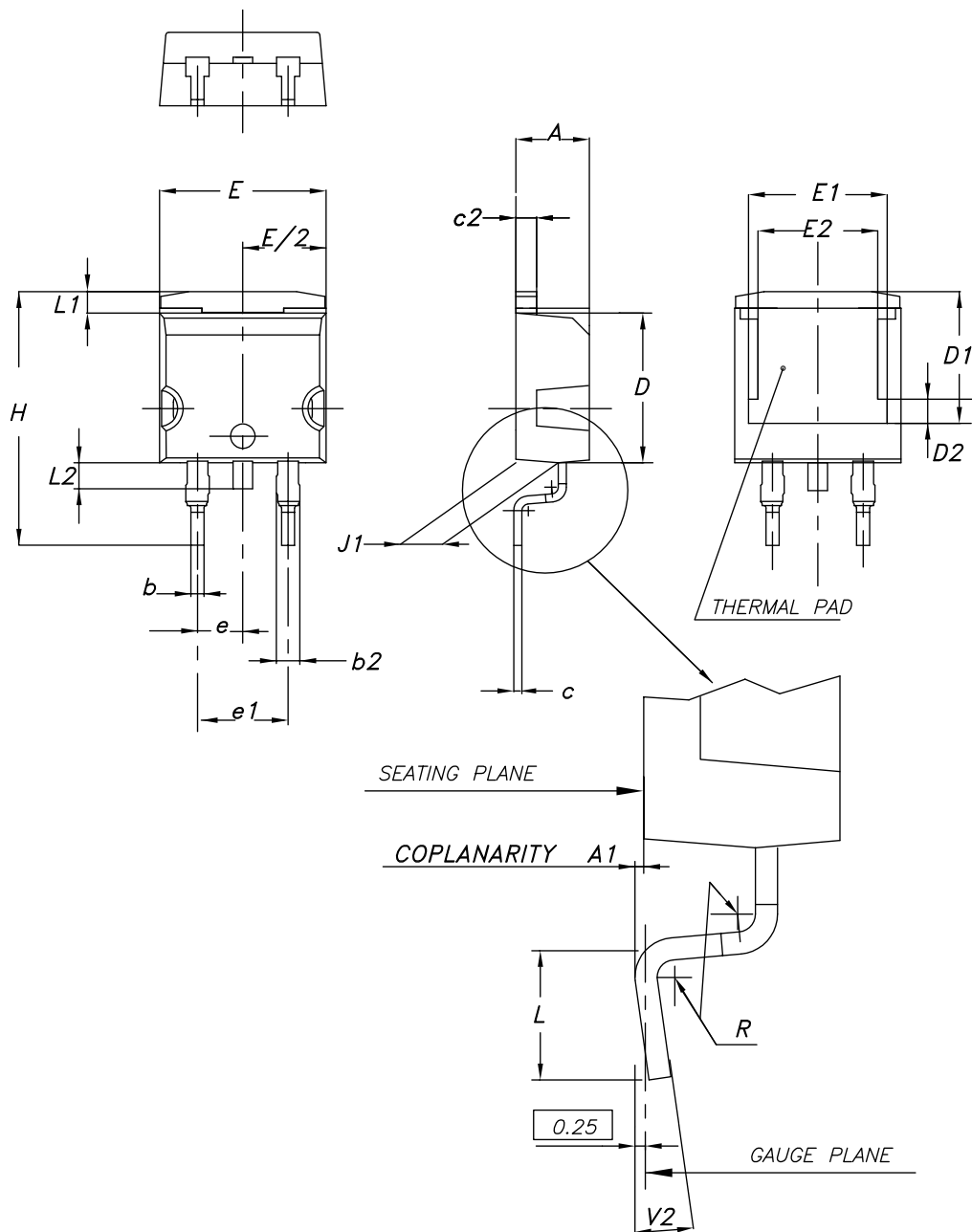
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 19. D²PAK (TO-263) type A2 package outline

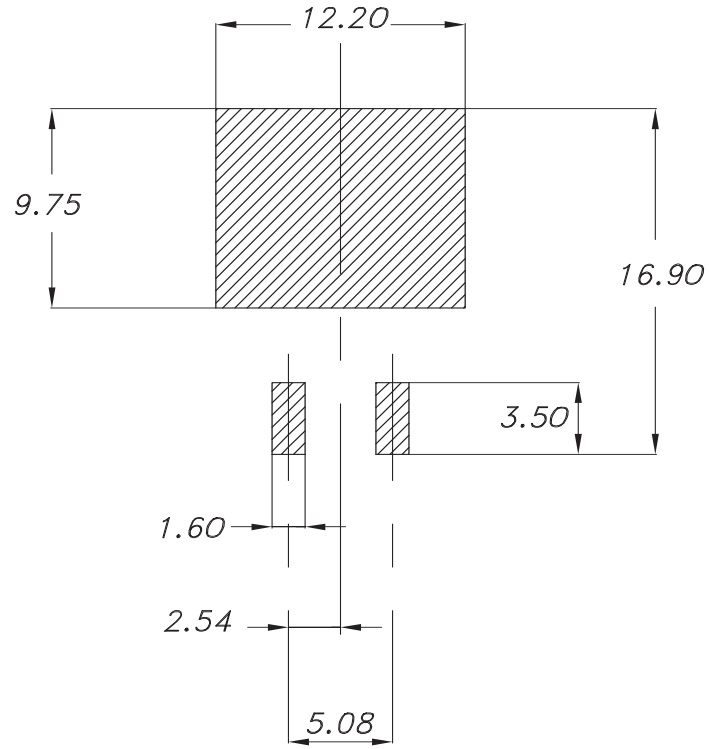


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Table 8. D²PAK (TO-263) type A2 package mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10.00 | | 10.40 |
| E1 | 8.70 | 8.90 | 9.10 |
| E2 | 7.30 | 7.50 | 7.70 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15.00 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.40 | |
| V2 | 0° | | 8° |

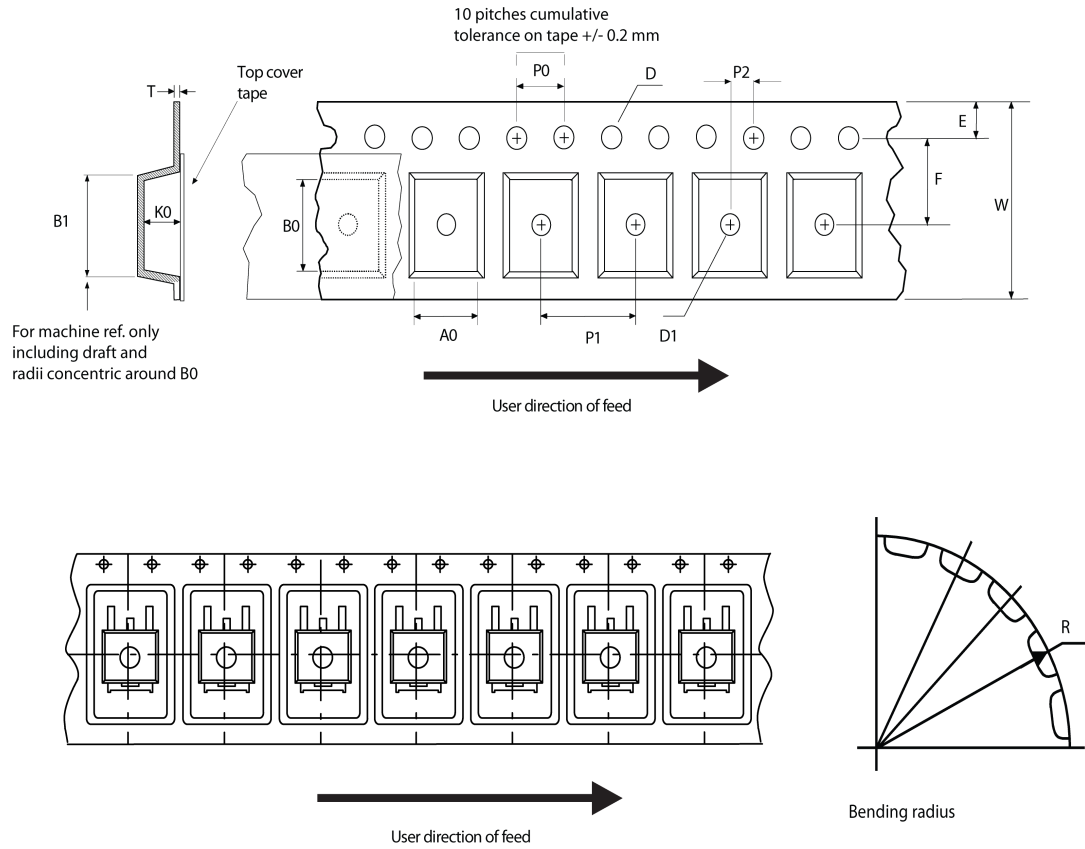
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



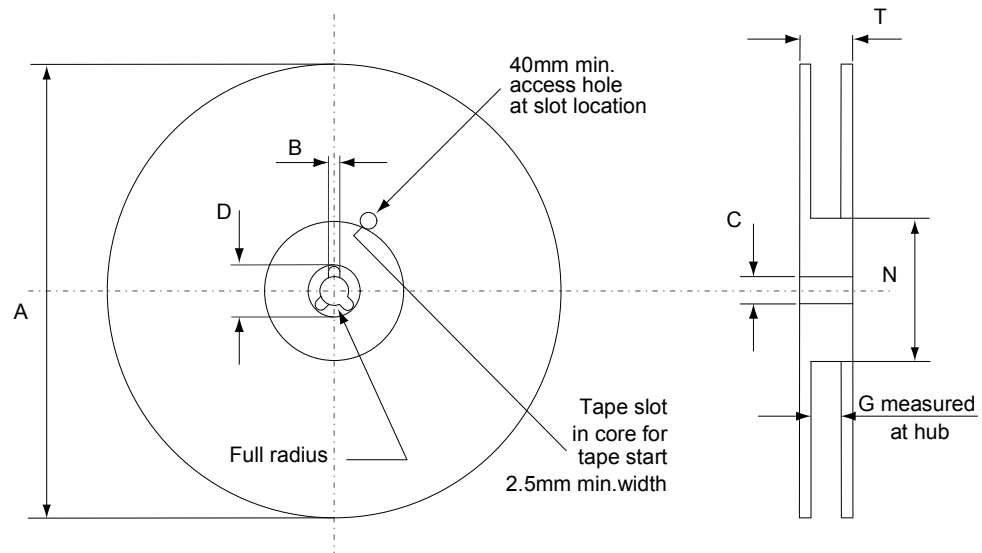
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4.2 D²PAK packing information

Figure 21. D²PAK tape outline



AM08852v1

Figure 22. D²PAK reel outline


AM06038v1

Table 9. D²PAK tape and reel mechanical data

| Dim. | Tape | | Dim. | Reel | |
|------|------|------|---------------|------|------|
| | mm | | | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base quantity | | 1000 |
| P2 | 1.9 | 2.1 | Bulk quantity | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 10-Jul-2017 | 1 | Initial release |
| 15-Jan-2018 | 2 | Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 8: "Source-drain diode"</i> . Modified <i>Figure 2: "Safe operating area"</i> .. Modified <i>Section 4: "Package information"</i> .. Minor text changes. |
| 27-Oct-2023 | 3 | Updated title and Features on cover page. Updated Table 1. Absolute maximum ratings . Updated Figure 6. Static drain-source on-resistance . Updated Section 4.1 D²PAK (TO-263) type A2 package information . Minor text changes. |

Contents

| | | |
|------------|---|-----------|
| 1 | Electrical ratings | 2 |
| 2 | Electrical characteristics | 3 |
| 2.1 | Electrical characteristics curves | 5 |
| 3 | Test circuits | 7 |
| 4 | Package information | 8 |
| 4.1 | D ² PAK (TO-263) type A2 package information | 8 |
| 4.2 | D ² PAK packing information | 11 |
| | Revision history | 13 |
| | Disclaimer | 15 |

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