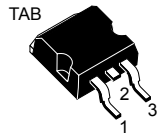
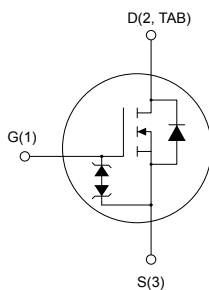


N-channel 600 V, 68 mΩ typ., 36 A, MDmesh M6 Power MOSFET in a D²PAK package


D²PAK


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Product status link
[STB46N60M6](#)
Product summary

Order code	STB46N60M6
Marking	46N60M6
Package	D ² PAK
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB46N60M6	600 V	80 mΩ	36 A

- Reduced switching losses
- Lower R_{DS(on)} per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Application

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R_{DS(on)} per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	36	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	23	
$I_{DM}^{(1)}$	Drain current (pulsed)	126	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		

- Pulse width limited by safe operating area.
- $I_{SD} \leq 36\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
- $V_{DD} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	$^\circ\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^\circ\text{C}/\text{W}$

- When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	5.2	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	760	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$		68	80	$\text{m}\Omega$

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2340	-	pF
C_{oss}	Output capacitance		-	147	-	
C_{rss}	Reverse transfer capacitance		-	3.7	-	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	339	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 36\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	53.5	-	nC
Q_{gs}	Gate-source charge		-	15.5	-	
Q_{gd}	Gate-drain charge		-	23.5	-	

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 18\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	20	-	ns
t_r	Rise time		-	15.5	-	
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	48.4	-	
t_f	Fall time		-	8.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		36	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		126	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 36\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 36\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	267		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	20.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 36\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	440		ns
Q_{rr}	Reverse recovery charge		-	5.8		μC
I_{RRM}	Reverse recovery current		-	26.4		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

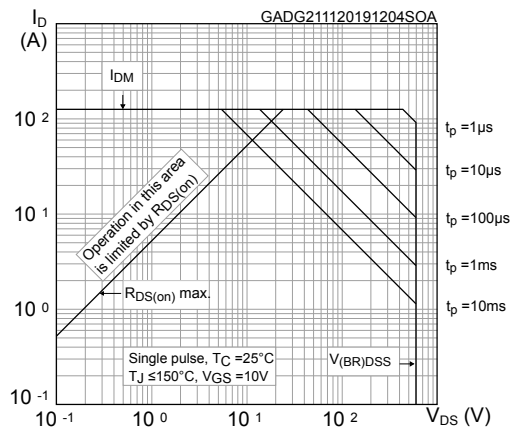
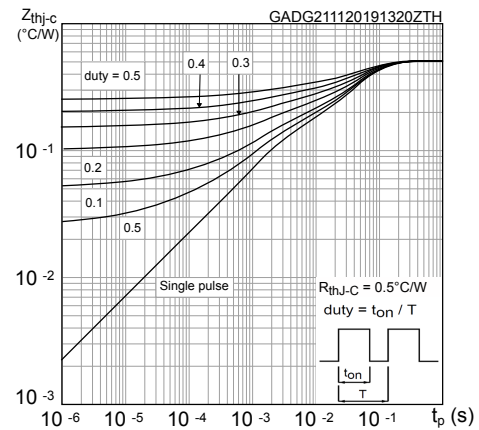
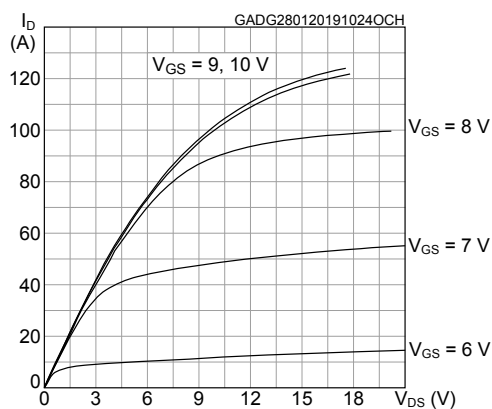
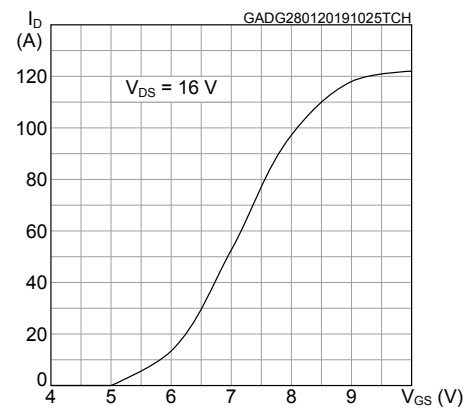
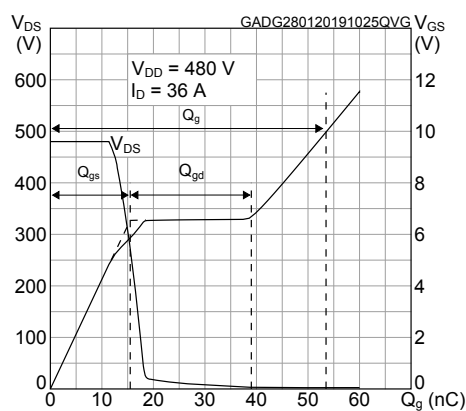
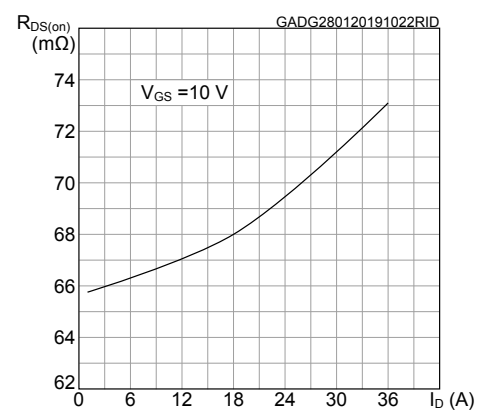
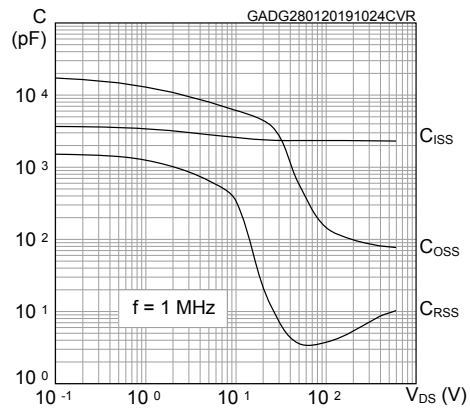
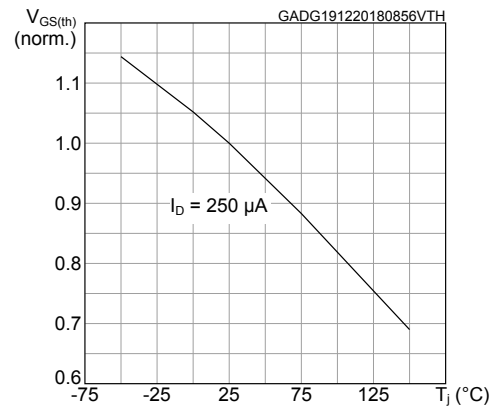
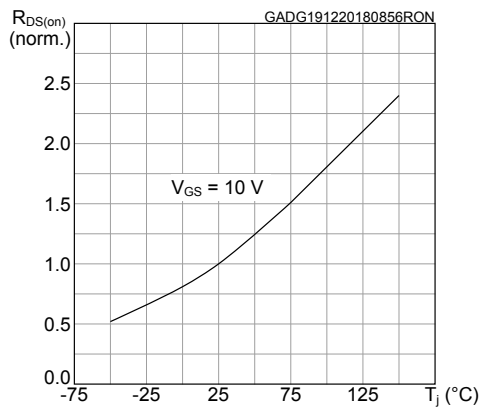
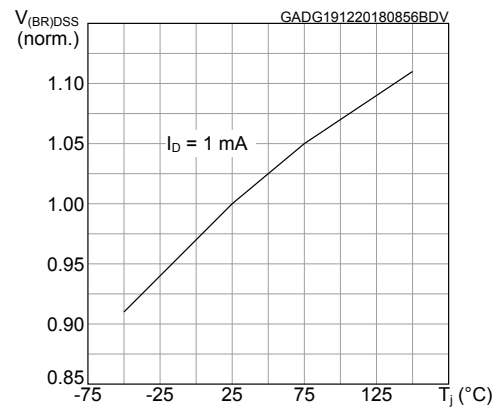
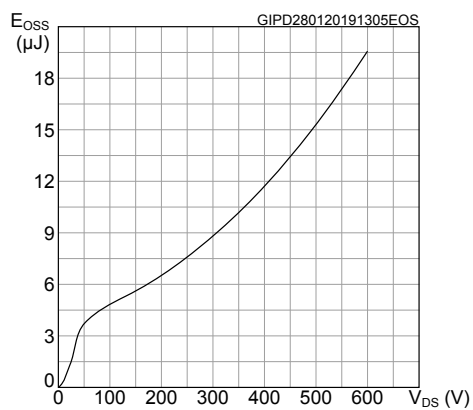
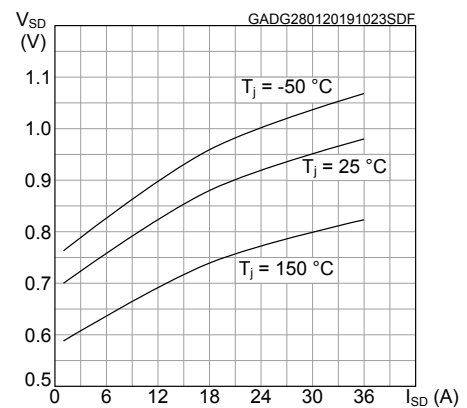
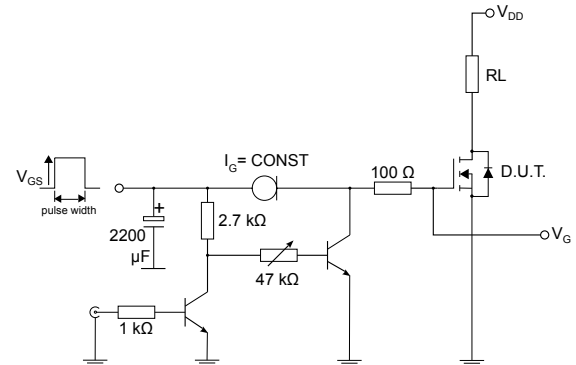
Figure 1. Safe operating area

Figure 2. Maximum transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

Figure 8. Normalized gate threshold vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical output capacitance stored energy

Figure 12. Typical reverse diode forward characteristics


3 Test circuits

Figure 13. Test circuit for resistive load switching times

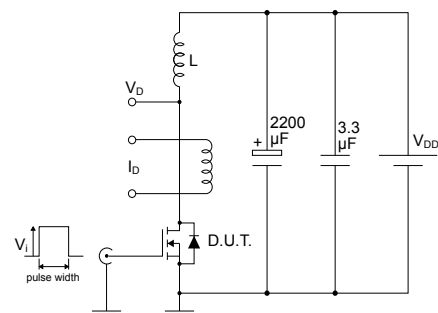

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Figure 14. Test circuit for gate charge behavior


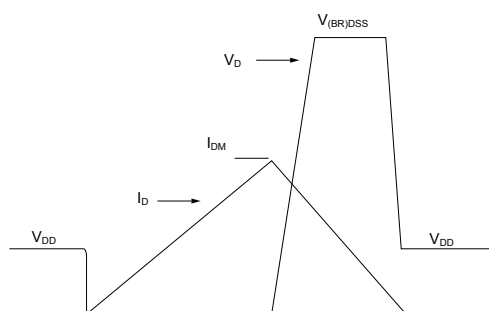
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Figure 15. Test circuit for inductive load switching and diode recovery times


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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform

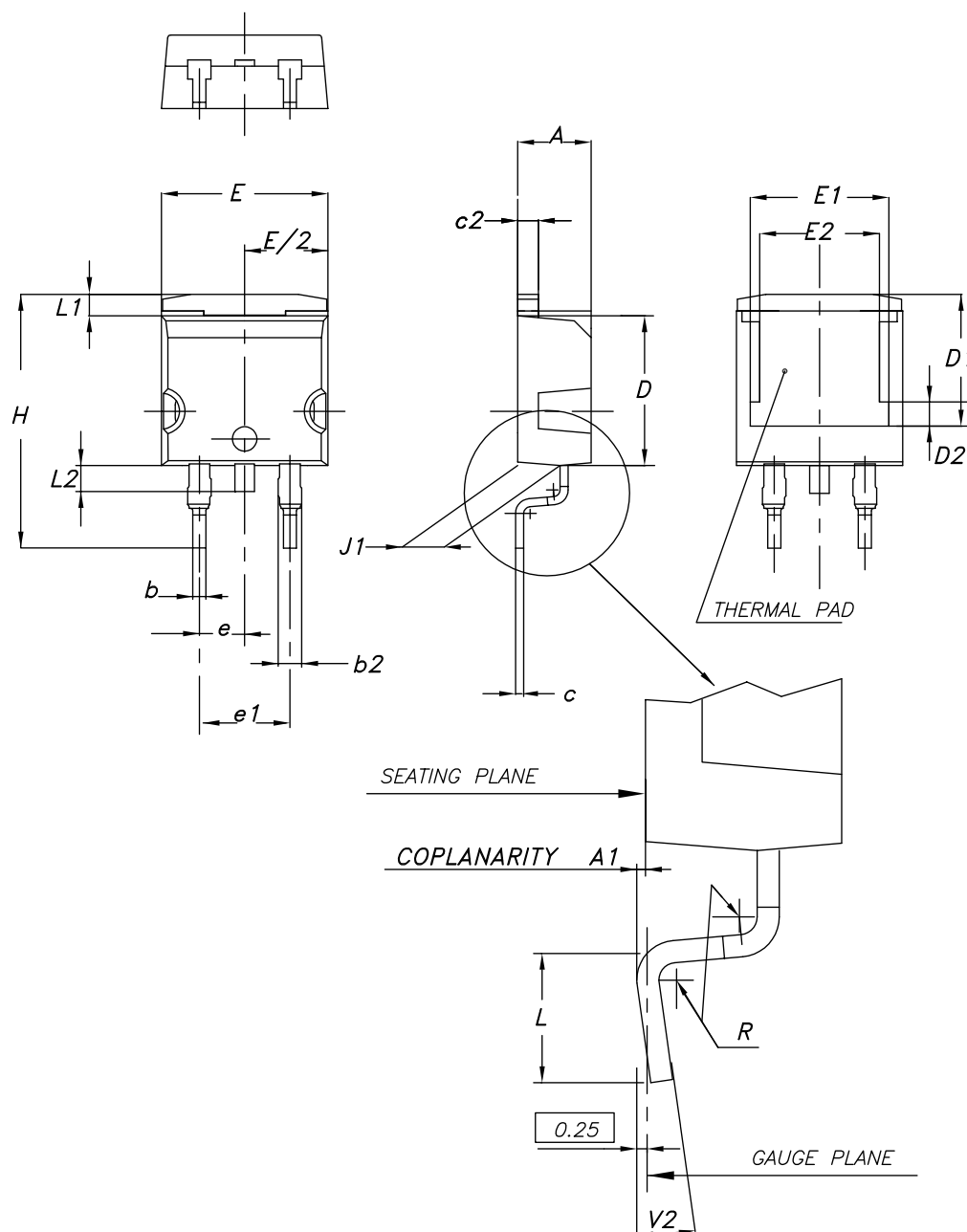

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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 19. D²PAK (TO-263) type A2 package outline

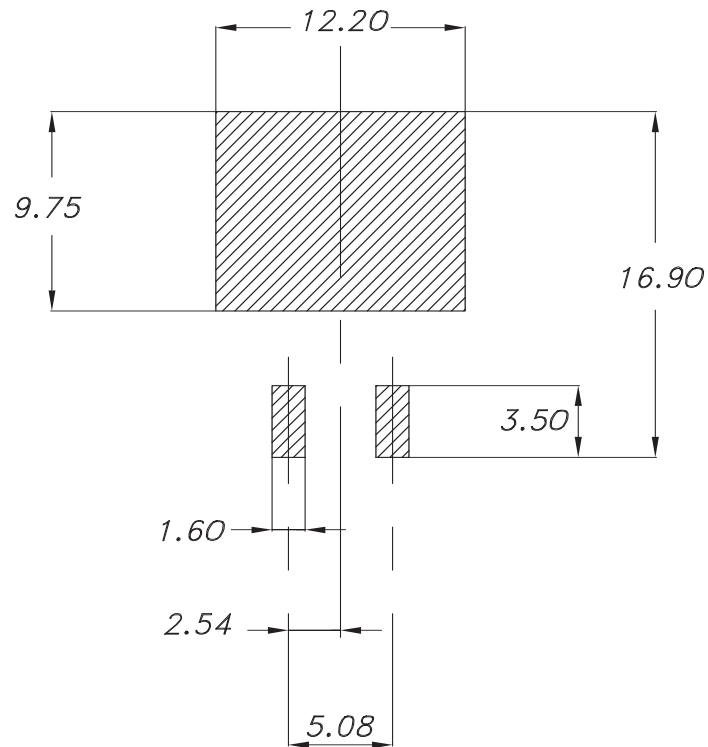


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Table 8. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

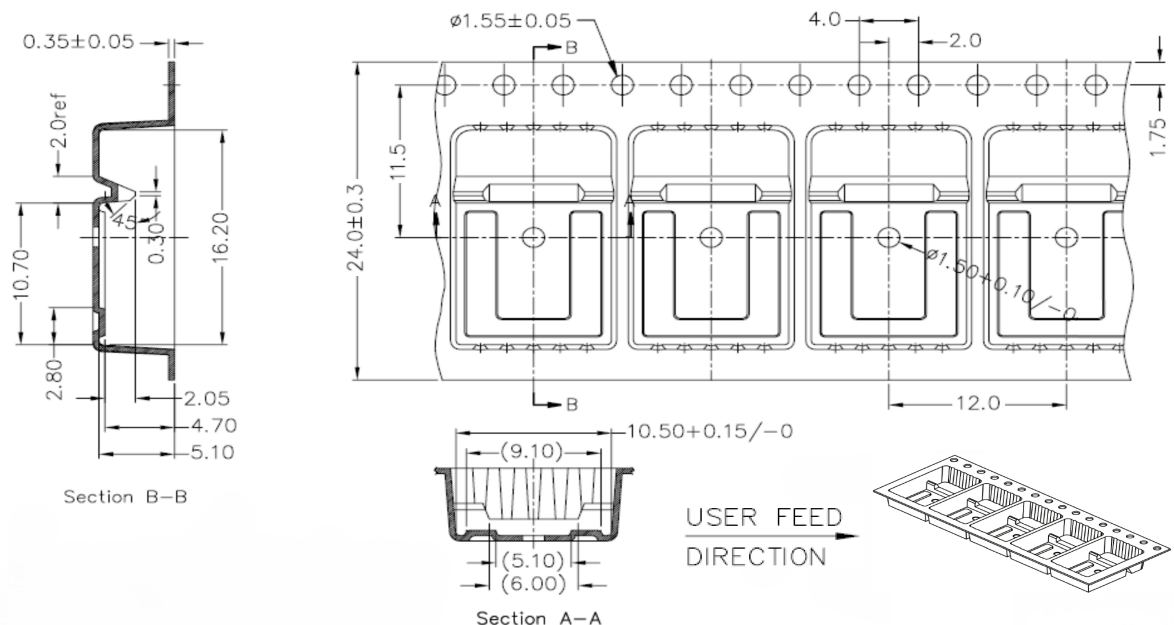
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



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4.2 D²PAK packing information

Figure 21. D²PAK tape drawing (dimensions are in mm)



DM01095771_2

Revision history

Table 9. Document revision history

Date	Version	Changes
20-Mar-2019	1	First release.
25-Nov-2019	2	Updated <i>Table 3. Avalanche characteristics</i> , <i>Section 2 Electrical characteristics</i> and <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes.
18-Sep-2025	3	Updated Section 4: Package information . Minor text changes.

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