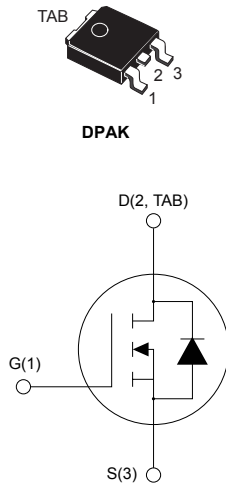


N-channel 600 V, 570 mΩ typ., 8 A FDmesh II Power MOSFET in a DPAK package



AM01475v1_noZen



Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STD10NM60ND	650 V	600 mΩ	8 A

- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

This FDmesh II Power MOSFET with fast-recovery body diode is produced using MDmesh II technology. Utilizing a new strip-layout vertical structure, this device features low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STD10NM60ND](#)

Product summary

Order code	STD10NM60ND
Marking	10NM60ND
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	8	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	5	
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	70	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Maximum operating junction temperature	150	°C

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.79	°C/W
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	130	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$		570	600	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	577	-	pF
C_{oss}	Output capacitance		-	32.4	-	pF
C_{rss}	Reverse transfer capacitance		-	1.76	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	138	-	pF
R_G	Gate input resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	20	-	nC
Q_{gs}	Gate-source charge		-	4.3	-	nC
Q_{gd}	Gate-drain charge		-	11.6	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	9.2	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	32	-	ns
t_f	Fall time		-	9.8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	118		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	680		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	11		A
t_{rr}	Reverse recovery time	$I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	150		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	918		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

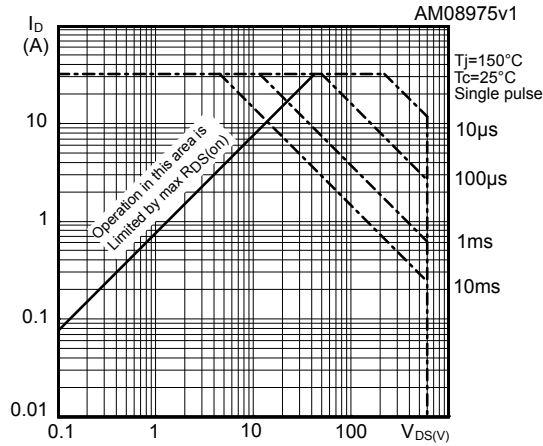


Figure 2. Normalized transient thermal impedance

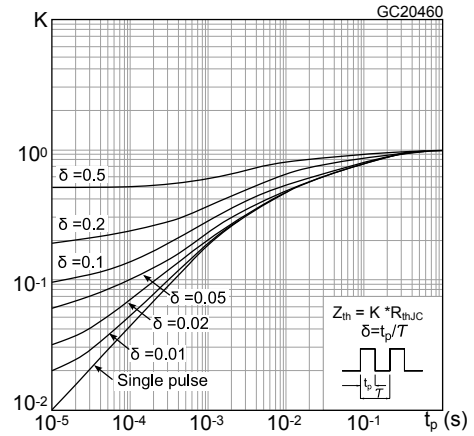


Figure 3. Typical output characteristics

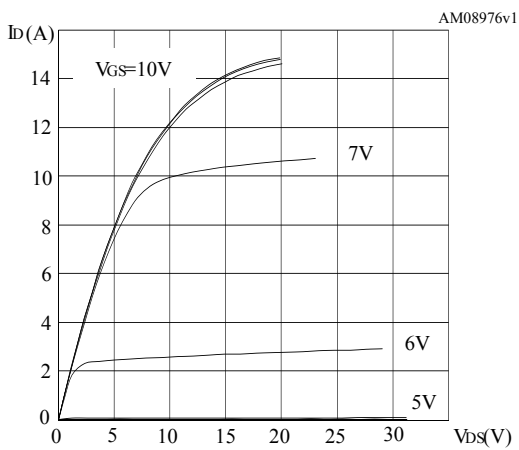


Figure 4. Typical transfer characteristics

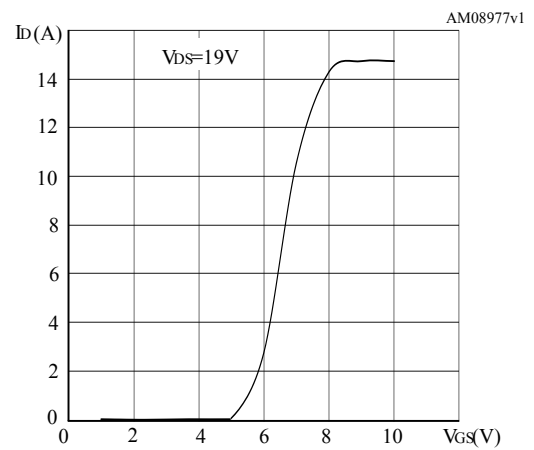


Figure 5. Normalized gate threshold vs temperature

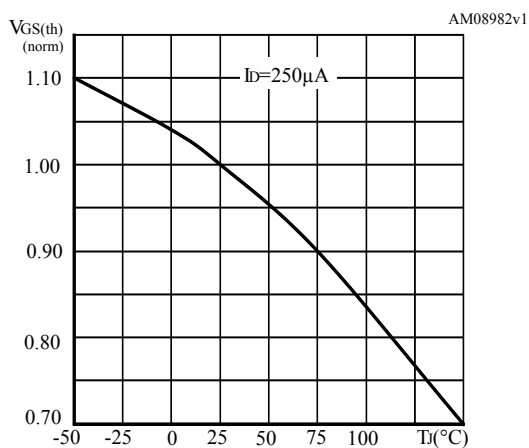


Figure 6. Normalized breakdown voltage vs temperature

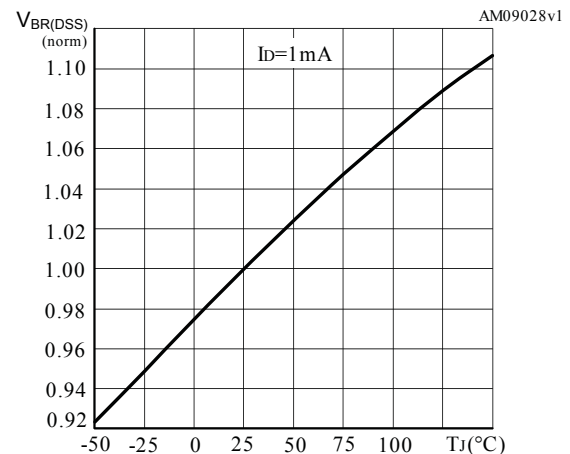


Figure 7. Typical drain-source on-resistance

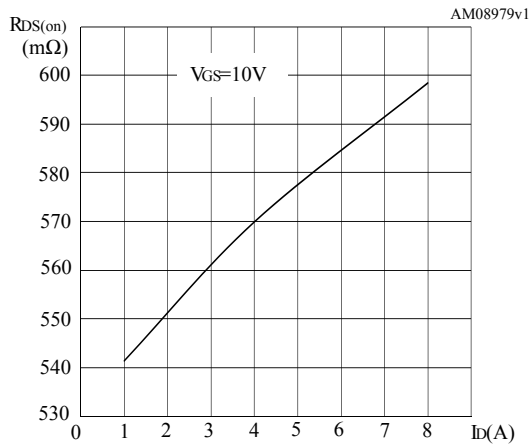


Figure 8. Normalized on-resistance vs temperature

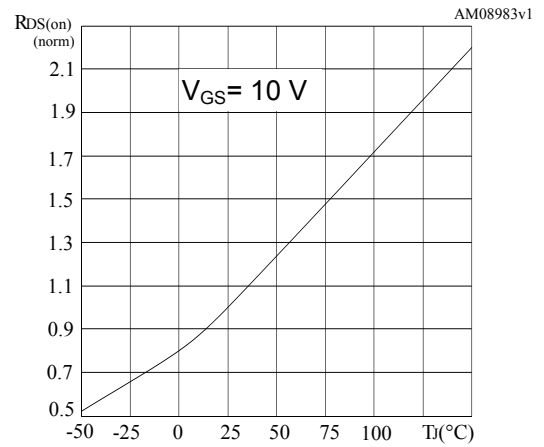


Figure 9. Typical gate charge characteristics

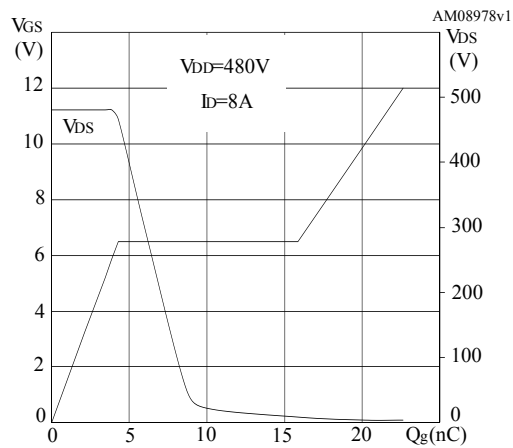


Figure 10. Typical capacitance characteristics

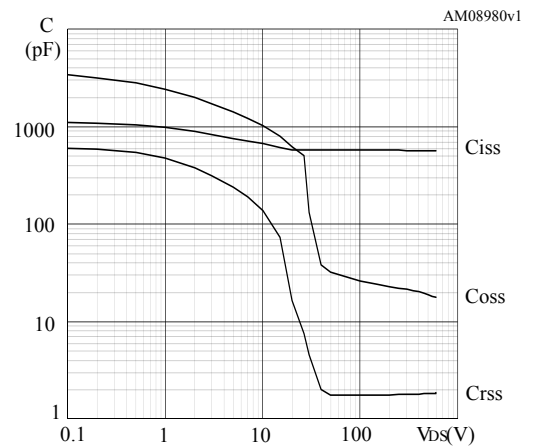


Figure 11. Typical output capacitance stored energy

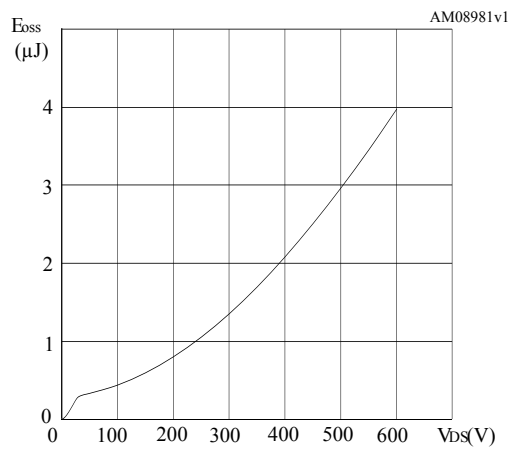
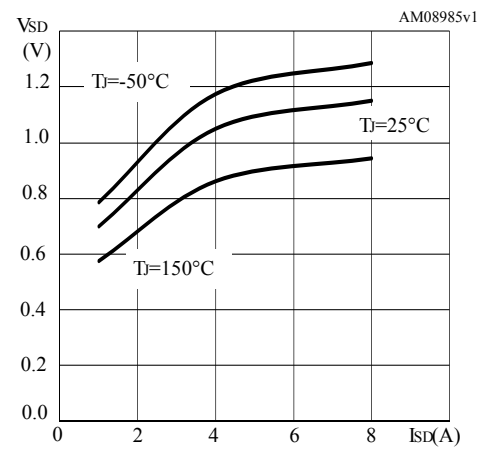
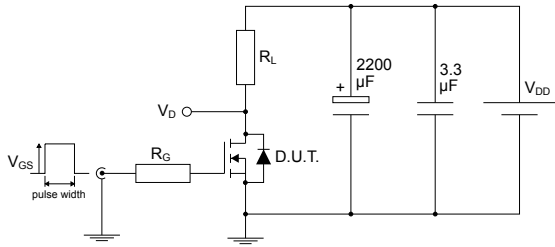


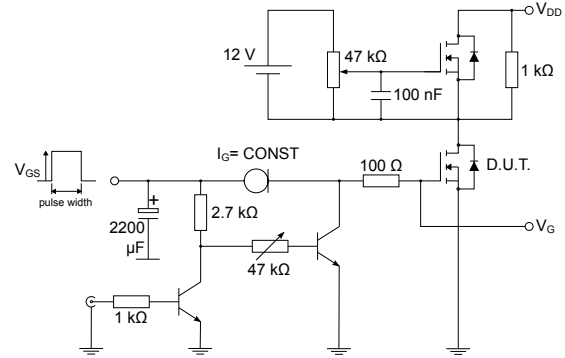
Figure 12. Typical reverse diode forward characteristics



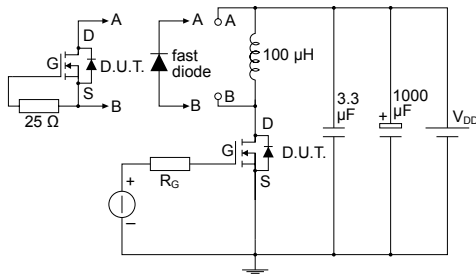
3 Test circuits

Figure 13. Test circuit for resistive load switching times


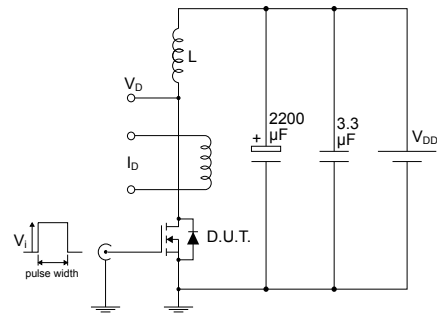
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Figure 14. Test circuit for gate charge behavior


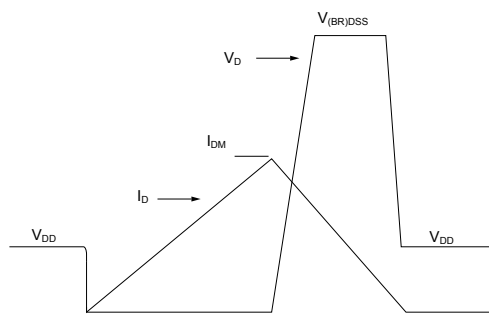
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Figure 15. Test circuit for inductive load switching and diode recovery times


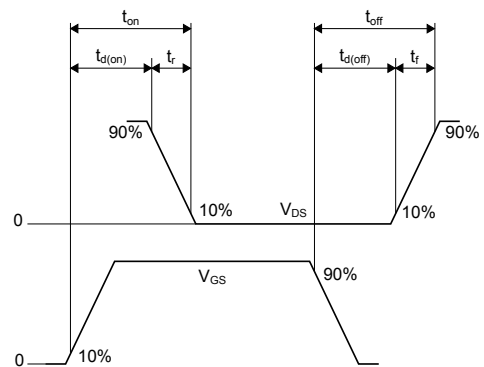
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


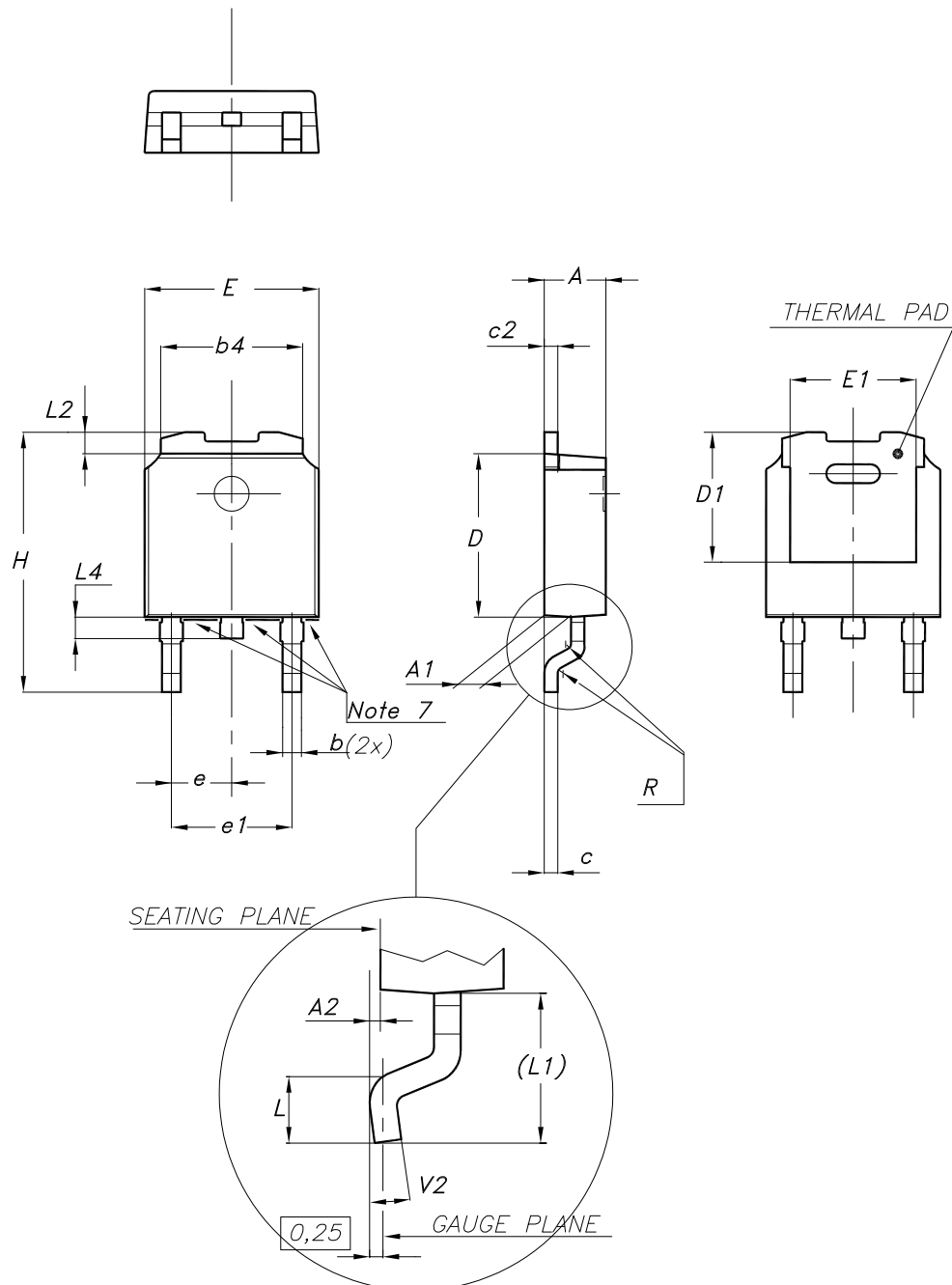
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



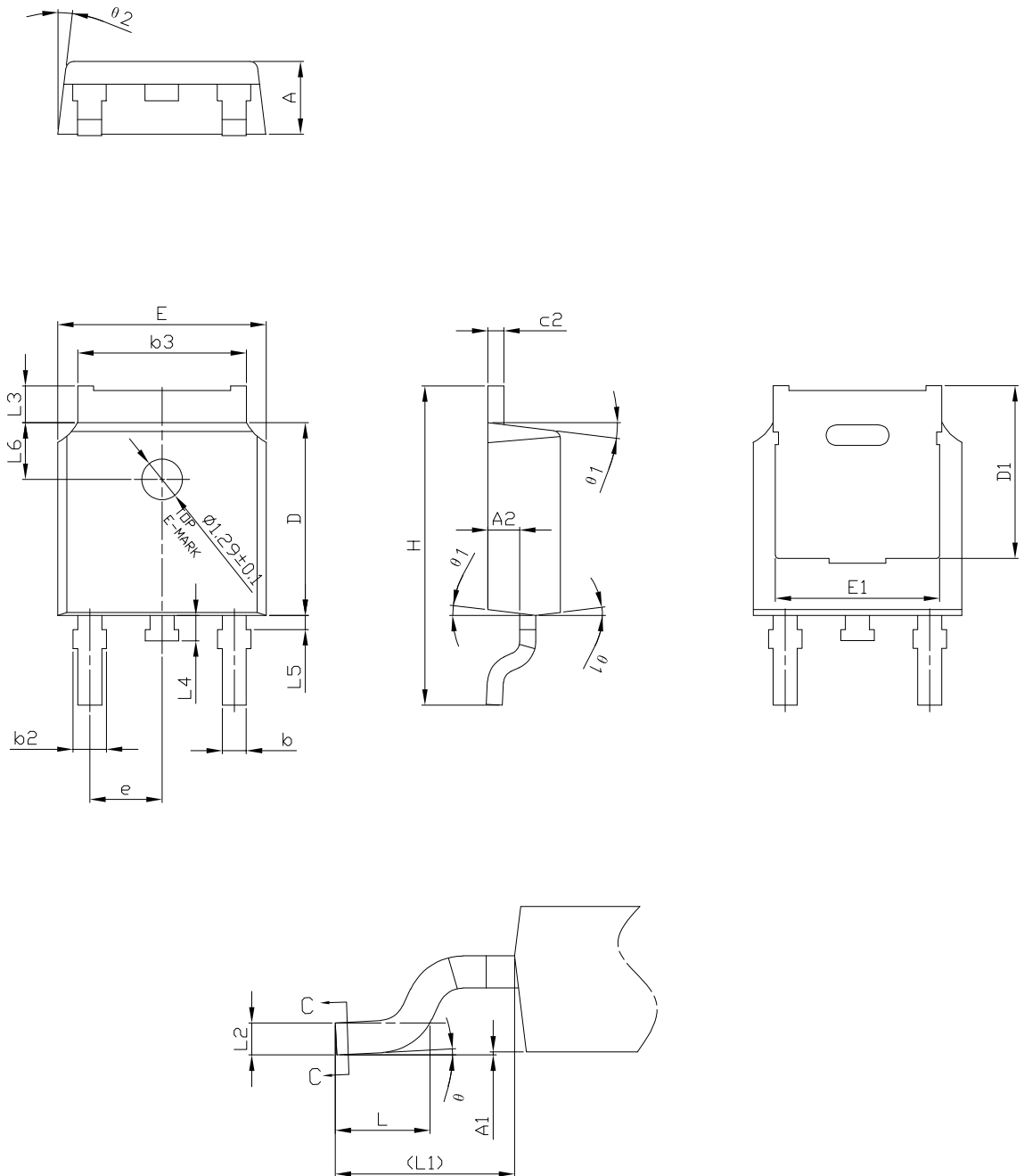
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Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C3 package information

Figure 20. DPAK (TO-252) type C3 package outline



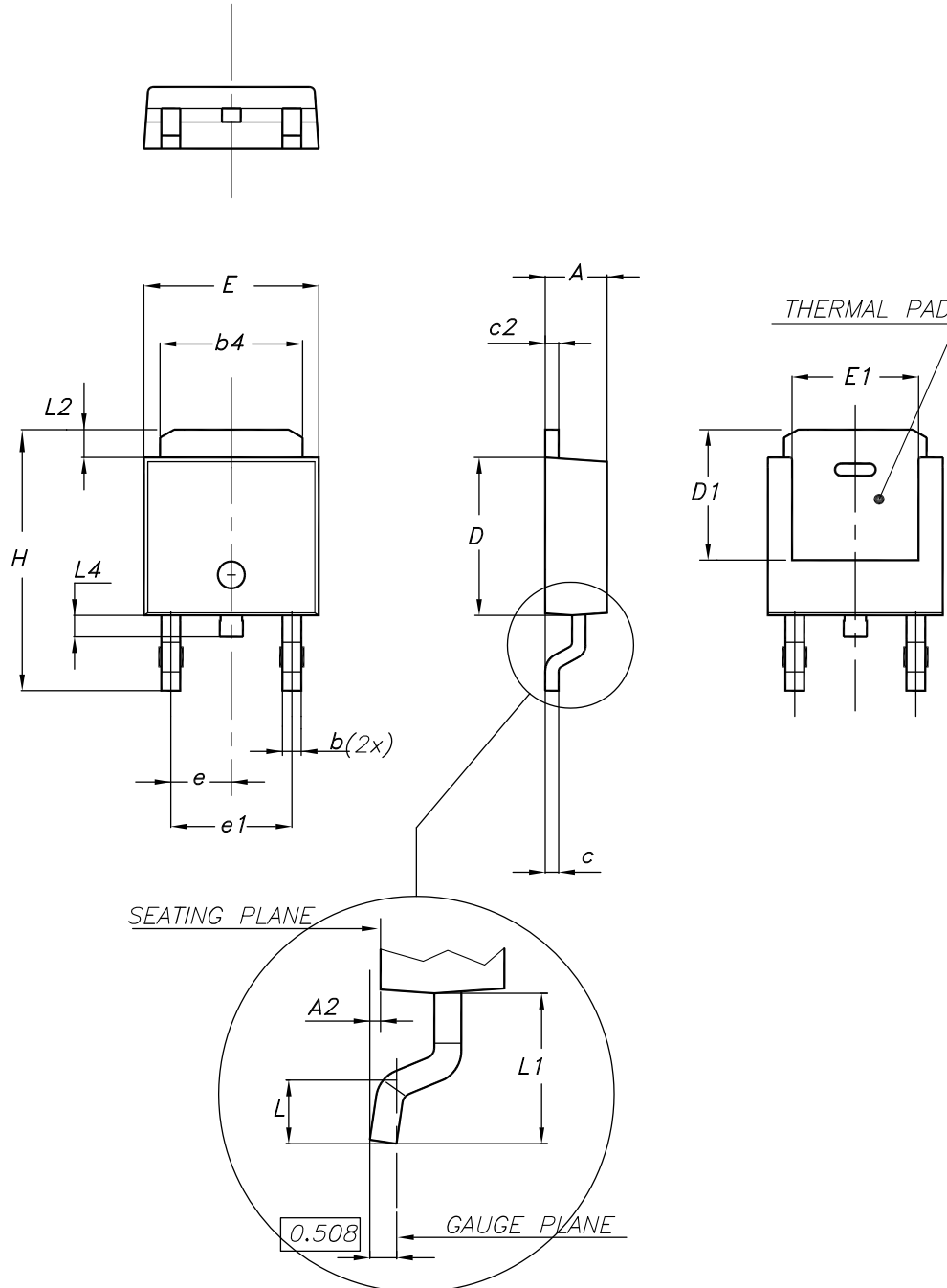
0068772_type-C3_rev34

Table 9. DPAK (TO-252) type C3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

4.3 DPAK (TO-252) type E package information

Figure 21. DPAK (TO-252) type E package outline

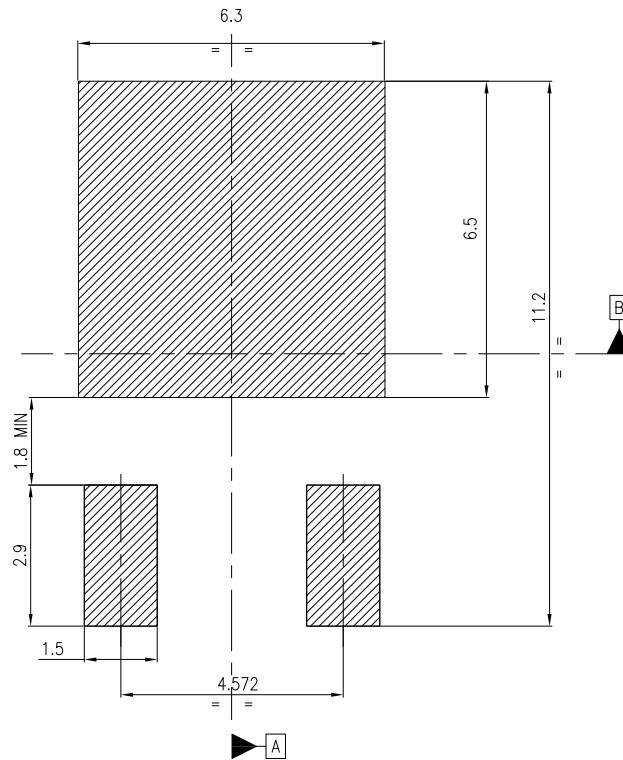


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Table 10. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)



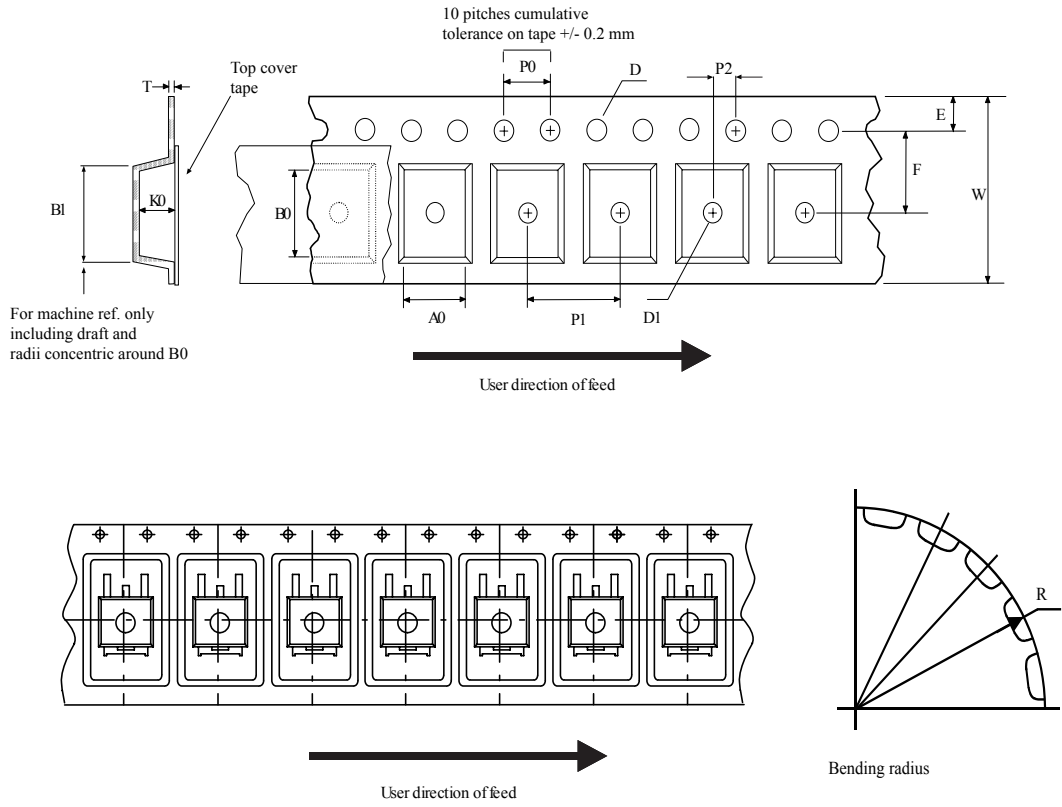
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\oplus 0.05$ A B

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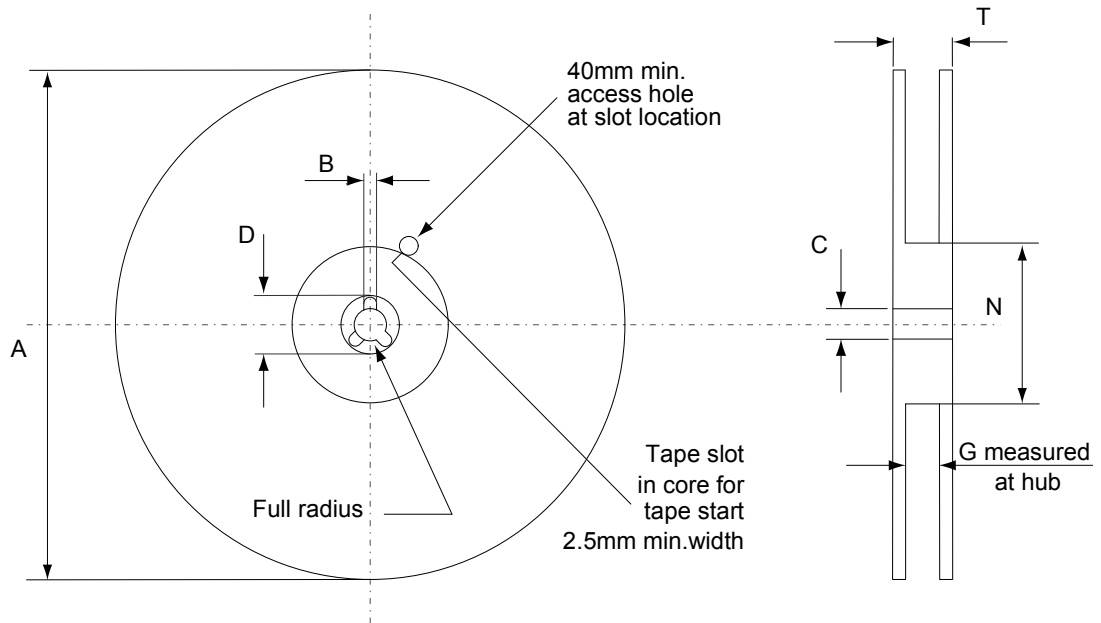
4.4 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline



AM08852v1

Figure 24. DPAK (TO-252) reel outline



AM06038v1

Table 11. DPAK (TO-252) tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 12. Document revision history

Date	Revision	Changes
10-Feb-2011	1	First release.
17-Nov-2011	2	Updated features in table and description in cover page. Updated <i>Table 2: Absolute maximum ratings</i> , <i>Table 5: On /off states</i> , <i>Table 15: Normalized on resistance vs temperature</i> , <i>Figure 17: Normalized V_{DS} vs temperature</i> and <i>Section 4: Package mechanical data</i> .
03-Nov-2017	3	Modified <i>Table 3: "Thermal data"</i> . Modified <i>Section 4: "Package information"</i> . Minor text changes.
16-Jun-2023	4	The part numbers STF10NM60ND, STP10NM60ND have been moved to separate datasheets and the documents have been updated accordingly. Updated the entire Section 4 Package information . Minor text changes.

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