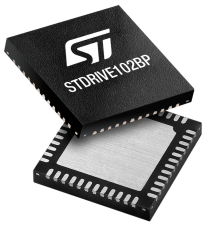
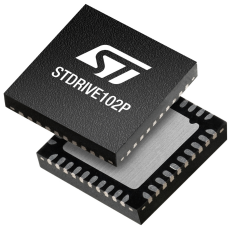
STDRIVE102BP, STDRIVE102P

Datasheet

Triple half-bridge gate driver with programmable currents and SPI configuration



VFQFPN 48L, 6x6x1 mm



VFQFPN 40L, 5x5x1 mm

STDRIVE

Product status link
STDRIVE102BP
STDRIVE102P

Product label
SUSTAINABLE TECHNOLOGY

Features

- Operating voltage from 6 to 50 V
- Gate drivers with programmable current capability up to:
  - 1 A source current
  - 2 A sink current
- High robustness against below-ground and overshoot
- Charge pump for 100 % duty cycle operation with dedicated undervoltage lockout protection
- Flexible power management:
  - 12 V LDO linear regulator with dedicated undervoltage lockout protection
  - 3.3 V LDO linear regulator with dedicated undervoltage lockout protection
- Standby mode for low consumption (less than 50 nA)
- Thermal shutdown protection
- V_{DS} monitoring for safe driving operation of the power MOSFETs
- Flexible analog front-end:
  - Up to three programmable-gain amplifiers
  - Up to three high-speed comparators
- Dual control modes:
  - ENx/INx
  - INHx/INLX with interlocking
- Matched propagation delay for all channels
- Logic inputs up to 5 V, TTL compatible
- Configurability and diagnostics through SPI

Applications

- Battery-supplied power tools
- Portable vacuum cleaners
- E-bikes
- Industrial automation
- Robotics
- Pumps and fans

Description

The STDRIVE102BP and the STDRIVE102P are triple half-bridge gate drivers suitable for 3-phase brushless motor driving.

The STDRIVE102BP/P is the optimal solution for battery-supplied motor driver applications such as power tools, vacuum cleaners and small appliances thanks to its very efficient standby mode, which strongly reduces the current consumption when the device is not active.

The gate drivers are designed to drive, with a programmable gate current, six external N-channel power MOSFETs, allowing a superior performance of the power stage and regulating the slew rate of power outputs without the need for external gate resistors. The gate current and the other configurations of the drivers are set through the SPI interface.

An integrated charge pump supplies the three high-side drivers, enabling unlimited on-time of the high-side MOSFETs.

An embedded 12 V LDO linear regulator provides the supply of the three low-side drivers and its output is available on the VCC pin, to also supply external loads.

Another LDO linear regulator provides a 3.3 V on the VDD pin to supply external low-voltage components and the embedded analog front end (AFE), which has a different configuration, depending on the device part number. The STDRIVE102BP integrates three programmable-gain amplifiers (PGAs) and three comparators, while the STDRIVE102P integrates one programmable-gain amplifier and one comparator. In a typical application, the PGAs can be used to amplify the current in each phase of the motor by monitoring the voltage across the shunt resistors on each low-side MOSFET. Concurrently, the comparators can be used to detect dangerous overcurrent conditions.

A full set of embedded protections is present to increase the overall application robustness: undervoltage lockout (UVLO) on each supply (VCC, VDD, and charge pump voltage), thermal shutdown, and the V_{DS} monitoring on both high-side and low-side MOSFETs.

In case a protection is triggered, the nFAULT and FLAG (STDRIVE102PB only) open-drain pins can be configured to signal which specific protection event has been triggered. Both the nFAULT and FLAG pins can be used in combination with the EN pin to implement an automatic rearm after a protection event.

In addition to the main supply pin (VS), the STDRIVE102BP/P has a dedicated pin VM, which should be connected to the motor supply voltage, in correspondence with the drains of the high side N-channel MOSFETs. The VM pin is used for the integrated V_{DS} monitoring as well as a reference voltage for the charge pump. To increase the device's flexibility, the VS and VM pin can operate at different voltages.

Both STDRIVE102BP and STDRIVE102P provide full configuration and diagnostics through a set of internal registers (accessible via the SPI interface).

1 Block diagram

Figure 1. **STDRIVE102BP block diagram**

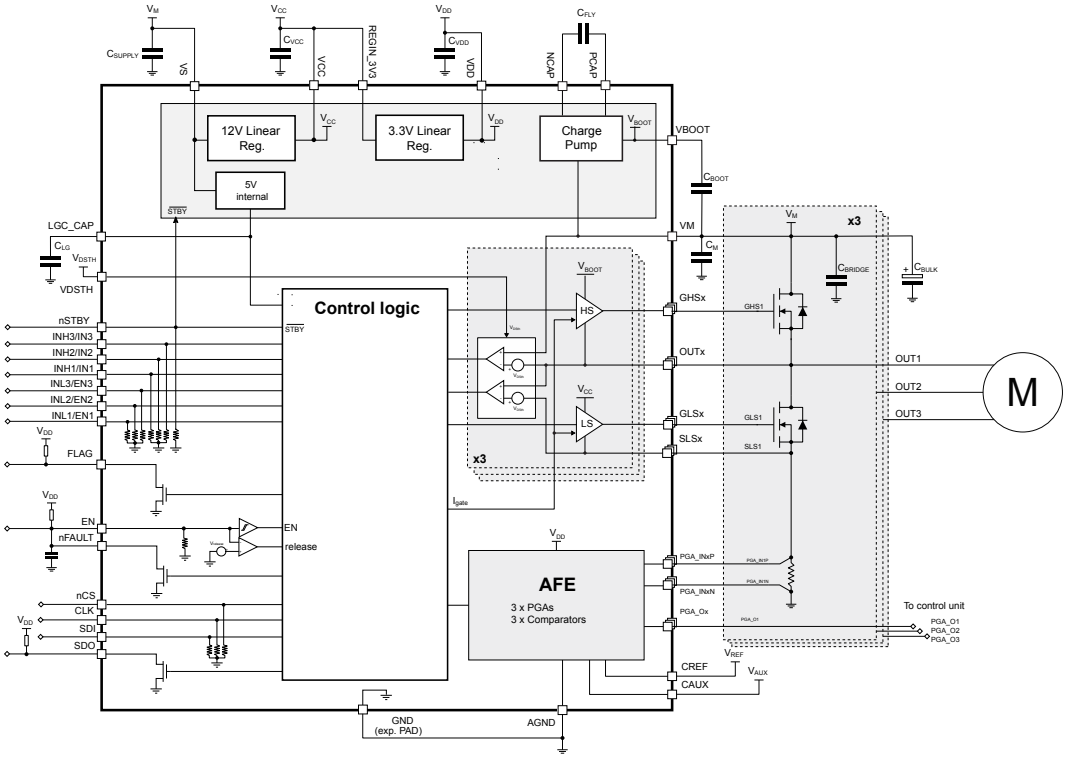
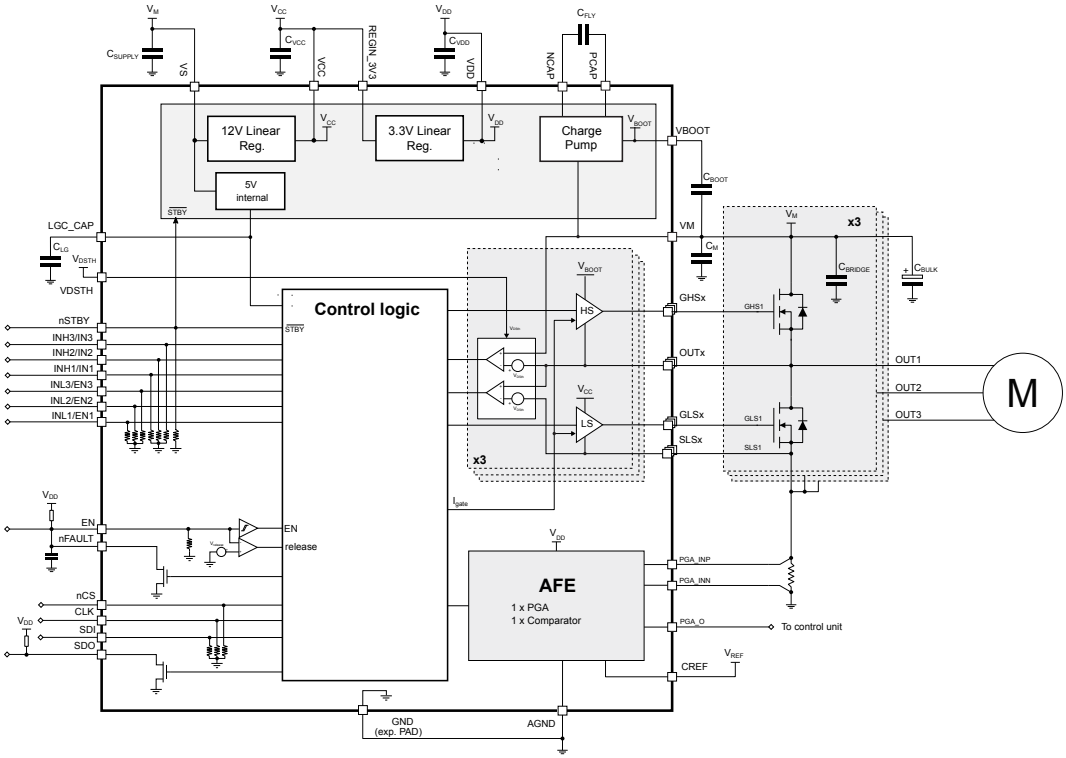


Figure 2. **STDRIVE102P block diagram**



2 Device ratings

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Two separate reference grounds are present in the device: GND and AGND. All voltages reported in Table 1 are considered with AGND and GND pins shorted, unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
Power supply				
V_M	Motor supply voltage		-0.3 to 55	V
V_S	12 V LDO linear regulator input and main supply		-0.3 to 55	V
V_{CC}	12 V LDO linear regulator output and gate drivers supply voltage		-0.3 to 18	V
V_{REGIN_3V3}	3.3 V LDO linear regulator input		-0.3 to 18	V
V_{DD}	3.3 V LDO linear regulator output and analog front end supply		-0.3 to 4	V
V_{NCAP}	Charge pump switching capacitor negative side		-0.3 to V_S+0.3	V
V_{PCAP}	Charge pump switching capacitor positive side		V_M-0.3 to V_{BOOT}+0.3	V
			65	V
V_{BOOT}	Charge pump output/ high-side boot supply		V_M-0.3 to V_M+18	V
			65	V
Gate drivers				
V_{SLSx}	Low-side reference pin voltage	DC	-2 to +2	V
		Transient pulse duration 200 ns Repetition frequency 20 kHz (1)	-8 to +8	V
V_{GLSx}	Low-side driver output voltage		V_{SLSx}-0.3 to V_{CC}+0.3	V
V_{GS_LSx}	Differential voltage between low-side driver output and its reference (V_{GLSx} - V_{SLSx})		-0.3 to 18	V
V_{supply_LS}	Supply rail of the low-side driver (V_{CC} - V_{SLSx})		-0.3 to 18	V
V_{OUTx}	OUTx pin voltage	DC	-4 to V_M+4	V
		Transient pulse duration between 200 ns and 5 µs Repetition frequency 20 kHz	-8 to V_M+8	V
		Transient pulse duration 200 ns Repetition frequency 20 kHz	-10 to V_M+10	V
V_{GHSx}	High-side driver output		V_{OUTx} -0.3 to V_{BOOT}+0.3	V
V_{GO_HSx}	Differential voltage between high-side gate driver's output and its reference (V_{GHSx} - V_{OUTx})	(2)	-0.3 to 16	V

Symbol	Parameter	Test condition	Value	Unit
$V_{BO,x}$	Supply rail of the high-side driver (V_{BOOT} - V_{OUTx})		-0.3 to 65	V
Analog pins and digital I/O				
V_{IO}	Logic I/O voltage (INHx/INx, INLx/ENx, nSTBY, EN, SDI, nCS, CLK pins)		-0.3 to 5.5	V
V_{DSTH}	VDSTH analog input pin voltage		-0.3 to 5.5	V
V_{OD}	Open-drain pins voltage (nFAULT, FLAG, SDO)		-0.3 to 5.5	V
V_{C_AUX}	C_AUX input		-0.3 to V_{DD}+0.3	V
V_{CREF}	CREF input		-0.3 to V_{DD}+0.3	V
V_{PGA_INxP}	PGAs positive inputs	DC	-2 to V_{DD} + 0.3	V
		Transient pulse duration 200 ns Repetition frequency 20 kHz	-8 to 8	V
V_{PGA_INxN}	PGAs negative inputs	DC	-0.4 to V_{DD} + 0.3	V
		Transient pulse duration 200 ns Repetition frequency 20 kHz	-2 to V_{DD} + 0.3	
V_{PGA_Ox}	PGAs outputs		-0.3 to V_{DD}+0.3	V
Temperature				
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Junction temperature		-40 to 150	°C
Reference grounds				
ΔV_{GND}	GND misalignment	AGND with respect to GND (exposed pad)	-0.3 to 0.3	V

1. *V_{supply_LS} AMR must be also considered.*
2. *Limit to avoid V_{GS} clamp turn-on.*

2.2 Recommended operating conditions

All voltages must be considered with AGND and GND pins shorted.

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_M	Motor supply voltage		6		50	V
V_S	12 V LDO linear regulator input	(1)	V_{CC}		50	V
V_{CC}	VCC gate driver supply voltage	VCC supplied by internal linear regulator		12		V
		VS shorted to VCC and externally supplied	6		15	V
I_{CC}	12 V linear regulator output current	(1) (2)			50	mA
C_{VCC}	12 V LDO linear regulator output capacitor	(3)		4.7		µF
V_{BOOT}	Charge pump output voltage			V_M + V_{CC}		V
I_{BOOT}	Charge pump current	(2)			35	mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{REGIN_3V3}	3.3 V LDO linear regulator input		V_{DD}		15	V
V_{DD}	3.3 V LDO linear regulator output	VDD supplied by internal linear regulator		3.3		V
		REGIN_3V3 shorted to VDD and externally supplied	3.1	3.3	3.6	V
I_{DD}	3.3 V LDO linear regulator output current	(1) (2)			30	mA
C_{VDD}	3.3 V output capacitor	(3)		4.7		µF
C_{LG}	Output capacitor for internal logic supply regulator (LGC_CAP pin)	(3)		4.7		µF
dV_{OUTx}/dt	OUTx slew rate				2.5	V/ns
$V_{IN,logic}$	Logic input voltage (INHx/INx, INLx/ENx, nSTBY, EN, SDI, nCS, CLK pins)	(4)	0		5	V
V_{OD}	nFAULT, FLAG, SDO pins pull-up voltage	(4)	0		5	V
I_{OD}	nFAULT, FLAG, SDO pins sink current				8	mA
V_{DSTH}	V_{DS} monitoring reference voltage	Protection enabled	0.05		2	V
		Protection disabled	3		3.3	V
V_{SLSx}	LSx driver sense pin		-1		+1	V
V_{PGA_INxP}	PGAs positive inputs	PGAx_GAIN[1:0] = 00 (G_{PGA} = 4)	-0.66		V_{DD}	V
		PGAx_GAIN[1:0] = 01 (G_{PGA} = 8)	-0.43		V_{DD}	V
		PGAx_GAIN[1:0] = 10 (G_{PGA} = 16)	-0.31		V_{DD}	V
		PGAx_GAIN[1:0] = 11 (G_{PGA} = 32)	-0.245		V_{DD}	V
V_{PGA_INxN}	PGAs negative inputs	PGAx_GAIN[1:0] = 00 (G_{PGA} = 4)	-0.3		V_{DD}	V
		PGAx_GAIN[1:0] = 01 (G_{PGA} = 8)	-0.25		V_{DD}	V
		PGAx_GAIN[1:0] = 10 (G_{PGA} = 16)	-0.22		V_{DD}	V
		PGAx_GAIN[1:0] = 11 (G_{PGA} = 32)	-0.2		V_{DD}	V
$R_{eqL,out}$	Equivalent load resistor connected to the PGA output (PGA_Ox)	Resistor to AGND or to VDD	1			kΩ
V_{C_AUX}	Comparator 3 auxiliary input (C_AUX pin)		0		V_{DD}	V
V_{CREF}	CREF input		0		V_{DD}	V
T_{amb}	Operative ambient temperature	(1)	-40		85	°C

1. *Actual operative range can be limited by thermal shutdown.*
2. *Consumption of internal circuitry included.*
3. *An additional 100 nF low-ESR bypass capacitor could be added to improve the noise immunity.*
4. *All digital inputs are compliant with TTL/CMOS thresholds and 5 V tolerant. They can be biased within the respective AMR whatever the supply condition of the device (supplied, floating, or shorted to ground) without damaging the device.*

2.3 Thermal data

Thermal values are calculated by simulation.

Table 3. STDRIVE102BP thermal data (VFQFPN 48L, 6x6x1 mm)

Symbol	Parameter	Test condition	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	Natural convection according to JESD51-2a	32.1	°C/W
$R_{thJCtop}$	Junction-to-case thermal resistance (top side)	Cold plate on top, according to JESD51-12	15.8	°C/W
$R_{thJCbot}$	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12	3.4	°C/W
R_{thJB}	Junction-to-board thermal resistance	According to JESD51-8	15.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	According to JESD51-2a	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	According to JESD51-2a	15	°C/W

Table 4. STDRIVE102P thermal data (VFQFPN 40L, 5x5x1 mm)

Symbol	Parameter	Test condition	Value	Unit
R_{thJA}	Junction-to-ambient thermal resistance	Natural convection according to JESD51-2a	36.3	°C/W
$R_{thJCtop}$	Junction-to-case thermal resistance (top side)	Cold plate on top, according to JESD51-12	19.5	°C/W
$R_{thJCbot}$	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12	4.0	°C/W
R_{thJB}	Junction-to-board thermal resistance	According to JESD51-8	18.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	According to JESD51-2a	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	According to JESD51-2a	17.7	°C/W

2.4 Electrical sensitivity characteristics

Table 5. ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2017	2	2000	V
CDM	Charge Device Model	Conforming to ANSI/ESDA/JEDEC JS-002-2018	C3	1000	V

3 Electrical characteristics

Testing conditions: V_M = 24 V, V_S = 12 V, V_{CC} = 12 V, V_{REGIN_3V3} = 3.3 V, V_{DD} = 3.3 V, V_{DSTH} = 3.3 V. All gate drivers LOW (sinking current) unless otherwise specified.

Typical values are tested at T_j = 25°C. Minimum and maximum values are guaranteed by thermal characterization over the temperature range of -40 to 125°C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply and UVLO protection						
$V_{CC(On)}$	V_{CC} UVLO turn-on threshold	V_{CC} rising, UV_SEL = 1		7.8	8.1	V
		V_{CC} rising, UV_SEL = 0		5.5	5.8	V
$V_{CC(Hyst)}$	V_{CC} UVLO hysteresis	V_{CC} falling, UV_SEL = 1		0.25		V
		V_{CC} falling, UV_SEL = 0		0.25		V
$V_{CC(Off)}$	V_{CC} UVLO turn-off threshold	V_{CC} falling, UV_SEL = 1	7.2	7.55		V
		V_{CC} falling, UV_SEL = 0	5.0	5.25		V
$V_{P\_GOOD(On)}$	V_{CC} power-good warning release threshold	V_{CC} rising, VCC_GOOD_SEL = 1		9.65		V
		V_{CC} rising, VCC_GOOD_SEL = 0		7.75		V
$V_{P\_GOOD(Hyst)}$	V_{CC} power-good warning hysteresis	V_{CC} falling, VCC_GOOD_SEL = 1		0.35		V
		V_{CC} falling, VCC_GOOD_SEL = 0		0.25		V
$V_{P\_GOOD(Off)}$	V_{CC} power-good warning threshold	V_{CC} falling, VCC_GOOD_SEL = 1		9.3		V
		V_{CC} falling, VCC_GOOD_SEL = 0		7.5		V
$V_{CPump(On)}$	V_{BOOT} - V_M UVLO turn-on threshold	'V_{BOOT} - V_M' rising, UV_SEL = 1		7.3	8.5	V
		'V_{BOOT} - V_M' rising, UV_SEL = 0		4.5	5.2	V
$V_{CPump(Hyst)}$	V_{BOOT} - V_M UVLO hysteresis	'V_{BOOT} - V_M' falling, UV_SEL = 1		0.3		V
		'V_{BOOT} - V_M' falling, UV_SEL = 0		0.2		V
$V_{CPump(Off)}$	V_{BOOT} - V_M UVLO turn-off threshold	'V_{BOOT} - V_M' falling, UV_SEL = 1	5.9	7		V
		'V_{BOOT} - V_M' falling, UV_SEL = 0	3.6	4.3		V
$V_{DD(On)}$	V_{DD} UVLO turn-on threshold	V_{DD} rising		2.6	2.9	V
$V_{DD(Hyst)}$	V_{DD} UVLO hysteresis	V_{DD} falling		0.2		V
$V_{DD(Off)}$	V_{DD} UVLO turn-off threshold	V_{DD} falling	2.2	2.4		V
I_{STBY}	Standby current consumption	V_S = 50 V , T_j = 25 °C			50	nA
12 V LDO linear regulator						
V_{CC}	12 V linear regulator output	V_S = 15 V, I_{CC} = 40 mA	11.45	12	12.55	V
$I_{CC,lim}$	12 V linear regulator current limiter	V_{CC} shorted to AGND	55	85	115	mA
3.3 V LDO linear regulator						
V_{DD}	3.3 V linear regulator output	V_{REGIN_3V3} = 12 V I_{DD} = 25 mA	3.13	3.3	3.47	V
$I_{DD,lim}$	3.3 V linear regulator current limiter	V_{DD} shorted to AGND	36	45	65	mA
Charge pump						
$f_{SW,CP}$	charge pump switching frequency			90		kHz

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Thermal shutdown and thermal warning						
$T_{j(THSD),rec}$	Thermal shutdown recovery temperature			135		°C
$T_{j(THSD)}$	Thermal shutdown temperature			150		°C
$T_{j(WRN),rec}$	Thermal warning recovery temperature			125		°C
$T_{j(WRN)}$	Thermal warning temperature			135		°C
Gate drivers						
$I_{GATE,on}$	Gate driver source current capability	IGATE[3:0] = 1111, see Table 32		1000		mA
$I_{GATE,off}$	Gate driver sink current capability	IGATE[3:0] = 1111, see Table 32 DRV_EQ_SEL = 0		2000		mA
$I_{hold,on}$	Gate driver hold current (source)			25		mA
$I_{hold,off}$	Gate driver hold current (sink)	DRV_EQ_SEL = 0		50		mA
I_{clamp}	Gate driver clamp current	DRV_EQ_SEL = 0		2140		mA
$t_{cc,on}$	Constant source current time	DRV_EQ_SEL = 0 TCC[3:0] = 0000, see Table 31		280		ns
		DRV_EQ_SEL = 0 TCC[3:0] = 1111, see Table 31		5400		ns
$t_{cc,off}$	Constant sink current time	DRV_EQ_SEL = 0 TCC[3:0] = 0000, see Table 31		140		ns
		DRV_EQ_SEL = 0 TCC[3:0] = 1111, see Table 31		2700		ns
$V_{GS,\ clamp}$	Clamping voltage protection on the high-side driver output	$I_{GS,clamp}$ = 25 mA		17.5		V
$I_{OUTx,bias}$	OUTx bias current	$V_{OUTx} = V_M$ = 40 V IGATE[3:0] = 1111		300		µA
$t_{d,on}$	Turn-on propagation delay (input to output) (1)	C_{LOAD} = 1 nF IGATE[3:0] = 1111		50		ns
$t_{d,off}$	Turn-off propagation delay (input to output) (1)	C_{LOAD} = 1 nF IGATE[3:0] = 1111		45		ns
MT_{on-off}	Propagation delay matching between turn-on and off (2)	C_{LOAD} = 1 nF IGATE[3:0] = 1111		5		ns
MT_{HL}	Propagation delay matching between HS and LS (3)	C_{LOAD} = 1 nF IGATE[3:0] = 1111		7		ns
MT_{CH}	Propagation delay matching between channels (4)	C_{LOAD} = 1 nF IGATE[3:0] = 1111		0		ns
V_{DS} monitoring protection						
$V_{DS,th}$	V_{DS} monitor protection threshold	VDSTH = 0.05 V	0.020	0.050	0.083	V
		VDSTH = 2 V	1.8	2	2.2	V
$V_{DSTH,en}$	VDS monitor protection enable voltage				2.4	V
$V_{DSTH,dis}$	VDS monitor protection disable voltage		3			V
$R_{PD,VDSTH}$	VDSTH pin pull-down resistor			450		kΩ

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PGA						
G_{PGA}	Programmable gain amplifiers differential gain	PGAx_GAIN[1:0] = 00, (G_{PGA} = 4)		4		V/V
		PGAx_GAIN[1:0] = 01, (G_{PGA} = 8)		8		V/V
		PGAx_GAIN[1:0] = 10, (G_{PGA} = 16)		16		V/V
		PGAx_GAIN[1:0] = 11, (G_{PGA} = 32)		32		V/V
$V_{PGA,io}$	PGA input offset voltage	PGAx_GAIN[1:0] = 11, (GPGA = 32)	-6	0	6	mV
V_{PGA_OH}	High level output voltage (V_{DD} - V_{PGA_Ox})	Output source current I_{PGA_Ox} = +1 mA		30	100	mV
V_{PGA_OL}	Low level output voltage	Output sink current I_{PGA_Ox} = -1 mA		30	100	mV
BW_{PGA}	PGA bandwidth at -3 dB	G_{PGA} = 4, C_L = 1 nF, R_L = 10 kΩ (5)		3.6		MHz
		G_{PGA} = 8, C_L = 1 nF, R_L = 10 kΩ (5)		2		MHz
		G_{PGA} = 16, C_L = 1 nF, R_L = 10 kΩ (5)		1.1		MHz
		G_{PGA} = 32 C_L = 1 nF, R_L = 10 kΩ		0.6		MHz
SR	Slew rate	G_{PGA} = 4 C_L = 1 nF, R_L = 10 kΩ		12		V/µs
Comparators						
$V_{COMP,io}$	Input offset voltage	CREF = 1.65 V	-16	0	16	mV
$V_{Hyst(COMP)}$	Comparator hysteresis high-to-low transition	T_j = 25°C		20		mV
I_{CREF}	CREF pin input current	T_j = 25°C (5)			1	nA
I_{C_AUX}	C_AUX pin input current	T_j = 25°C (5)			1	nA
$t_{pd(COMP)}$	Comparator propagation delay	CREF = 1.65 V COMP<x> DEG = 00		200		ns
Logic inputs and outputs						
V_{IL}	Low logic input voltage				0.8	V
V_{IH}	High logic input voltage		2			V
$V_{IL,stby}$	nSTBY pin low logic input voltage				0.6	V
$V_{IH,stby}$	nSTBY pin high logic input voltage		2			V
$R_{PD,in}$	Pull-down resistor on input lines INHx/INx, INLx/ENx, nCS, CLK, SDI			220		kΩ
$R_{PD,STBY}$	nSTBY pin pull-down resistor			440		kΩ
$R_{PD,EN}$	EN pin pull-down resistor			440		kΩ
$V_{OD,L}$	Open-drain output low voltage (nFAULT, FLAG, SDO)	I_{OD} = 8 mA			0.35	V
$V_{release}$	EN pin latch release threshold		0.37			V
$t_{EN,pulse\_rel}$	Latch release time		400			ns

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{STBY}	Standby time	From nSTBY falling edge			100	µs

1. *See Figure 20, Figure 21, Figure 22.*
2. *The matching time, on the same driver, between the on and off transition is defined as $|t_{d,on} - t_{d,off}|$.*
3. *The matching of the same parameter ($t_{d,on}$ or $t_{d,off}$) between the two drivers (HS and LS) of the same half bridge is defined as $|t_{d,on,HS} - t_{d,on,LS}|$ or $|t_{d,off,HS} - t_{d,off,LS}|$.*
4. *The matching of the same parameter ($t_{d,on}$ or $t_{d,off}$) between the two drivers (HS and LS) of two different half-bridges (channels) "x" and "y" is defined as $|t_{d,on,HSx} - t_{d,on,HSy}|$, $|t_{d,off,HSx} - t_{d,off,HSy}|$, $|t_{d,on,LSx} - t_{d,on,LSy}|$, $|t_{d,off,LSx} - t_{d,off,LSy}|$.*
5. *Guaranteed by design.*

4 Pin description

4.1 STDRIVE102BP pin description

Figure 3. **STDRIVE102BP pin description**

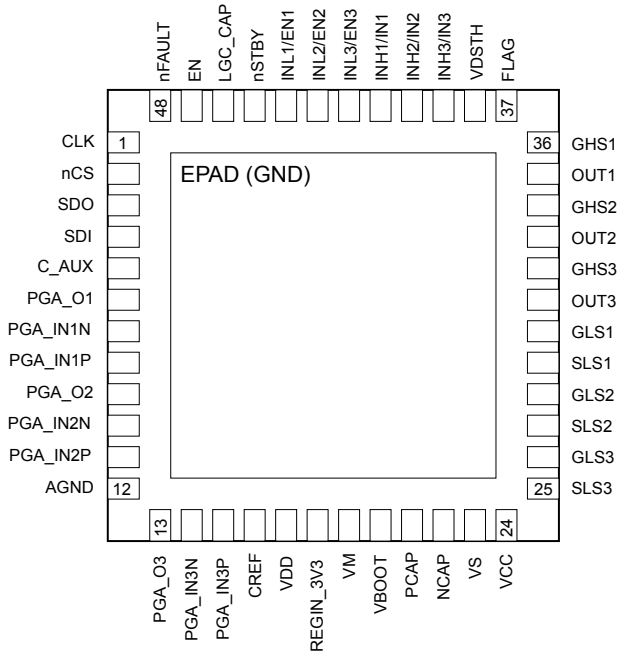


Table 7. **STDRIVE102BP pin list**

Pin N.	Name	Type	Function
1	CLK	Digital In	Serial clock of the SPI. Internal pull-down.
2	nCS	Digital In	Chip-select of the SPI (active low). Internal pull-down.
3	SDO	Digital Out	Serial data output of the SPI (open-drain).
4	SDI	Digital In	Serial data input of the SPI. Internal pull-down.
5	C_AUX	Analog In	Auxiliary non-inverting input of the comparator 3.
6	PGA_O1	Analog Out	Output of the PGA 1.
7	PGA_IN1N	Analog In	Inverting input of the PGA 1.
8	PGA_IN1P	Analog In	Non-inverting input of the PGA 1.
9	PGA_O2	Analog Out	Output of the PGA 2.
10	PGA_IN2N	Analog In	Inverting input of the PGA 2.
11	PGA_IN2P	Analog In	Non-inverting input of the PGA 2.
12	AGND	Power	Analog ground of the device. Connect this pin to the EPAD or a suitable reference GND point.
13	PGA_O3	Analog Out	Output of the PGA 3.
14	PGA_IN3N	Analog In	Inverting input of the PGA 3.
15	PGA_IN3P	Analog In	Non-inverting input of the PGA 3.

Pin N.	Name	Type	Function
16	CREF	Analog In	Common reference voltage for the three comparators (inverting input).
17	VDD	Power	3.3 V LDO linear regulator output and supply voltage of the Analog front end (AFE).
18	REGIN_3V3	Power	3.3 V LDO linear regulator input.
19	VM	Power	Motor supply voltage: reference for the internal charge pump and V_{DS} monitoring protection.
20	VBOOT	Power	Charge pump output voltage: high-side drivers supply.
21	PCAP	Power	Charge pump fly capacitor positive pin.
22	NCAP	Power	Charge pump fly capacitor negative pin.
23	VS	Power	Device power supply and 12 V LDO linear regulator input.
24	VCC	Power	12 V LDO linear regulator output and supply voltage of the low-side drivers.
25	SLS3	Analog	Phase 3 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 3).
26	GLS3	Analog	Phase 3 low-side driver output.
27	SLS2	Analog	Phase 2 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 2).
28	GLS2	Analog	Phase 2 low-side driver output.
29	SLS1	Analog	Phase 1 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 1).
30	GLS1	Analog	Phase 1 low-side driver output.
31	OUT3	Analog	Phase 3 high-side reference voltage (external half-bridge 3 output).
32	GHS3	Analog	Phase 3 high-side driver output.
33	OUT2	Analog	Phase 2 high-side reference voltage (external half-bridge 2 output).
34	GHS2	Analog	Phase 2 high-side driver output.
35	OUT1	Analog	Phase 1 high-side reference voltage (external half-bridge 1 output).
36	GHS1	Analog	Phase 1 high-side driver output.
37	FLAG	Digital Out	Open-drain pin for event signaling (configurable).
38	VDSTH	Analog In	V_{DS} monitoring threshold. Internal pull-down.
39	INH3/IN3	Digital In	Digital control signal for the high-side of the phase 3 or control of the OUT3 voltage level. Internal pull-down.
40	INH2/IN2	Digital In	Digital control signal for the high-side of the phase 2 or control of the OUT2 voltage level. Internal pull-down.
41	INH1/IN1	Digital In	Digital control signal for the high-side of the phase 1 or control of the OUT1 voltage level. Internal pull-down.
42	INL3/EN3	Digital In	Digital control signal for the low-side of the phase 3 or enable of the half-bridge on OUT3. Internal pull-down.
43	INL2/EN2	Digital In	Digital control signal for the low-side of the phase 2 or enable of the half-bridge on OUT2. Internal pull-down.
44	INL1/EN1	Digital In	Digital control signal for the low-side of the phase 1 or enable of the half-bridge on OUT1. Internal pull-down.
45	nSTBY	Digital In	Digital control for the standby mode (active low). Internal pull-down.
46	LGC_CAP	Power	Pin for external bypass capacitor – internal logic supply stabilization (not intended for external supply purposes).
47	EN	Digital In	Drivers enable with “FAULT release” feature. Internal pull-down.
48	nFAULT	Digital Out	Open-drain pin for failure/protection events signaling (configurable).
EPAD	GND	Power	Ground.

4.2 STDRIVE102P pin description

Figure 4. **STDRIVE102P pin description**

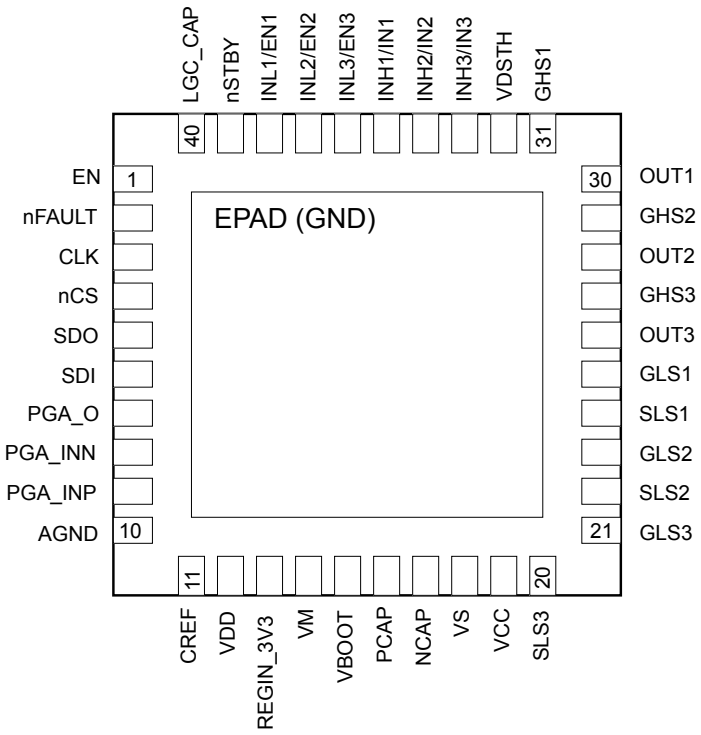


Table 8. **STDRIVE102P pin list**

Pin N.	Name	Type	Function
1	EN	Digital In	Drivers enable with “FAULT release” feature. Internal pull-down.
2	nFAULT	Digital Out	Open-drain pin for failure/protection events signaling (configurable).
3	CLK	Digital In	Serial clock of the SPI. Internal pull-down.
4	nCS	Digital In	Chip-select of the SPI (active low). Internal pull-down.
5	SDO	Digital Out	Serial data output of the SPI (open-drain).
6	SDI	Digital In	Serial data input of the SPI. Internal pull-down.
7	PGA_O	Analog Out	Output of the PGA.
8	PGA_INN	Analog In	Inverting input of the PGA.
9	PGA_INP	Analog In	Non-inverting input of the PGA.
10	AGND	Power	Analog ground of the device. Connect this pin to the EPAD or a suitable reference GND point.
11	CREF	Analog In	Common reference voltage for the comparator (inverting input).
12	VDD	Power	3.3 V LDO linear regulator output and supply voltage of the Analog Front-End (AFE).
13	REGIN_3V3	Power	3.3 V LDO linear regulator input.
14	VM	Power	Motor supply voltage: reference for the internal charge pump and V_{DS} monitoring protection.
15	VBOOT	Power	Charge pump output voltage: high-side drivers supply.
16	PCAP	Power	Charge pump fly capacitor positive pin.

Pin N.	Name	Type	Function
17	NCAP	Power	Charge pump fly capacitor negative pin.
18	VS	Power	Device power supply and 12 V LDO linear regulator input.
19	VCC	Power	12 V LDO linear regulator output and supply voltage of the low-side drivers.
20	SLS3	Analog	Phase 3 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 3).
21	GLS3	Analog	Phase 3 low-side driver output.
22	SLS2	Analog	Phase 2 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 2).
23	GLS2	Analog	Phase 2 low-side driver output.
24	SLS1	Analog	Phase 1 low-side reference voltage (source of the external low-side MOSFET in the half-bridge 1).
25	GLS1	Analog	Phase 1 low-side driver output.
26	OUT3	Analog	Phase 3 high-side reference voltage (external half-bridge 3 output).
27	GHS3	Analog	Phase 3 high-side driver output.
28	OUT2	Analog	Phase 2 high-side reference voltage (external half-bridge 2 output).
29	GHS2	Analog	Phase 2 high-side driver output.
30	OUT1	Analog	Phase 1 high-side reference voltage (external half-bridge 1 output).
31	GHS1	Analog	Phase 1 high-side driver output.
32	VDSTH	Analog In	V_{DS} monitoring threshold. Internal pull-down.
33	INH3/IN3	Digital In	Digital control signal for the high-side of the phase 3 or control of the OUT3 voltage level. Internal pull-down.
34	INH2/IN2	Digital In	Digital control signal for the high-side of the phase 2 or control of the OUT2 voltage level. Internal pull-down.
35	INH1/IN1	Digital In	Digital control signal for the high-side of the phase 1 or control of the OUT1 voltage level. Internal pull-down.
36	INL3/EN3	Digital In	Digital control signal for the low-side of the phase 3 or enable of the half-bridge on OUT3. Internal pull-down.
37	INL2/EN2	Digital In	Digital control signal for the low-side of the phase 2 or enable of the half-bridge on OUT2. Internal pull-down.
38	INL1/EN1	Digital In	Digital control signal for the low-side of the phase 1 or enable of the half-bridge on OUT1. Internal pull-down.
39	nSTBY	Digital In	Digital control for the standby mode (active low). Internal pull-down.
40	LGC_CAP	Power	Pin for external bypass capacitor – internal logic supply stabilization (not intended for external supply purposes).
EPAD	GND	Power	Ground.

5 Device description

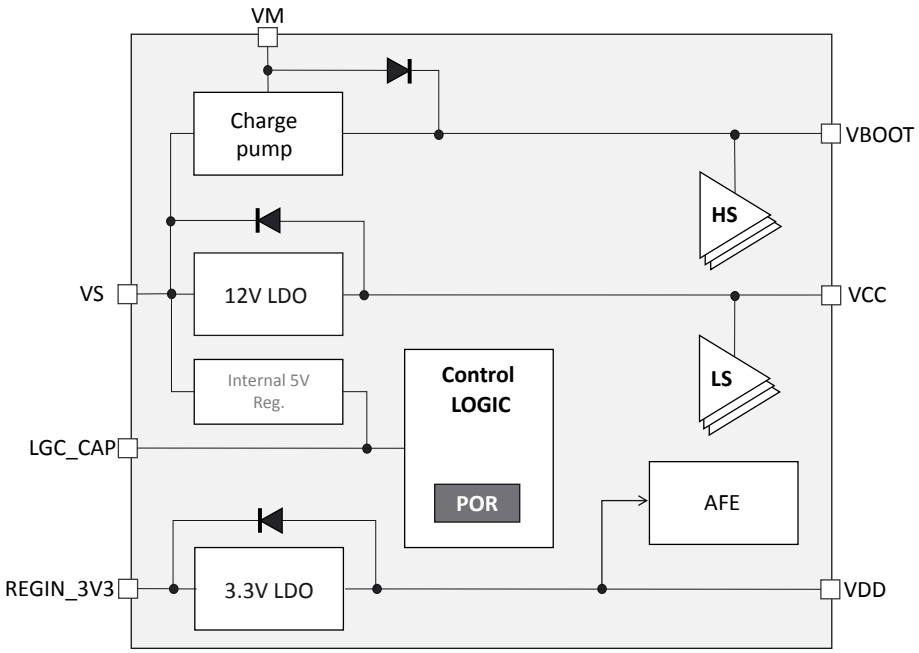
The STDRIVE102BP and the STDRIVE102P are triple half-bridge gate drivers suitable for 3-phase brushless motor driving. From now on, the naming convention STDRIVE102BP/P will be used to refer to either one indistinctly.

5.1 Power management section

The power management section of the STDRIVE102BP/P (Figure 5) is composed of:

- One LDO linear regulator with 12 V output; it is used to generate the VCC for the gate drivers' supply. Its input VS can be connected to the VM or to an external voltage (up to 50 V operative).
- One LDO linear regulator, which generates the 3.3 V supply (VDD). Its input REGIN_3V3 ranges between 3.6 V and 15 V. It can also be connected to the VCC or be fed by an external supply.
- One internal regulator, which supplies the STDRIVE102BP/P control logic at 5 V. This voltage is for internal use only. No external load or circuitry can be connected to the LGC_CAP pin, which must only be used to connect an external decoupling capacitor (low-ESR ceramic, 4.7 µF / 16 V). This capacitor stabilizes all the internal control circuits, including the power-on reset (POR).
- A charge pump, supplied by VS and referenced to VM, which generates the VBOOT supply rail for the high-side gate drivers.

Figure 5. Power management block diagram

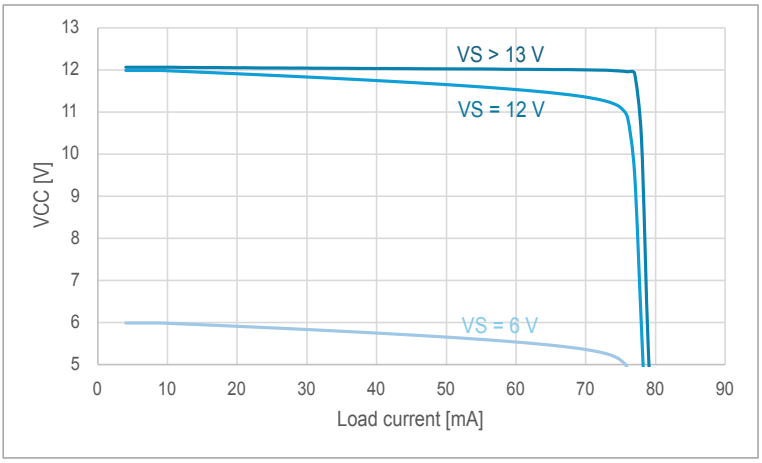


5.1.1 12 V LDO linear regulator

This regulator generates the voltage on the VCC pin, which is the supply for the low-side gate drivers and the set point for the 'V_{BOOT} - V_M' voltage provided by the charge pump (refer to Section 5.1.3). A low ESR ceramic capacitor of 4.7 µF, 25 V must be placed as close as possible to the VCC pin, to ensure the stability of the V_{CC} and support the currents required by the low-side gate drivers.

In addition, external loads can be connected to the VCC pin, provided they stay within the operating range. The output current of the regulator is limited at $I_{CC,lim}$ protecting it against short circuit and overload. The overall consumption of the external loads plus the drivers must be smaller than this current limitation.

Figure 6. 12 V LDO output according to the current load at different VS input



The linear regulator input is connected to the main supply VS. The regulator can be bypassed by connecting the VCC and the VS together and forcing an external voltage equal to the target VCC value, which must always be within the operative range of the VCC pin.

The regulator is disabled in standby mode in order to reduce the current consumption.

The output of the regulator V_{CC} has two different thresholds: the “power-good” threshold and the undervoltage lockout (UVLO) threshold. Both thresholds have a hysteresis as shown in Figure 7.

The V_{CC} good thresholds values can be selected using VCC_GOOD_SEL bit (refer to Section 5.12.4.6).

The V_{CC} undervoltage lockout (UVLO) thresholds are selectable as well using UV_SEL bit (refer to Section 5.12.4.6). This bit also affects the undervoltage thresholds on the charge pump voltage (refer to Section 5.1.3.

In case the VCC voltage falls below the UVLO threshold ($V_{CC(Off)}$), the gate drivers turn off all the external MOSFETs, forcing the power stage into a safe condition. As soon as the VCC voltage rises above the $V_{CC(On)}$ threshold, the nFAULT is released and the drivers return to an active condition, according to the status of the digital inputs.

It is possible to report the UVLO condition on the nFAULT pin, by setting the VCC_UV_FAULT_SIG at 1 (see Section 5.12.4.9). In this case the nFAULT pin is kept low during the UVLO condition, and then released when V_{CC} rises above the $V_{CC(On)}$ threshold. In case the VCC_UV_FAULT_SIG = 0, the UVLO condition is not reported on nFAULT pin, but the UVLO protection is still active.

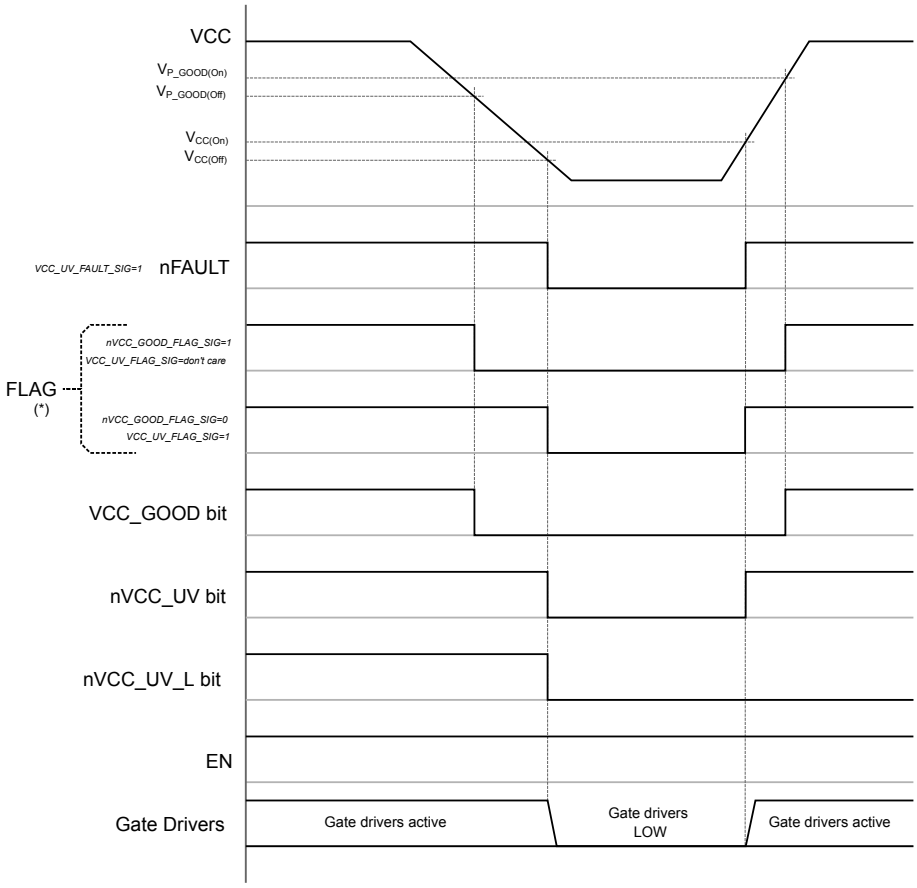
In case the VCC voltage falls below the “power-good” threshold ($V_{P\_GOOD(Off)}$), but stays above the UVLO threshold ($V_{CC(Off)}$), there are no other effects on the functional blocks of the devices. The gate drivers stay active according to the status of the digital inputs.

If nVCC_GOOD_FLAG_SIG = 1 (see Section 5.12.4.10), when the VCC voltage falls below the “power-good” threshold ($V_{P\_GOOD(Off)}$), the FLAG open-drain pin is forced low. The FLAG pin is then released as soon as the VCC voltage rises above the $V_{P\_GOOD(On)}$ threshold. This situation is represented in Figure 7 on the upper instance of FLAG signal.

In case VCC_UV_FLAG_SIG = 1 (see Section 5.12.4.11) and nVCC_GOOD_FLAG_SIG = 0, the FLAG pin reports the UVLO condition. This situation is represented in Figure 7 on the lower instance of FLAG signal.

The status bits related to the power-good and VCC UVLO conditions are also shown in Figure 7. The actual meaning of each bit (VCC_GOOD, nVCC_UV and nVCC_UV_L) is reported in Section 5.12.4.1 and Section 5.12.4.2.

Figure 7. V_{CC} thresholds (power-good and UVLO)



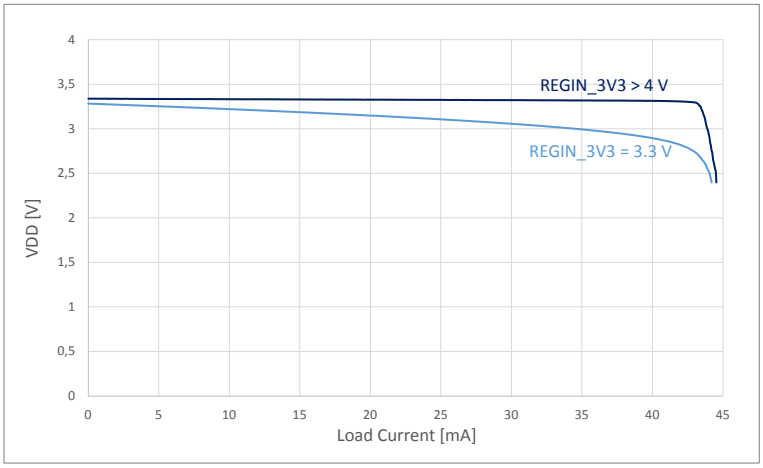
Note: (*) The FLAG pin is available only on the STDRIVE102BP.

5.1.2 3.3 V LDO linear regulator

The device integrates a 3.3 V regulator, which supplies the embedded analog front end (AFE). In addition, external loads can be connected to the VDD pin, provided they stay within the operating range. It is recommended to place a low ESR ceramic capacitor of 4.7 µF 16 V as close as possible to the VDD pin, to ensure the stability of the VDD voltage.

The output current of the regulator is limited at $I_{DD,lim}$, protecting it against short-circuit and overload. The overall consumption of the external loads plus the AFE must be smaller than this current limitation.

Figure 8. 3.3 V LDO output according to the current load at different REGIN_3V3 input



The regulator is disabled in standby mode in order to reduce the current consumption.

The regulator can be bypassed by connecting the VDD and the REGIN_3V3 pins together and forcing externally a voltage equal to the target VDD value, which must always be within the operative range of the VDD pin.

The 3.3 V regulator has a dedicated UVLO protection. The UVLO helps to avoid unexpected behavior related to all the circuitries supplied by the VDD. In particular, it avoids spurious events coming from the AFE comparators.

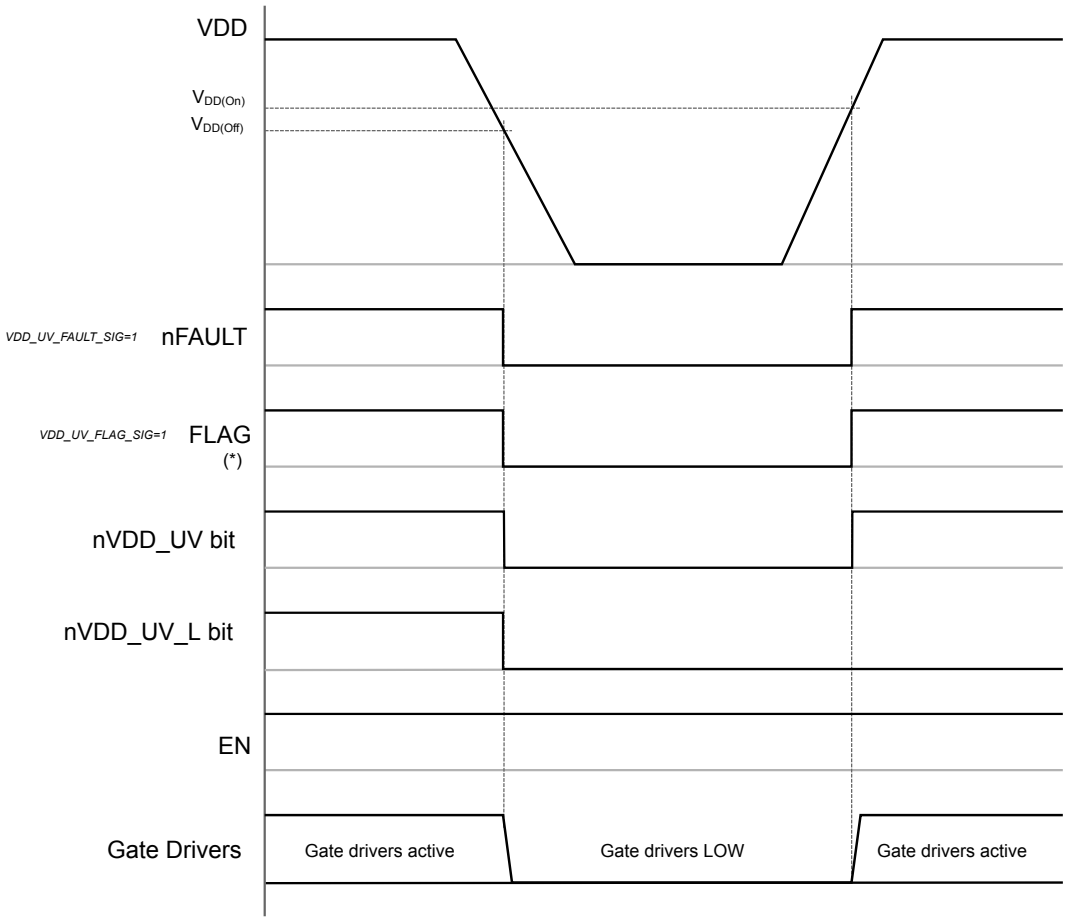
In case of UVLO condition (VDD falls below the $V_{DD(off)}$ threshold), the drivers turn off all the external MOSFETs, forcing the power stage into a safe condition. As soon as the VDD voltage rises above the $V_{DD(On)}$ threshold, the drivers return to an active condition, depending on the status of the digital inputs.

It is possible to report the UVLO condition on the nFAULT pin, by setting the VDD_UV_FAULT_SIG at 1 (see Section 5.12.4.9). In this case, the nFAULT pin is kept low during the UVLO condition, and then released when VDD rises above the $V_{DD(On)}$ threshold. In case the VDD_UV_FAULT_SIG = 0, the UVLO condition is not reported on nFAULT pin, but the UVLO protection is still active.

It is also possible to report the UVLO condition on the FLAG pin, by setting the VDD_UV_FLAG_SIG at 1 (see Section 5.12.4.11). In this case the FLAG pin is kept low during the UVLO condition, and then released when VDD rises above the $V_{DD(On)}$ threshold. In case the VDD_UV_FLAG_SIG = 0, the UVLO condition is not reported on the FLAG pin, but the UVLO protection is still active.

The status bits related to the VDD UVLO condition are also shown in Figure 9. The actual meaning of each bit (nVDD_UV_L and nVDD_UV) is reported in Section 5.12.4.1 and Section 5.12.4.3.

Figure 9. **VDD thresholds (UVLO)**

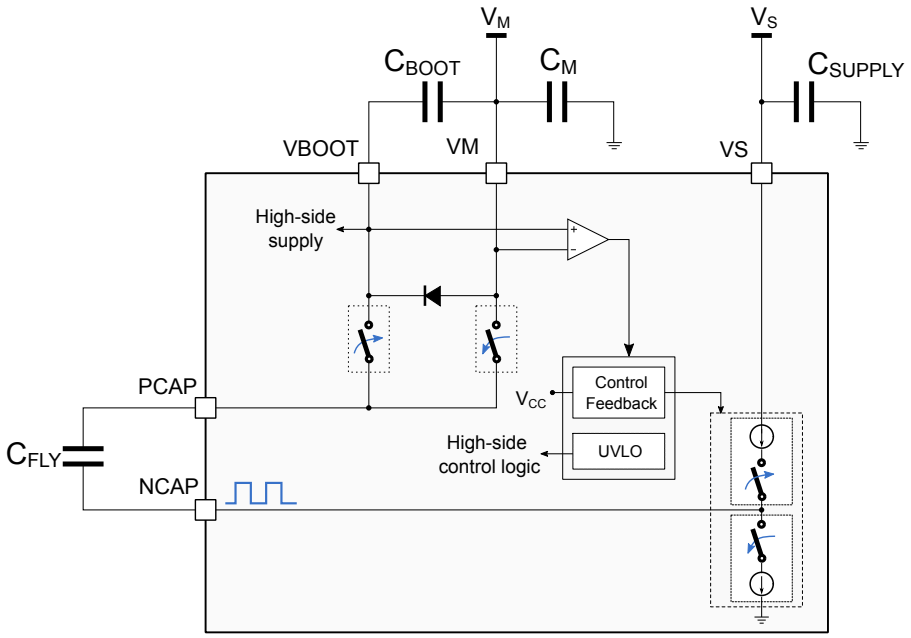


Note: (*) The FLAG pin is available only on the STDRIVE102BP.

5.1.3 Charge pump

The embedded charge pump supplies the high-side gate drivers and ensures an unlimited on-time of the high-side MOSFETs with a PWM duty cycle of 100%.

Figure 10. Charge pump simplified block diagram



The charge pump is supplied directly by the VS pin and generates the voltage V_{BOOT} referenced to the motor supply V_M. The V_{BOOT} is the supply of the three high-side gate drivers and it must be greater than V_M to properly turn on the high-side MOSFETs. The internal feedback circuit of the charge pump tracks the value of the voltage on the VCC pin and regulates the V_{BOOT} to be equal to 'V_M + V_{CC}'. In this way, both the low-side and the high-side MOSFETs are driven with the same V_{GS}, thus ensuring a more balanced behavior of the power stage.

The circuit on the NCAP pin charges the capacitor C_{FLY}. The charge is then transferred to the C_{BOOT} capacitor through the PCAP pin. The amount of charge stored in the C_{FLY} capacitor is controlled by the internal feedback, in order to meet the target voltage on VBOOT pin.

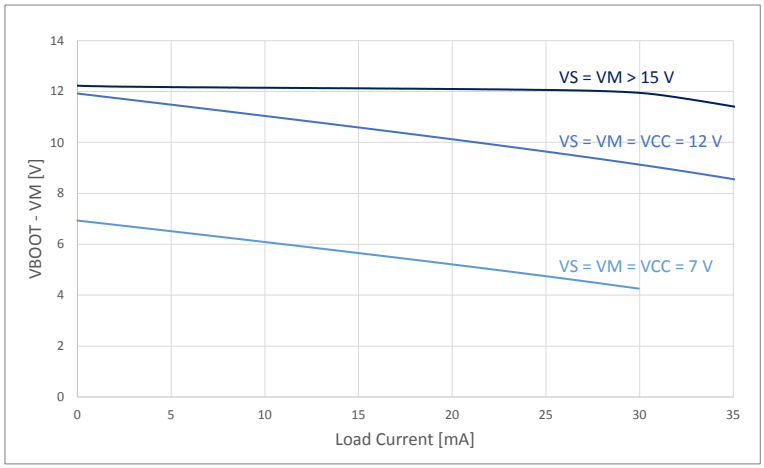
The drop between the target value of V_{BOOT} and its actual value depends on the voltage on the VS pin and the average load current required by the high-side drivers. The drop increases for lower V_S and higher current load. Figure 11 shows the charge pump output voltage with respect to the load current at T_{amb} = 25°C, using the recommended values for C_{FLY} = 220 nF and C_{BOOT} = 1 µF.

The pulsed current required by the high-side drivers is provided by the C_{BOOT} capacitor. This capacitor should be sized according to the maximum allowed ripple and total gate charge of the external MOSFETs. A ceramic low ESR capacitor of the same value of C_{BOOT} must be placed close to the VM pin and the exposed pad (GND) of the STDRIVE102BP/P.

The high-side drivers are connected to VBOOT by an internal connection. Under no circumstances should other external loads be connected to the VBOOT pin. The VBOOT pin is referred to the VM pin. Any external event forcing a 'V_{BOOT} - V_M' voltage below the limit reported in Table 1 results in device breakdown.

The charge pump is disabled in standby mode in order to reduce the current consumption.

Figure 11. Charge pump output voltage with respect to the load current



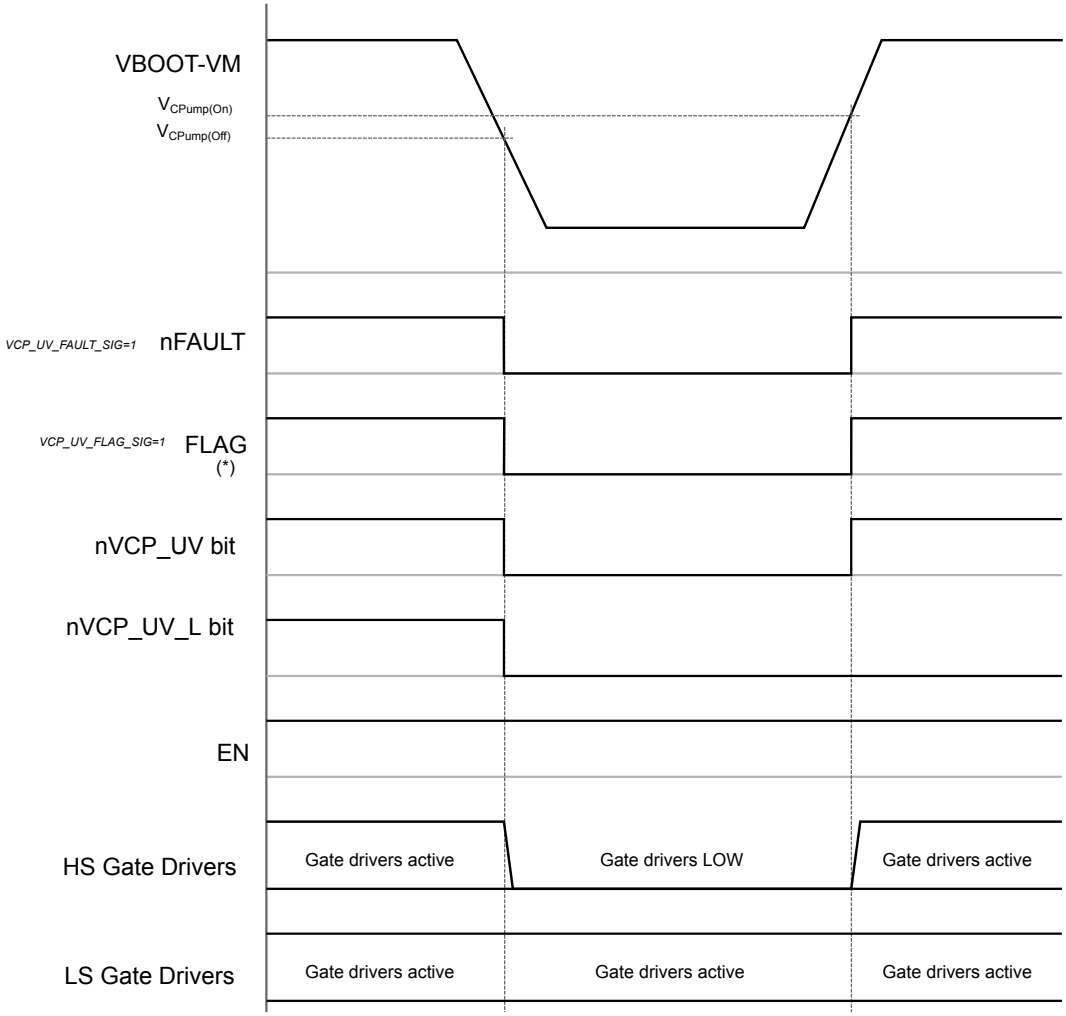
In case of undervoltage ('V_{BOOT} - V_M ' < $V_{CPump(Off)}$), the UVLO protection turns off the high-side MOSFETs, while the low-side drivers keep operating. The high-side drivers resume operation when 'V_{BOOT} - V_M' > $V_{CPump(On)}$.

The charge pump undervoltage thresholds can be selected using the bit UV_SEL bit in the SYS_CFG register (see Section 5.12.4.6). This bit also affects the undervoltage thresholds on the VCC (see Section 5.1.1).

It is possible to report the UVLO condition on the nFAULT pin, by setting the VCP_UV_FAULT_SIG at 1 (Section 5.12.4.9). In this case, the nFAULT pin is kept low during the UVLO condition, and then released when 'V_{BOOT} - V_M' rises above the $V_{CPump(On)}$ threshold. In case the VCP_UV_FAULT_SIG = 0, the UVLO condition is not reported on nFAULT pin, but the UVLO protection is still active.

The status bits related to the charge pump UVLO condition are also shown in Figure 12. The actual meaning of each bit (nVCP_UV_L and nVCP_UV) is reported in Section 5.12.4.1 and Section 5.12.4.2.

Figure 12. Charge pump thresholds (UVLO)



Note: (*) The FLAG pin is available only on the STDRIVE102BP.

5.2 Gate drivers

The gate drivers use a constant-current approach, enabling the following advantages:

- No external components are required between the MOSFETs' gates and the drivers.
- The slew rate of the half-bridge outputs is better controlled.

The high-side drivers (Figure 13) and the low-side drivers (Figure 14) have a similar structure:

- A reference pin for the low level (OUTx for the high-side and SLSx for the low-side).
- The output pin (GHSx for the high-side or GLSx for the low-side), which directly drives the external MOSFET's gate.
- The supply pins (VBOOT shared by the three high side drivers and VCC shared by the three low side drivers).

When the driver is not operative (for example, in standby mode or for very low supply), an equivalent 100 kΩ resistor keeps the external MOSFETs off. Under normal conditions, the gate driver must force a voltage on the gate of its respective MOSFET, in order to keep it in a well-defined state. This datasheet uses the following definitions:

- Setting the gate driver to HIGH means that the driver sources a controlled current to increase the V_{GS} of the MOSFET and turn it on. The gate current comes from the supply VCC for the low-side driver, or from VBOOT for the high-side driver.
- Setting the gate driver to LOW means that the driver sinks a controlled current from the gate of the MOSFET to turn it off. The sink circuitry of the driver is referred to the OUTx pin for the high-side, and to the SLSx pin for the low-side. This approach ensures that the MOSFET is kept off, even in the presence of below-GND transients.

In normal mode operation, when a high-side driver is set HIGH, the voltage on the GHSx pin increases up to its target level V_{BOOT} . At the same time, the OUTx voltage increases up to V_M, so that the V_{GS} of the external MOSFET is kept under control (less or equal to V_{CC}). In case the OUTx pin cannot follow the GHSx pin, the gate driver protects the gate of the external MOSFET from breakdown by clamping the V_{GS} at $V_{GS,\ clamp}$.

The six gate drivers (three low-side and three high-side) are controlled by six digital inputs, INH1/IN1, INH2/IN2, INH3/IN3, INL1/EN1, INL2/EN2, INL3/EN3. Each digital input has an internal pull-down resistor $R_{PD,in}$. Each half-bridge (driven by a low-side driver and a high-side driver) is controlled by a couple of inputs. For example, INH1/IN1 and INL1/EN1 refer to half-bridge 1. The label INHx/INx or INLx/ENx can be used to indicate one of the three half-bridges, with no specific reference to a particular channel. Note that the terms "channel" or "phase" may be used interchangeably to refer to the half-bridge output.

The STDRIVE102BP/P implements two control modes: the enable/input mode (EN/IN) or the direct mode (INH/INL), respectively explained in Section 5.2.3 and Section 5.2.2. The digital inputs assume a different function according to the input mode selected:

- In case the device is configured in Enable/Input mode:
  - INHx/INx → INx
  - INLx/ENx → ENx
- In case the device is configured in Direct mode:
  - INHx/INx → INHx
  - INLx/ENx → INLx

In addition to the six digital inputs mentioned above, another digital input named EN (pin 47 for the STDRIVE102BP and pin 1 for the STDRIVE102P) is used as general enable. In case it is forced to 0, all the six gate drivers are set to LOW, turning off all the external power MOSFETs. Setting EN to 1 activates the gate drivers, which behave according to their related digital inputs. The EN pin also integrates an analog threshold $V_{release}$, to release the latched condition after a FAULT event (refer to Section 5.8.1).

Figure 13. **High-side driver simplified block diagram**

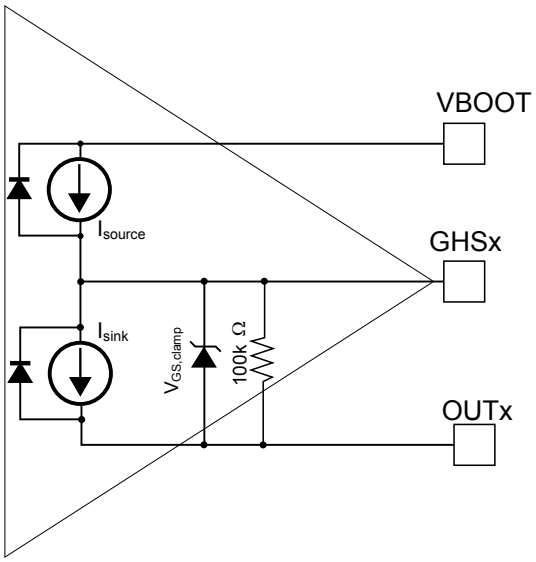
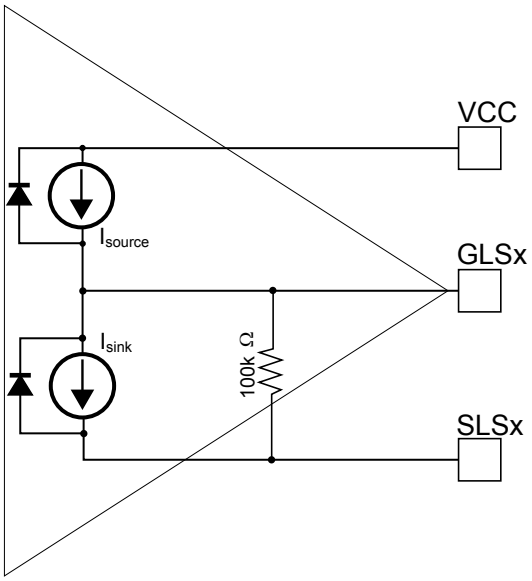


Figure 14. **Low-side driver simplified block diagram**



5.2.1 Driving current management

The gate driver turns on the respective MOSFET by sourcing the programmed current $I_{GATE,on}$ for a time equal to the programmed $t_{cc,on}$ time. After this time, the MOSFET's gate should be fully charged, so the driver reduces the source current to a hold value $I_{hold,on}$.

The gate driver turns off the respective MOSFET by sinking the programmed current $I_{GATE,off}$ for a time equal to the programmed $t_{cc,off}$ time. After this time, the MOSFET's gate should be fully discharged, so the driver reduces the sink current to a hold value $I_{hold,off}$.

To avoid induced turn-on effects, during the turn-on phase of a MOSFET (that is, when a driver is forcing $I_{GATE,on}$) the complementary driver sinks the maximum available current I_{clamp} for the entire $t_{cc,on}$ duration.

In case the interlocking protection is disabled (see Section 5.2.3), the I_{clamp} is not used.

The relation between currents and timings as a function of the programmed configuration can be summarized as:

- The value of the source current and the sink current is programmed with the bits IGATE[3:0] in the DRV_CFG register (see Section 5.12.4.5) and the relation between them depends on the DRV_EQ_SEL bit in the SYS_CFG register (see Section 5.12.4.6):
  - DRV_EQ_SEL = 0: $I_{GATE,off} = 2 \times I_{GATE,on}$, ensuring a turn-off faster than the turn-on.
  - DRV_EQ_SEL = 1: $I_{GATE,off} = I_{GATE,on}$.
- According to the setting of DRV_EQ_SEL, the relation between the timing programmed using the TCC[3:0] bits in the DRV_CFG register (see Table 31) is:
  - DRV_EQ_SEL = 0: $t_{cc,off} = 0.5 \times t_{cc,on}$.
  - DRV_EQ_SEL = 1: $t_{cc,off} = t_{cc,on}$.
    In this case, it is also possible to select the t_{cc} value among two sets of values, using the TCC_EQ_SEL bit. The TCC_EQ_SEL bit has no effect when DRV_EQ_SEL = 0.
- The $I_{hold,on}$ cannot be programmed and corresponds to the minimum source current that is 25 mA.
- The $I_{hold,off}$ corresponds to the minimum sink current in the selected configuration (25 mA when DRV_EQ_SEL = 1 and 50 mA when DRV_EQ_SEL = 0).
- The I_{clamp} corresponds to the maximum sink capability in the selected configuration (1070 mA when DRV_EQ_SEL = 1 and 2140 mA when DRV_EQ_SEL = 0).

Table 31 and Table 32 give all full decoded combinations possible for gate currents and timings.

Bolded cells indicate the default values at power-up or when the devices leave standby state.

5.2.2 Direct mode (INH/INL)

In direct mode (MODE_SEL = 0 in the SYS_CFG register, see Section 5.12.4.6), each digital input is directly related to the state of each driver. The digital input INHx/INx (simply indicated as INHx) directly controls the high-side driver; the INLx/ENx (simply indicated as INLx) controls the low-side driver. High digital input implies the gate driver turns on the respective MOSFET; low digital input turns it off.

The six digital inputs are managed as reported in Table 9, where x = 1, 2, 3 refers to the half-bridge driven. The driving logic also depends on the setting of bit INTLOCK of the SYS_CFG register:

- INTLOCK = 1 (default)
  The interlocking protection is enabled and prevents both power MOSFETs of the same half bridge from turning on simultaneously, avoiding possible cross-conduction. If both INHx and INLx inputs are high, both MOSFETs in the half-bridge x are turned off.
- INTLOCK = 0
  The interlocking protection is disabled. The high-side and low-side drivers on the same channel operate independently and their related MOSFETs can be turned on simultaneously. **This configuration is intended for power stage topologies other than half-bridge**. For this reason, since induced turn-on risk does not apply here, I_{clamp} is not used (see Figure 18).

Attention: *Do not select INTLOCK = 0 whenever a half-bridge topology is employed in the power stage; select INTLOCK = 1 to avoid cross conduction.*

Figure 15. Example of the interlocking protection

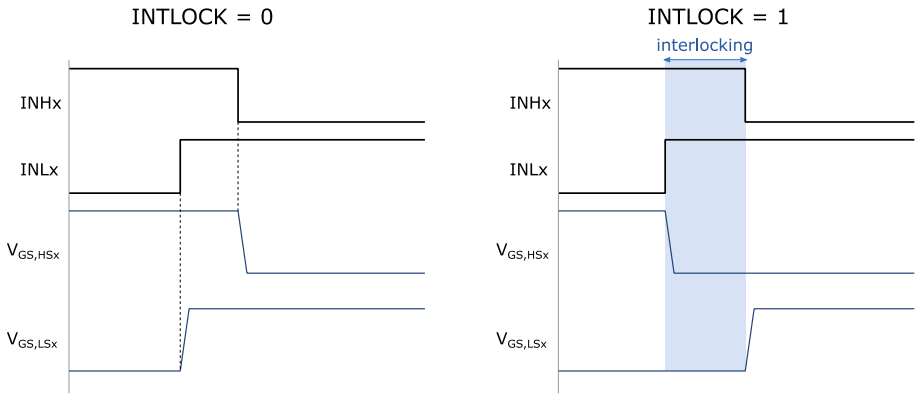


Table 9. Truth table for the direct mode

EN	INLx	INHx	INTLOCK	GLSx	GHSx	OUTx Half-bridge status
0	Do not care	Do not care	Do not care	All GLS sink current All drivers LOW All low-side MOSFETs OFF	All GHS sink current All drivers LOW All high-side MOSFETs OFF	All three phases are in high impedance
1	0	0	Do not care	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx in high impedance
1	0	1	Do not care	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx source current Driver *x* status HIGH High-side MOSFET *x* ON	OUTx at VM
1	1	0	Do not care	GLSx source current Driver *x* status HIGH Low-side MOSFET *x* ON	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx at GND
1	1	1	1	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx in high impedance Interlocking
1	1	1	0	GLSx source current Driver *x* status HIGH Low-side MOSFET *x* ON	GHSx source current Driver *x* status HIGH High-side MOSFET *x* ON	Not applicable. (INTLOCK = 0 must not be used in half-bridge configurations).

When INTLOCK = 1, the TCC_WAIT bit in the SYS_CFG register allows for more flexibility in controlling the driver on/off timings:

- TCC_WAIT = 0, it is possible to set a driver to HIGH (source current) as soon as the complementary one has been set to LOW (sink current). As a consequence, the deadtime (t_{DT}) between the turn-off of one driver and the turn-on of the complementary one is only defined by the digital inputs (Figure 16). The deadtime t_{DT} must be enough to ensure that the V_{GS} of the MOSFET that is turning off is equal to 0 V, before turning on the complementary MOSFET in the half-bridge. The criteria used should follow what is explained in Section 5.2.4, thus considering the total gate charge $Q_{G,tot}$ of the MOSFET and the $I_{GATE,off}$ selected.
  Equation 1

$$t_{DT} > \frac{Q_{G,tot}}{I_{GATE,off}} \quad (1)$$

- TCC_WAIT = 1: when a driver is set to LOW and the complementary one is set to HIGH by their digital inputs, the internal logic waits until the $t_{cc,off}$ related to the first driver (sinking current) has passed before sourcing the $I_{GATE,on}$ current on the complementary one.
  As a consequence, the actual deadtime between the drivers corresponds to the longer between the $t_{cc,off}$ selected and the t_{DT} imposed by the digital inputs.
  Figure 17 shows the case where the actual deadtime on the drivers is $t_{cc,off}$, which is greater than t_{DT} in the example.

Figure 16. Current management using direct mode INH/INL with TCC_WAIT = 0

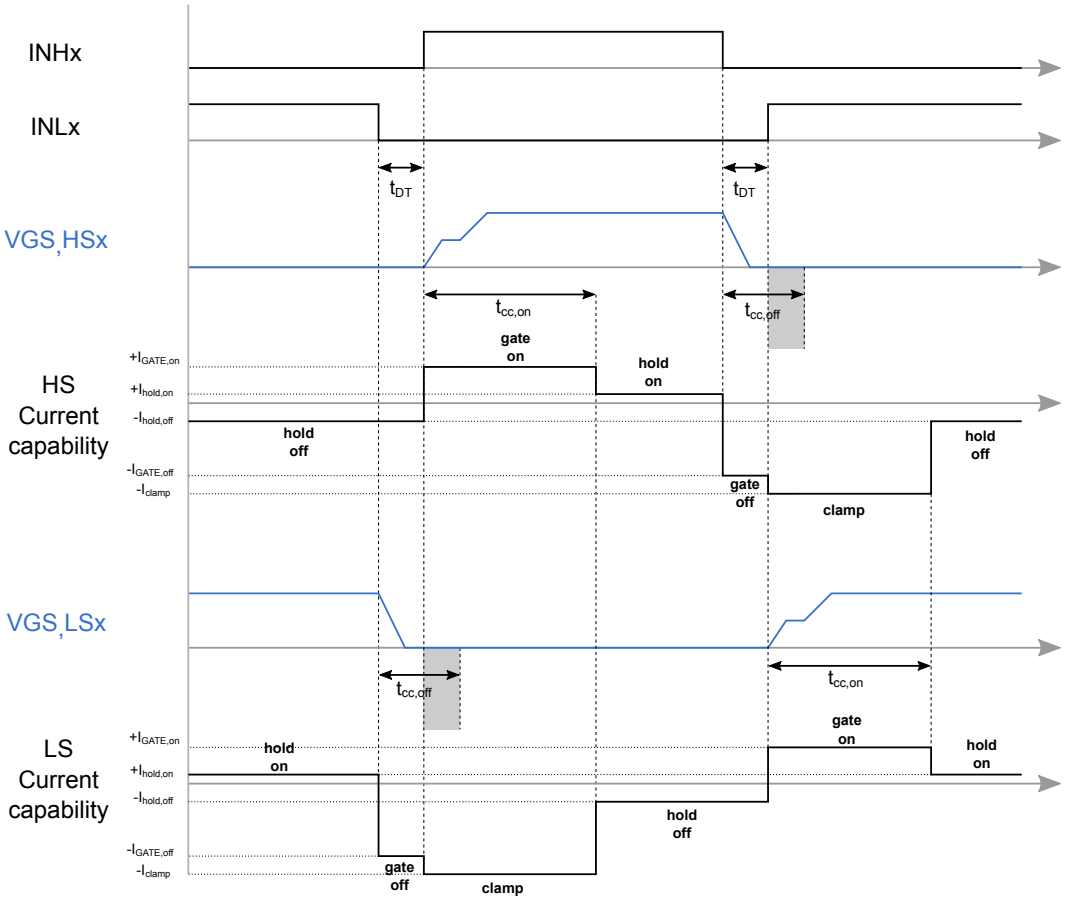


Figure 17. **Current management using direct mode INH/INL with TCC_WAIT = 1**

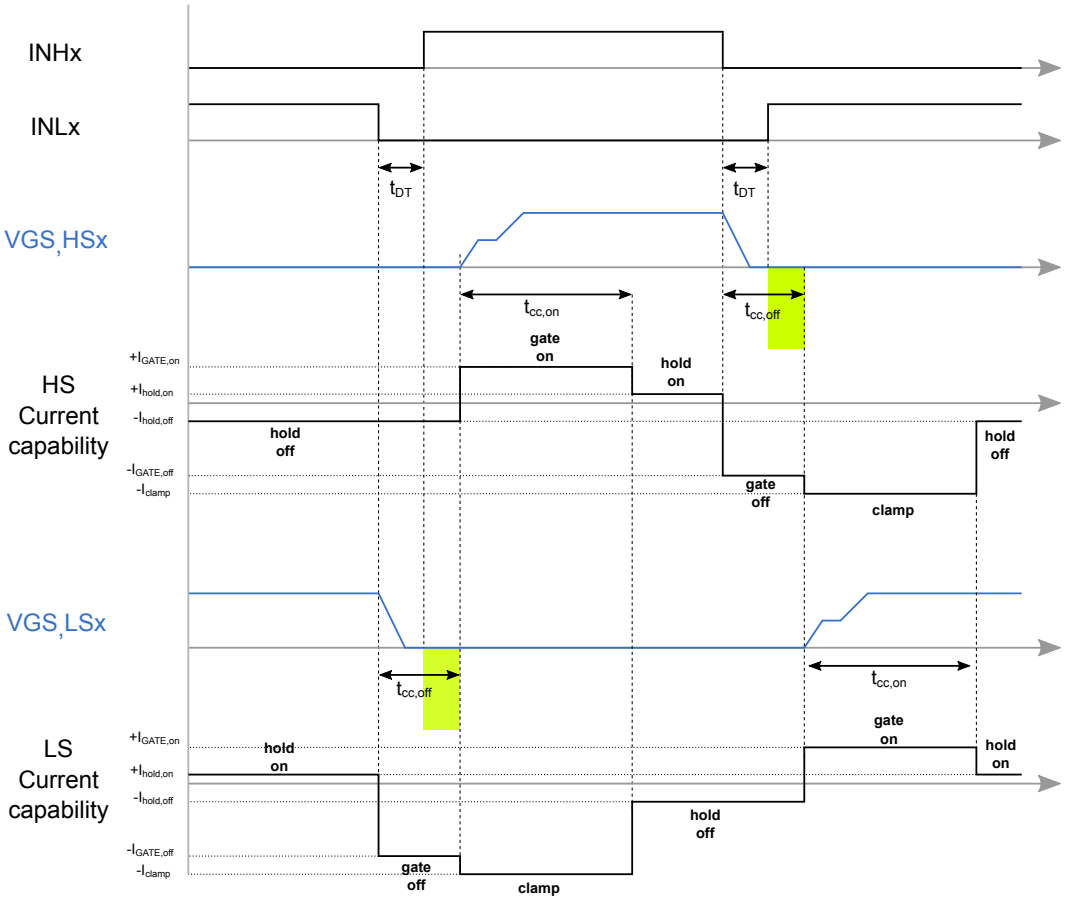
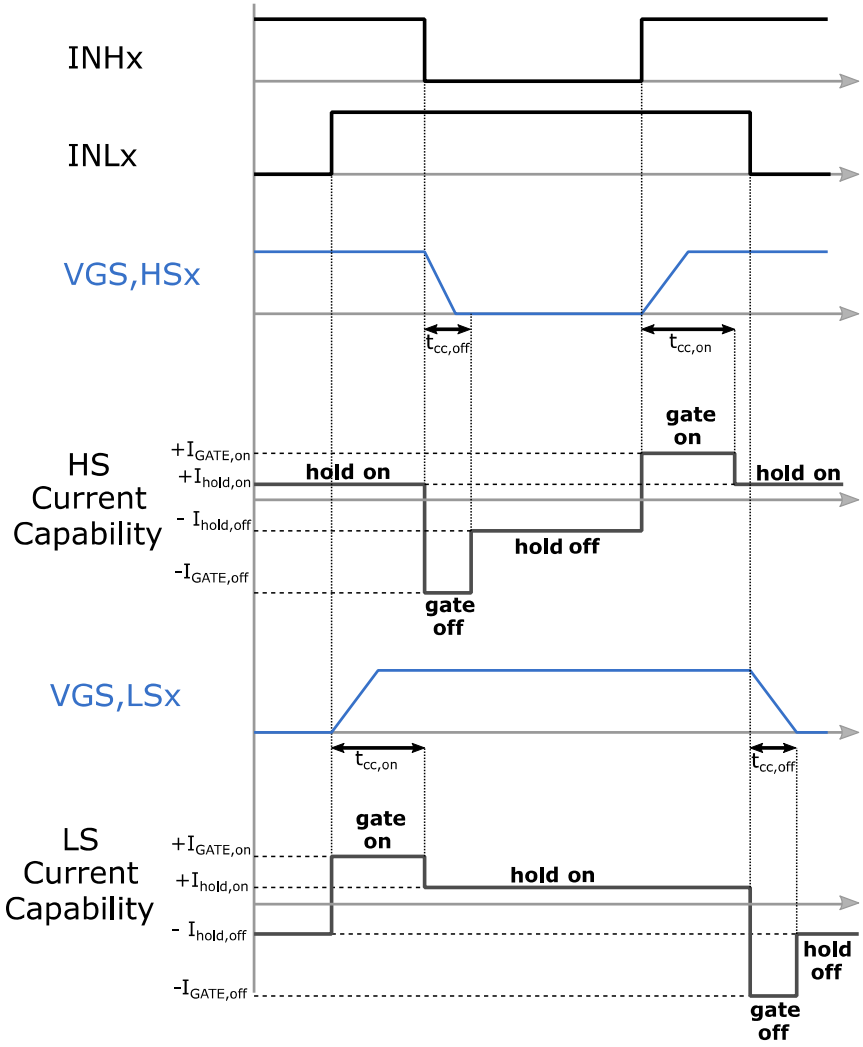


Figure 18. **Current management using direct mode INH/INL with interlocking protection disabled**



5.2.3 Enable/input mode (EN/IN)

When enable/input mode is selected (MODE_SEL = 1 default in the SYS_CFG register, see Section 5.12.4.6), the six digital inputs are managed as described in Table 10, where x = 1, 2, 3 refers to the half-bridge driven. The digital input INHx/INx is simply indicated as INx and INLx/ENx as ENx.

The half-bridge x is enabled by setting ENx = 1. Otherwise, when ENx = 0, the half-bridge is left in high impedance. When enabled, the half-bridge status is determined by the INx input: INx = 0 sets the state to LOW (OUTx at GND), INx = 1 sets the state to HIGH (OUTx = VM). The general EN pin is also reported in Table 10.

Table 10. Truth table for the enable/input mode

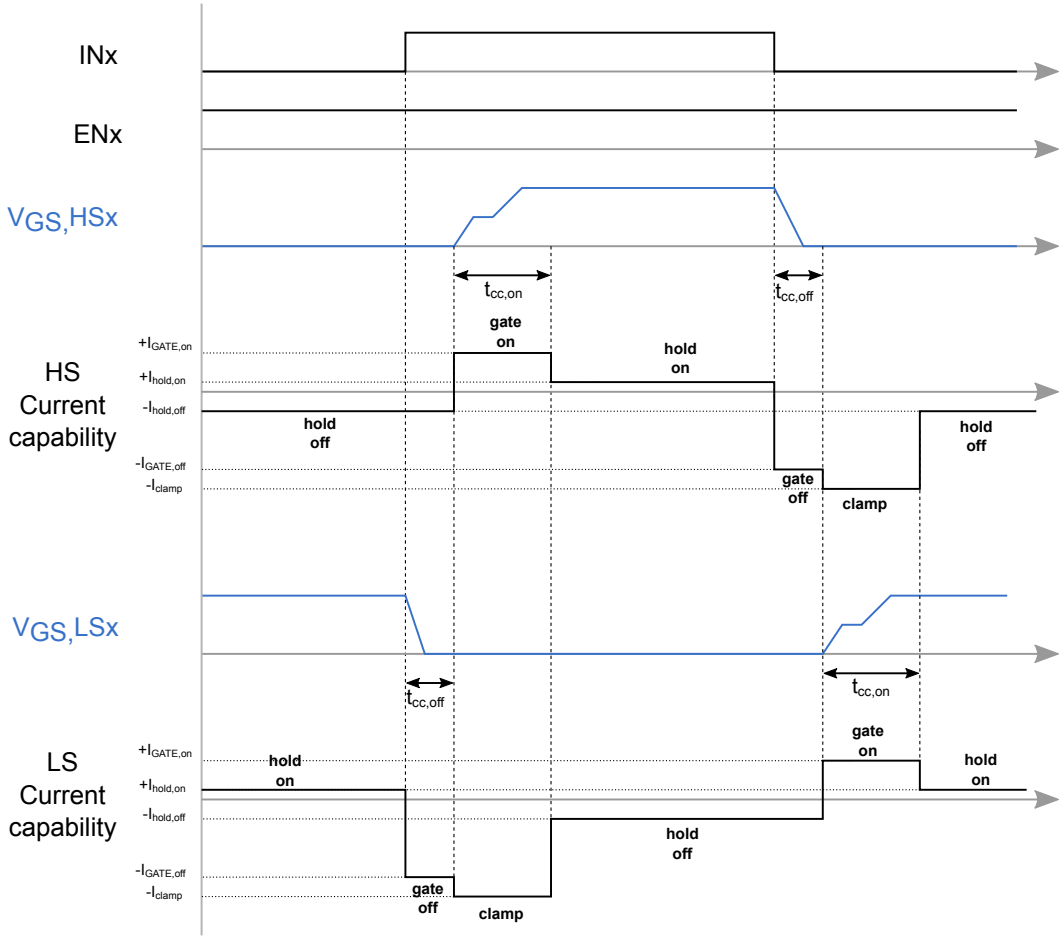
EN	ENx	INx	GLSx	GHSx	OUTx Half-bridge status
0	Do not care	Do not care	All GLS sink current All drivers LOW All low-side MOSFETs OFF	All GHS sink current All drivers LOW All high-side MOSFETs OFF	All three phases are in high impedance
1	0	Do not care	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx in high impedance
1	1	0	GLSx source current Driver *x* status HIGH Low-side MOSFET *x* ON	GHSx sink current Driver *x* status LOW High-side MOSFET *x* OFF	OUTx at GND
1	1	1	GLSx sink current Driver *x* status LOW Low-side MOSFET *x* OFF	GHSx source current Driver *x* status HIGH High-side MOSFET *x* ON	OUTx at VM

When INx is toggled, the logic changes the state of both the high-side x and the low-side x with a specific sequence: the driver that is currently HIGH is set to LOW; then, after a deadtime, the complementary driver is set to HIGH.

The deadtime is necessary to avoid cross-conduction. The deadtime is managed by the internal logic and it is equivalent to $t_{cc,off}$ (Figure 19). The user's responsibility is only to ensure that the selected combination of $I_{GATE,off}$ and $t_{cc,off}$ is adequate to completely turn off the power MOSFETs (see Section 5.2.4).

In enable/input mode, the TCC_WAIT and INTLOCK configuration bits of the SYS_CFG register are not used and do not affect the driver behavior.

Figure 19. **Current management using EN/IN mode**



5.2.4 Gate current and timing setting

The current and the timing of the driver are strictly related. They must be configured by the user through the TCC[3:0] and IGATE[3:0] bits, according to the external power MOSFETs and the slew rate required by the application. Additional selections can be made using the DRV_EQ_SEL and the TCC_EQ_SEL bits (see Section 5.12.4.6).

The IGATE level must be chosen according to Table 32, considering the gate-drain charge Q_{gd} of the driven MOSFET and the rising time/fall time, and thus the slew rate of the OUTx pin of the half-bridge.

Equation 2

$$I_{GATE,on/off} \cong \frac{Q_{gd}}{t_{sw}} \quad (2)$$

The current to be considered, whether $I_{GATE,on}$ or $I_{GATE,off}$, depends on which MOSFET of the half-bridge is hard-switching. Eq. (2) provides an indication to select a suitable driving current for the application; however, it must be considered that C_{gd} varies with the V_{DS} of the MOSFET, therefore some margin must be allowed.

The t_{sw} in Eq. (2) represents the switching time of the half-bridge OUTx, and it is strictly related to the slew-rate.

Equation 3

$$SR_{OUTx} \cong \frac{V_M}{t_{sw}} \quad (3)$$

For a given couple of values of $I_{GATE,on}$ or $I_{GATE,off}$, a couple of $t_{cc,on}$ and $t_{cc,off}$ can be selected from the values of Table 31. In this case the total gate charge $Q_{g,tot}$ of the external MOSFET must be considered, in order to ensure the complete charge/discharge of the gate within the t_{cc} time selected.

Equation 4

$$t_{cc,on} > \frac{Q_{G,tot}}{I_{GATE,on}} \quad , \quad t_{cc,off} > \frac{Q_{G,tot}}{I_{GATE,off}} \tag{4}$$

In case of MODE_SEL = 1 (EN/IN mode), the internal logic of the STDRIVE102BP/P imposes a deadtime that is equal to $t_{cc,off}$ so the condition in Eq. (4) ensures that one MOSFET is completely off before turning on the complementary one, preventing possible cross-conduction.

In case of MODE_SEL = 0 and TCC_WAIT = 0, the deadtime is determined by the digital input signals and indicated as t_{DT}. In this case, both the settings of $t_{cc,off}$ and t_{DT} should be selected according to the following:

Equation 5

$$t_{cc,off} > t_{DT} > \frac{Q_{G,tot}}{I_{GATE,off}} \tag{5}$$

The conditions reported in Eq. (4) state that the t_{cc} selected must be greater than the time required to completely turn on or turn off one MOSFET.

In case DRV_EQ_SEL = 0, $I_{GATE,on}$ is half the $I_{GATE,off}$; Eq. (4) yields $t_{cc,on}$ to be twice the $t_{cc,off}$, and for this reason the STDRIVE102BP/P imposes this relation between $t_{cc,on}$ and $t_{cc,off}$. It is possible to select the couple of values $t_{cc,on}/t_{cc,off}$ among 16 possibilities, using the TCC[3:0] bits.

In case DRV_EQ_SEL = 1, $I_{GATE,on} = I_{GATE,off}$; Eq. (4) yields $t_{cc,on} = t_{cc,off}$. The value selected using the TCC[3:0] bits is applied to both $t_{cc,on}$ and $t_{cc,off}$. In this case, there are two different timings available for each TCC[3:0] setting, selected according to the value of the TCC_EQ_SEL bit.

The list of values for $t_{cc,on}$ and $t_{cc,off}$ according to TCC[3:0], DRV_EQ_SEL and TCC_EQ_SEL parameters are listed in Table 31.

Section 5.2.5 shows a practical example of how to select proper IGATE and TCC settings, based on what is described in this section.

5.2.5 Configuration example

To guarantee a proper charge or discharge of the gate of the external MOSFETs, a proper $t_{cc,on}$/ $t_{cc,off}$ must be selected. The criteria used should follow what is explained in Section 5.2.4.

This section describes an example of how to configure the gate drivers in a three-phase half-bridge, assuming that:

- The MOSFETs have a total gate charge $Q_{G,tot}$ = 120 nC at 12 V of V_{GS}
- The same sink and source currents are used by setting the DRV_EQ_SEL bit equal to 1
- The INTLOCK bit is set to 1 to avoid cross-conduction between high-side and low-side MOSFETs.

Using $I_{GATE,on}$ = 350 mA (IGATE[3:0] = 0101b, refer to Table 32) allows for a complete charge/discharge of the gate in less than 350 ns. Therefore, adding some extra margin to this value, a good choice for $t_{cc,on}$ and $t_{cc,off}$ could be a value around 500 ns, which provides enough margin for a safe operation of the power stage.

From this example, it is possible to list two common cases:

Case 1 - MODE_SEL = 0 and TCC_WAIT = 0

This configuration can be selected when the device works in direct mode and the deadtime is fully imposed through the INHx/INLx signals. In this condition, the $t_{cc,off}$ only determines the time during which the driver's sink capability is equal to $I_{GATE,off}$. Consider a further requirement, where the deadtime between INHx/INLx can be changed dynamically from 500 ns to 600 ns. It is possible to select $t_{cc,off}$ higher than 600 ns, for example 700 ns, while the signals INHx/INLx implement the actual deadtime required. Therefore TCC[3:0] = 0100b and TCC_EQ_SEL = 1.

According to this specific example, configure the device by writing:

- Register DRV_CFG (Address 0x04) = 0x45 (see Section 5.12.4.5);
- Register SYS_CFG (Address 0x05) = 0x19 (see Section 5.12.4.6).

Case 2 - MODE_SEL = 1

This configuration can be selected when the device works in enable/input mode. The deadtime between the high- and low-side is generated by the logic of the device. It is possible to select one of the values from the ones reported in Table 31. Choosing TCC[3:0] = 0011b and TCC_EQ_SEL = 1 provides a $t_{cc,off}$ and a deadtime of 560 ns.

According to this specific example, configure the device by writing:

- Register DRV_CFG (Address 0x04) = 0x35 (see Section 5.12.4.5);
- Register SYS_CFG (Address 0x05) = 0x1C (see Section 5.12.4.6).

5.2.6 Propagation delays

The propagation delays between the edges of the digital inputs and the actuation of the gate drivers are represented in Figure 20, Figure 21, and Figure 22.

Figure 20. Propagation delay in direct mode (INHx/INLx)

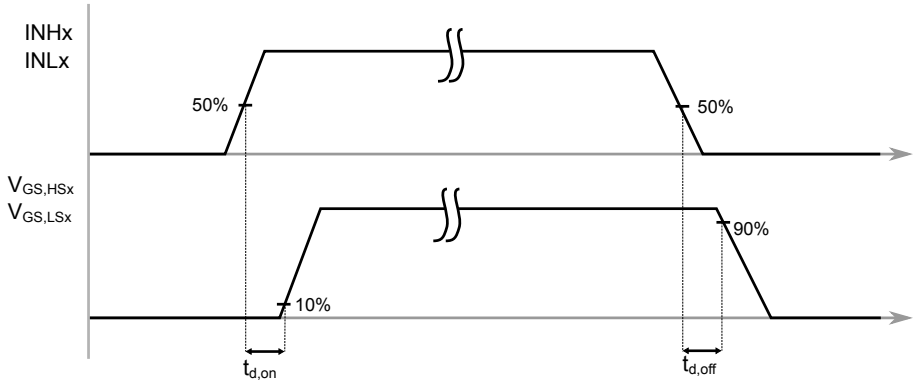


Figure 21. Propagation delay in enable/input mode, ENx pin high

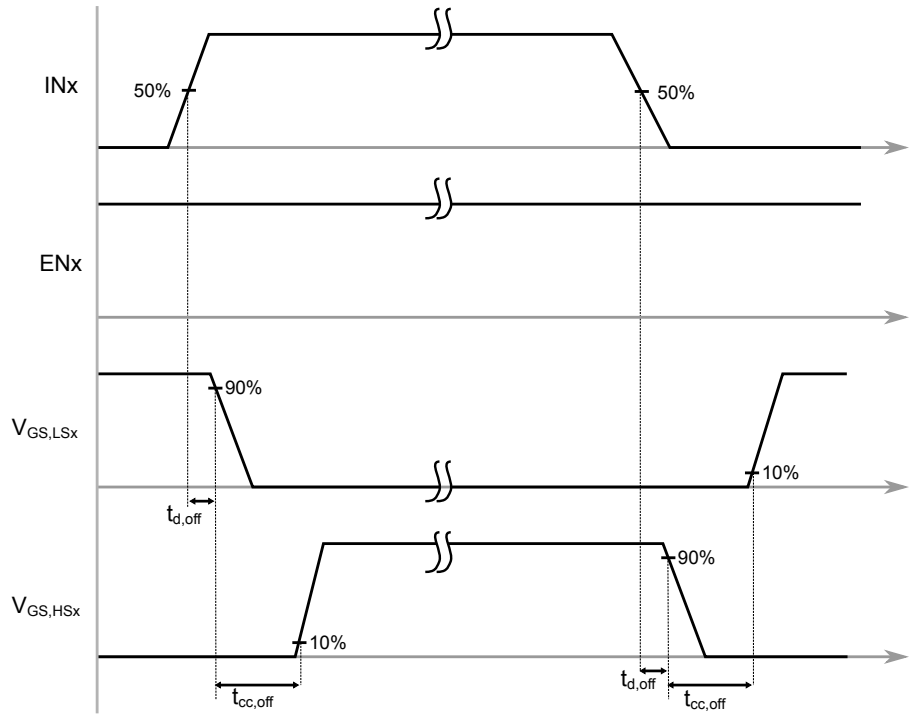
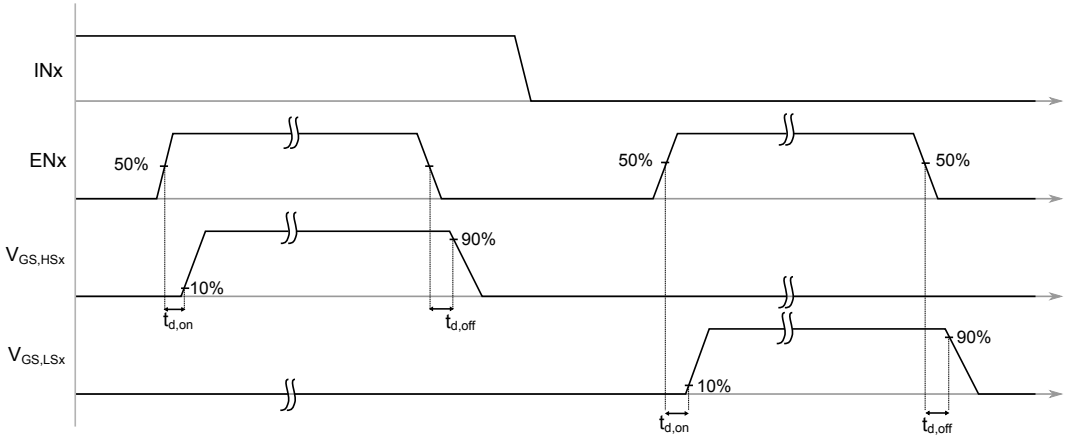


Figure 22. **Propagation delay in enable/input mode, ENx pin switching**



5.2.7 V_{DS} monitoring

The STDRIVE102BP/P implements a monitoring of the drain-source voltage drop (V_{DS}) of each MOSFET. During all the time the MOSFET is on, the V_{DS} is expected to stay below a threshold, which depends on the $R_{DS,on}$ and on the current flowing in the MOSEFT. If the V_{DS} exceeds the threshold value set on the VDSTH analog pin when the MOSFET is on (refer to Figure 23), the device triggers a FAULT condition.

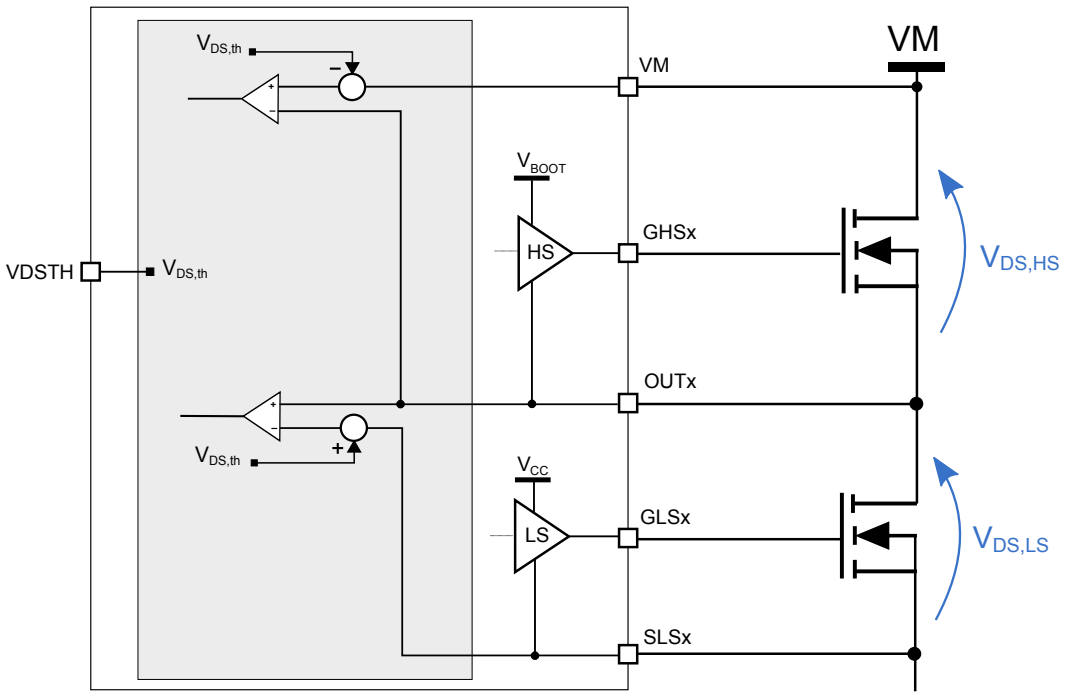
Since the three high-side MOSFETs are supposed to be connected to the same supply V_M, the three different V_{DS} are monitored with reference to the same VM pin.

Note that the threshold voltage is an analog value, so it can be set to any value between the recommended ones. The protection can be disabled by setting a voltage on VDSTH pin higher than $V_{DSTH,dis}$.

To avoid unexpected triggering of the protection during the transients of the power stage, a deglitch filter is present. To trigger the protection, the V_{DS} must exceed the threshold for a time longer than the deglitch time $t_{dg(VDS)}$ which can be selected using VDS_TDG[2:0] bits in the register VDS_CFG (see Section 5.12.4.7).

Note: When INTLOCK = 0, it is recommended to disable the V_{DS} monitoring by forcing the VDSTH pin above $V_{DSTH,dis}$.

Figure 23. **V_{DS} monitoring basic diagram**



The V_{DS} monitoring protection can detect different failures related to the power stage:

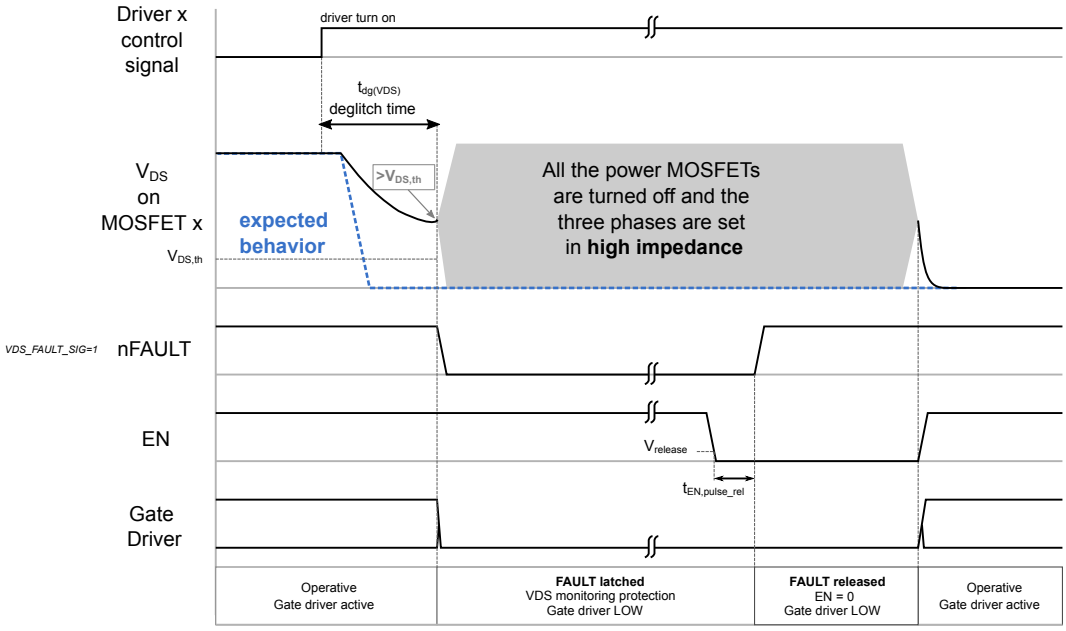
- Gate open. The gate connection is missing, or the gate is damaged.
- Gate short. The gate is damaged and there is a short between the gate and the source.
- OUT short. The OUT pin may be shorted to another motor phase, to GND or to VM.

In all these cases, the MOSFET does not turn on and its V_{DS} does not fall below the expected threshold (set on the VDSTH pin).

In other cases, the MOSFETs turn on and work correctly, but unexpected behavior can be detected as well by the V_{DS} monitoring.

- Overload. In the case of current overload on the motor, the V_{DS} on the MOSFET can increase and become higher than the threshold. Moreover, the temperature increase due to higher current can also lead to an increase of the $R_{DS,on}$ of the MOSFET and thus a further increase of the V_{DS} measured.
- Wrong TCC/IGATE configuration. If the driver current $I_{GATE,on}$ or the time $t_{cc,on}$ are too small, the external MOSFET turns on too slowly or with higher $R_{DS,on}$ and its V_{DS} may not fall below the expected $V_{DS,th}$ threshold within the $t_{dg(VDS)}$ time.

Figure 24. V_{DS} monitoring example



The example in Figure 24 shows how the V_{DS} monitoring protection works. When the driver turns on, it is expected that the V_{DS} of the respective MOSFET falls below the threshold (as shown by the dotted line). If the V_{DS} stays above the threshold $V_{DS,th}$ for a time longer than the deglitch time $t_{dg(VDS)}$, the protection is triggered.

The V_{DS} monitoring protection is configurable through the VDS_CFG and the VDS_COUNT registers. The only exceptions are the threshold and the enable of the protection, which are configured by the analog pin VDSTH.

Refer to Figure 25 and Figure 26 for the following description.

- Whenever the V_{DS} protection triggers, the power stage is disabled: all the gate drivers are set to LOW with or without the soft-off feature (see Section 5.4) depending on the VDS_SOFT_OFF bit (refer to Section 5.12.4.7). This safe state is maintained until a release request occurs (see below).
- Whenever the V_{DS} protection triggers, the nFAULT open-drain pin is forced low, provided VDS_FAULT_SIG bit is equal to 1 (refer to Section 5.12.4.9).
- Whenever the V_{DS} protection triggers, the FLAG open-drain pin is forced low, provided VDS_FLAG_SIG bit is equal to 1 (refer to Section 5.12.4.11).
- Whenever the V_{DS} protection triggers, VDS_COUNT[7:0] is decremented by 1 (end count is 0x00), provided VDS_COUNT_EN bit is equal to 1 (see Section 5.12.4.7). If VDS_COUNT_EN = 0 the V_{DS} fault events down-counter remains frozen at the current value.
- Whenever the V_{DS} protection triggers and VDS_COUNT[7:0] ≠ 0x00, the fault condition is *temporarily* latched until the expiration of the programmed disable time.
- Whenever the V_{DS} protection triggers and VDS_COUNT[7:0] = 0x00, the fault condition is *permanently* latched.

When the fault condition is temporarily latched, after the programmed disable time (VDS_TDIS[2:0], see Section 5.12.4.7) the device attempts a self-restart (i.e. the fault condition is automatically released). During the whole disable time, the nVDS_HSx_FAULT and nVDS_LSx_FAULT bits of STATUS3 register report which one(s) of the six power MOSFETs caused the *current* V_{DS} fault event (see Section 5.12.4.3).

When the fault condition is permanently latched, the device does not attempt any self-restart. In this case, a user-driven release request is necessary to return to normal operation. In this case, the nVDS_HSx_FAULT and nVDS_LSx_FAULT bits of STATUS3 register report which one(s) of the six power MOSFETs caused the *last* V_{DS} fault event (see Section 5.12.4.3). The value 0 in these bits indicates that a VDS FAULT condition occurred. These bits are restored to the default value upon a user-driven release request.

A user-driven release request can be done in one of the following ways:

- Forcing the EN pin low for at least $t_{EN,pulse\_rel}$.
- Writing a proper command code in the CMD_CLEAR register, as explained in Section 5.12.4.23.

Referring to Figure 26:

- **Entering the standby state releases the fault condition, all device configurations are lost and the registers are restored to their default values.**
- Overwriting VDS_COUNT[7:0] ≠ 0x00 is not a user-driven release request (the effect is simply to preset the down-counter to the new value, but the latch is not released).
- Clearing nVDS_FAULT_L (refer to Section 5.12.4.1) is not a user-driven release request (the fault is not released).
- Disabling nFAULT pin physical signaling by setting VDS_FAULT_SIG = 0 (refer to Section 5.12.4.9) is not a user-driven release request (the fault is not released).
- Disabling FLAG pin physical signaling by setting VDS_FLAG_SIG = 0 (refer to Section 5.12.4.11) is not a user-driven release request (the fault is not released).

At the first V_{DS} fault event, regardless whether the fault condition is temporary or permanently latched, the nVDS_FAULT_L bit in the STATUS1 register is forced low (see Section 5.12.4.1). This bit is cleared by writing a specific command code in the CMD_CLEAR register (see Section 5.12.4.23).

By default, VDS_COUNT[7:0] = 0x00: this means that if the protection is enabled, the device is latched permanently at the first V_{DS} fault event occurrence. The VDS_COUNT register can be written asynchronously at any value to modify the V_{DS} event down-counter value. Once the VDS_COUNT register reaches 0x00, it stays in this condition unless overwritten.

Figure 25. V_{DS} protection down-counter and latch

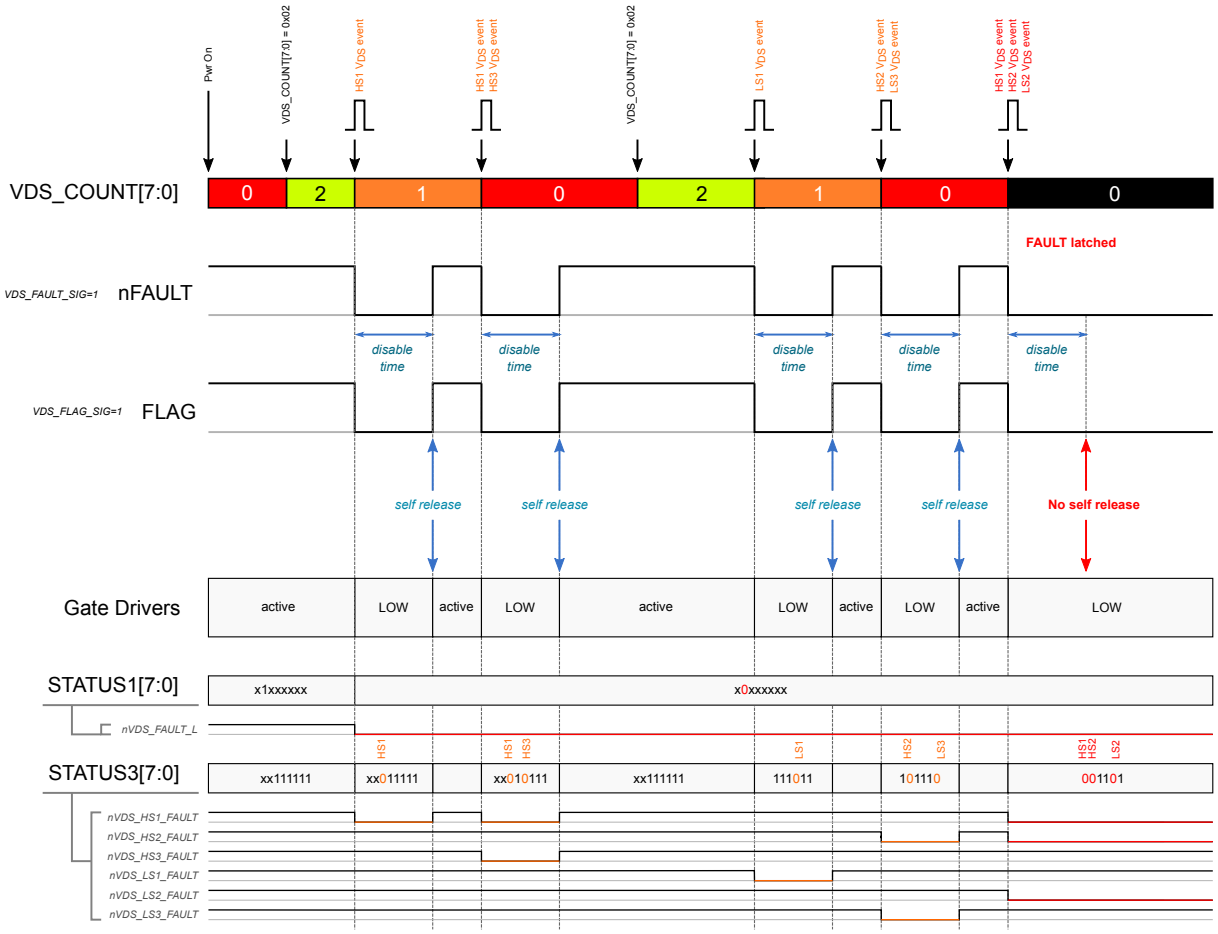
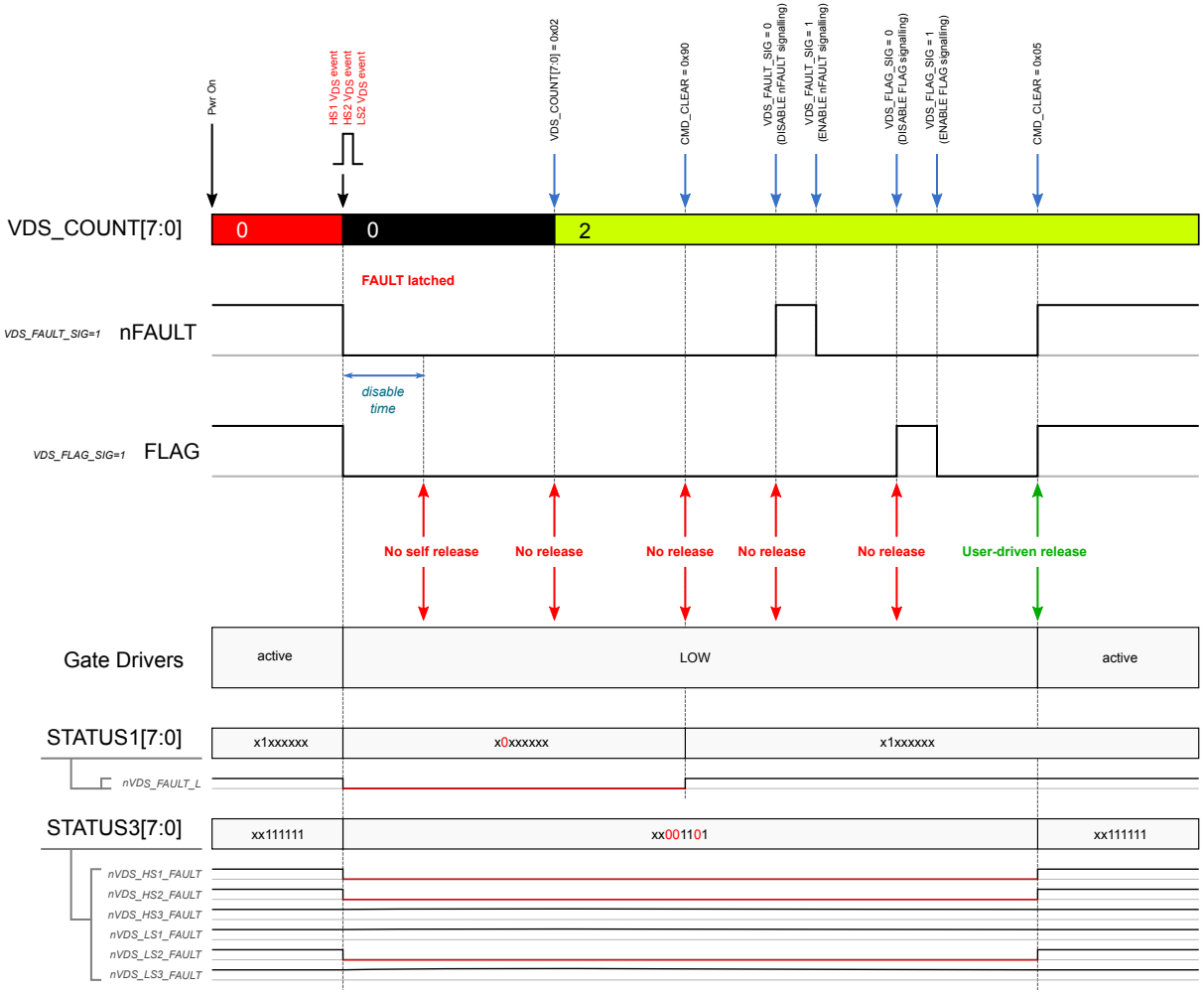


Figure 26. V_{DS} protection release example



5.3 Analog Front-End (AFE)

This section describes the Analog Front End (AFE) integrated into the devices.

The STDRIVE102BP integrates three Programmable Gain Amplifiers (PGA) and three comparators (see Figure 27), while the STDRIVE102P integrates one PGA and one comparator (see Figure 28).

The AFE is supplied by the VDD pin (internally connected) and it is referred to the dedicated AGND pin, to improve immunity against ground noise.

The overall current consumption of the AFE is part of the overall current availability of the 3.3 V internal LDO (I_{DD}), when using external loads connected to VDD.

The AFE allows for flexibility in enabling/disabling each sub-block in accordance with application-specific needs:

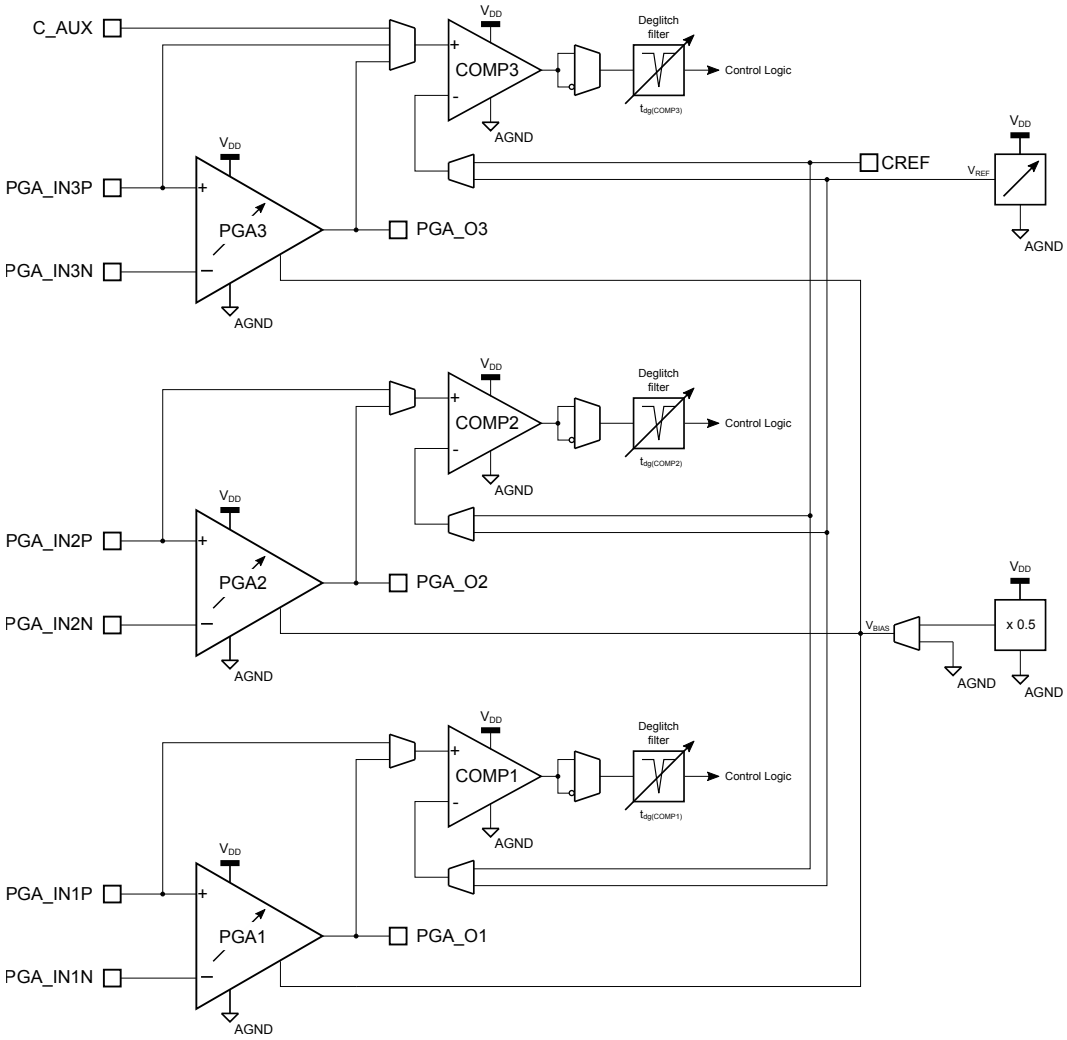
- The complete AFE can be disabled, setting AFE_MASTER_EN = 0 (refer to Section 5.12.4.12).
- Each PGA can be disabled individually, setting PGAx_EN = 0 (refer to Section 5.12.4.13, Section 5.12.4.14 and Section 5.12.4.15).
- Each comparator can be disabled individually, setting COMPx_EN = 0 (refer to Section 5.12.4.13, Section 5.12.4.14 and Section 5.12.4.15).

It is recommended to configure all the parameters of the AFE before enabling the master enable by setting AFE_MASTER_EN = 1 (refer also to Section 5.9.1).

5.3.1 AFE Block Diagram – STDRIVE102BP

The STDRIVE102BP integrates a configurable AFE composed of three Programmable Gain Amplifiers (PGA) and three comparators.

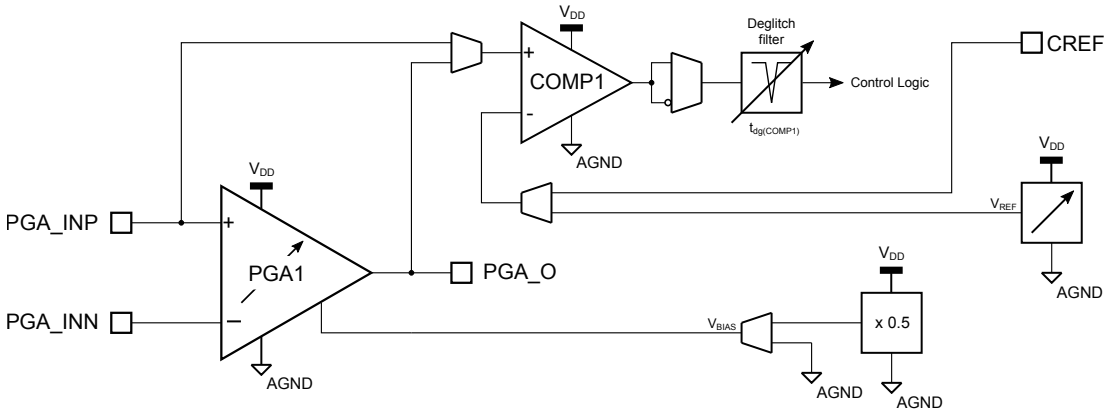
Figure 27. AFE block diagram in STDRIVE102BP



5.3.2 AFE Block Diagram – STDRIVE102P

The STDRIVE102P AFE is a reduced version of the STDRIVE102BP AFE, and it is composed of one PGA and one comparator.

Figure 28. AFE block diagram in STDRIVE102P



5.3.3 PGAs

The programmable gain amplifiers can be used for signal amplification. For example, they can be connected to the shunt resistors of the power stage.

The differential gain G_{PGA} can be selected independently for each PGA of the AFE from four values (4, 8, 16 and 32) using PGAx_GAIN[1:0] (see Section 5.12.4.13).

The mid-point bias of all the PGAs is set to AGND or VDD/2, acting on PGA_REF_SEL; this means that with a differential input of 0 mV, the PGA_O output is biased at 0 mV or VDD/2, respectively.

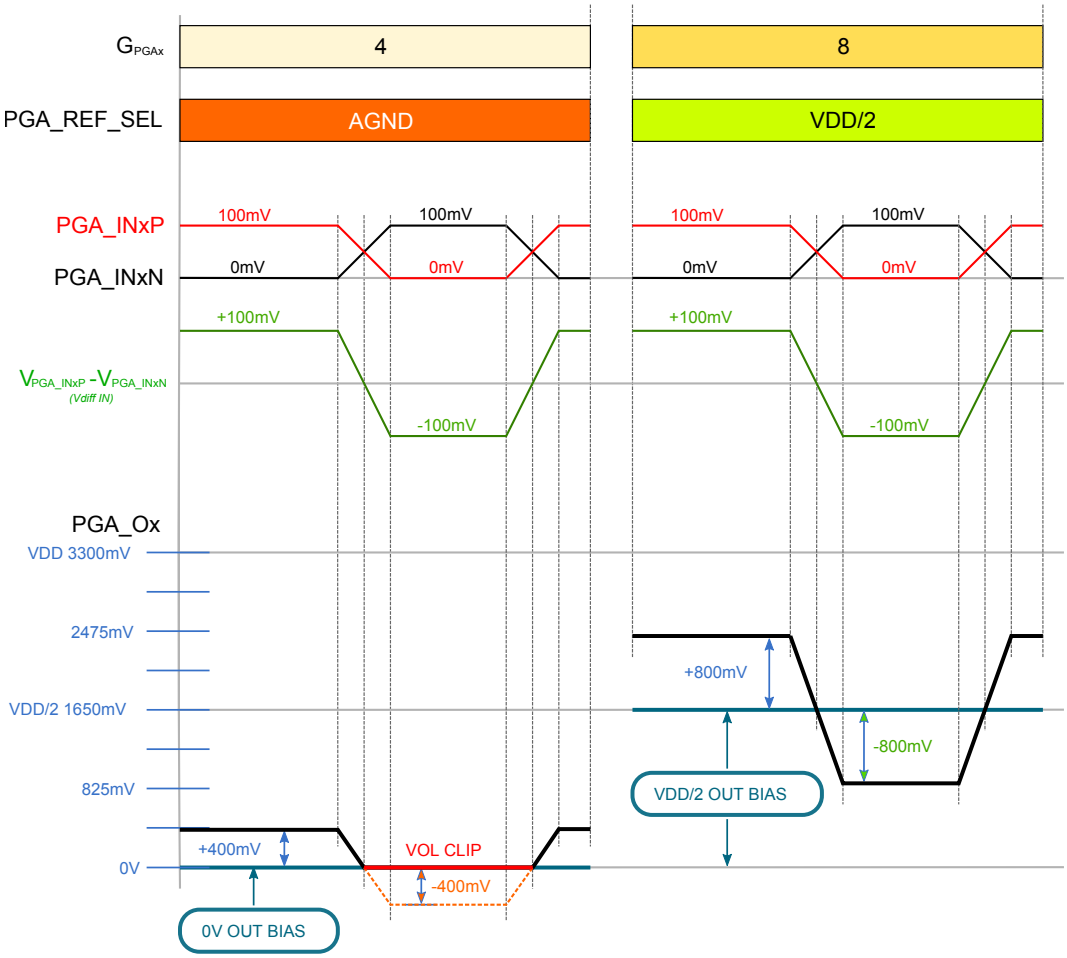
Equation 6

$$V_{PGA\_Ox} = G_{PGAx} \cdot (V_{PGA\_INxP} - V_{PGA\_INxN}) + V_{BIAS} \quad (6)$$

The output bias at 0 mV (AGND) only allows for positive differential input (negative differential input results in the output clipped to V_{OL}), but enables twice the dynamic range of the output. Conversely, choosing output bias at VDD/2 allows both positive and negative differential input with the drawback of the full output dynamic being split between positive and negative input ranges.

In the following Figure 29, an example of two possible configurations of the PGAs is reported for clarity. As shown, biasing the output at VDD/2 allows coping with a bipolar differential input (positive and negative) without any clipping and with a higher gain.

Figure 29. **PGA gain and output bias example**



5.3.4 AFE reference voltage generator

A common block generates the internal reference voltage used by the comparators.

The COMP_REF_SEL[3:0] bits define the reference voltage (refer to Section 5.12.4.12) which can be applied to the inverting inputs according to the COMPx_INN bit.

An internally generated single voltage threshold is shared by all comparators in the AFE.

5.3.5 Comparators and protection circuitry

With reference to Figure 27 and Figure 28, the internal connection of the inputs of each comparator x can be configured in different modes (refer to Section 5.12.4.13, Section 5.12.4.14 and Section 5.12.4.15):

- COMPx_INN bit selects the signal feeding the inverting input of the comparator x; two options are possible:
  - Inverting input connected to the CREF input pin.
  - Inverting input connected to the AFE internal reference voltage generator (refer to Section 5.3.4).
- COMPx_INP bit selects the signal feeding the non-inverting input of the comparator x:
  - Non-inverting input connected to the respective PGA_INxP input pin. In this case, the signal applied to this pin feeds both the PGA and the comparator.
  - Non-inverting input connected to the respective PGA_Ox output pin. In this case, the signal applied to the comparator is the result of the PGAx amplification.

  An additional option is only available for comparator 3 in the STDRIVE102BP:
  - Non-inverting input connected to the C_AUX input pin.

The output of each comparator passes through a logic defining if the direct or inverted signal is used (selected by COMPx_INV bit) and then it passes into a deglitch filter. Filter duration is adjusted through COMPx_TDG[1:0] (refer to Section 5.12.4.17, Section 5.12.4.18 and Section 5.12.4.19).

Finally, the deglitched output is provided to the control logic.

Figure 30. Comparator 1 - fault logic

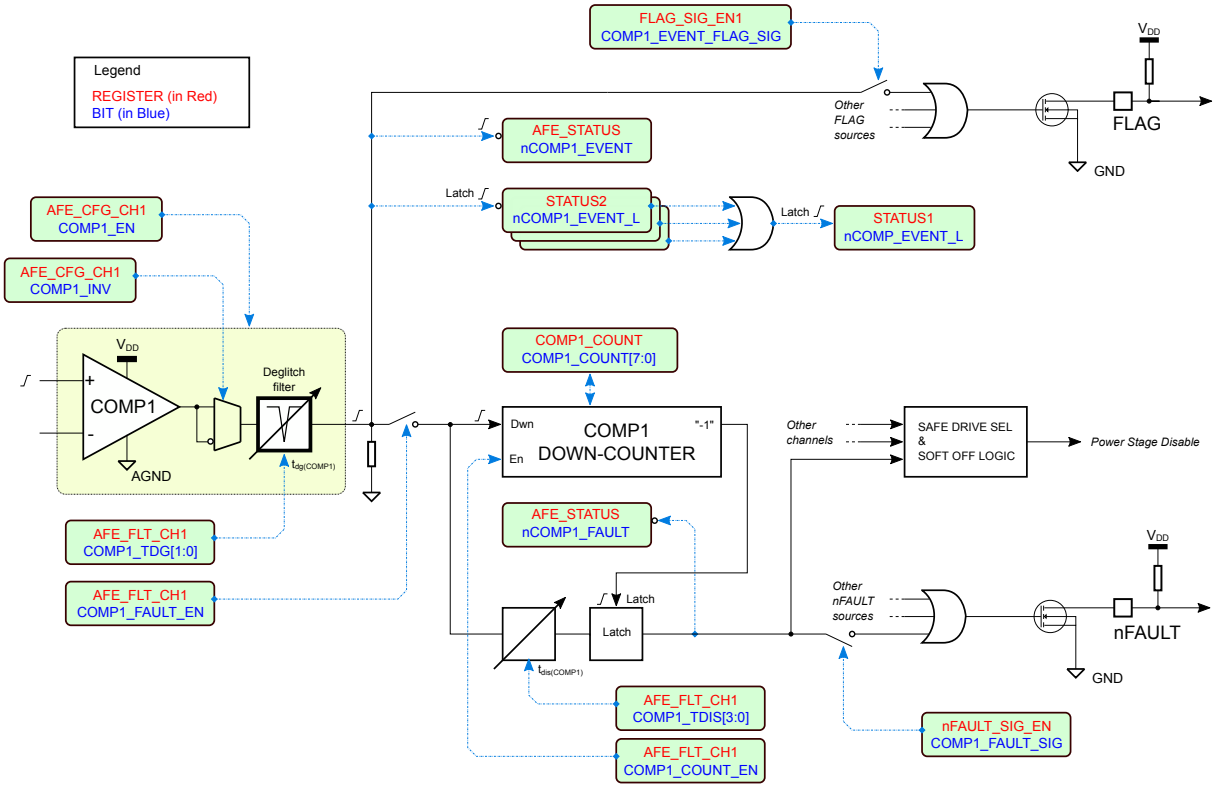


Figure 30 represents a behavioral model of the logic downstream of the deglitch filter. The figure and the following description include only the chain relating to comparator 1, but they can be extended to comparators 2 and 3 for STDRIVE102BP.

- At the first occurrence of a *detected event* (i.e. deglitch filter output asserted high) by comparator 1, nCOMP1_EVENT_L and nCOMP_EVENT_L bits are latched at 0 (refer to Section 5.12.4.2 and Section 5.12.4.1).
- While an event detected by comparator 1 is present (deglitch filter output asserted high), nCOMP1_EVENT bit is 0 (refer to section Section 5.12.4.4) and reverts to 1 as soon as the detected event is over (deglitch filter output asserted low).
- On STDRIVE102BP only, the state of nCOMP1_EVENT bit can be reported on the FLAG open drain pin by setting COMP1_EVENT_FLAG_SIG = 1. Note that other warning events can be reported, in logic-OR, on the FLAG pin too (refer to Section 5.12.4.10 and Section 5.12.4.11).

A detected event can generate a fault condition setting COMP1_FAULT_EN = 1 (refer to Section 5.12.4.17). This fault condition triggers different actions on the gate drivers.

- Whenever a fault event by comparator 1 is triggered, COMP1_COUNT[7:0] is decremented by 1 (end count is 0x00), provided COMP1_COUNT_EN = 1 (see Section 5.12.4.17). If COMP1_COUNT_EN = 0 instead, the comparator 1 fault event down-counter remains frozen at the current value.
- Whenever a fault event by comparator 1 is triggered and COMP1_COUNT[7:0] ≠ 0x00, the fault condition is *temporarily* latched until the deglitch filter output is asserted high and after the disable time associated to comparator 1 has passed.
- Whenever a fault event by comparator 1 is triggered and COMP1_COUNT[7:0] = 0x00, the fault condition is *permanently* latched.
- When the fault condition is temporarily latched and the deglitch filter output is asserted low, after the programmed disable time (COMP1_TDIS[3:0], see section Section 5.12.4.17) the fault condition is self-released.

A permanently latched fault can be released only with a user-driven request:

- Forcing the EN pin low for at least $t_{EN,pulse\_rel}$.
- Writing a proper command code in the CMD_CLEAR register, as explained in Section 5.12.4.23.

Note that:

- **Entering the standby state releases the fault condition, all device configurations are lost and the registers are restored to their default values.**
- Overwriting COMP1_COUNT[7:0] ≠ 0x00 is not a user-driven release request (the effect is simply to preset the down-counter to the new value, but the fault is not released).
- Clearing nCOMP_EVENT_L is not a user-driven release request (the fault is not released).
- Clearing nCOMP1_EVENT_L is not a user-driven release request (the fault is not released).
- Disabling nFAULT pin physical signaling by setting COMP1_FAULT_SIG bit = 0 (refer to Section 5.12.4.9) is not a user-driven release request (the fault is not released).
- Disabling FLAG pin physical signaling by setting COMP1_EVENT_FLAG_SIG bit = 0 (refer to Section 5.12.4.10) is not a user-driven release request (the fault is not released).
- Disabling the fault event generation by setting COMP1_FAULT_EN bit = 0 is not a user-driven release request (the fault is not released).
- Disabling the comparator 1 by setting COMP1_EN = 0 is not a user-driven release request (the fault is not released).
- Disabling the AFE by setting AFE_MASTER_EN = 0 is not a user-driven release request (the fault is not released).

Figure 31. Comparator 1 - fault latching example

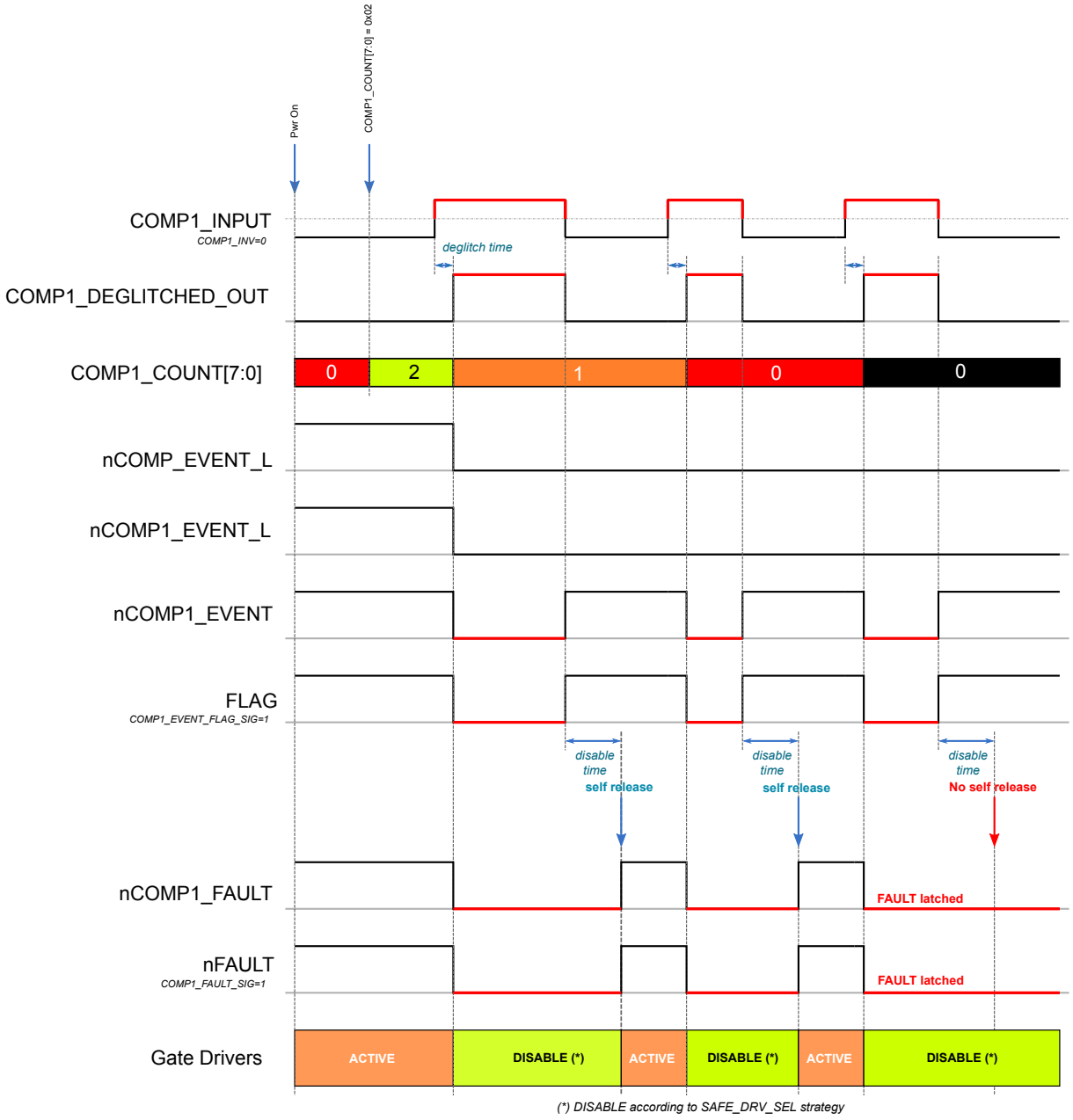
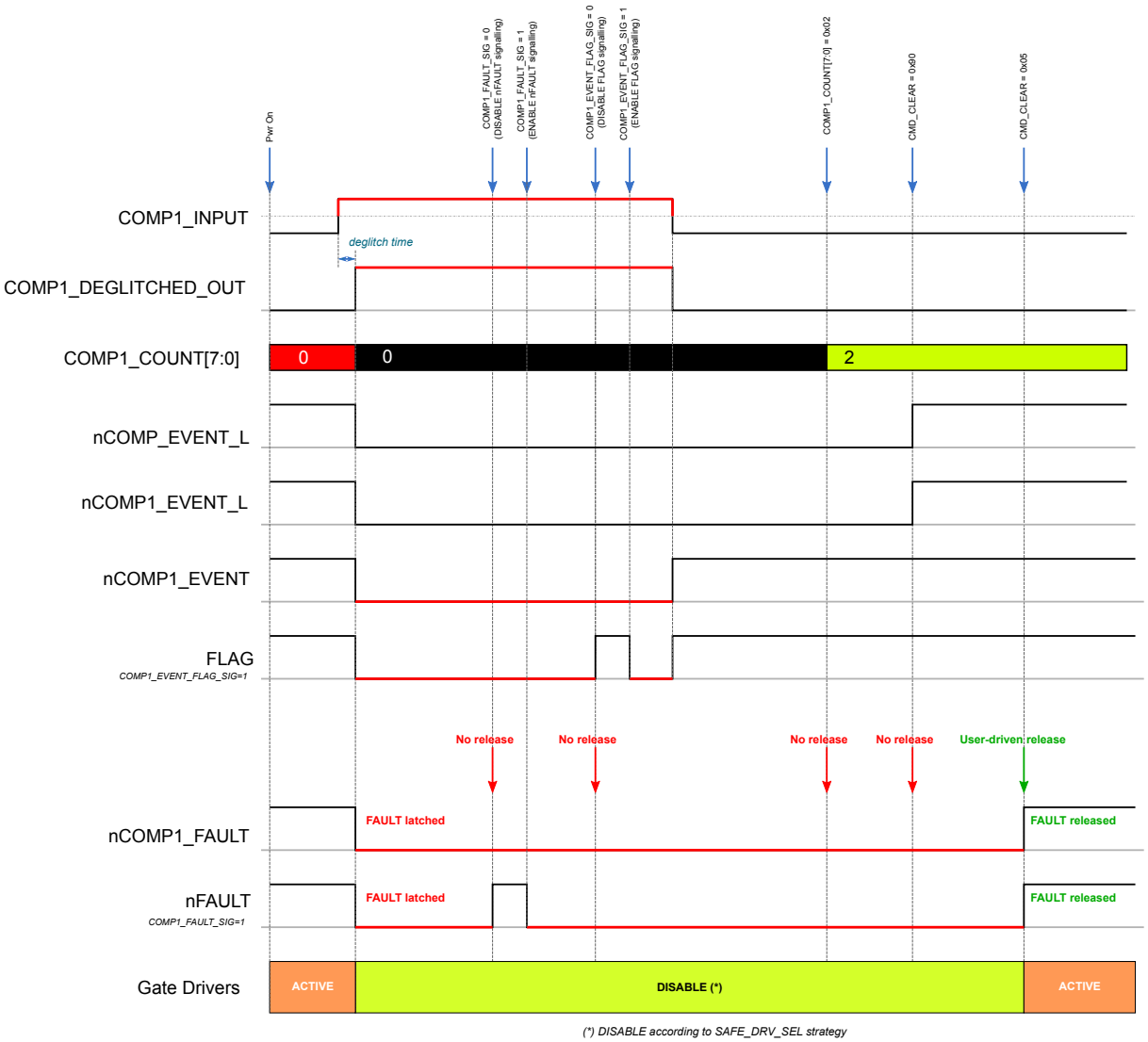


Figure 32. **Comparator 1 - fault release example**



The state of nCOMP1_FAULT bit can be routed on the nFAULT open drain pin by setting COMP1_FAULT_SIG = 1. Note that other fault events can be routed, in logic-OR, on the nFAULT pin (refer to Section 5.12.4.9).

The gate drivers' protection strategy in case of a fault event on the AFE comparators is selected through SAFE_DRV_SEL[1:0] bits (refer to Section 5.12.4.16 and Table 67) from four different safe states:

- "All HS & LS": the device turns off all the external MOSFETs, regardless of which comparator has generated the fault event.
- "Matched HS & LS": the device turns off only the external high-side and low-side MOSFETs of the half-bridge <x> corresponding to the comparator <x> generating the event.
  This option is available only for the STDRIVE102BP (refer to Section 5.12.4.16).
- "All HS": the device turns off all the external high-side MOSFETs, regardless of which comparator has generated the fault event.
  No action is taken on the low-side MOSFETs: the device drives them according to the related digital inputs.
- "Bypass": no action is taken on the power stage.

Moreover, it is possible to impose a soft turn-off (refer to Section 5.4) setting COMPx_SOFT_OFF = 1 (refer to Section 5.12.4.16 and Table 66).

5.4 Soft turn-off

When the V_{DS} monitoring protection or the AFE comparators are triggered, it could indicate a severe overcurrent event on the power stage (for example, short-circuit). In this case, the soft turn-off function reduces the sink current of the gate drivers, avoiding a fast dI/dt transition on the power stage.

The functionality is enabled by default but can be disabled by setting VDS_SOFT_OFF = 0 (refer to Section 5.12.4.7).

The soft turn-off functionality can also be invoked in case the request to switch off the power stage comes from the AFE comparators, rather than the V_{DS} monitoring protection (refer to Section 5.3.5 for details). Also in this case, the functionality is enabled by default on all three comparators: COMPx_SOFT_OFF bit = 1, where x represents the comparator of the AFE triggering the soft turn-off. The soft turn-off feature can be disabled on a specific comparator x by setting the related COMPx_SOFT_OFF bit = 0 (refer to Section 5.12.4.16 and Table 66).

If the soft turn-off is enabled, the drivers turn off the power MOSFETs using the current $I_{GATE,off(SO)}$, which is a fraction of the $I_{GATE,off}$ current programmed by the IGATE[3:0] bits (see Table 34). Consequently, the $t_{cc,off(SO)}$ is increased with respect to the $t_{cc,off}$ programmed by the TCC[3:0] bits, to ensure a correct discharge of the MOSFETs' gates (refer to Table 33). After this time, the current capability of the drivers turns to $I_{hold,off}$.

5.5 3FG logic (STDRIVE102BP only)

Referring to Figure 27, the deglitched outputs of the three comparators feeding the control logic also feed the "3FG Logic" function, which consists of a three-input XOR.

The output of the logic XOR can be reported on the FLAG pin by setting the 3FG bit to 1, see Section 5.12.4.10.

When the output of the XOR logic is 1, the open drain is enabled and the FLAG pin is pulled low. When the output of the XOR logic is 0, the open drain is released and the pull-up resistor brings the FLAG pin high.

Table 11. 3FG XOR function truth table

COMP1_OUT	COMP2_OUT	COMP3_OUT	XOR output	FLAG pin
0	0	0	0	High Open-drain released
0	0	1	1	Low Open-drain enabled
0	1	0	1	Low Open-drain enabled
0	1	1	0	High Open-drain released
1	0	0	1	Low Open-drain enabled
1	0	1	0	High Open-drain released
1	1	0	0	High Open-drain released
1	1	1	1	Low Open-drain enabled

5.6 Thermal shutdown and thermal warning

The STDRIVE102BP/P has a thermal shutdown protection. If the junction temperature of the device exceeds the thermal shutdown threshold $T_{j(THSD)}$, the driver turns off the external power MOSFETs and, after a $t_{cc,off}$, the linear regulators and the charge pump are also disabled.

If THSD_FAULT_SIG bit = 1 (see Section 5.12.4.9), the thermal shutdown event is reported on the nFAULT pin, which is forced low.

Turning off the 12 V linear regulator results in an undervoltage and “power-good” failure, regardless of the actual voltage on VCC pin.

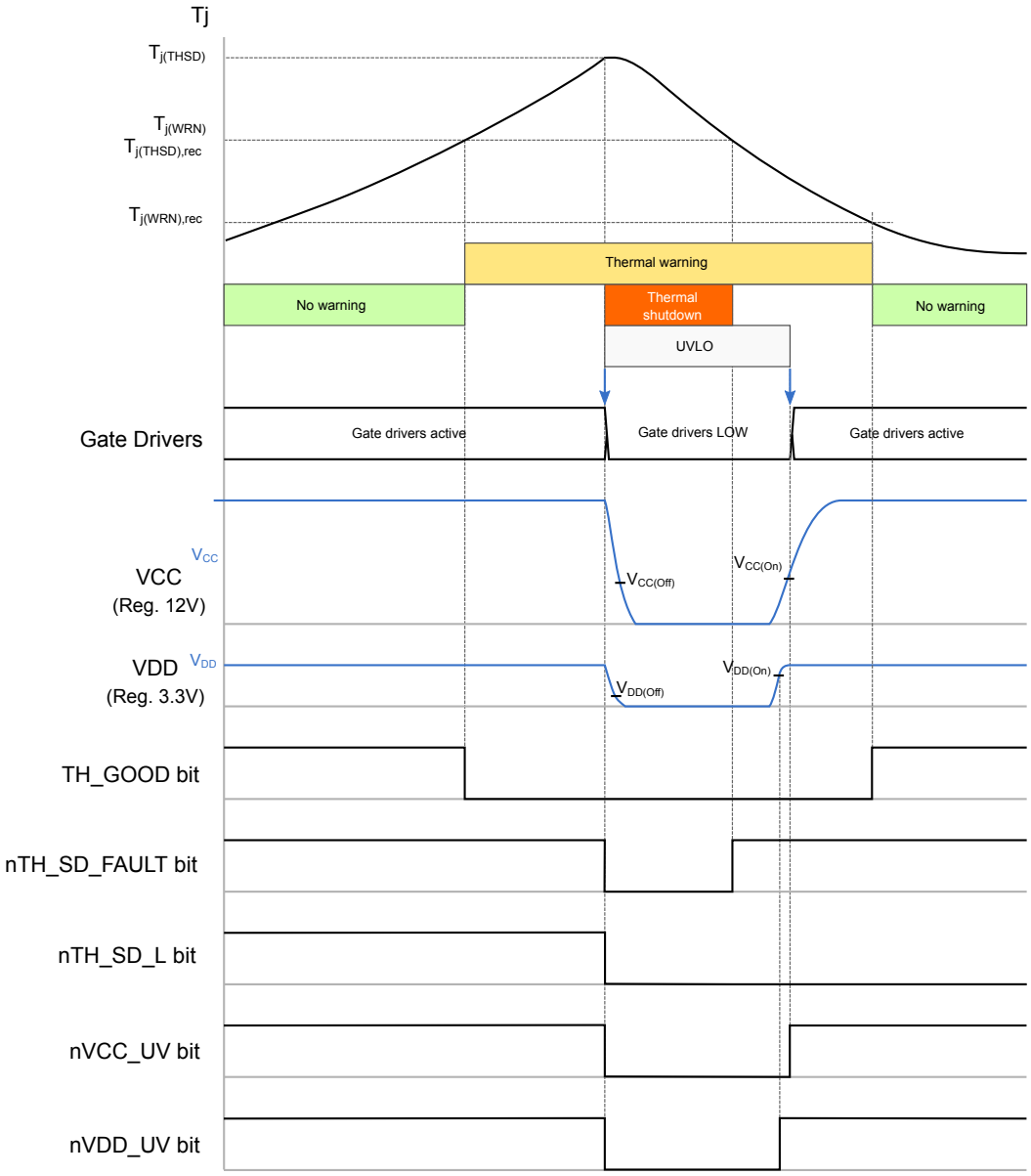
Note that the blocks generating the supply of the drivers (V_{CC} and V_{BOOT}) are turned off. Therefore, the supplies slowly decrease according to the external capacitor present on the VCC and VBOOT pins. When the capacitors are fully discharged, the external MOSFETs are kept off only by the 100 kΩ resistors present on each driver’s output.

Since the VDD regulator is switched off, all the pull-up resistors referred to this supply cannot operate correctly. If they are required to be operative also during a thermal shutdown event, they must be connected to another external supply. For example, the pull-up resistor on the nFAULT pin or on the SDO for SPI communication must use an external supply if there is a need to read the registers during thermal shutdown.

As soon as the temperature of the device decreases below the $T_{j(THSD),rec}$ temperature, all the functional blocks are enabled again. According to the duration of the thermal transient, the regulators and their different supplies (V_{BOOT}, V_{CC} and V_{DD}) can be in an UVLO condition. In this case, the drivers become active only after all the supplies rise above UVLO thresholds.

Before entering the thermal shutdown condition, the device generates a warning event when the junction temperature exceeds $T_{j(WRN)}$. This event can be monitored through the TH_GOOD bit (see Section 5.12.4.2) and, on the STDRIVE102BP only, it can be reported on the FLAG pin, by setting nTH_GOOD_FLAG_SIG bit = 1, see Section 5.12.4.10). The thermal warning condition expires when the device temperature returns below $T_{j(WRN),rec}$.

Figure 33. **STDRIVE102BP/P thermal thresholds**



5.7 Protection management summary

A summary of the protections and the effects on the functional blocks of the device can be found in Table 12. The protections embedded in the device guarantee safe operation of the gate drivers and the external power stage. The protections include:

- Undervoltage lock-out (UVLO) for:
  - 12 V LDO regulator: V_{CC} supply (Section 5.1.1)
  - 3.3 V LDO regulator: V_{DD} supply (Section 5.1.2)
  - Charge pump: V_{BOOT} - V_M supply (Section 5.1.3)
- V_{DS} monitor protection (Section 5.2.7)
- AFE comparators protection (Section 5.3.5)
- Thermal shutdown protection (Section 5.6)

When a protection is triggered, the nFAULT pin is set low (provided the signaling is enabled in nFAULT_SIG_EN register, see Section 5.12.4.9) and is kept low as long as the fault condition is present, including the disable time when provided by the protection. Depending on the fault condition, one or more functional blocks are disabled.

Table 12. Device protections summary

Protection	Condition	Driver HS	Driver LS	12 V LDO	3.3 V LDO	Charge pump	Release condition	Notes
V_{CC} UVLO	$V_{CC} < V_{CC(Off)}$	LOW	LOW	Active	Active	Active	$V_{CC} > V_{CC(On)}$	$V_{CC(Off)}$ and $V_{CC(On)}$ selectable by UV_SEL bit
UVLO V_{DD}	$V_{DD} < V_{DD(Off)}$	LOW	LOW	Active	Active	Active	$V_{DD} > V_{DD(On)}$	The AFE could not work properly, drivers are disabled
Charge pump UVLO	$(V_{BOOT} - V_M) < V_{CPump(Off)}$	LOW	Active	Active	Active	Active	$(V_{BOOT} - V_M) > V_{CPump(On)}$	$V_{CPump(Off)}$ and $V_{CPump(On)}$ selectable by UV_SEL bit
Thermal shutdown	$T_j > T_{j(THSD)}$	LOW (1)	LOW (1)	Disable	Disable	Disable	$T_j < T_{j(THSD),rec}$	
V_{DS} monitor	$V_{DS} > V_{DS,th}$	LOW	LOW	Active	Active	Active	Refer to Section 5.2.7	
AFE comparators	According to the AFE configuration Refer to Section 5.3.5	According to SAFE_DRV_SEL[1:0] (see Section 5.12.4.16)		Active	Active	Active	Refer to Section 5.3.5	
V_{CC} Warning	$V_{CC} < V_{P\_GOOD(Off)}$	Active	Active	Active	Active	Active	$V_{CC} > V_{P\_GOOD(On)}$	Warning only, $V_{P\_GOOD(Off)}$ and $V_{P\_GOOD(On)}$ selectable by VCC_GOOD_SEL bit
Thermal warning	$T_j > T_{j(WRN)}$	Active	Active	Active	Active	Active	$T_j < T_{j(WRN),rec}$	Warning only

1. *The drivers can force the MOSFETs' gates to LOW only if V_{CC} and V_{BOOT} supplies are present. Thermal shutdown turns off both the 12 V regulator and the charge pump, so the gate drivers' ability to turn off the MOSFET may be affected.*

Referring to Table 12, the state of the functional blocks can be in three different conditions:

- **Active**: the block is fully operative.
- **LOW** (gate drivers only): despite the digital inputs, the drivers are set to LOW and they sink current. Therefore, the external power MOSFET is turned off, regardless of the digital input applied.
- **Disable**: the functional block is disabled.

5.8 EN and nFAULT pins management

The basic block diagram for the EN and nFAULT management is reported in Figure 34.

The nFAULT pin is an open-drain output that can be used to signal the failure conditions of the device, triggered by the internal protections.

The nFAULT_SIG_EN register (see Section 5.12.4.9) selects which failure event is to be reported on the nFAULT pin:

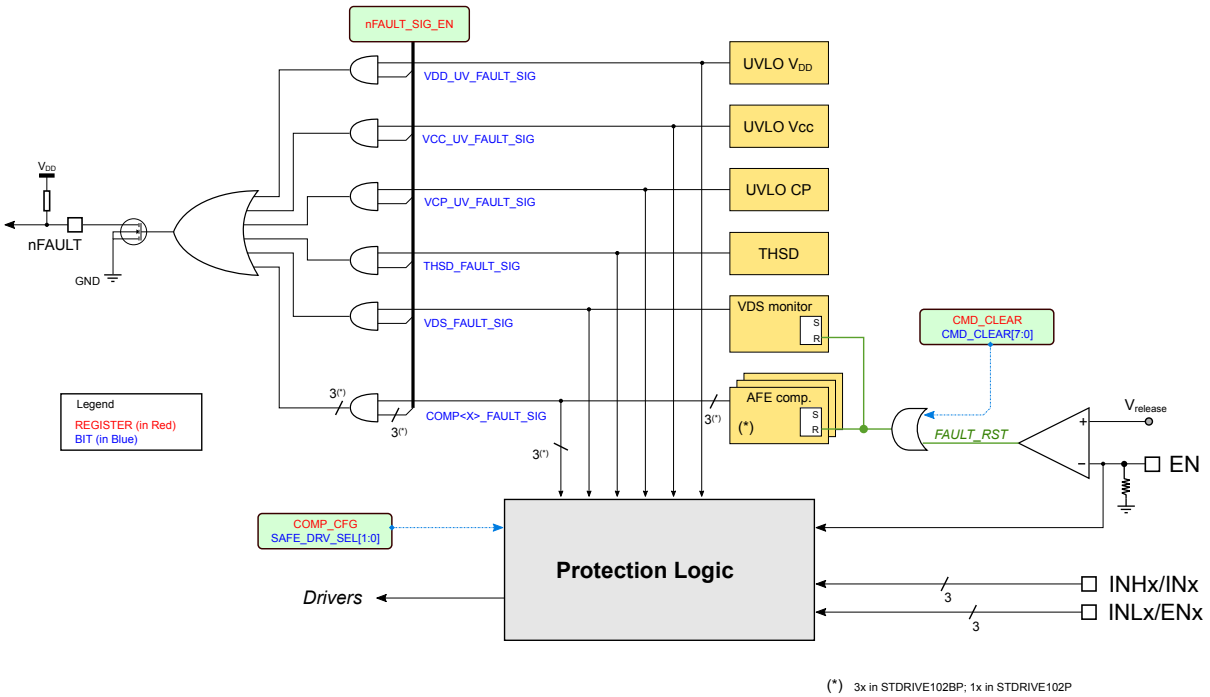
- V_{DD} UVLO
- V_{CC} UVLO
- Charge Pump UVLO
- Thermal Shutdown
- V_{DS} monitoring
- AFE comparators

By default, all these bits are set to 1, meaning that all the protections are reported on the open-drain pin nFAULT.

The failure events are also sent to the protection logic, which manages the state of the gate drivers, implementing the behavior described in Table 12.

The EN pin is the master enable of the drivers and has a comparator which detects if its input voltage falls below the release threshold $V_{release}$ in order to release the latched faults. The same effect can be achieved by writing the proper command in the CMD_CLEAR register, as explained in Section 5.12.4.23.

Figure 34. Enable and fault management basic block diagram



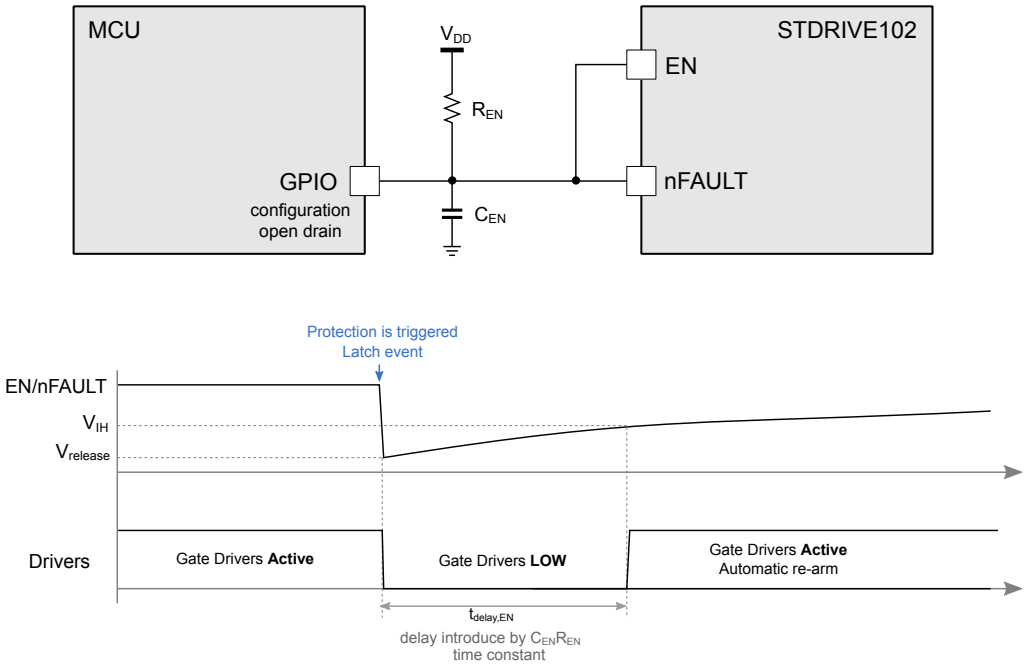
5.8.1 Automatic re-arm using the nFAULT pin

While the undervoltage and thermal protection are self-rearming (i.e. the device resumes normal operation when the triggering condition is removed), the V_{DS} monitoring and the AFE comparators protections can latch the power stage. In case one of these protections triggers and the fault condition is *permanently* latched (see Section 5.2.7 and Section 5.3.5), the device stays in safe state until the fault condition is released by user-driven release request.

One of the possible methods to release the latched fault is to force the EN pin below the $V_{release}$ threshold. Therefore, it is possible to automatically release the fault by connecting the EN and the nFAULT pins as shown in Figure 35.

This hardware configuration can be used in addition to the internal configuration available in the STDRIVE102BP/P, which is accessible through the SPI.

Figure 35. **Automatic re-arm using EN and nFAULT pins**



When a protection is triggered, provided the respective signaling enable pin is set (see Section 5.12.4.9), the nFAULT open drain drives the EN pin low and its voltage falls below the $V_{release}$ threshold, releasing the latched condition.

To set the re-arm timing of the power stage, a delay can be introduced using a capacitor C_{EN} together with the pull-up resistor R_{EN}. If the EN pin is directly driven by a control logic, care must be taken to use an open drain configuration to avoid any conflict.

It is important to consider that the EN pin has an internal pull-down resistor $R_{PD,EN}$ so the voltage of the EN pin at the end of the rising transient is:

Equation 7

$$V_{EN,high} = V_{DD} \cdot \frac{R_{PD,EN}}{R_{PD,EN} + R_{EN}} \tag{7}$$

The time constant of the rising transient is:

Equation 8

$$\tau_{EN} = \frac{R_{EN} \cdot R_{PD,EN}}{R_{EN} + R_{PD,EN}} \cdot C_{EN} \tag{8}$$

Using the values calculated in Eq. (7) and in Eq. (8), the delay time required to re-arm the power MOSFETs, after a FAULT condition can be found as:

Equation 9

$$t_{delay,EN} = \tau_{EN} \cdot ln\left(\frac{V_{EN,high} - V_{release}}{V_{EN,high} - V_{IH}}\right) \tag{9}$$

According to Eq. (7), the value of R_{EN} should be chosen to be several times smaller than $R_{PD,EN}$ to avoid an excessive drop in the high level on the EN pin ($V_{EN,high}$). Under this assumption, it is possible to approximate Eq. (9) as:

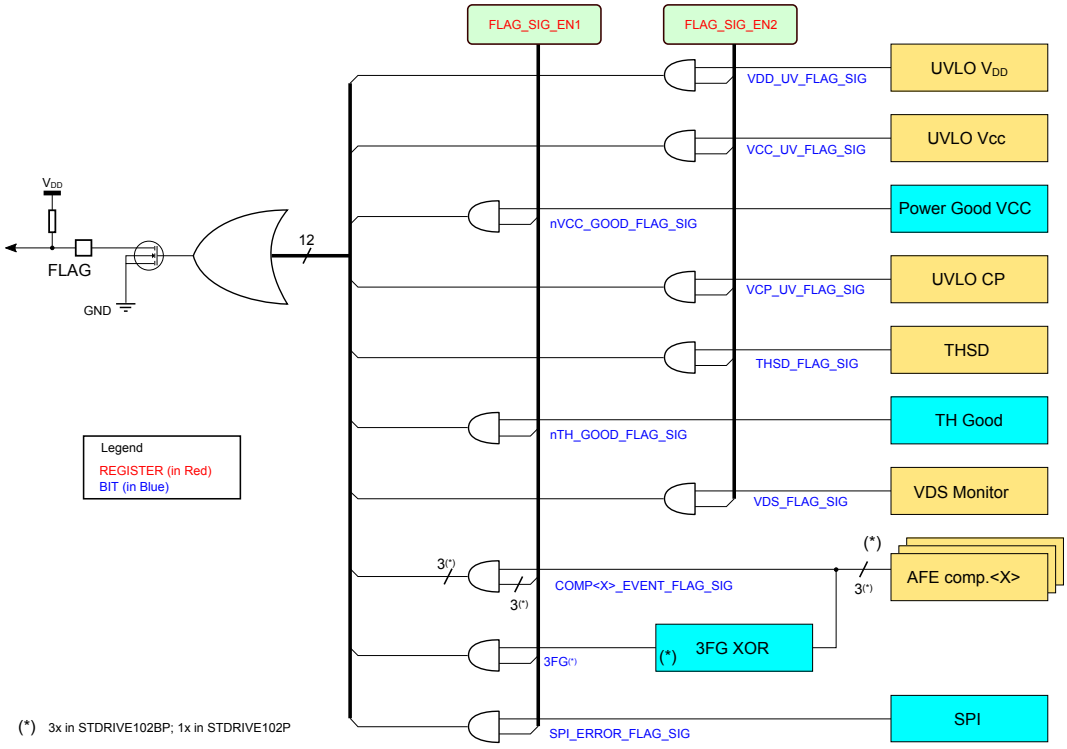
Equation 10

$$t_{delay,EN} \cong R_{EN} \cdot C_{EN} \cdot ln\left(\frac{V_{DD} - V_{release}}{V_{DD} - V_{IH}}\right) \tag{10}$$

5.8.2 FLAG pin (STDRIVE102BP only)

The STDRIVE102BP features the FLAG pin, an open-drain output that can be flexibly configured to signal one or more events. These are brought together using a logic-OR which drives the open-drain n-MOS connected to the FLAG pin.

Figure 36. FLAG pin management basic block diagram



Each event can be gated through FLAG_SIG_EN1 and FLAG_SIG_EN2 registers (detailed in Section 5.12.4.10 and Section 5.12.4.11), so that the FLAG pin signal can be associated with one or different events:

- By setting COMPx_EVENT_FLAG_SIG = 1, the FLAG pin reports the detected event by AFE comparator x. This allows monitoring the status of the comparator x, after the deglitch filter.
- By setting 3FG = 1, the FLAG pin reports the output signal of the 3FG logic (see Section 5.5).
- By setting SPI_ERROR_FLAG_SIG = 1, the FLAG pin reports an error related to the SPI communication protocol.
- By setting nTH_GOOD_FLAG_SIG = 1, the FLAG pin reports the occurrence of a thermal warning condition.
- By setting THSD_FLAG_SIG = 1, the FLAG pin reports the occurrence of a thermal shutdown condition.
- By setting nVCC_GOOD_FLAG_SIG = 1, the FLAG pin reports a warning related to the VCC rail.
- By setting one of VCC_UV_FLAG_SIG, VDD_UV_FLAG_SIG or VCP_UV_FLAG_SIG = 1, the FLAG pin reports the corresponding undervoltage fault condition.
- By setting VDS_FLAG_SIG = 1, the FLAG pin reports the V_{DS} monitoring fault condition.

5.8.3 Automatic disable using FLAG pin

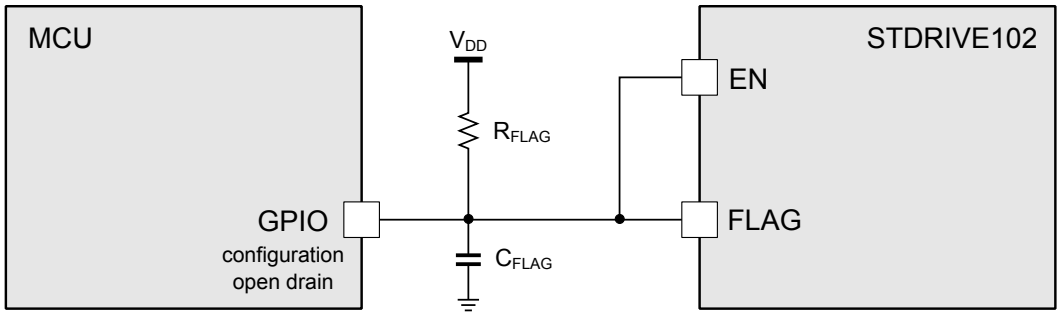
Similarly to the nFAULT pin, the FLAG pin can be exploited to temporarily disable and automatically re-arm the device upon the occurrence of one or more events, configurable through the FLAG_SIG_EN1 and FLAG_SIG_EN2 registers.

It is possible to connect the EN and the FLAG pins as shown in Figure 37. A capacitor can be added to set a delay for the enabling of the drivers. The delay is determined by the following formula:

Equation 11

$$t_{delay,EN} \cong R_{FLAG} \cdot C_{FLAG} \cdot ln\left(\frac{V_{DD}}{V_{DD} - V_{IH}}\right) \quad (11)$$

Figure 37. FLAG and EN management



5.9 Device power-up

The power-up sequence starts at the rising edge of the main supply applied on the VS pin, supposing that the nSTBY pin is forced high.

In case the VM and VS pins are supplied by different voltage sources, the VM voltage must be applied before the VS voltage. This sequence is not important if the nSTBY pin is kept low and it is raised after the supplies are stable.

The internal 5 V regulator begins to charge the capacitor on the LGC_CAP pin. When the POR threshold is met, the internal logic starts to operate and initialize all the internal circuits. During this phase the nFAULT signal is kept low.

Then, the regulators are enabled and they can charge their external bypass capacitors. Most of the time required by the device to be operative is due to the charge of the external bypass capacitor. Depending on the capacitor value, the current capability of the LDO regulators, and the charge pump, this may require hundreds of microseconds.

The typical sequence for the supplies is:

- VDD UVLO is released (V_{DD} > $V_{DD(On)}$): the AFE is operative.
- VCC UVLO is released (V_{CC} > $V_{CC(On)}$): the low-side drivers are operative.
- Charge pump UVLO is released (V_{BOOT} - V_M > $V_{CPump(On)}$): the high-side drivers are operative.

Following the release of all the UVLO protections, the nFAULT pin is set high by the external pull-up resistor.

5.9.1 Recommended power-up procedure

The following procedure can be followed to power up the device and bring it to the fully operative condition following a controlled sequence:

1. Set EN pin low.
2. Set nSTBY pin low.
3. Set ENx/INLx and INx/INHx pins low.
4. Apply main supply (VM and VS).
5. Set nSTBY pin high.
6. As soon as the supplies are stable, the nFAULT pin is released and goes high. It is recommended but not mandatory to clear the status registers:
   a. Write CMD_CLEAR register with command code 0x68 (clear RESET_STATE bit).
   b. Write CMD_CLEAR register with command code 0x95 (clear undervoltage events during power-up transient).
   c. Read STATUS1, STATUS2, STATUS3, and AFE_STATUS, checking that no other faults are present.
7. Configure nFAULT physical signaling:
   a. Write nFAULT_SIG_EN register as needed.
8. Configure FLAG physical signaling (STDRIVE102BP only):
   a. Write FLAG_SIG_EN1 register as needed.
   b. Write FLAG_SIG_EN2 register as needed.
9. Write CMD_LOCK register with command code 0x4B to unlock the registers.
10. Configure system and drivers:
    a. Write DRV_CFG register as needed.
    b. Write SYS_CFG register as needed.
11. Configure AFE:
    a. Write PGA_REF_SEL and COMP_REF_SEL[3:0] as needed. Keep AFE_MASTER_EN = 0.
    b. Write AFE_CFG_CH1, AFE_CFG_CH2 (STDRIVE102BP only), and AFE_CFG_CH3 (STDRIVE102BP only) as needed.
    c. Write COMP_CFG as needed.
    d. Write AFE_FLT_CH1, AFE_FLT_CH2 (STDRIVE102BP only), and AFE_FLT_CH3 (STDRIVE102BP only) as needed.
    e. Write PGA_REF_SEL and COMP_REF_SEL[3:0] as needed and AFE_MASTER_EN = 1.
12. Write CMD_LOCK register with command code 0x71 to lock the registers.
13. Preset fault down-counters:
    a. Write VDS_COUNT[7:0] as needed.
    b. Write COMP1_COUNT[7:0], COMP2_COUNT[7:0] (STDRIVE102BP only), and COMP3_COUNT[7:0] (STDRIVE102BP only) as needed.
14. Read STATUS1, STATUS2, STATUS3, and AFE_STATUS to check the device status.
15. Set EN pin high.

5.10 Standby and wake-up

The standby pin is active low (nSTBY low: standby mode, nSTBY high: normal mode).

The standby mode strongly reduces the current consumption down to I_{STBY}. The transition to standby mode, which takes a t_{STBY} to be completed, follows a sequence of steps managed by the internal logic:

1. Before being disabled, all the drivers turn off the external MOSFETs. Then, the V_{GS} of the external MOSFET is kept low by the internal 100 kΩ pull-down resistor, present on the GHSx/GLSx pins.
2. The AFE is disabled.
3. Both the linear regulators and the charge pump are switched off to reduce current consumption.
4. Open-drain pins are released.
5. The internal logic enters the standby state, and most of its circuitries are disabled.

It is always recommended to force nSTBY = 0 before removing the main supply VS in the turn-off sequence of the device.

When the nSTBY pin returns high, the device leaves the standby mode following the wake-up sequence:

1. Internal logic is initialized, and all the registers are reset to their default value.
2. The linear regulators and the charge pump are turned on.

The device can be considered operative as soon as its supplies (V_{CC}, V_{DD}, and V_{BOOT}) are stable above the respective UVLO thresholds (nFAULT open-drain released).

5.11 SPI interface

The integrated serial peripheral interface (SPI) is used for communication between the host MCU (always controller) and the device (always target). The SPI uses four signals: chip select (nCS, active low), serial clock (CLK), serial data input (SDI also known as MOSI) and serial data output (SDO also known as MISO).

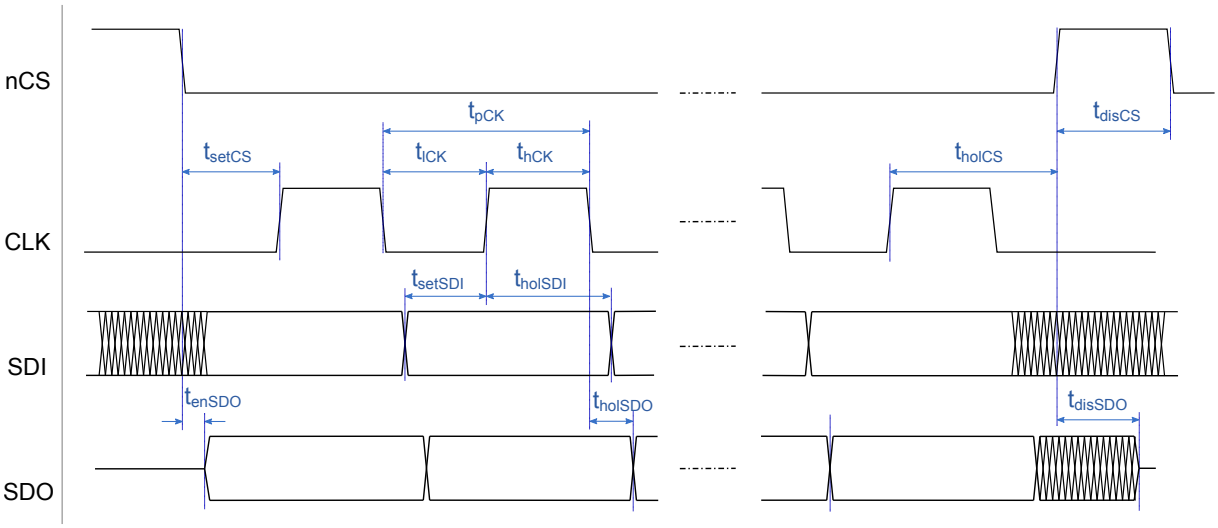
The SDO is an open-drain output pin. When the nCS is not active, the SDO line is released by the device and its level depends on the external pull-up resistor.

The SPI interface is disabled during the standby mode.

5.11.1 Waveforms and timings

The communication is based on SPI with clock polarity 0 (clock low at the beginning of communication) and clock phase 0 (data lines sampled on the first edge).

Figure 38. SPI message timing



CLK must be low when nCS commutates from high to low.

The data bits on SDI line (MOSI) are sampled by the device on the CLK rising edges, the last data bit is sampled on the 16th CLK rising edge.

Upon nCS falling edge, the device asserts the first data bit on SDO line (MISO): data are asserted from MSB to LSB at each falling edge of the CLK signal.

After the 16th falling edge of CLK, the nCS input must be forced high.

When nCS is set high, the SDO line is released.

The SDO output is open-drain, so the high-state is obtained by means of an external pull-up circuitry.

Table 13. SPI timings

Param	Description	Min.	Max.	Unit
t_{disCS}	Inter-message delay	200	-	ns
t_{setCS}	From nCS falling edge to CLK rising edge	200	-	ns
t_{enSDO}	From nCS falling to SDO commutation (open-drain output pin)	-	25	ns

Param	Description	Min.	Max.	Unit
t_{holSDO}	From CLK falling edge to SDO commutation (open-drain output pin)	-	35	ns
t_{disSDO}	From nCS rising edge to SDO line released to Hi-Z	-	30	ns
t_{holCS}	From last CLK rising edge to nCS rising edge	60	-	ns
t_{setSDI}	SDI setup time wrt CLK rising edge	10	-	ns
t_{holSDI}	SDI hold time wrt CLK rising edge	10	-	ns
t_{lCK}	CLK pulse low	28	-	ns
t_{hCK}	CLK pulse high	28	-	ns
t_{pCK}	CLK pulse period	100	-	ns

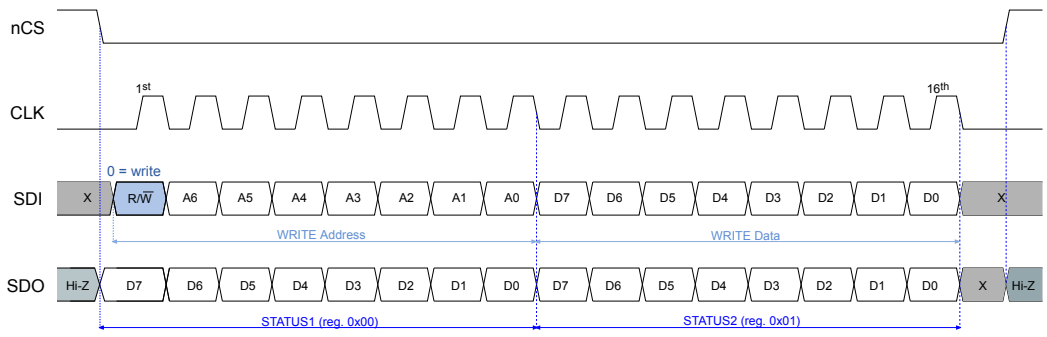
5.11.2 Protocol description

Data exchange with the controller is based on two types of messages: the "write" message and the "read" message. They are analyzed in detail in the following two sections.

5.11.2.1 Write operation

A write operation updates the internal registers of the STDRIVE102BP/P or sends a specific command to the device (see command registers in Section 5.12.4.23, Section 5.12.4.24, and Section 5.12.4.25).

Figure 39. SPI write message frame



In a write message, the controller sends both the register address and data on the SDI line. At the same time, the STDRIVE102BP/P returns the current values of STATUS1 and STATUS2 registers to the controller via the SDO line.

The configuration registers providing critical configuration parameters are protected against unwanted writing (see Table 14 and Table 15). Writing to these registers requires an unlock command (see Section 5.12.1).

Following the sequence of a write message:

- The controller device starts the communication by asserting nCS (low).
- While nCS is low, the controller transmits a 16-bit word to the device, composed of the following bits in order, from the first transmitted to the last:
  - 1-bit set to zero, identifying the write operation
  - 7-bits representing the address of the register (MSB first)
  - 8-bits data field (MSB first) to be written into the addressed register
- The STDRIVE102BP/P returns a 16-bit word to the controller, composed of:
  - STATUS1 register (MSB first)
  - STATUS2 register (MSB first)
- The controller device ends the communication by de-asserting nCS (high).

In case of valid write message, the addressed register is updated immediately according to data field. Otherwise, the SPI_ERROR bit is set in the STATUS1 register and the write request is not executed.

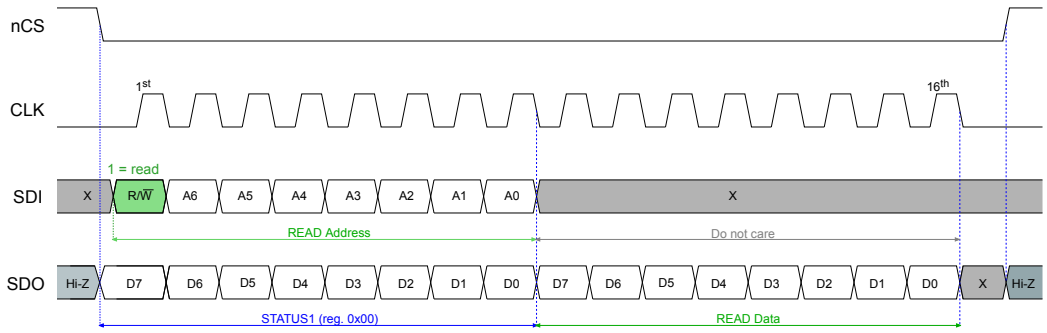
Not-valid write operations are listed below:

- Number of CLK rising edges within transmission is different from 16.
- nCS low and no CLK transitions.
- Address refers to a read-only or a reserved register.
- Address is invalid (not present in the register map).
- Address refers to a command register but the data field is not an allowed command code (see Section 5.12.4.23, Section 5.12.4.24, and Section 5.12.4.25).
- Address refers to a write protected register when the registers are locked.

5.11.2.2 *Read operation*

The read operation fetches the value of an internal register of the STDRIVE102BP/P.

Figure 40. SPI read message frame



In a read message, the controller sends the register address on the SDI line, and the STDRIVE102BP/P returns the current value of STATUS1 and the value of the addressed register to the controller via the SDO line.

Following the sequence of a read message:

- The controller device starts the communication by asserting nCS (low).
- While nCS is low, the controller transmits a 16-bit word to the device composed by:
  - 1-bit set to one, identifying the read operation
  - 7-bits representing the address of the register (MSB first)
  - 8-bits dummy field (any value is allowed)
- The device returns a 16-bit word to the controller, composed of:
  - STATUS1 register (MSB first)
  - Read data from addressed register (MSB first)
- The controller device ends the communication by de-asserting nCS (high).

In case of not-valid read message, the SPI_ERROR bit is set in the STATUS1 register and the read data content must be considered as dummy.

Not-valid read messages are reported below:

- Number of CLK rising edges within transmission is different from 16.
- nCS low and no CLK transitions.
- Address refers to a write-only or a reserved register.
- Address is invalid (not present in the register map).

Accessing a write-protected register in read mode while it is locked is allowed (no error reporting).

5.12 Configuration registers

This section provides details on the configuration registers of the devices.

5.12.1 Protected registers

Some parameters are critical from the device operation point of view:

- Gate driver configuration
- V_{DS} monitoring protection configuration
- AFE configuration

Changing their value during operation could results in incorrect operation. For this reason, the related registers are protected by a lock/unlock feature avoiding unwanted writing.

The protected registers must be unlocked to write them (see Table 14 and Table 15). Any attempt to write the protected registers when they are locked results in a SPI protocol violation, and the SPI_ERROR bit in the STATUS1 register is set.

When the registers are unlocked, all gate driver outputs (GLSx and GHSx) are forced LOW regardless of the control input signals (the power stage is disabled).

At power-up or when exiting standby state, the registers are locked.

To lock or unlock the registers, a dedicated command is provided as described in Section 5.12.4.25.

5.12.2 STDRIVE102BP register map

Table 14. STDRIVE102BP register map

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type (1)
0x00	STATUS1	LOCKED	nVDS_FAULT_L	nVCP_UV_L	nVCC_UV_L	nVDD_UV_L	nTH_SD_L	nCOMP_EVENT_L	SPI_ERROR	RDO
0x01	STATUS2	RESET_STATE	nVCP_UV	nVCC_UV	VCC_GOOD	TH_GOOD	nCOMP1_EVENT_L	nCOMP2_EVENT_L	nCOMP3_EVENT_L	RDO
0x02	STATUS3	nTH_SD_FAULT	nVDD_UV	nVDS_HS1_FAULT	nVDS_HS2_FAULT	nVDS_HS3_FAULT	nVDS_LS1_FAULT	nVDS_LS2_FAULT	nVDS_LS3_FAULT	RDO
0x03	AFE_STATUS	nCOMP1_EVENT	nCOMP2_EVENT	nCOMP3_EVENT	NOT USED	NOT USED	nCOMP1_FAULT	nCOMP2_FAULT	nCOMP3_FAULT	RDO
0x04	DRV_CFG	TCC[3:0]				IGATE[3:0]				WRP/RD
0x05	SYS_CFG	NOT USED	VCC_GOOD_SEL	UV_SEL	TCC_EQ_SEL	DRV_EQ_SEL	MODE_SEL	TCC_WAIT	INTLOCK	WRP/RD
0x06	VDS_CFG	VDS_SOFT_OFF	VDS_COUNT_EN	VDS_TDIS[2:0]			VDS_TDG[2:0]			WRP/RD
0x07	VDS_COUNT	VDS_COUNT[7:0]								WR/RD
0x08	nFAULT_SIG_EN	VCC_UV_FAULT_SIG	VCP_UV_FAULT_SIG	VDD_UV_FAULT_SIG	THSD_FAULT_SIG	VDS_FAULT_SIG	COMP3_FAULT_SIG	COMP2_FAULT_SIG	COMP1_FAULT_SIG	WR/RD
0x09	FLAG_SIG_EN1	SPI_ERROR_FLAG_SIG	nTH_GOOD_FLAG_SIG	nVCC_GOOD_FLAG_SIG	3FG	NOT USED	COMP3_EVENT_FLAG_SIG	COMP2_EVENT_FLAG_SIG	COMP1_EVENT_FLAG_SIG	WR/RD
0x0A	FLAG_SIG_EN2	NOT USED	NOT USED	NOT USED	VDS_FLAG_SIG	VCP_UV_FLAG_SIG	VCC_UV_FLAG_SIG	VDD_UV_FLAG_SIG	THSD_FLAG_SIG	WR/RD
0x0B	AFE_MAIN_CFG	AFE_MASTER_EN	NOT USED	NOT USED	PGA_REF_SEL	COMP_REF_SEL[3:0]				WRP/RD
0x0C	AFE_CFG_CH1	PGA1_EN	COMP1_EN	COMP1_INP[1:0]		COMP1_INN	COMP1_INV	PGA1_GAIN[1:0]		WRP/RD
0x0D	AFE_CFG_CH2	PGA2_EN	COMP2_EN	COMP2_INP[1:0]		COMP2_INN	COMP2_INV	PGA2_GAIN[1:0]		WRP/RD
0x0E	AFE_CFG_CH3	PGA3_EN	COMP3_EN	COMP3_INP[1:0]		COMP3_INN	COMP3_INV	PGA3_GAIN[1:0]		WRP/RD
0x0F	COMP_CFG	NOT USED	NOT USED	NOT USED	SAFE_DRV_SEL[1:0]		COMP3_SOFT_OFF	COMP2_SOFT_OFF	COMP1_SOFT_OFF	WRP/RD
0x10	AFE_FLT_CH1	COMP1_FAULT_EN	COMP1_COUNT_EN	COMP1_TDG[1:0]		COMP1_TDIS[3:0]				WRP/RD
0x11	AFE_FLT_CH2	COMP2_FAULT_EN	COMP2_COUNT_EN	COMP2_TDG[1:0]		COMP2_TDIS[3:0]				WRP/RD
0x12	AFE_FLT_CH3	COMP3_FAULT_EN	COMP3_COUNT_EN	COMP3_TDG[1:0]		COMP3_TDIS[3:0]				WRP/RD
0x13	COMP1_COUNT	COMP1_COUNT[7:0]								WR/RD
0x14	COMP2_COUNT	COMP2_COUNT[7:0]								WR/RD
0x15	COMP3_COUNT	COMP3_COUNT[7:0]								WR/RD
0x16	Reserved	Reserved								FWR/FRD
0x17										
0x18										
0x19										
0x1A	CMD_CLEAR	CMD_CLEAR[7:0]								WRO
0x1B	DEV_RESET	DEV_RESET[7:0]								WRP/WRO
0x1C	CMD_LOCK	CMD_LOCK[7:0]								WRO

1. *RD: Read, RDO: Read only, FRD: Forbidden Read, WR: Write, WRO: Write only, WRP: Write protected, FWR: Forbidden Write.*

Note: Access to "Reserved" registers both in read and write mode (regardless of the registers being locked or unlocked) raises an SPI protocol violation (SPI_ERROR bit in STATUS1 register set to 1).

5.12.3 STDRIVE102P register map

Table 15. STDRIVE102P register map

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Type [1]
0x00	STATUS1	LOCKED	nVDS_FAULT_L	nVCP_UV_L	nVCC_UV_L	nVDD_UV_L	nTH_SD_L	nCOMP_EVENT_L	SPI_ERROR	RDO
0x01	STATUS2	RESET_STATE	nVCP_UV	nVCC_UV	VCC_GOOD	TH_GOOD	nCOMP1_EVENT_L	NOT USED	NOT USED	RDO
0x02	STATUS3	nTH_SD_FAULT	nVDD_UV	nVDS_HS1_FAULT	nVDS_HS2_FAULT	nVDS_HS3_FAULT	nVDS_LS1_FAULT	nVDS_LS2_FAULT	nVDS_LS3_FAULT	RDO
0x03	AFE_STATUS	nCOMP1_EVENT	NOT USED	NOT USED	NOT USED	NOT USED	nCOMP1_FAULT	NOT USED	NOT USED	RDO
0x04	DRV_CFG	TCC[3:0]				IGATE[3:0]				WRP/RD
0x05	SYS_CFG	NOT USED	VCC_GOOD_SEL	UV_SEL	TCC_EQ_SEL	DRV_EQ_SEL	MODE_SEL	TCC_WAIT	INTLOCK	WRP/RD
0x06	VDS_CFG	VDS_SOFT_OFF	VDS_COUNT_EN	VDS_TDIS[2:0]			VDS_TDG[2:0]			WRP/RD
0x07	VDS_COUNT	VDS_COUNT[7:0]								WR/RD
0x08	nFAULT_SIG_EN	VCC_UV_FAULT_SIG	VCP_UV_FAULT_SIG	VDD_UV_FAULT_SIG	THSD_FAULT_SIG	VDS_FAULT_SIG	NOT USED	NOT USED	COMP1_FAULT_SIG	WR/RD
0x09 0x0A	Not used	Not used								Not used
0x0B	AFE_MAIN_CFG	AFE_MASTER_EN	NOT USED	NOT USED	PGA_REF_SEL	COMP_REF_SEL[3:0]				WRP/RD
0x0C	AFE_CFG_CH1	PGA1_EN	COMP1_EN	COMP1_INP[1:0]		COMP1_INN	COMP1_INV	PGA1_GAIN[1:0]		WRP/RD
0x0D 0x0E	Not used	Not used								Not used
0x0F	COMP_CFG	NOT USED	NOT USED	NOT USED	SAFE_DRV_SEL[1:0]		NOT USED	NOT USED	COMP1_SOFT_OFF	WRP/RD
0x10	AFE_FLT_CH1	COMP1_FAULT_EN	COMP1_COUNT_EN	COMP1_TDG[1:0]		COMP1_TDIS[3:0]				WRP/RD
0x11 0x12	Not used	Not used								Not used
0x13	COMP1_COUNT	COMP1_COUNT[7:0]								WR/RD
0x14 0x15	Not used	Not used								Not used
0x16 0x17 0x18 0x19	Reserved	Reserved								FWR/FRD
0x1A	CMD_CLEAR	CMD_CLEAR[7:0]								WRO
0x1B	DEV_RESET	DEV_RESET[7:0]								WRP/WRO
0x1C	CMD_LOCK	CMD_LOCK[7:0]								WRO

1. *RD: Read, RDO: Read only, FRD: Forbidden Read, WR: Write, WRO: Write only, WRP: Write protected, FWR: Forbidden Write.*

Note: Access to "Reserved" registers both in read and write mode (regardless of the device being in locked or unlocked state) is considered an SPI protocol violation and consequently returns an SPI_ERROR bit set in STATUS1 register.

5.12.4 STDRIVE102BP and STDRIVE102P registers detailed description

This section provides details about all the configuration registers of the STDRIVE102BP/P.

In the following tables, the column “Type” reports the behavior of the specific bit as per the following:

- Real Time: the bit reflects the condition of the device in real time.
- Latching Low: the bit goes low at the first occurrence of its related event and remains low until it is cleared by the user.
- Latching High: the bit goes high at the first occurrence of its related event and remains high until it is cleared by the user.
- Disable Time / Latching Low:
  these bits are associated with the VDS monitoring protection faults and comparators faults. The bit goes low at the occurrence of its related event and remains low until the disable time following the event is over. The bit may also be permanently latched Low depending on the value of the counter associated with the specific protection, until cleared by the user. Refer to Section 5.2.7 and Section 5.3.5.

5.12.4.1 STATUS 1 register

- Address: 0x00
- Access mode: read-only. Accessing this register in write mode has no effect but latching the SPI_ERROR bit in this register (bit 0).
- Default value: 0xFE. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 16. STATUS1 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	LOCKED	nVDS_FAULT_L	nVCP_UV_L	nVCC_UV_L	nVDD_UV_L	nTH_SD_L	nCOMP_EVENT_L	SPI_ERROR
Default value	1	1	1	1	1	1	1	0

Table 17. STATUS1 register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	LOCKED	nVDS_FAULT_L	nVCP_UV_L	nVCC_UV_L	nVDD_UV_L	nTH_SD_L	nCOMP_EVENT_L	SPI_ERROR
Default value	1	1	1	1	1	1	1	0

Table 18. **STATUS1 register fields description**

Field name	Description	Type	Notes
LOCKED	Indicates if the registers are locked or unlocked. • 0: write-protected registers are unlocked and can be accessed in read/write mode. • 1: write protected registers are locked and can be accessed in read mode only.	Real Time	At power-up and the exiting standby state, the registers are locked. See Section 5.12.1.
nVDS_FAULT_L	Indicates the intervention of the V_{DS} monitoring protection. • 0: the V_{DS} monitoring protection has been triggered on at least one of the six power MOSFETs • 1: the V_{DS} monitoring protection has not been triggered.	Latching Low	See Section 5.2.7 This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nVCP_UV_L	Indicates the occurrence of an undervoltage lock-out (UVLO) event on the charge pump. • 0: one or more UVLO events on the charge pump has occurred. • 1: no UVLO events on the charge pump has occurred.	Latching Low	See Section 5.1.3. When exiting standby state, this bit may or may not be set, depending on the actual voltage on VBOOT and VM pins. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nVCC_UV_L	Indicates the occurrence of an undervoltage lock-out (UVLO) event on the V_{CC} supply. • 0: one or more UVLO events on the V_{CC} supply has occurred. • 1: no UVLO events on the V_{CC} supply has occurred.	Latching Low	See Section 5.1.1. When exiting standby state, this bit may or may not be set, depending on the device actual voltage on the VCC pin. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nVDD_UV_L	Indicates the occurrence of an undervoltage lock-out (UVLO) event on the V_{DD} supply. • 0: one or more UVLO events on the V_{DD} supply has occurred. • 1: no UVLO events on the V_{DD} supply has occurred.	Latching Low	See Section 5.1.2. When exiting standby state, this bit may or may not be set, depending on the actual voltage on the VDD pin. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nTH_SD_L	Indicates the occurrence of a thermal shutdown. • 0: one or more thermal shutdown has occurred. • 1: no thermal shutdown has occurred.	Latching Low	See Section 5.6. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nCOMP_EVENT_L	Indicates an event detection by at least one of the comparators in the AFE. • 0: at least one of the comparators has detected an event. • 1: no event has been detected by any comparator.	Latching Low	See Section 5.3.5. This bit is: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
SPI_ERROR	Indicates if a communication error has occurred during the SPI communication. • 0: no communication error has been detected. • 1: at least one communication error has occurred.	Latching High	See Section 5.11.2. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95

5.12.4.2 *STATUS2 register*

- Address: 0x01
- Access mode: read-only. Accessing this register in write mode has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xFF. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 19. STATUS2 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	RESET_STATE	nVCP_UV	nVCC_UV	VCC_GOOD	TH_GOOD	nCOMP1_EVENT_L	nCOMP2_EVENT_L	nCOMP3_EVENT_L
Default value	1	1	1	1	1	1	1	1

Table 20. STATUS2 register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	RESET_STATE	nVCP_UV	nVCC_UV	VCC_GOOD	TH_GOOD	nCOMP1_EVENT_L	NOT USED	NOT USED
Default value	1	1	1	1	1	1	1	1

Table 21. **STATUS2 register fields description**

Field name	Description	Type	Notes
RESET_STATE	Indicates if the device has been reset. • 0: the device has not been reset. • 1: the device has been reset. This bit is cleared by set at 1 during the power-up, exiting the standby mode, or whenever a reset command is issued by the DEV_RESET register.	Latching High	See Section 5.12.4.24. This bit is cleared by: • Writing CMD_CLEAR = 0x68
nVCP_UV	Indicates if an undervoltage condition on the charge-pump is currently present. • 0: undervoltage condition. • 1: no undervoltage condition.	Real Time	See Section 5.1.3.
nVCC_UV	Indicates if an undervoltage condition on the V_{CC} supply is currently present. • 0: undervoltage condition. • 1: no undervoltage condition.	Real Time	See Section 5.1.2)
VCC_GOOD	Indicates if the current V_{CC} supply voltage is above or below the $V_{P\_GOOD(On/Off)}$ threshold. • 0: V_{CC} supply below the $V_{P\_GOOD(Off)}$ threshold. • 1: V_{CC} supply above the $V_{P\_GOOD(On)}$ threshold.	Real Time	See Section 5.1.2.
TH_GOOD	Indicates if a thermal warning condition is currently present. • 0: device's temperature above the warning threshold $T_{j(WRN)}$. • 1: device's temperature below the warning recovery threshold $T_{j(WRN),rec}$.	Real Time	See Section 5.6.
nCOMP1_EVENT_L	Indicates an event detection by comparator 1 in the AFE. • 0: comparator 1 has detected at least one event. • 1: no event detected by comparator 1.	Latching Low	See Section 5.3.5. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nCOMP2_EVENT_L	Indicates an event detection by comparator 2 in the AFE (STDRIVE102BP only). • 0: comparator 2 has detected at least one event. • 1: no event detected by comparator 2.	Latching Low	See Section 5.3.5. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95
nCOMP3_EVENT_L	Indicates an event detection by comparator 3 in the AFE (STDRIVE102BP only). • 0: comparator 3 has detected at least one event. • 1: no event detected by comparator 3.	Latching Low	See Section 5.3.5. This bit is cleared by: • Writing CMD_CLEAR = 0x90 • Writing CMD_CLEAR = 0x95

5.12.4.3 *STATUS3 register*

- Address: 0x02
- Access mode: read-only. Accessing this register in write mode has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xFF. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$

Table 22. STATUS3 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	nTH_SD_FAULT	nVDD_UV	nVDS_HS1_FAULT	nVDS_HS2_FAULT	nVDS_HS3_FAULT	nVDS_LS1_FAULT	nVDS_LS2_FAULT	nVDS_LS3_FAULT
Default value	1	1	1	1	1	1	1	1

Table 23. STATUS3 register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	nTH_SD_FAULT	nVDD_UV	nVDS_HS1_FAULT	nVDS_HS2_FAULT	nVDS_HS3_FAULT	nVDS_LS1_FAULT	nVDS_LS2_FAULT	nVDS_LS3_FAULT
Default value	1	1	1	1	1	1	1	1

Table 24. STATUS3 register fields description

Field name	Description	Type	Notes
nTH_SD_FAULT	Indicates if a thermal shutdown is currently present. • 0: thermal shutdown • 1: no thermal shutdown	Real Time	See Section 5.6.
nVDD_UV	Indicates if an undervoltage condition on the V_{DD} supply is currently present. • 0: undervoltage condition • 1: no undervoltage condition	Real Time	See Section 5.1.2.
nVDS_HS1_FAULT nVDS_HS2_FAULT nVDS_HS3_FAULT nVDS_LS1_FAULT nVDS_LS2_FAULT nVDS_LS3_FAULT	nVDS_<x>_FAULT indicates if the V_{DS} monitoring protection of the driver <x> (HS1, HS2, HS3, LS1, LS2, and LS3) is currently signaling a fault condition on its respective MOSFET. • 0: the V_{DS} monitoring protection of the driver <x> is currently active or is latched. • 1: the V_{DS} monitoring protection of the driver <x> is not currently active nor latched.	Disable Time / Latching Low	See Section 5.2.7. These bits are automatically cleared after a disable time. In case of permanent latch, they are cleared by: • Writing CMD_CLEAR = 0x05 • Writing CMD_CLEAR = 0x95 • Forcing EN pin low

5.12.4.4 *AFE_STATUS register*

- Address: 0x03
- Access mode: read-only. Accessing this register in write mode has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xE7. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 25. AFE_STATUS register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	nCOMP1_EVENT	nCOMP2_EVENT	nCOMP3_EVENT	NOT USED	NOT USED	nCOMP1_FAULT	nCOMP2_FAULT	nCOMP3_FAULT
Default value	1	1	1	0	0	1	1	1

Table 26. AFE_STATUS register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	nCOMP1_EVENT	NOT USED	NOT USED	NOT USED	NOT USED	nCOMP1_FAULT	NOT USED	NOT USED
Default value	1	1	1	0	0	1	1	1

Table 27. AFE_STATUS register fields description

Field name	Description	Type	Notes
nCOMP1_EVENT nCOMP2_EVENT nCOMP3_EVENT	nCOMP<x>_EVENT reports the negated output of the deglitch filter <x> related to the comparator <x>. • 0: the output of the deglitch filter <x> is high • 1: the output of the deglitch filter <x> is low	Real Time	See Section 5.3.5. This bit is real time, and its status does not include the additional disable time associated with comparator protection.
nCOMP1_FAULT nCOMP2_FAULT nCOMP3_FAULT	nCOMP<x>_FAULT bit reports the actual value of the fault logic related to the comparator <x> after the latch/disable logic. • 0: a fault event from comparator <x> logic is present • 1: no fault event from comparator <x> logic is present	Disable Time / Latching Low	See Section 5.3.5. This bit includes the additional disable time and latching function associated with comparator protection. Automatically cleared after a disable time. In case of permanent latch, it is cleared by: • Writing CMD_CLEAR = 0x95 • Writing CMD_CLEAR = 0x05 • Forcing EN pin low

5.12.4.5 *DRV_CFG register*

- Address: 0x04
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0x3C. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 28. DRV_CFG register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	TCC[3:0]				IGATE[3:0]			
Default value	0	0	1	1	1	1	0	0

Table 29. DRV_CFG register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	TCC[3:0]				IGATE[3:0]			
Default value	0	0	1	1	1	1	0	0

Table 30. DRV_CFG register fields description

Field name	Description	Type	Notes
TCC[3:0]	This parameter sets the turn-on and turn-off time ($t_{cc,on}$ and $t_{cc,off}$) of the gate drivers, according to Table 31. Note that the actual value also depends on the current setting of DRV_EQ_SEL and TCC_EQ_SEL bits (see Section 5.12.4.6).	-	Refer to Section 5.2.1 for details.
IGATE[3:0]	This parameter sets the source and sink currents ($I_{GATE,on}$ and $I_{GATE,off}$) of the gate drivers, according to Table 32. Note that the actual value also depends on the current setting of DRV_EQ_SEL bit (see Section 5.12.4.6).	-	Refer to Section 5.2.1 for details.

Table 31. **Programmable time TCC at constant current**

TCC level	TCC [3:0]	DRV_EQ_SEL = 0 TCC_EQ_SEL = Do not care		DRV_EQ_SEL = 1 TCC_EQ_SEL = 0	DRV_EQ_SEL = 1 TCC_EQ_SEL = 1
		$t_{cc,on}$ [ns]	$t_{cc,off}$ [ns]	$t_{cc,on} = t_{cc,off}$ [ns]	$t_{cc,on} = t_{cc,off}$ [ns]
0	0000	280	140	280	140
1	0001	560	280	560	280
2	0010	840	420	840	420
3 (default)	**0011**	**1120**	**560**	1120	560
4	0100	1400	700	1400	700
5	0101	1680	840	1680	840
6	0110	1960	980	1960	980
7	0111	2240	1120	2240	1120
8	1000	2520	1260	2520	1260
9	1001	2800	1400	2800	1400
10	1010	3080	1540	3080	1540
11	1011	3360	1680	3360	1680
12	1100	3800	1900	3800	1900
13	1101	4400	2200	4400	2200
14	1110	4800	2400	4800	2400
15	1111	5400	2700	5400	2700

Table 32. Programmable gate current settings IGATE

IGATE level	IGATE[3:0]	DRV_EQ_SEL = 0 (default)					DRV_EQ_SEL = 1				
		$I_{GATE,on}$ [mA]	$I_{GATE,off}$ [mA]	$I_{hold,on}$ [mA]	$I_{hold,off}$ [mA]	I_{clamp} [mA]	$I_{GATE,on}$ [mA]	$I_{GATE,off}$ [mA]	$I_{hold,on}$ [mA]	$I_{hold,off}$ [mA]	I_{clamp} [mA]
0	0000	25	50	25	50	2140	25	25	25	25	1070
1	0001	75	150	25	50	2140	75	75	25	25	1070
2	0010	150	300	25	50	2140	150	150	25	25	1070
3	0011	250	500	25	50	2140	250	250	25	25	1070
4	0100	300	600	25	50	2140	300	300	25	25	1070
5	0101	350	700	25	50	2140	350	350	25	25	1070
6	0110	400	800	25	50	2140	400	400	25	25	1070
7	0111	500	1000	25	50	2140	500	500	25	25	1070
8	1000	550	1100	25	50	2140	550	550	25	25	1070
9	1001	600	1200	25	50	2140	600	600	25	25	1070
10	1010	650	1300	25	50	2140	650	650	25	25	1070
11	1011	700	1400	25	50	2140	700	700	25	25	1070
12	**1100**	**800**	**1600**	**25**	**50**	**2140**	800	800	25	25	1070
13	1101	850	1700	25	50	2140	850	850	25	25	1070
14	1110	900	1800	25	50	2140	900	900	25	25	1070
15	1111	1000	2000	25	50	2140	1000	1000	25	25	1070

The reduced $I_{GATE,off(SO)}$ gate current and the increased $t_{cc,off(SO)}$ time used to implement the soft turn-off (see Section 5.4) are listed respectively in Table 33 and Table 34.

The values depend on the actual setting of the IGATE[3:0] and the TCC[3:0].

Table 33. **Soft-off turn-off time according to the TCC level**

TCC level	TCC[3:0]	DRV_EQ_SEL = 0 TCC_EQ_SEL = Do not care		DRV_EQ_SEL = 1 TCC_EQ_SEL = 0		DRV_EQ_SEL = 1 TCC_EQ_SEL = 1	
		$t_{cc,off}$ [ns]	$t_{cc,off(SO)}$ [µs]	$t_{cc,off}$ [ns]	$t_{cc,off(SO)}$ [µs]	$t_{cc,off}$ [ns]	$t_{cc,off(SO)}$ [µs]
0	0000	140	1.1	280	2.2	140	1.1
1	0001	280	2.2	560	4.5	280	2.2
2	0010	420	3.4	840	6.7	420	3.4
3 (default)	**0011**	**560**	**4.5**	1120	9.0	560	**4.5**
4	0100	700	5.6	1400	11.2	700	5.6
5	0101	840	6.7	1680	13.4	840	6.7
6	0110	980	7.8	1960	15.7	980	7.8
7	0111	1120	9.0	2240	17.9	1120	9.0
8	1000	1260	10.1	2520	20.2	1260	10.1
9	1001	1400	11.2	2800	22.4	1400	11.2
10	1010	1540	12.3	3080	24.6	1540	12.3
11	1011	1680	13.4	3360	26.9	1680	13.4
12	1100	1900	15.2	3800	30.4	1900	15.2
13	1101	2200	17.6	4400	35.2	2200	17.6
14	1110	2400	19.2	4800	38.4	2400	19.2
15	1111	2700	21.6	5400	43.2	2700	21.6

Table 34. **Soft-off gate currents according to the IGATE level**

IGATE level	IGATE[3:0]	DRV_EQ_SEL = 0 (default)		DRV_EQ_SEL = 1	
		$I_{GATE,off}$ [mA]	$I_{GATE,off(SO)}$ [mA]	$I_{GATE,off}$ [mA]	$I_{GATE,off(SO)}$ [mA]
0	0000	50	50	25	25
1	0001	150	50	75	25
2	0010	300	50	150	25
3	0011	500	150	250	75
4	0100	600	150	300	75
5	0101	700	150	350	75
6	0110	800	150	400	75
7	0111	1000	300	500	150
8	1000	1100	300	550	150
9	1001	1200	300	600	150
10	1010	1300	300	650	150
11	1011	1400	300	700	150
12 (default)	**1100**	**1600**	**500**	800	250
13	1101	1700	500	850	250
14	1110	1800	500	900	250
15	1111	2000	500	1000	250

5.12.4.6 *SYS_CFG register*

- Address: 0x05
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0x07. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 35. SYS_CFG register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	NOT USED	VCC_GOOD_SEL	UV_SEL	TCC_EQ_SEL	DRV_EQ_SEL	MODE_SEL	TCC_WAIT	INTLOCK
Default value	0	0	0	0	0	1	1	1

Table 36. SYS_CFG register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	NOT USED	VCC_GOOD_SEL	UV_SEL	TCC_EQ_SEL	DRV_EQ_SEL	MODE_SEL	TCC_WAIT	INTLOCK
Default value	0	0	0	0	0	1	1	1

Table 37. SYS_CFG register fields description

Field name	Description	Type	Notes
VCC_GOOD_SEL	Sets the power-good thresholds $V_{P\_GOOD(On)}$ and $V_{P\_GOOD(Off)}$ for the V_{CC} supply rail. • 0: the low thresholds selected • 1: the high thresholds selected High and low thresholds are reported in Table 6.	-	See Section 5.1.1.
UV_SEL	Sets the threshold of the undervoltage protection for both the V_{CC} supply ($V_{CC(On)}$ and $V_{CC(Off)}$) and the charge pump output rail ($V_{CPump(On)}$ and $V_{CPump(Off)}$) . • 0: the low thresholds selected • 1: the high thresholds selected High and low thresholds are reported in Table 6.	-	See Section 5.1.1 and Section 5.1.3.
TCC_EQ_SEL	Defines which set of values to use for TCC timing. This bit has an effect only when DRV_EQ_SEL = 1 (refer to Table 31).	-	See Section 5.2.1 for details.
DRV_EQ_SEL	Defines which set of values to use for IGATE currents (refer to Table 32) and TCC timing (refer to Table 31). • 0: the sink current $I_{GATE,off}$ is twice the source current $I_{GATE,on}$ and the $t_{cc,off}$ is half the $t_{cc,on}$. • 1: the $I_{GATE,off}$ is equal to the $I_{GATE,on}$ and the $t_{cc,off}$ is equal to the $t_{cc,on}$.	-	See Section 5.2.1 for details.
MODE_SEL	Sets the input strategy mode: • 0: Direct mode (refer to Section 5.2.2). • 1: Enable/Input mode (refer to Section 5.2.3).	-	
TCC_WAIT	Selects whether to wait for the $t_{cc,off}$ completion before performing the $t_{cc,on}$ on the complementary driver when Direct mode is selected (MODE_SEL = 0): • 0: do not wait for $t_{cc,off}$ completion. • 1: wait for $t_{cc,off}$ completion.	-	Refer to Section 5.2.2 for more details. When Enable/Input mode is selected (MODE_SEL = 1), this bit is ineffective.
INTLOCK	Enables/disables the interlocking protection when Direct mode is selected (MODE_SEL = 0): • 0: the interlocking protection is disabled. • 1: the interlocking protection enabled.	-	Refer to Section 5.2.2 for more details. When Enable/Input mode is selected (MODE_SEL = 1), this bit is ineffective.

5.12.4.7 *VDS_CFG register*

- Address: 0x06
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xDD. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

For more details about VDS monitoring, see Section 5.2.7.

Table 38. VDS_CFG register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	VDS_SOFT_OFF	VDS_COUNT_EN	VDS_TDIS[2:0]			VDS_TDG[2:0]		
Default value	1	1	0	1	1	1	0	1

Table 39. VDS_CFG register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	VDS_SOFT_OFF	VDS_COUNT_EN	VDS_TDIS[2:0]			VDS_TDG[2:0]		
Default value	1	1	0	1	1	1	0	1

Table 40. VDS_CFG register fields description

Field name	Description	Type	Notes
VDS_SOFT_OFF	Enables the soft-off feature when the V_{DS} monitoring protection is triggered. • 0: soft-off feature disabled • 1: soft-off feature enabled	-	See Section 5.4.
VDS_COUNT_EN	Enables the counter of the V_{DS} monitoring protection. • 0: the counter is disabled, VDS_COUNT[7:0] is frozen at its current value. • 1: the counter is enabled, VDS_COUNT[7:0] decrements by 1 each time a fault condition occurs due to the V_{DS} monitoring protection triggering See also Section 5.12.4.8.	-	See Section 5.2.7.
VDS_TDIS[2:0]	Selects the disable time after a V_{DS} monitoring protection event according to Table 41.	-	See Section 5.2.7.
VDS_TDG[2:0]	Selects the deglitch filter for the V_{DS} monitoring protection according to Table 42.	-	See Section 5.2.7.

Table 41. **Disable time values for V_{DS} monitoring**

VDS_TDIS[2:0]	$t_{dis,Vds}$ [ms]
000	0.55
001	0.85
010	1.1
011 (default)	**2.2**
100	3.3
101	5.5
110	11
111	22

Table 42. **V_{DS} monitoring deglitch filter time**

VDS_TDG[2:0]	$t_{dg(VDS)}$ [µs]
000	9
001	8
010	7
011	6
100	4.5
101 (default)	3.5
110	2.5
111	Reserved

5.12.4.8 *VDS_COUNT register*

- Address: 0x07
- Access mode: write / read.
- Default value: 0x00. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register stores the number of the V_{DS} monitoring remaining fault events before a permanent latch. See Section 5.2.7 for details.

Table 43. VDS_COUNT register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	VDS_ COUNT[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 44. VDS_COUNT register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	VDS_ COUNT[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 45. VDS_COUNT register fields description

Field name	Description	Type	Notes
VDS_ COUNT[7:0]	Down-counter of the V_{DS} monitoring fault events. If enabled by VDS_COUNT_EN = 1, it decrements by 1 each time a V_{DS} monitoring fault event occurs. If its value is 0x00 (end count), the next V_{DS} monitoring fault causes the V_{DS} monitoring protection to be permanently latched in fault state.	Real Time	See Section 5.2.7.

5.12.4.9 *nFAULT_SIG_EN register*

- Address: 0x08
- Access mode: write / read.
- Default value: 0xFF. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This is a read/write register. Each bit of this register enables the physical signaling of one or more specific protection events on the nFAULT pin (see Section 5.8)

Note: Writing one of these bits to 0 does not disable the protection, but only prevents the nFAULT pin to go low when the specific protection is triggered.

Table 46. nFAULT_SIG_EN register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	VCC_UV_FAULT_SIG	VCP_UV_FAULT_SIG	VDD_UV_FAULT_SIG	THSD_FAULT_SIG	VDS_FAULT_SIG	COMP3_FAULT_SIG	COMP2_FAULT_SIG	COMP1_FAULT_SIG
Default value	1	1	1	1	1	1	1	1

Table 47. nFAULT_SIG_EN register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	VCC_UV_FAULT_SIG	VCP_UV_FAULT_SIG	VDD_UV_FAULT_SIG	THSD_FAULT_SIG	VDS_FAULT_SIG	NOT USED	NOT USED	COMP1_FAULT_SIG
Default value	1	1	1	1	1	1	1	1

Table 48. **nFAULT_SIG_EN register fields description**

Field name	Description	Type	Notes
VCC_UV_FAULT_SIG	Enables/disables the physical signaling of a V_{CC} UVLO condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nVCC_UV bit is mapped on the nFAULT pin of the device.
VCP_UV_FAULT_SIG	Enables/disables the physical signaling of a charge pump UVLO condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nVCP_UV bit is mapped on the nFAULT pin of the device.
VDD_UV_FAULT_SIG	Enables/disables the physical signaling of a V_{DD} UVLO condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nVDD_UV bit is mapped on the nFAULT pin of the device.
THSD_FAULT_SIG	Enables/disables the physical signaling of a thermal shutdown condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nTH_SD_FAULT bit is mapped on the nFAULT pin of the device.
VDS_FAULT_SIG	Enables/disables the physical signaling of the V_{DS} monitoring fault condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the combination of the six nVDS_<x>_FAULT bits is mapped on the nFAULT pin of the device.
COMP3_FAULT_SIG	Enables/disables the physical signaling of the comparator 3 fault condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nCOMP3_FAULT bit is mapped on the nFAULT pin of the device.
COMP2_FAULT_SIG	Enables/disables the physical signaling of the comparator 2 fault condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nCOMP2_FAULT bit is mapped on the nFAULT pin of the device (only for STDRIVE102BP).
COMP1_FAULT_SIG	Enables/disables the physical signaling of the comparator 1 fault condition on the nFAULT pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nCOMP1_FAULT bit is mapped on the nFAULT pin of the device (only for STDRIVE102BP).

5.12.4.10 *FLAG_SIG_EN1 register*

- Address: 0x09
- Access mode: write / read.
- Default value: 0x20. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Each bit of this register enables the physical signaling of one or more specific events on the FLAG pin (see Section 5.8.2).

This register is not available in STDRIVE102P.

Table 49. FLAG_SIG_EN1 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	SPI_ERROR_FLAG_SIG	nTH_GOOD_FLAG_SIG	nVCC_GOOD_FLAG_SIG	3FG	NOT USED	COMP3_EVENT_FLAG_SIG	COMP2_EVENT_FLAG_SIG	COMP1_EVENT_FLAG_SIG
Default value	0	0	1	0	0	0	0	0

Table 50. FLAG_SIG_EN1 register fields description

Field name	Description	Type	Notes
SPI_ERROR_FLAG_SIG	Enables/disables the physical signaling of an SPI error condition on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the SPI_ERROR bit is inverted and mapped on the FLAG pin of the device.
nTH_GOOD_FLAG_SIG	Enables/disables the physical signaling of thermal warning condition on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the TH_GOOD bit is mapped on the FLAG pin of the device.
nVCC_GOOD_FLAG_SIG	Enables/disables the physical signaling of V_{CC} “power-good” on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the VCC_GOOD bit is mapped on the FLAG pin of the device.
3FG	Enables/disables the physical signaling of 3FG signal of the AFE on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the 3FG bit is mapped on the FLAG pin of the device.
COMP3_EVENT_FLAG_SIG	Enables/disables the physical signaling of the event related to the comparator 3 on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nCOMP3_EVENT bit is mapped on the FLAG pin of the device.
COMP2_EVENT_FLAG_SIG	Enables/disables the physical signaling of the event related to the comparator 2 on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nCOMP2_EVENT bit is mapped on the FLAG pin of the device.
COMP1_EVENT_FLAG_SIG	Enables/disables the physical signaling of the event related to the comparator 1 on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nCOMP1_EVENT bit is mapped on the FLAG pin of the device.

5.12.4.11 *FLAG_SIG_EN2 register*

- Address: 0x0A
- Access mode: write / read.
- Default value: 0x00. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Each bit of this register enables the physical signaling of one or more specific protection events on the FLAG pin (see Section 5.8.2).

This register is not available in STDRIVE102P.

Table 51. FLAG_SIG_EN2 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	NOT USED	NOT USED	NOT USED	VDS_FLAG_SIG	VCP_UV_FLAG_SIG	VCC_UV_FLAG_SIG	VDD_UV_FLAG_SIG	THSD_FLAG_SIG
Default value	0	0	0	0	0	0	0	0

Table 52. FLAG_SIG_EN2 register fields description

Field name	Description	Type	Notes
VDS_FLAG_SIG	Enables/disables the physical signaling of V_{DS} monitoring fault condition on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the combination of the six nVDS_<x>_FAULT bits is mapped on the FLAG pin of the device.
VCP_UV_FLAG_SIG	Enables/disables the physical signaling of an UVLO condition on the charge pump output rail on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nVCP_UV bit is mapped on the FLAG pin of the device.
VCC_UV_FLAG_SIG	Enables/disables the physical signaling of an UVLO condition on the V_{CC} on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nVCC_UV bit is mapped on the FLAG pin of the device.
VDD_UV_FLAG_SIG	Enables/disables the physical signaling of an UVLO condition on the V_{DD} on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nVDD_UV bit is mapped on the FLAG pin of the device.
THSD_FLAG_SIG	Enables/disables the physical signaling of thermal shutdown condition on the FLAG pin: • 0: signaling is disabled. • 1: signaling is enabled.	Real Time	If signaling is enabled, the nTH_SD_FAULT bit is mapped on the FLAG pin of the device.

5.12.4.12 *AFE_MAIN_CFG register*

- Address: 0x0B
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0x00. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 53. AFE_MAIN_CFG register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	AFE_MASTER_EN	NOT USED	NOT USED	PGA_REF_SEL	COMP_REF_SEL[3:0]			
Default value	0	0	0	0	0	0	0	0

Table 54. AFE_MAIN_CFG register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	AFE_MASTER_EN	NOT USED	NOT USED	PGA_REF_SEL	COMP_REF_SEL[3:0]			
Default value	0	0	0	0	0	0	0	0

Table 55. AFE_MAIN_CFG register fields description

Field name	Description	Type	Notes
AFE_MASTER_EN	AFE master enable (see Section 5.3): • 0: AFE fully disabled. • 1: AFE blocks enabled according to the dedicated enable bit of each block.	-	Refer to Section 5.12.4.13, Section 5.12.4.14, Section 5.12.4.15)
PGA_REF_SEL	Sets the PGA output bias voltage: • 0: AGND (to be used in unipolar configuration). • 1: $V_{DD}/2$ (to be used in bipolar configuration).	-	See Section 5.3.3. The PGA_REF_SEL bit is common to all the PGAs present in the AFE.
COMP_REF_SEL[3:0]	Sets the value of the internal reference voltage for the comparators' threshold according to Table 56.	-	See Section 5.3.4.

Table 56. **Reference voltage selection for the comparators**

COMP_REF_SEL[3:0]	Reference voltage value
0000 (default)	**100 mV**
0001	250 mV
0010	300 mV
0011	500 mV
0100	600 mV
0101	1200 mV
0110	$V_{DD}/2$ typ. 1.65 V
0111	13/22 V_{DD} typ. 1.65 V + 0.3 V
1000	15/22 V_{DD} typ. 1.65 V + 0.6 V
1001	19/22 V_{DD} typ. 1.65 V + 1.2 V
1010	21/22 V_{DD} typ. 1.65 V + 1.5 V
1011 to 1111	Reserved

5.12.4.13 *AFE_CFG_CH1 register*

- Address: 0x0C
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xC9. Default value is to be intended as the read-value expected software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$..

This register configures the channel 1 of the AFE (refer to Section 5.3).

Table 57. AFE_CFG_CH1 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	PGA1_EN	COMP1_EN	COMP1_INP[1:0]		COMP1_INN	COMP1_INV	PGA1_GAIN[1:0]	
Default value	1	1	0	0	1	0	0	1

Table 58. AFE_CFG_CH1 register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	PGA1_EN	COMP1_EN	COMP1_INP[1:0]		COMP1_INN	COMP1_INV	PGA1_GAIN[1:0]	
Default value	1	1	0	0	1	0	0	1

Table 59. **AFE_CFG_CH1 register fields description**

Field name	Description	Type	Notes
PGA1_EN	Enables the PGA of AFE channel 1: • 0: PGA1 disabled. • 1: PGA1 enabled.	-	
COMP1_EN	Enables the comparator of AFE channel 1: • 0: comparator 1 disabled. • 1: comparator 1 enabled.	-	
COMP1_INP[1:0]	Selects the comparator 1 positive input connection: • 00 or 10: connected to PGA1 positive input (PGA_IN1P). • 01 or 11: connected to PGA1 output (PGA_O1).	-	
COMP1_INN	Selects the comparator 1 negative input connection: • 0: connected to the internal adjustable threshold. • 1: connected to CREF pin.	-	The internal threshold can be selected by COMP_REF_SEL[3:0] bits (see Table 55). The internal threshold is in common to all the AFE channels.
COMP1_INV	Sets the comparator 1 output polarity: • 0: direct output. The comparator's logic triggers when the positive input is above the negative input. • 1: inverted output. The comparator's logic triggers when the positive input is below the negative input.	-	
PGA1_GAIN[1:0]	Sets the PGA1 differential gain: • 00: Gain = 4 • 01: Gain = 8 (default) • 10: Gain = 16 • 11: Gain = 32	-	

5.12.4.14 *AFE_CFG_CH2 register*

- Address: 0x0D
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xC9. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register configures the channel 2 of the AFE (refer to Section 5.3). This register is not available in STDRIVE102P.

Table 60. AFE_CFG_CH2 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	PGA2_EN	COMP2_EN	COMP2_INP[1:0]		COMP2_INN	COMP2_INV	PGA2_GAIN[1:0]	
Default value	1	1	0	0	1	0	0	1

Table 61. AFE_CFG_CH2 register fields description

Field name	Description	Type	Notes
PGA2_EN	Enables the PGA of AFE channel 2: • 0: PGA2 disabled. • 1: PGA2 enabled.	-	
COMP2_EN	Enables the comparator of AFE channel 2: • 0: comparator 2 disabled. • 1: comparator 2 enabled.	-	
COMP2_INP[1:0]	Selects the comparator 2 positive input connection: • 00 or 10: connected to PGA2 positive input (PGA_IN2P). • 01 or 11: connected to PGA2 output (PGA_O2).	-	
COMP2_INN	Selects the comparator 2 negative input connection: • 0: connected to the internal adjustable threshold. • 1: connected to CREF pin.	-	The internal threshold can be selected by COMP_REF_SEL[3:0] bits (see Table 55). The internal threshold is in common to all the AFE channels.
COMP2_INV	Sets the comparator 2 output polarity: • 0: direct output. The comparator's logic triggers when the positive input is above the negative input. • 1: inverted output. The comparator's logic triggers when the positive input is below the negative input.	-	
PGA2_GAIN[1:0]	Sets the PGA2 differential gain: • 00: Gain = 4 • 01: Gain = 8 (default) • 10: Gain = 16 • 11: Gain = 32	-	

5.12.4.15 *AFE_CFG_CH3 register*

- Address: 0x0E
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xC9. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register configures the channel 3 of the AFE (refer to Section 5.3). This register is not available in STDRIVE102P.

Table 62. AFE_CFG_CH3 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	PGA3_EN	COMP3_EN	COMP3_INP[1:0]		COMP3_INN	COMP3_INV	PGA3_GAIN[1:0]	
Default value	1	1	0	0	1	0	0	1

Table 63. AFE_CFG_CH3 register fields description

Field name	Description	Type	Notes
PGA3_EN	Enables the PGA of AFE channel 3: • 0: PGA3 disabled. • 1: PGA3 enabled.	-	
COMP3_EN	Enables the comparator of AFE channel 3: • 0: comparator 3 disabled. • 1: comparator 3 enabled.	-	
COMP3_INP[1:0]	Selects the comparator 3 positive input connection: • 00: connected to PGA3 positive input (PGA_IN3P). • 01: connected to PGA3 output (PGA_O3). • 10 or 11: connected to C_AUX pin.	-	
COMP3_INN	Selects the comparator 3 negative input connection: • 0: connected to the internal adjustable threshold. • 1: connected to CREF pin.	-	The internal threshold can be selected by COMP_REF_SEL[3:0] bits (see Table 55). The internal threshold is in common to all the AFE channels.
COMP3_INV	Sets the comparator 3 output polarity: • 0: direct output. The comparator's logic triggers when the positive input is above the negative input. • 1: inverted output. The comparator's logic triggers when the positive input is below the negative input.	-	
PGA3_GAIN[1:0]	Sets the PGA3 differential gain: • 00: Gain = 4 • 01: Gain = 8 (default) • 10: Gain = 16 • 11: Gain = 32	-	

5.12.4.16 *COMP_CFG register*

- Address: 0x0F
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0x07. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

Table 64. COMP_CFG register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	NOT USED	NOT USED	NOT USED	SAFE_DRV_SEL[1:0]		COMP3_SOFT_OFF	COMP2_SOFT_OFF	COMP1_SOFT_OFF
Default value	0	0	0	0	0	1	1	1

Table 65. COMP_CFG register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	NOT USED	NOT USED	NOT USED	SAFE_DRV_SEL[1:0]		NOT USED	NOT USED	COMP1_SOFT_OFF
Default value	0	0	0	0	0	1	1	1

Table 66. COMP_CFG register fields description

Field name	Description	Type	Notes
SAFE_DRV_SEL[1:0]	Selects the gate drivers' turn-off strategy in case of a fault on the AFE comparators according to Table 67.	-	See Section 5.3.5.
COMP3_SOFT_OFF	Enables/disables the soft-off feature in case of a fault triggered by the comparator 3. • 0: soft-off feature disabled. • 1: soft-off feature enabled.	-	See Section 5.4. The soft turn-off is applied to all the MOSFETs in the power stage or only to a part of them, according to the SAFE_DRV_SEL[1:0] setting (see Table 67)
COMP2_SOFT_OFF	Enables/disables the soft-off feature in case of a fault triggered by the comparator 2. • 0: soft-off feature disabled. • 1: soft-off feature enabled.	-	See Section 5.4. The soft turn-off is applied to all the MOSFETs in the power stage or only to a part of them, according to the SAFE_DRV_SEL[1:0] setting (see Table 67)
COMP1_SOFT_OFF	Enables/disables the soft-off feature in case of a fault triggered by the comparator 1. • 0: soft-off feature disabled. • 1: soft-off feature enabled.	-	See Section 5.4. The soft turn-off is applied to all the MOSFETs in the power stage or only to a part of them, according to the SAFE_DRV_SEL[1:0] setting (see Table 67)

Table 67. **Safe state of the gate drivers' outputs after a comparator's event**

SAFE_DRV_SEL[1:0]	Safe state description
00	**"All HS & LS" (default)** **The STDRIVE102BP/P turns off all the external MOSFETs.**
01	"Matched HS & LS" The STDRIVE102BP turns off only the high-side and low-side MOSFETs of the half-bridge <x> corresponding to the comparator <x> generating the event. This configuration should not be used for STDRIVE102P.
10	"All HS" the STDRIVE102BP/P turns off all the high-side MOSFETs, while it drives the low-side MOSFETs according to their digital inputs.
11	"Bypass" No action is taken on the power stage.

5.12.4.17 *AFE_FLT_CH1 register*

- Address: 0x10
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xED. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register allows the configuration of the fault-management logic related to the comparator of the AFE channel 1 (refer to Section 5.3.5).

Table 68. AFE_FLT_CH1 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP1_FAULT_EN	COMP1_COUNT_EN	COMP1 _TDG[1:0]		COMP1_TDIS[3:0]			
Default value	1	1	1	0	1	1	0	1

Table 69. AFE_FLT_CH1 register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP1_FAULT_EN	COMP1_COUNT_EN	COMP1 _TDG[1:0]		COMP1_TDIS[3:0]			
Default value	1	1	1	0	1	1	0	1

Table 70. AFE_FLT_CH1 register fields description

Field name	Description	Type	Notes
COMP1_FAULT_EN	Defines if a detected event by comparator 1 generates a fault event: • 0: a detected event by comparator 1 is not considered a fault. • 1: a detected event by comparator 1 is considered a fault.	-	
COMP1_COUNT_EN	Enables/disables the fault down-counter associated with comparator 1 (COMP1_COUNT register): • 0: the down-counter is disabled; its value is frozen at the current value. • 1: the down-counter is enabled; its value decrements by 1 at every event triggered by comparator 1.	-	See also Section 5.12.4.20. Note that the down-counter decrements only when the COMP1_FAULT_EN = 1.
COMP1 _TDG[1:0]	Sets the deglitch time $t_{DG(COMP)}$ of comparator 1: • 00: disabled • 01: 0.6 µs • 10: 1.3 µs (default) • 11: 2.5 µs	-	
COMP1_TDIS[3:0]	Sets the disable time of comparator 1 according to Table 71.	-	

Table 71. **Disable time of comparators values ($t_{dis,comp}$)**

COMP<x>_TDIS[3:0]	$t_{dis,comp}$ [µs]
0000	0
0001	10
0010	15
0011	20
0100	25
0101	35
0110	45
0111	55
1000	75
1001	110
1010	160
1011	220
1100	330
1101	**550 (default)**
1110	880
1111	1100

5.12.4.18 *AFE_FLT_CH2 register*

- Address: 0x11
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xED. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register allows the configuration of the fault-management logic related to the comparator of the AFE channel 2 (refer to Section 5.3.5).

This register is not available in STDRIVE102P.

Table 72. AFE_FLT_CH2 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP2_FAULT_EN	COMP2_COUNT_EN	COMP2 _TDG[1:0]		COMP2_TDIS[3:0]			
Default value	1	1	1	0	1	1	0	1

Table 73. AFE_FLT_CH2 register fields description

Field name	Description	Type	Notes
COMP2_FAULT_EN	Defines if a detected event by comparator 2 generates a fault event: • 0: a detected event by comparator 2 is not considered a fault. • 1: a detected event by comparator 2 is considered a fault.	-	
COMP2_COUNT_EN	Enables/disables the fault down-counter associated with comparator 2 (COMP2_COUNT register): • 0: the down-counter is disabled; its value is frozen at the current value. • 1: the down-counter is enabled; its value decrements by 1 at every event triggered by comparator 2.	-	See also Section 5.12.4.21. Note that the down-counter decrements only when the COMP2_FAULT_EN = 1.
COMP2 _TDG[1:0]	Sets the deglitch time $t_{DG(COMP)}$ of comparator 2: • 00: disabled • 01: 0.6 µs • 10: 1.3 µs (default) • 11: 2.5 µs	-	
COMP2_TDIS[3:0]	Sets the disable time of comparator 2 according to Table 71.	-	

5.12.4.19 *AFE_FLT_CH3 register*

- Address: 0x12
- Access mode: write-protected / read. Accessing this register in write mode while the registers are locked has no effect but latching the SPI_ERROR bit in the STATUS1 register (bit 0).
- Default value: 0xED. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register allows the configuration of the fault-management logic related to the comparator of the AFE channel 3 (refer to Section 5.3.5). This register is not available in STDRIVE102P.

Table 74. AFE_FLT_CH3 register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP3_FAULT_EN	COMP3_COUNT_EN	COMP3 _TDG[1:0]		COMP3_TDIS[3:0]			
Default value	1	1	1	0	1	1	0	1

Table 75. AFE_FLT_CH3 register fields description

Field name	Description	Type	Notes
COMP3_FAULT_EN	Defines if a detected event by comparator 3 generates a fault event: • 0: a detected event by comparator 3 is not considered a fault. • 1: a detected event by comparator 3 is considered a fault.	-	
COMP3_COUNT_EN	Enables/disables the fault down-counter associated with comparator 3 (COMP3_COUNT register): • 0: the down-counter is disabled; its value is frozen at the current value. • 1: the down-counter is enabled; its value decrements by 1 at every event triggered by comparator 3.	-	See also Section 5.12.4.22. Note that the down-counter decrements only when the COMP3_FAULT_EN = 1.
COMP3 _TDG[1:0]	Sets the deglitch time $t_{DG(COMP)}$ of comparator 3: • 00: disabled • 01: 0.6 µs • 10: 1.3 µs (default) • 11: 2.5 µs	-	
COMP3_TDIS[3:0]	Sets the disable time of comparator 3 according to Table 71.	-	

5.12.4.20 *COMP1_COUNT register*

- Address: 0x13
- Access mode: write / read.
- Default value: 0x00. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register stores the number of the remaining fault events related to comparator 1 before a permanent latch occurs. See Section 5.3.5 for details.

Table 76. COMP1_COUNT register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP1_COUNT[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 77. COMP1_COUNT register in STDRIVE102P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP1_COUNT[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 78. COMP1_COUNT register fields description

Field name	Description	Type	Notes
COMP1_COUNT[7:0]	Down-counter of the comparator 1 fault events. If enabled by COMP1_COUNT_EN = 1, it decrements by 1 each time a fault event by comparator 1 occurs. If its value is 0x00 (end count), the next fault causes the protection to be permanently latched in the fault state.	Real Time	See Section 5.3.5 for details.

5.12.4.21 *COMP2_COUNT register*

- Address: 0x14
- Access mode: write / read.
- Default value: 0x00. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register stores the number of the remaining fault events related to comparator 2 before a permanent latch occurs. See Section 5.3.5 for details.

This register is not available in STDRIVE102P.

Table 79. COMP2_COUNT register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP2_COUNT[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 80. COMP2_COUNT register fields description

Field name	Description	Type	Notes
COMP2_COUNT[7:0]	Down-counter of the comparator 2 fault events. If enabled by COMP2_COUNT_EN = 1, it decrements by 1 each time a fault event by comparator 2 occurs. If its value is 0x00 (end count), the next fault causes the protection to be permanently latched in the fault state.	Real Time	See Section 5.3.5 for details.

5.12.4.22 *COMP3_COUNT register*

- Address: 0x15
- Access mode: write / read.
- Default value: 0x00. Default value is to be intended as the read-value expected after software reset (see DEV_RESET register, Section 5.12.4.24) with all the supply rails stable (VS, VM, VCC, VBOOT) and $T_j < T_{j(WRN)}$.

This register stores the number of the remaining fault events related to comparator 3 before a permanent latch occurs. See Section 5.3.5 for details.

This register is not available in STDRIVE102P.

Table 81. COMP3_COUNT register in STDRIVE102BP

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	COMP3_COUNT[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 82. COMP3_COUNT register fields description

Field name	Description	Type	Notes
COMP3_COUNT[7:0]	Down-counter of the comparator 3 fault events. If enabled by COMP3_COUNT_EN = 1, it decrements by 1 each time a fault event by comparator 3 occurs. If its value is 0x00 (end count), the next fault causes the protection to be permanently latched in the fault state.	Real Time	See Section 5.3.5 for details.

5.12.4.23 *CMD_CLEAR command register*

- Address: 0x1A
- Access mode: write-only.

This command register can be accessed and its commands are executed regardless if the register is locked or unlocked (see Section 5.12.1).

According to the written data (command code), a different action is performed, as per Table 84. Any other command code is ignored and latches the SPI_ERROR bit in the STATUS1 register (bit 0).

Access in read mode is allowed and does not generate a SPI_ERROR, however the returned data are meaningless.

Table 83. CMD_CLEAR register in STDRIVE102BP/P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	CMD_CLEAR[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 84. **CMD_CLEAR register command codes description**

CMD_CLEAR[7:0] (command code)	Actions	Details
0x90	Resets all the latched bits in the STATUS1 register (bits 6 down to 0)	nVDS_FAULT_L ⇒ 1 nVCP_UV_L ⇒ 1 nVCC_UV_L ⇒ 1 nVDD_UV_L ⇒ 1 nTH_SD_L ⇒ 1 nCOMP_EVENT_L ⇒ 1 SPI_ERROR ⇒ 0
	Resets all the latched bits in the STATUS2 register (bits 2 down to 0)	nCOMP1_EVENT_L ⇒ 1 nCOMP2_EVENT_L ⇒ 1 nCOMP3_EVENT_L ⇒ 1
	This command allows clearing only the latched status bits, which keep track of the occurrence of previous events. This command does not release the permanent latch introduced by comparators / V_{DS} monitoring. In case a permanent latch is present, the power stage is kept disabled.	
0x05	Releases the permanently latched faults due to comparators and V_{DS} monitoring: the protection is released and the power stage returns operative. As a consequence, the bits related to the comparators and V_{DS} monitoring protections are cleared. In particular, for the comparators refer to bits 2:0 in the AFE_STATUS register; for V_{DS} monitoring refers to bits 5:0 in the STATUS3 register. This command does not clear the latched status bits in STATUS1 and STATUS2 register tracking the previous events occurrence.	nVDS_HS1_FAULT ⇒ 1 nVDS_HS2_FAULT ⇒ 1 nVDS_HS3_FAULT ⇒ 1 nVDS_LS1_FAULT ⇒ 1 nVDS_LS2_FAULT ⇒ 1 nVDS_LS3_FAULT ⇒ 1 nCOMP1_FAULT ⇒ 1 nCOMP2_FAULT ⇒ 1 nCOMP3_FAULT ⇒ 1
0x95	Has the same cumulative effect of command codes 0x90 and 0x05	
0x68	Resets RESET_STATE bit in the STATUS2 register. This bit is set to 1 only by a software reset (Section 5.12.4.24), at power-up or entering the standby mode.	RESET_STATE ⇒ 0

5.12.4.24 *DEV_RESET command register*

- Address: 0x1B
- Access mode: write-protected / write-only.

This register is a write-protected command register which resets the device to the default condition, including all registers values.

Write access must be done while the registers are unlocked (see Section 5.12.1); any attempt to write the DEV_RESET register when the registers are locked has no effect but latches the SPI_ERROR bit in the STATUS1 register (bit 0).

The only command code accepted by this register is 0xA7; any other value is ignored and latches the SPI_ERROR bit in the STATUS1 register (bit 0).

Access in read mode is allowed and does not generate a SPI_ERROR, however the returned data are meaningless.

After a DEV_RESET command, the device reverts to the locked state.

Table 85. DEV_RESET register in STDRIVE102BP/P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	DEV_RESET[7:0]							
Default value	0	0	0	0	0	0	0	0

5.12.4.25 *CMD_LOCK command register*

- Address: 0x1C
- Access mode: write-only.

This register is a write only command register, it is used to lock or unlock the protected registers (see Section 5.12.1).

Accepted command codes are listed in Table 87; any other value is ignored and latches the SPI_ERROR bit in the STATUS1 register (bit 0)

Access in read mode is allowed and does not generate a SPI_ERROR, however the returned data are meaningless.

Table 86. CMD_LOCK register in STDRIVE102BP/P

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field name	CMD_LOCK[7:0]							
Default value	0	0	0	0	0	0	0	0

Table 87. CMD_LOCK register command codes description

CMD_CLEAR[7:0] (command code)	Actions	Notes
0x4B	Protected registers are unlocked and it is possible to write them.	Sending command code 0x4B while the registers are already unlocked has no effects.
0x71	Protected registers are locked and it is not possible to write them.	Sending command code 0x71 while the registers are already locked has no effects.

6 Application examples

6.1 3-phase brushless motor application with triple shunt current sensing based on STDRIVE102BP

Figure 41 shows an application example using the STDRIVE102BP to drive a 3-phase motor with triple shunt configuration. The list of components is summarized in Table 88.

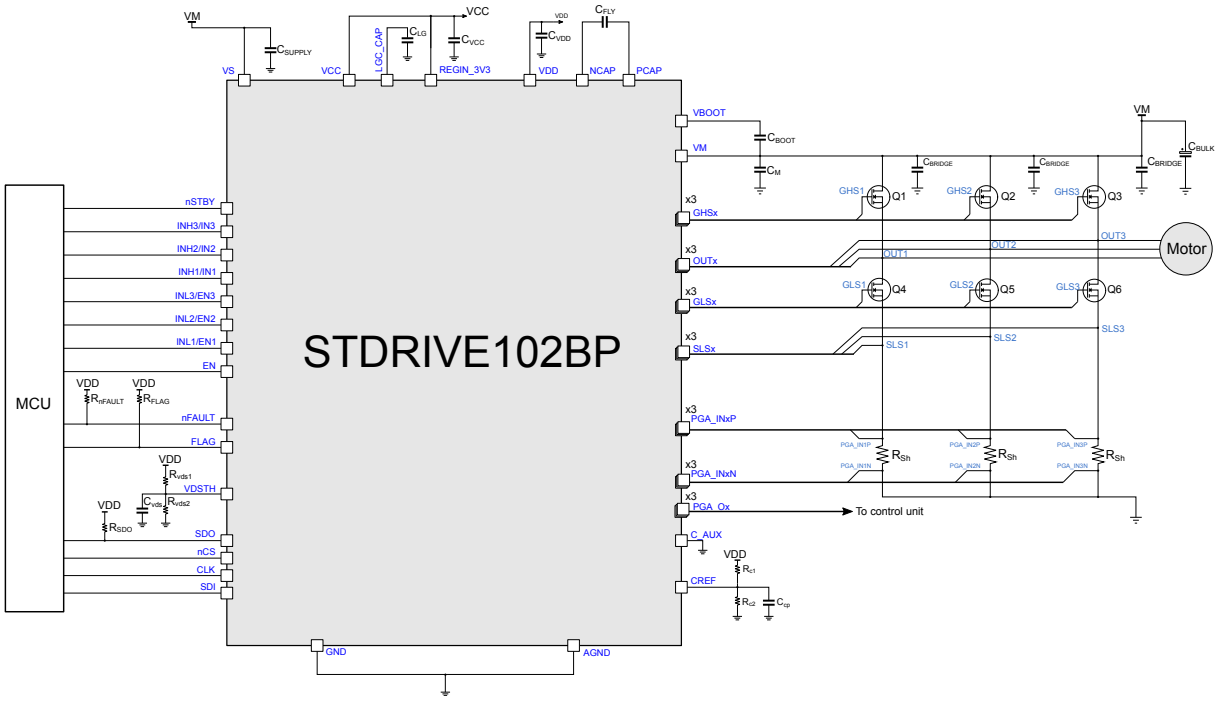
The values reported in Table 88 refer to a generic example. The actual components' values must be chosen to fit the specific application requirements. The value of the resistors on VDSTH pins must be sized according to the specific power stage. The shunt resistors must be sized according to the current rating of the application.

Table 88. STDRIVE102BP list of components

	Value
C_{BRIDGE}	220 nF (to be tuned according to the current rating of the power stage)
C_{BULK}	470 µF (to be tuned according to the current rating of the power stage)
C_M	1 µF low ESR to be placed close to the driver
R_{sh}	According to the current rating of the application (for example 2 mΩ)
R_{c1}, R_{c2}	According to the CREF threshold (for example 100 kΩ, 7.5 kΩ: V_{CREF} = 230 mV)
C_{cp}	10 nF / 16 V
R_{vds1} , R_{vds2}	1% precision, values according to V_{DS} monitoring threshold (for example R_{vds1} = 220 kΩ, R_{vds2} = 15 kΩ: V_{DSTH} = 210 mV)
C_{vds}	10 nF / 16 V
R_{nFAULT}	33 kΩ
R_{FLAG}	33 kΩ
R_{SDO}	33 kΩ (1)
C_{SUPPLY}	1 µF low ESR to be placed close to the driver
C_{LG}	4.7 µF / 16 V
C_{VCC}	4.7 µF / 25 V
C_{VDD}	4.7 µF / 16 V
C_{BOOT}	1 µF / 25 V
C_{FLY}	220 nF (according to V_M rating)

1. *Consider that this value must be reduced if the communication speed increases. For example, at 10 MHz (maximum speed) and 20 pF line capacitance, use 1 kΩ.*

Figure 41. **STDRIVE102BP typical application example**



6.2 3-phase brushless motor application with single shunt current sensing based on STDRIVE102P

Figure 42 shows an application example using STDRIVE102P to drive a 3-phase motor with single shunt configuration. The list of components is summarized in Table 89.

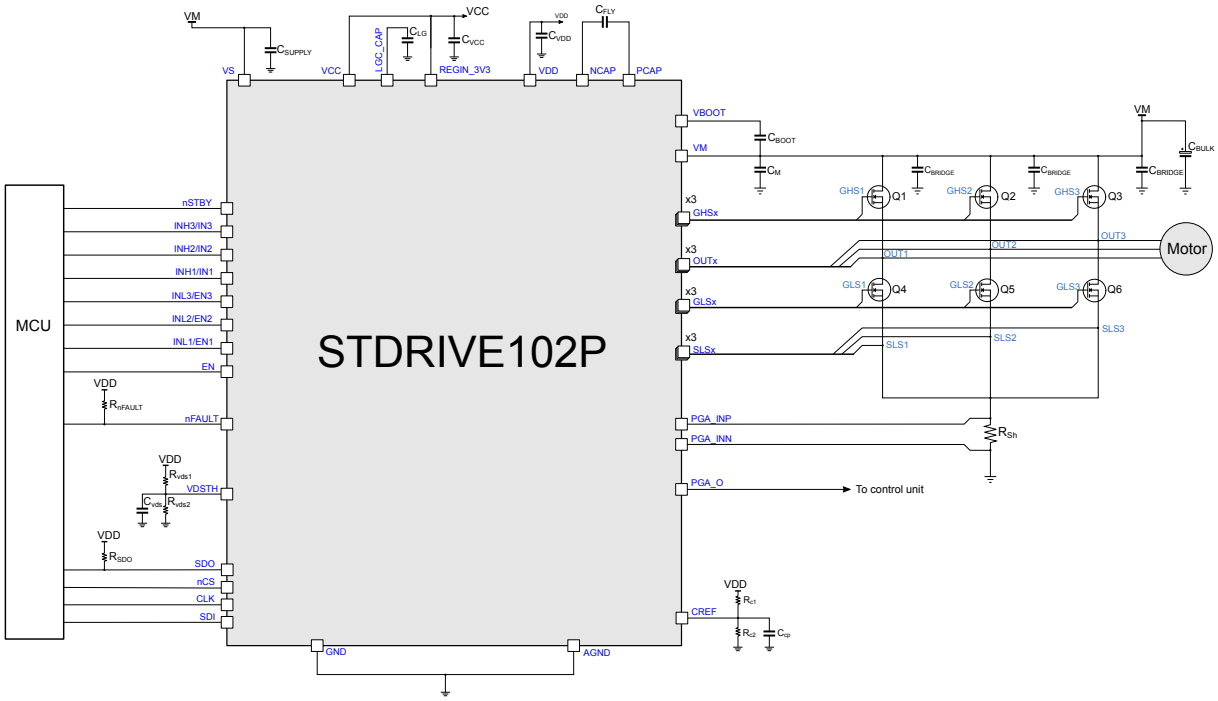
The values reported in Table 89 refer to a generic example. The actual components' values must be chosen to fit the specific application requirements. The value of the resistors on the VDSTH pins must be sized according to the specific power stage. The shunt resistor must be sized according to the current rating of the application.

Table 89. STDRIVE102P list of components

	Value
C_{BRIDGE}	220 nF (to be tuned according to the current rating of the power stage)
C_{BULK}	470 µF (to be tuned according to the current rating of the power stage)
C_M	1 µF low ESR to be placed close to the driver
R_{sh}	According to the current rating of the application (for example 2 mΩ)
R_{c1}, R_{c2}	According to the CREF threshold (for example 100 kΩ, 7.5 kΩ: V_{CREF} = 230 mV)
C_{cp}	10 nF / 16 V
R_{vds1} , R_{vds2}	1% precision, values according to V_{DS} monitoring threshold (for example R_{vds1} = 220 kΩ, R_{vds2} = 15 kΩ: V_{DSTH} = 210 mV)
C_{vds}	10 nF / 16 V
R_{nFAULT}	33 kΩ
R_{SDO}	33 kΩ (1)
C_{SUPPLY}	1 µF low ESR to be placed close to the driver
C_{LG}	4.7 µF / 16 V
C_{VCC}	4.7 µF / 25 V
C_{VDD}	4.7 µF / 16 V
C_{BOOT}	1 µF / 25 V
C_{FLY}	220 nF (according to V_M rating)

1. *Consider that this value must be reduced if the communication speed increases. For example, at 10 MHz (maximum speed) and 20 pF line capacitance, use 1 kΩ.*

Figure 42. **STDRIVE102P typical application example**



7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 VFQFPN 48L 6x6x1 mm, pitch 0.4 mm package information

Figure 43. VFQFPN 48L 6x6x1 mm, pitch 0.4 mm package outline

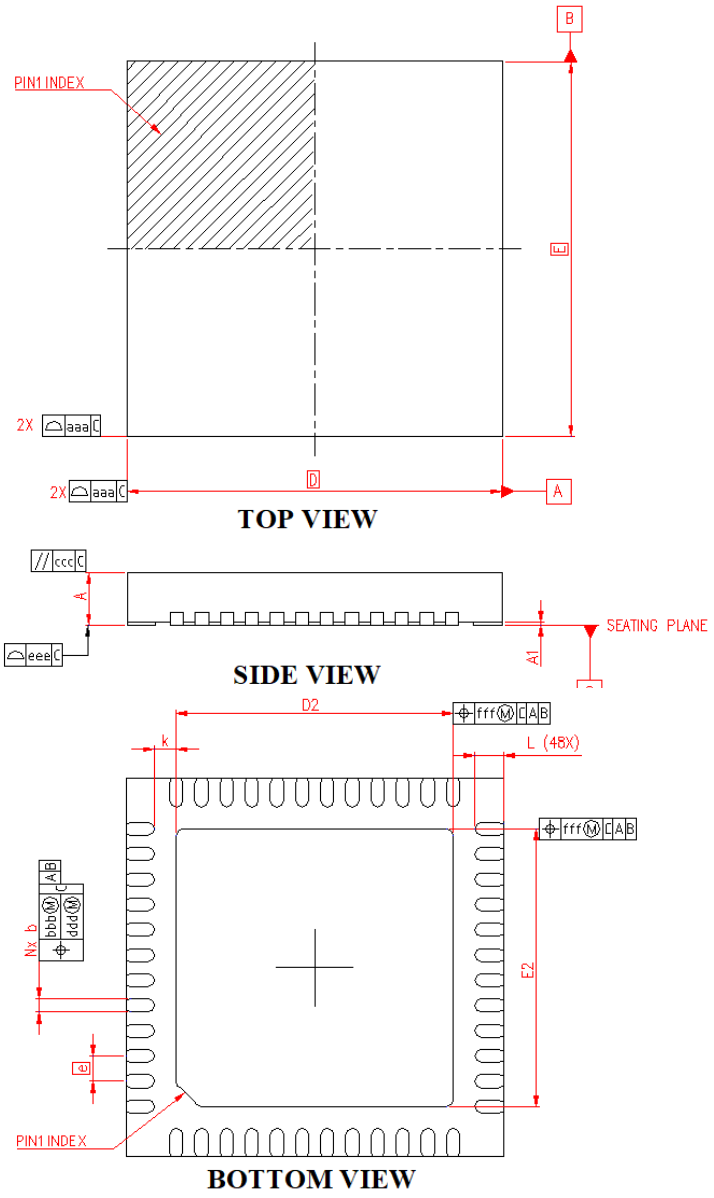
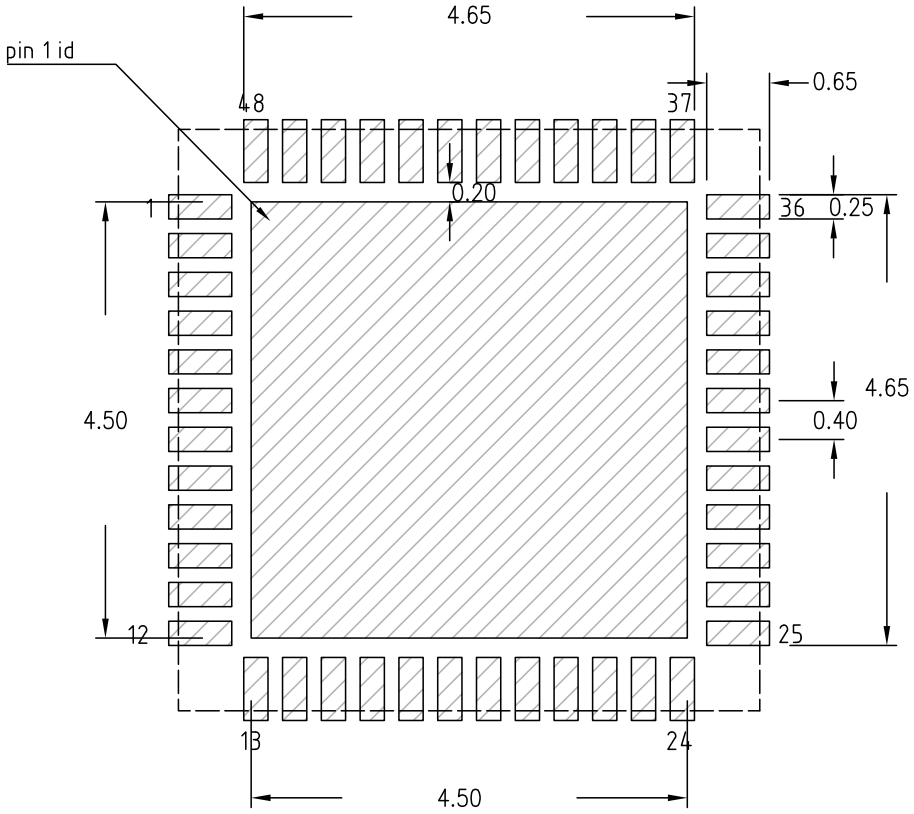


Table 90. **VFQFPN 48L 6x6x1 mm, pitch 0.4 mm package mechanical data**

Symbol	Dimensions [mm]		
	Min.	Typ.	Max.
A	0.80	0.85	1.00
A1	0.00	-	0.05
b	0.17	0.21	0.25
D		6.0 BSC	
D2	4.3	4.4	4.5
e		0.4 BSC	
E		6.0 BSC	
E2	4.3	4.4	4.5
L	0.35	0.45	0.55
K	0.24		
N		48	
Tolerance			
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

7.1.1 Suggested footprint

Figure 44. **VFQFPN 48L 6x6x1 mm, pitch 0.4 mm suggested footprint**



7.2 VFQFPN 40L 5x5x1 mm, pitch 0.4 package information

Figure 45. **VFQFPN 40L 5x5x1 mm, pitch 0.4 package outline**

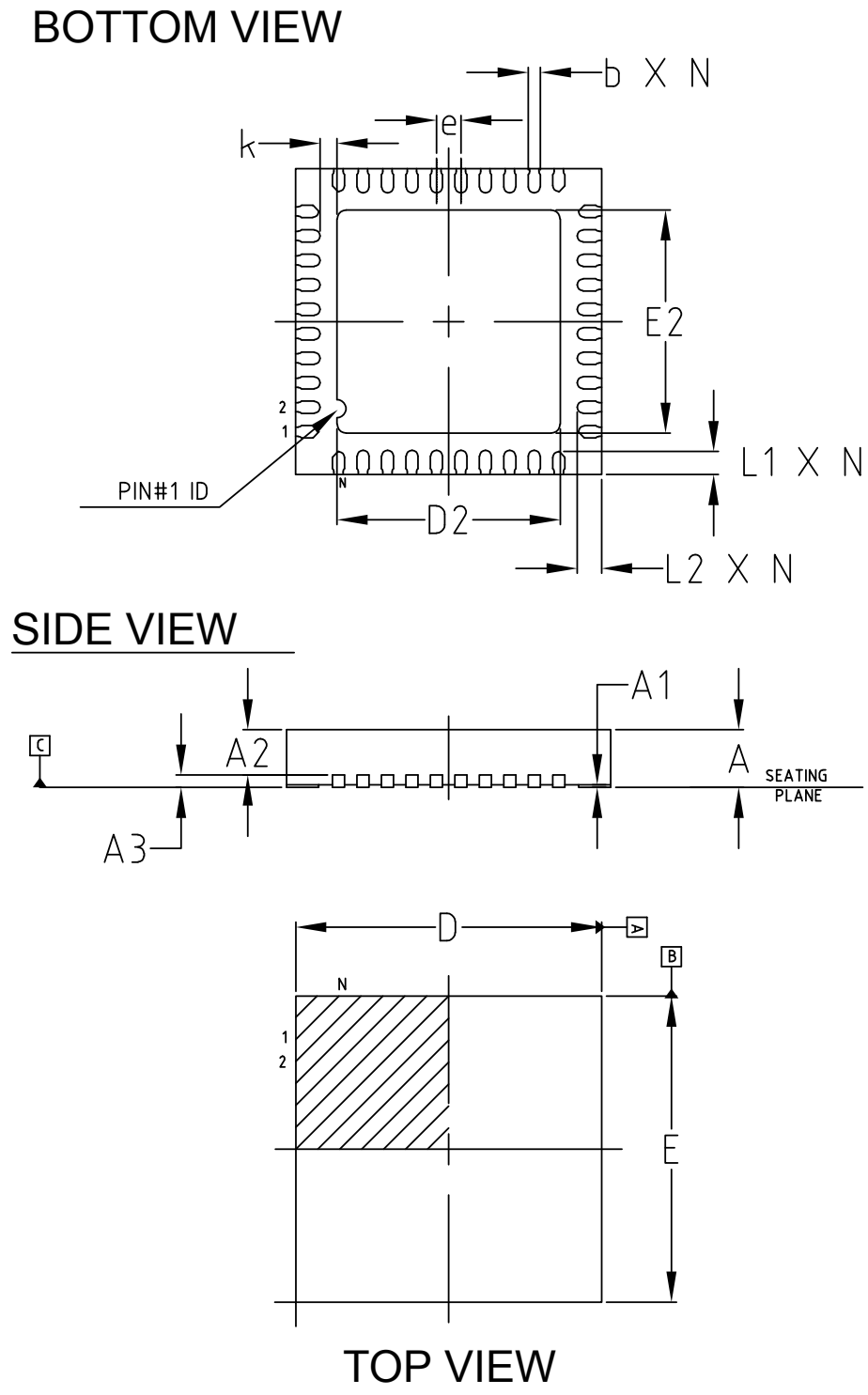
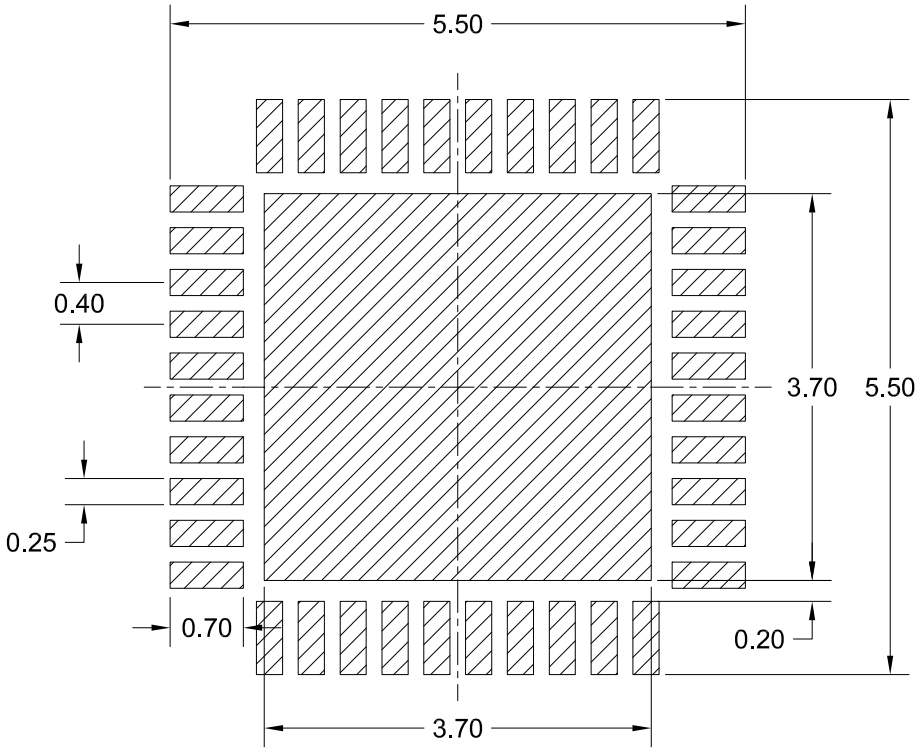


Table 91. **VFQFPN 40L 5x5x1 mm, pitch 0.4 package mechanical data**

Symbol	Dimensions [mm]		
	Min.	Typ.	Max.
A	0.80	0.85	1.00
A1	0.00	-	0.05
A2	0.55	0.65	0.75
A3		0.20 REF	
b	0.15	0.20	0.25
D		5.00 BSC	
D2	3.55	3.65	3.75
e		0.40 BSC	
E		5.00 BSC	
E2	3.55	3.65	3.75
L1	0.277	0.377	0.477
L2	0.30	0.40	0.50
k	0.2	-	-
N		40	
Tolerance			
aaa		0.15	
bbb		0.10	
ccc		0.08	
ddd		0.05	
eee		0.10	

7.2.1 Suggested footprint

Figure 46. **VFQFPN 40L 5x5x1 mm, pitch 0.4 mm suggested footprint**



8 Ordering information

Table 92. **Order code**

Order code	Package	Package marking	Packing
STDRIVE102BP	VFQFPN 48L 6x6x1 mm, pitch 0.4 mm	DRV102BP	Tray
STDRIVE102BPTR	VFQFPN 48L 6x6x1 mm, pitch 0.4 mm	DRV102BP	Tape and reel
STDRIVE102P	VFQFPN 40L 5x5x1 mm, pitch 0.4 mm	DRV102P	Tray
STDRIVE102PTR	VFQFPN 40L 5x5x1 mm, pitch 0.4 mm	DRV102P	Tape and reel

Revision history

Table 93. **Document revision history**

Date	Version	Changes
19-Jan-2026	1	Initial release.

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