

## RF power amplifier demonstration board based on the STAC2942B

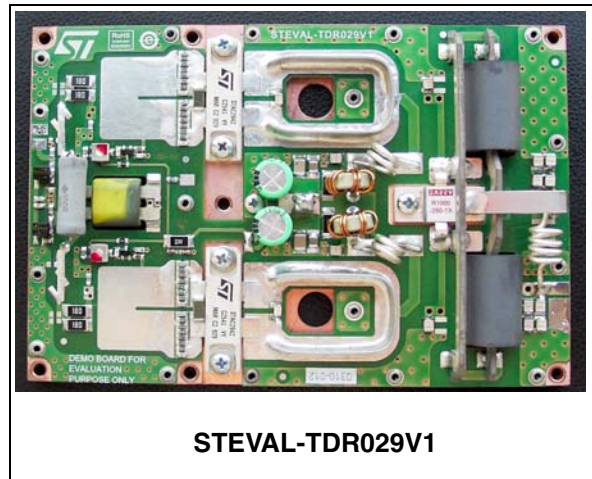
### Features

- Excellent thermal stability
- Frequency: 87.5 - 108 MHz
- Supply voltage: 48 V
- Output power: 700 W min
- Gain: 20 dB typ.
- Efficiency: 77 % typ
- Harmonics: - 36 dBc max
- Gain flatness:  $\pm 0.5$  dB max

### Description

The STEVAL-TDR029V1 is a RF broadband power amplifier intended for FM broadcast radio transmitters over the band 87.5 to 108 MHz using 2x STAC2942B N-channel MOS field-effect transistors.

STEVAL-TDR029V1 is designed in cooperation with InnovAction S.r.l in Italy.



**Table 1. Device summary**

Order code
STEVAL-TDR029V1

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# 1 Electrical data

## 1.1 Maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
P <sub>IN</sub>	Input power	15	W
P <sub>OUT</sub>	Output power	800	W
T <sub>STG</sub>	Storage temperature range	-20 to +70	°C
T <sub>C</sub>	Operating base plate temperature	0 to +70	°C
I <sub>DD</sub>	Drain current	22	A
P <sub>DISS</sub>	Power dissipation	400	W

## 2 Electrical characteristics

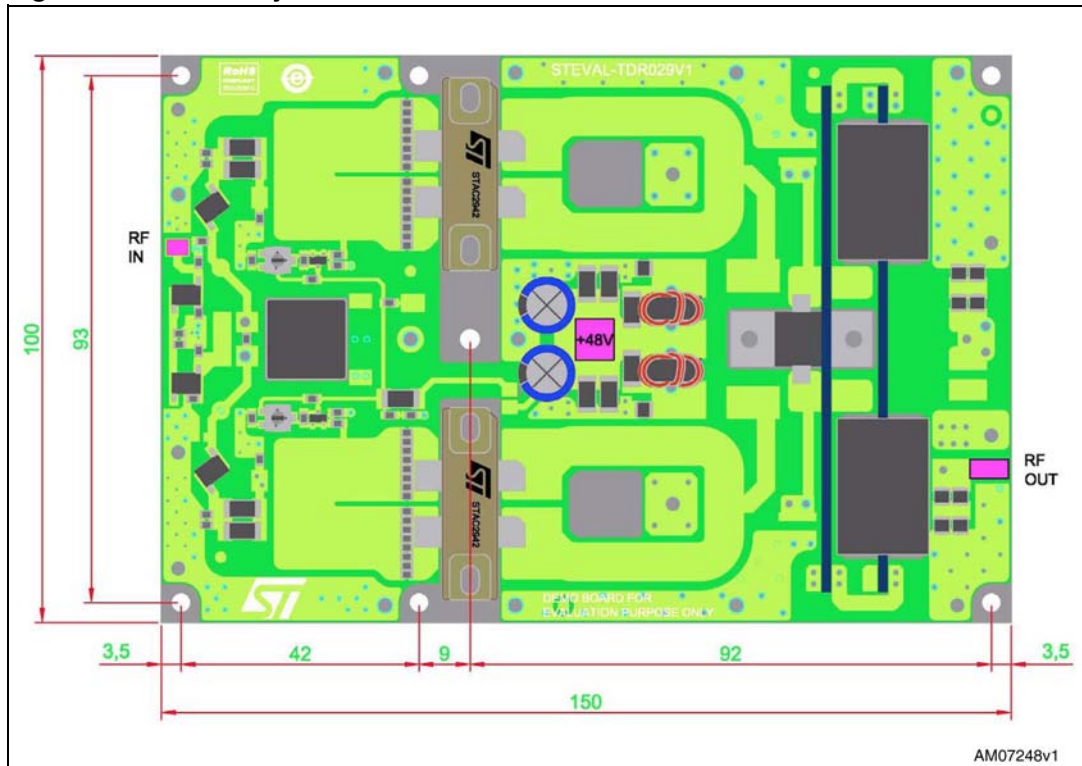
T<sub>A</sub> = +25 °C, V<sub>DD</sub> = 48 V, I<sub>dq</sub> = 2 x 200 mA

**Table 3. Electrical specification**

Symbol	Test conditions	Min	Typ	Max	Unit
Frequency	Frequency range	87.5		108	MHz
P <sub>OUT</sub>		700		750	W
Gain	P <sub>OUT</sub> = 700 W	20 ± 1			dB
ND	P <sub>OUT</sub> = 700 W	77			%
H2	2 <sup>nd</sup> harmonic @ P <sub>OUT</sub> = 700 W	-40			dBc
H3	3 <sup>rd</sup> harmonic @ P <sub>OUT</sub> = 700 W	-45			dBc
FL	Gain flatness @ P <sub>OUT</sub> = 700 W			± 0.5	dB

### 3 Circuit layout and connections

Figure 1. Circuit layout and connections



## 4 STAC2942B mounting recommendations

### 4.1 Introduction

RF power transistors are amongst the highest power density devices in the semiconductor industry. It is crucial to the reliability and performance of such devices to give additional consideration to mechanical stresses and thermal and electrical resistances within the application environment.

The general purpose of this section is to provide guidelines for mechanically mounting STAC™ bolt-down packages so as to minimize stress and resistance. More specifically, attention is paid to the STAC244B and STAC265B package families which are used for various VDMOS and LDMOS products.

### 4.2 Heat sink selection and preparation

The choice of heatsinking system depends on the specific device and application needs; this decision results in the total power dissipation capability for the amplifier assembly.

In most cases, the power transistor may be mounted directly to a typical heatsink, such as a low-cost, extruded aluminum heatsink with fins. Such a system has good thermal and electrical properties for most operating conditions.

In cases of higher power dissipation, additional spreading of the thermal flux can be managed with a copper core heat-spreading layer between the transistor and heatsink. Such a system can be designed for excellent thermal and electrical properties for the most demanding operating conditions.

When the operating conditions of the device are such that the dissipated power is low, for example in low duty cycle or back-off power conditions, a basic thermal core layer without fins may be all that is required to maintain a high MTTF or adherence to a maximum rating.

The preferred material layer to which the package is attached is OFHC (UNS C10100) copper, but may also be a lower quality copper or aluminum as required by detailed application needs. Based on requirements for typical applications, the thickness of this layer is expected to be:

- Min.: 0.12 in (3.0 mm)
- Typ.: 0.22 in (5.6 mm)
- Max.: 0.32 in (8.1 mm)

Since holes are to be tapped into the thermal core layer for device attachment, it is advised to drill and tap through the entire layer whenever possible. For the recommended screws, the minimum tapped hole depth should be 0.12 in (3.0 mm).

By design, the STAC244B and STAC265B package family do not require complex heatsink or core preparation, such as channels, pockets, cavities, etc., assuming a typical PCB thickness is selected for the application.

### 4.3 Surface conditions of the mounting base

The mounting base, or surface of the heatsink to which the backside of the package is mounted, must be flat, clean, and free of tool marks.

- Flatness: 400  $\mu\text{in/in}$  (0.4  $\mu\text{m/mm}$ )
- Roughness:  $R_a < 30 \mu\text{in}$  (0.8  $\mu\text{m}$ )

Flatness and roughness values can be achieved on the above-mentioned materials with standard machining processes, such as milling.

Holes for screws, solder wells, etc. should be slightly countersunk and/or de-burred.

### 4.4 Thermal interface material

Careful consideration must be paid to the actual interface layer between the backside of the package and the mounting base. Cleanliness is key: particulates, grease, and oxidation should be removed using standard practices.

A thermal interface material (TIM) of good thermal conductivity should be used in order to fill any discontinuities between the package and mounting base surface. The decision of which TIM material to use is based on many factors. Many types of TIMs are available today with an incredible range of thermal/electrical/mechanical properties. Several are listed here:

- WPSII (a silicone-free compound, Austerlitz Electronics),
- Type 340 (Dow Corning)
- Type 120 (a silicone compound, Wakefield Thermal Solutions)
- Indium foil (Indium Corp.)
- Sn63Pb37 or Pb-free solder

In all cases, the chosen TIM should be no thicker than necessary and applied as evenly as possible. For liquid compounds, it is easiest to apply to the backside of the package, keeping in mind that excessive TIM thickness results in a higher thermal resistance than using no TIM at all. For foils and soldering it is best to specify an appropriately-sized "preform" and apply it to the thermal base.

### 4.5 Seating plane

The seating plane refers to the distance between the thermal base and the bottom of the transistor leads. This is shown on the package outline drawing to indicate the total thickness of the PCB, or PCB+channel depth of the heatsink. Some points to consider are:

- The leads of the transistor should launch perpendicular to the package body onto the traces of the PCB to reduce mechanical stress to the package and solder joints. In some cases, the PCB fabrication tolerances are such that the leads extend above the plane defined by the top of the PCB; this situation is best handled with a judicious selection of solder pad preform or paste thickness, or by a slight downward bending of the transistor leads (no more than 0.01 in (0.25 mm)). In no case should the leads be bent higher than the topside of the PCB, to avoid shear stresses which could cause damage to the interface between the lead and the package body.
- Care should be taken to factor in the thickness of the TIM used, which is equivalent to increasing the seating plane dimension.

If the PCB is fused to the heatsink by means of a bonding film, solder layer, etc., the corresponding thickness of this layer should be factored into the PCB thickness.

## 4.6 Printed circuit board (PCB) considerations

It is advisable to specify a “package-cut”, or slot, through the board and mount the transistor directly to the heatsink for optimum performance. The dimensions for this slot should be approximately 0.010 to 0.025 in (0.25 to 0.6 mm) larger than the outside dimensions of the package body to ensure a good fit and to relieve stress upon the leads.

These packages were designed to be compatible with PCBs having dielectric thicknesses in the range of 0.020 to 0.060 in (0.51 to 1.52 mm) - a wide range, covering a large scope of applications. As a general rule, as the thickness of the PCB increases within this range, the greater the offset dimensions for the slot should be designed.

Often, the PCB traces are slightly pulled back from the edge of the slot, which is also helpful in reducing stress upon the leads of the device. Solder pad layouts for the transistor leads should be designed to be as large as the circuit topology allows, but it is recommended that pad area be at least the maximum width and remaining length of the leads (approximately 0.15 in or 3.8 mm). In most cases a border around the leads of at least 0.01 in (0.25 mm) for solder is advised, which allows for a good solder fillet along three sides of each transistor lead.

## 4.7 Package attachment to thermal base

### 4.7.1 Hardware:

The recommended fastener system consists of:

- 2 4UNC (or M3) Torx, hex or Phillips cap screws (one for each end of the package body)
- 2 spring washers, ID=0.150" (3.81 mm) OD=0.275" (6.98 mm) t=0.015" (0.38 mm) h=0.025" (0.62 mm)

The procedure begins with the application of the TIM to the back of the package, followed by the insertion of the package into the application board. It is best to start the screws in both tapped holes, continuing in an alternating fashion to insure the package is seated flat and without obstructions.

To evenly distribute the pressure from the screw head/split washer combination, a flat washer with an outer diameter no greater than 0.28 in (7.1 mm) can be inserted between the split washer and the package body.

As a substitute for a split washer, a conical, Belleville, or wave washer can be used.

When this system is properly applied, uniform pressure with tolerance for thermal expansion is provided. The mechanical features designed into the STAC™ bolt-down package translate the force toward the center of the package at the prescribed screw torque. Along with the material set featuring low creep and fatigue resistance, the complete system insures that pressure is maintained uniformly over time.

### 4.7.2 Procedure:

Tighten both fastener systems to each end of the package body to a “finger-tight” condition, approximately 0.4 in-lb (0.05 N-m, 0.5 kg-cm).

Use a torque driver or equivalent means to tighten both screws to the recommended torque of 5 in-lbs (0.6 N-m, 5.8 kg-cm).

Depending upon the choice of TIM, the required torque may be adjusted within the following ranges without mechanical damage to the device:

- Min.: 3.5 in-lb (0.4 N-m, 4 kg-cm)
- Max.: 6.5 in-lb (0.75 N-m, 7.5 kg-cm)

## 4.8 Electrical connection

Leads and/or flanges should be attached to the PCB and/or copper heatsinks using typical Sn63Pb37 or Pb-free solders, in accordance with the supplier's recommendations. However, the following guidelines with respect to the package should be considered:

- Avoid, as much as possible, the use of flux or flux solutions as it is a potential source of contamination to the device.
- The leads of the transistor may be tinned prior to assembly into the PCB. This practice is used in situations when it is undesirable to introduce even a small amount of gold into the solder composition, forestalling the possibility of solder embrittlement issues. The source of Au stems from the lead and/or backside surfaces, which are plated with 40 to 100  $\mu\text{in}$  (1 to 2.5  $\mu\text{m}$ ) of Au.
- The amount of solder to be used depends on the type of solder and the amount of allowable Au in the final solder composition. It is desirable to increase the amount of solder when Au content is a concern, such as in Pb-free soldering applications.
- It is recommended to use either a solder preform or solder paste having a thickness of 0.001 to 0.010 in (0.03 to 0.3 mm), typically 0.006 in (.15 mm).
- Adjustment of the solder preform or paste thickness may be used advantageously to account for thickness variations in the PCB manufacturing process.

In cases where the backside of the flange is soldered to a copper core or heatsink, the package design and previously discussed mechanical mounting procedure provide sufficient downward pressure on the solder preform, resulting in a thin, high-quality bondline after a typical solder reflow procedure. In such cases, solder-wells or a solder-moat around the perimeter of the flange should be considered, to provide a region for excess solder to flow.

## 4.9 Conclusion

This section has provided a set of guidelines to be considered for the proper attachment of the STAC244B and STAC265B packages in the majority of applications. In most cases, these recommendations are expected to result in reliable mechanical, electrical, and thermal performance.

In terms of thermal resistance, these recommendations should provide an exceptionally low thermal resistance between the transistor case and the mounting base ( $R_{\text{thc-mb}}$ ), on the order of 0.05  $^{\circ}\text{C}/\text{W}$  for most products.



## 5 Revision history

Table 4. Document revision history

Date	Revision	Changes
03-Jun-2010	1	Initial release.

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