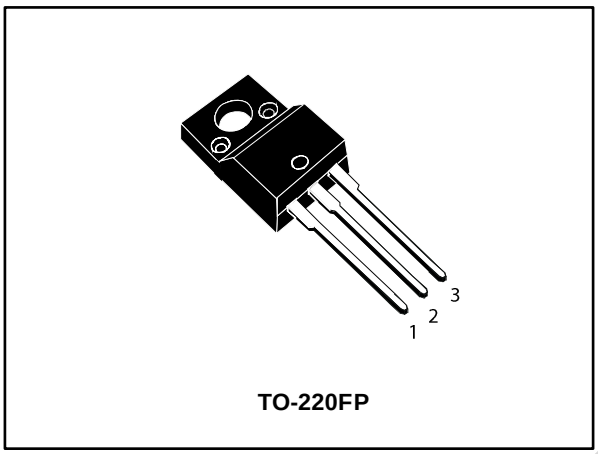
STF120NF10

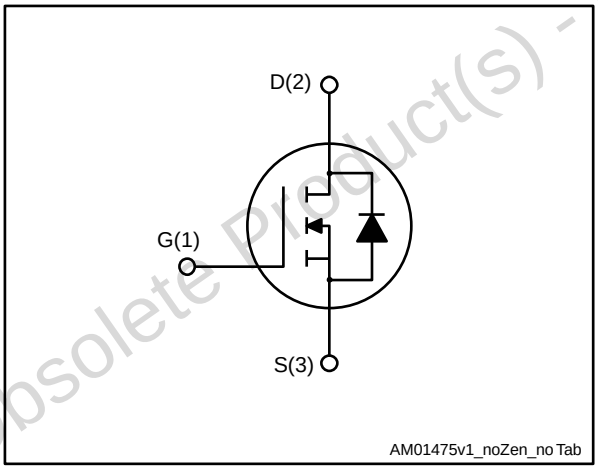
N-channel 100 V, 0.009 Ω, 110 A STripFET™ II Power MOSFET in TO-220FP package

Datasheet - obsolete product



TO-220FP

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF120NF10	100 V	<0.0105 Ω	41 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET series has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STF120NF10	120NF10	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0 V)	100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	41	A
	Drain current (continuous) at T_C = 100 °C	29	A
I_{DM}(1)	Drain current (pulsed)	164	A
P_{TOT}	Total dissipation at T_C = 25 °C	45	W
dv/dt(2)	Peak diode recovery voltage slope	10	V/ns
E_{AS}(3)	Single pulse avalanche energy	550	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width is limited by safe operating area.

(2)I_{SD} ≤ 120 A, di/dt ≤ 300 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

(3)Starting T_j =25 °C, I_D = 60 A, V_{DD} = 50 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.33	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_{CASE}= 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
		V_{GS} = 0 V, V_{DS}= 100 V, T_c = 125 °C(1)			10	µA
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A		0.009	0.0105	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 25 V, I_D = 60 A	-	90		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS}= 0 V	-	5200		pF
C_{oss}	Output capacitance			785		pF
C_{rss}	Reverse transfer capacitance			325		pF
Q_g	Total gate charge	V_{DD} = 80 V, I_D= 120 A, V_{GS} = 0 to 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	172	233	nC
Q_{gs}	Gate-source charge			32		nC
Q_{gd}	Gate-drain charge			64		nC

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 60 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	25	-	ns
t_r	Rise time		-	90	-	ns
$t_{d(off)}$	Turn-off delay time		-	132	-	ns
t_f	Fall time		-	68	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source drain current		-		110	A
I_{SDM}(1)	Source-drain current (pulsed)		-		440	A
V_{SD}(2)	Forward on voltage	I_{SD} = 120 A, V_{GS}= 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs, V_{DD} = 40 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	152		ns
Q_{rr}	Reverse recovery charge		-	760		nC
I_{RRM}	Reverse recovery current		-	10		A

Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

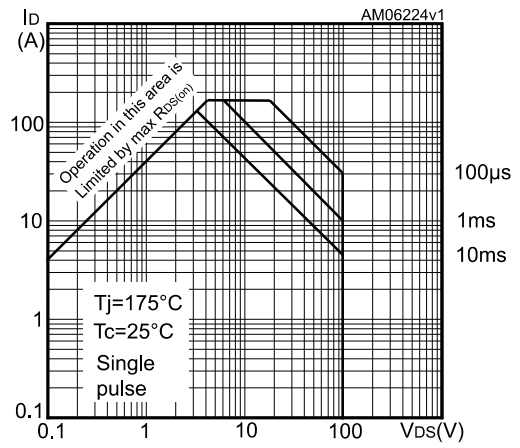


Figure 3: Thermal impedance

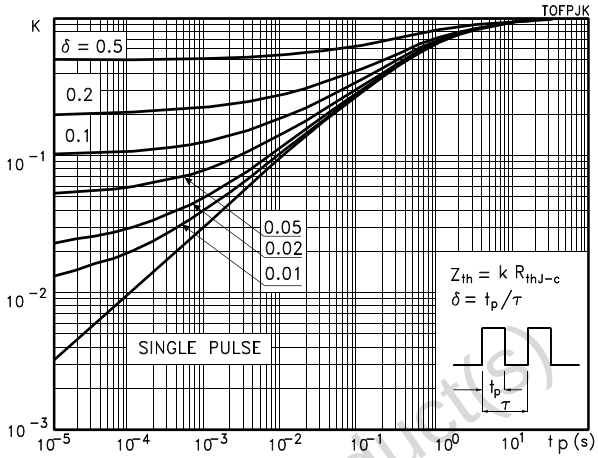


Figure 4: Output characteristics

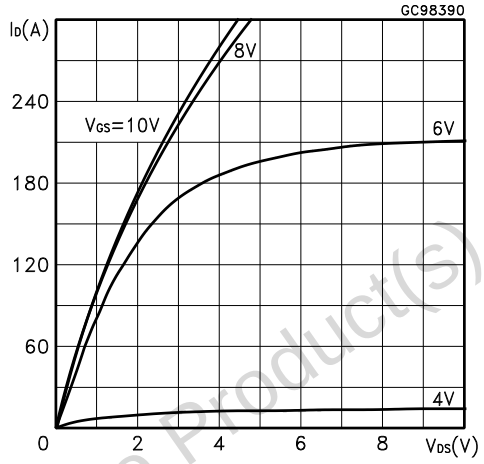


Figure 5: Transfer characteristics

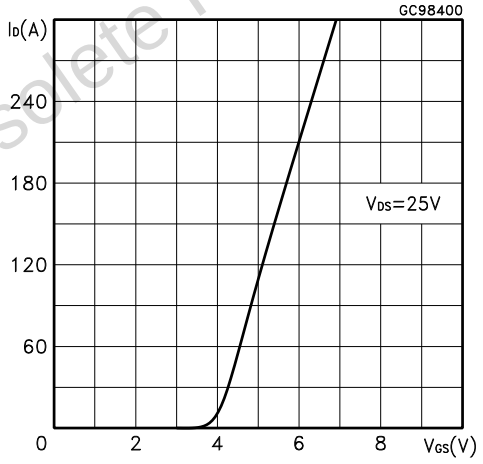


Figure 6: Normalized B_{VDSS} vs temperature

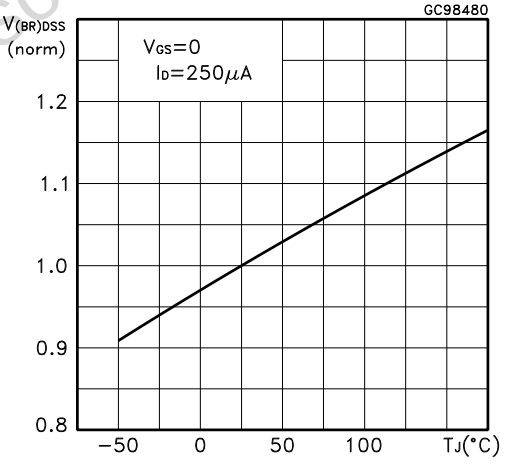


Figure 7: Static drain-source on resistance

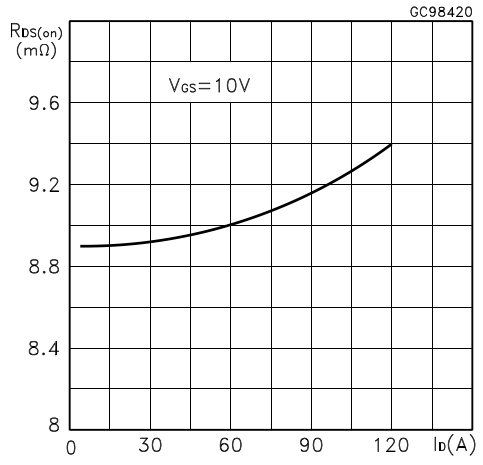


Figure 8: Gate charge vs gate-source voltage

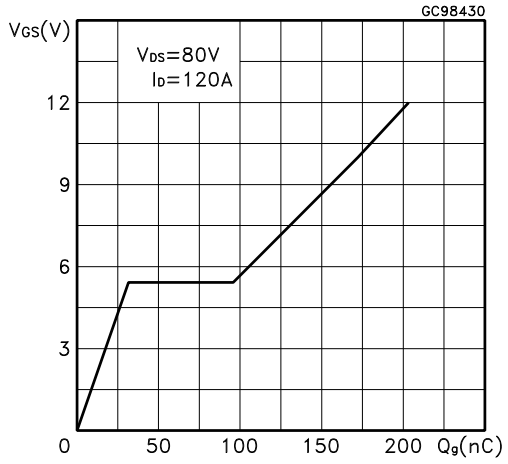


Figure 9: Capacitance variations

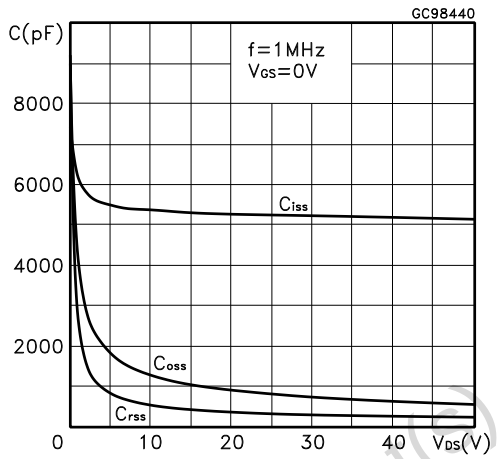


Figure 10: Normalized gate threshold voltage vs temperature

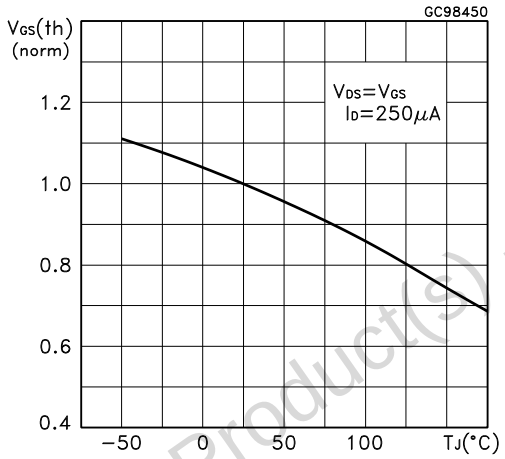


Figure 11: Normalized on-resistance vs temperature

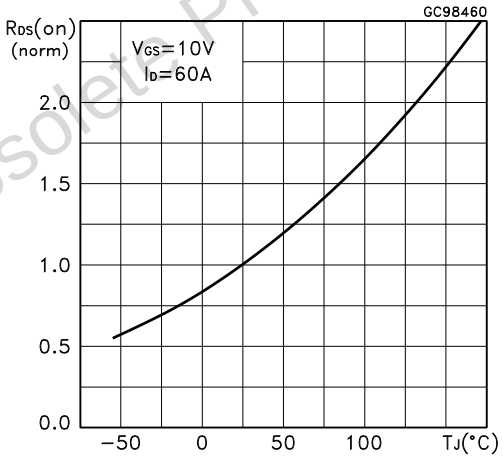
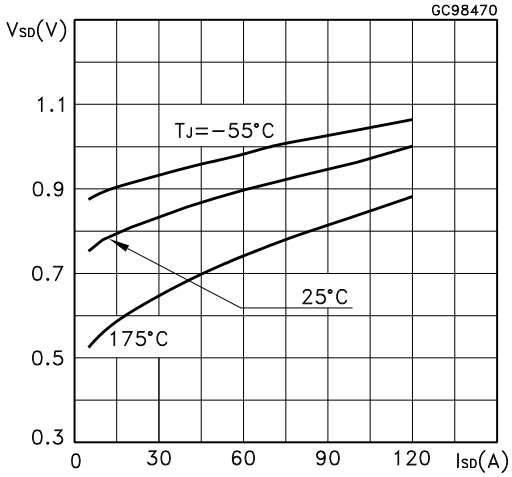


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

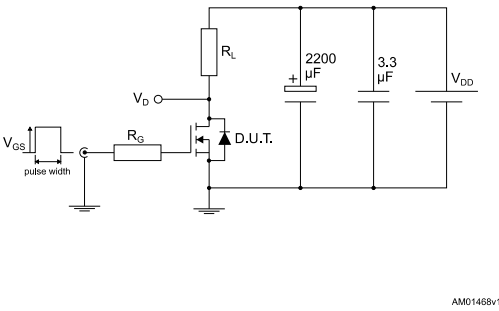


Figure 14: Test circuit for gate charge behavior

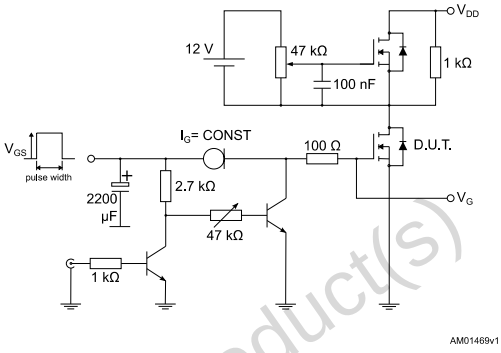


Figure 15: Test circuit for inductive load switching and diode recovery times

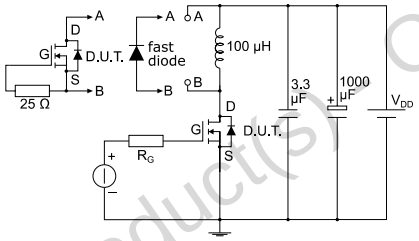


Figure 16: Unclamped inductive load test circuit

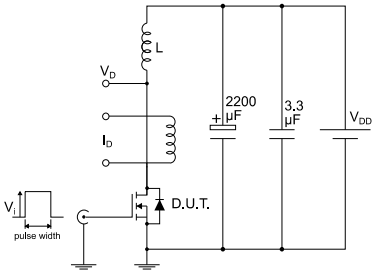


Figure 17: Unclamped inductive waveform

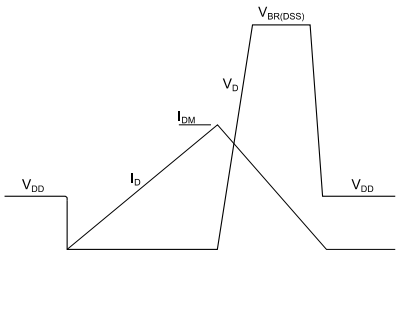
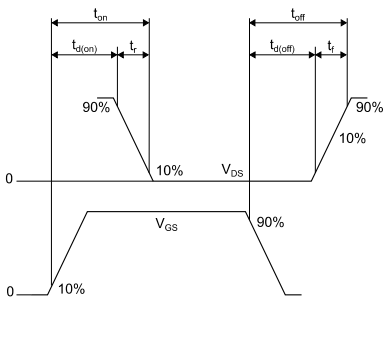


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19: TO-220FP package outline

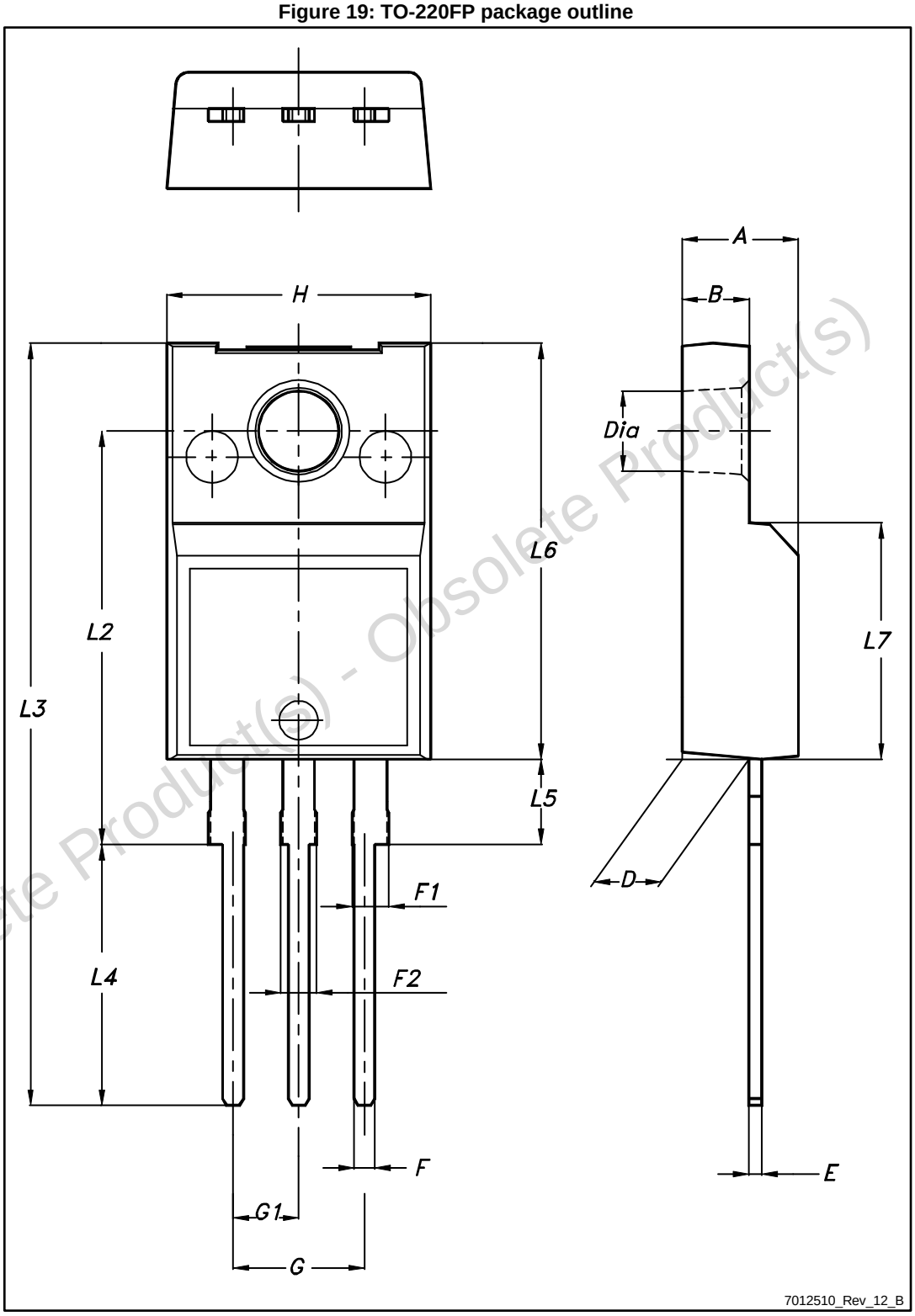


Table 8: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
02-Nov-2017	1	First release, part number previously included in datasheet DocID9522.

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