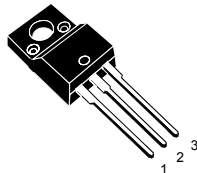
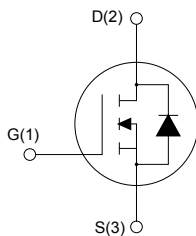


N-channel 600 V, 325 mΩ typ., 11 A FDmesh II Power MOSFET in a TO-220FP package



TO-220FP



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Features

Order code	V_{DS} at T_J max.	$R_{DS(on)}$ max.	I_D
STF13NM60ND	650 V	380 mΩ	11 A

- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

This FDmesh II Power MOSFET with fast-recovery body diode is produced using MDmesh II technology. Utilizing a new strip-layout vertical structure, this device features low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.



Product status link

[STF13NM60ND](#)

Product summary

Order code	STF13NM60ND
Marking	13NM60ND
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	11	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	6.93	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	44	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	40	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ °C}$)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Maximum operating junction temperature	150	°C

1. This value is limited by maximum junction temperature.
2. Pulse width is limited by safe operating area.
3. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
4. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	5	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	162	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$		325	380	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	845	-	pF
C_{oss}	Output capacitance		-	47	-	pF
C_{rSS}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	121	-	pF
R_G	Gate input resistance	$f = 1\text{ MHz}$, Gate DC bias = 0 V, test signal level = 20 mV, open drain	-	4.3	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	24.5	-	nC
Q_{gs}	Gate-source charge		-	4.8	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 5.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	46.5	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	9.6	-	ns
t_f	Fall time		-	15.4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	150		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$	-	755		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	12		A
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	187		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	1271		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	13.6		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

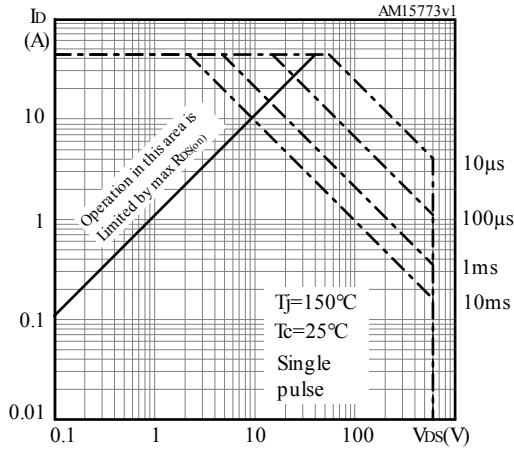


Figure 2. Thermal impedance

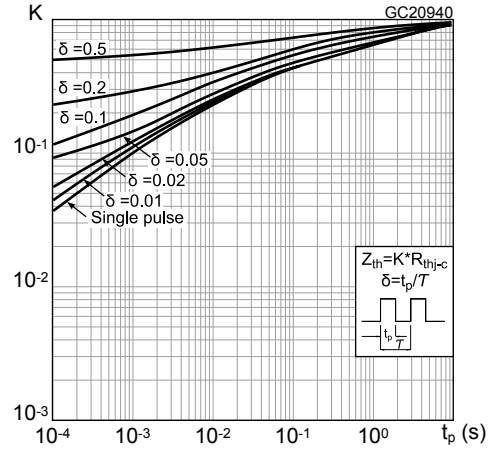


Figure 3. Output characteristics

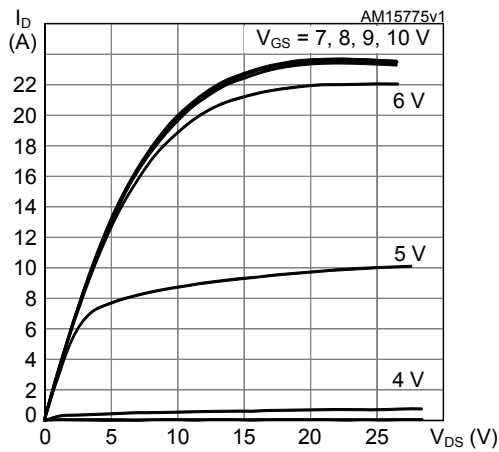


Figure 4. Transfer characteristics

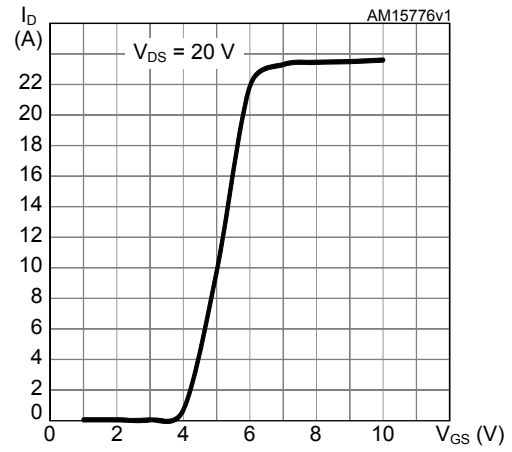


Figure 5. Static drain-source on resistance

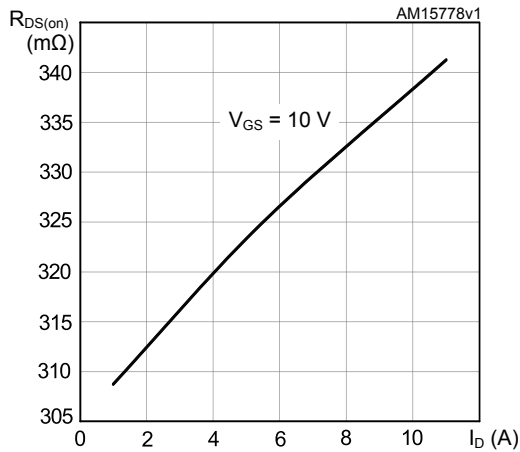


Figure 6. Gate charge vs gate-source voltage

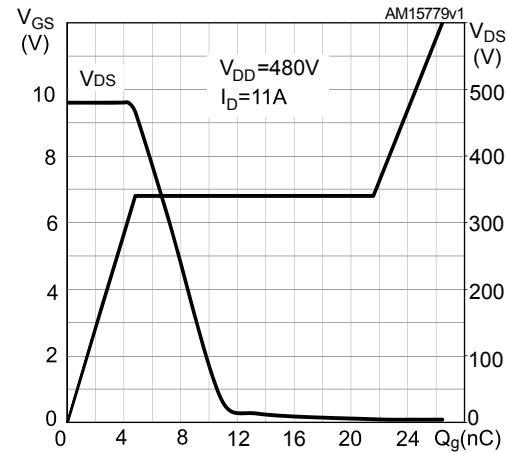


Figure 7. Capacitance variations

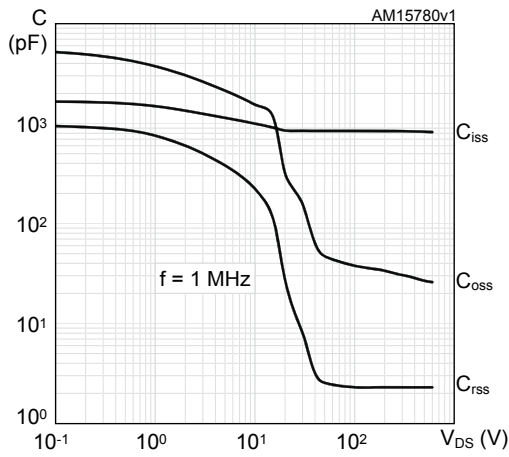


Figure 8. Normalized gate threshold voltage vs temperature

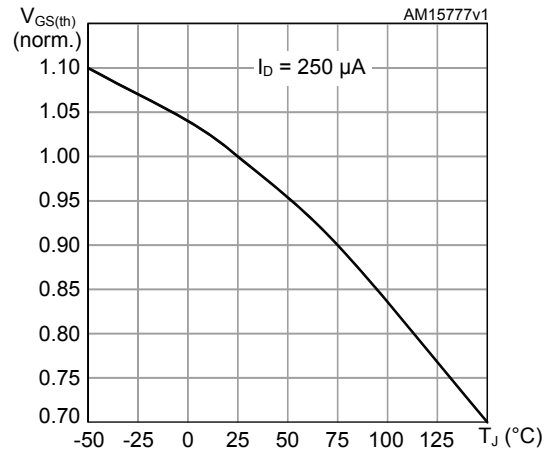


Figure 9. Normalized on resistance vs temperature

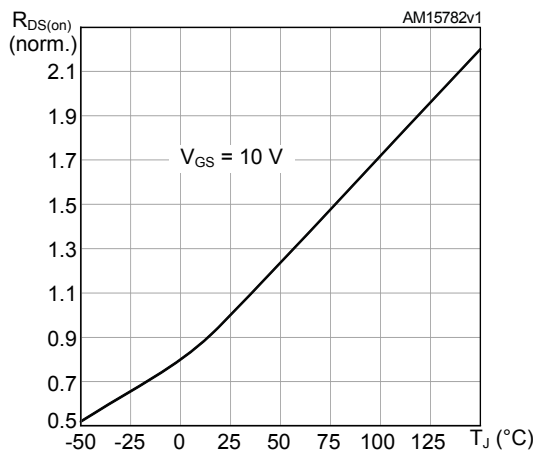


Figure 10. Source-drain diode forward characteristics

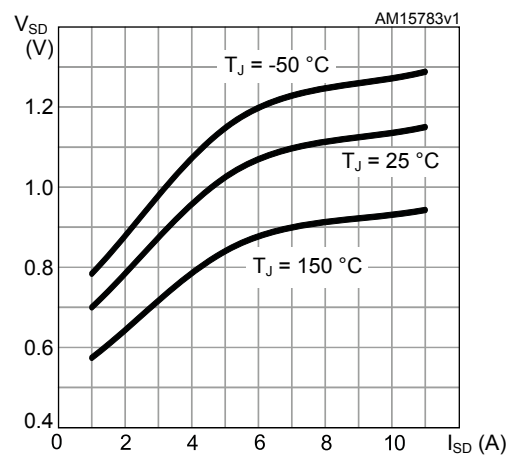
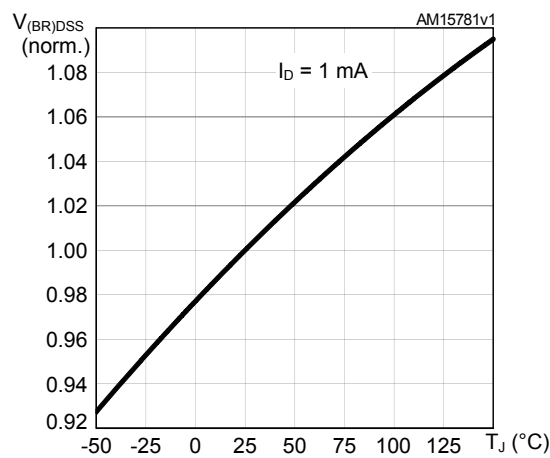


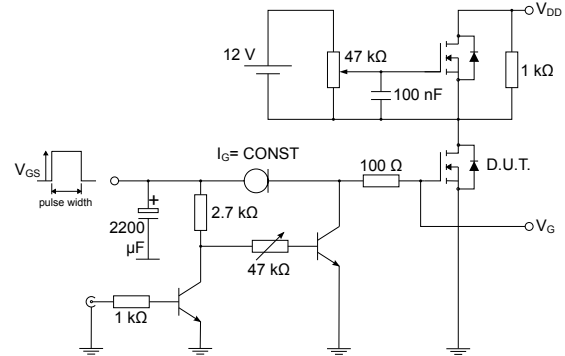
Figure 11. Normalized breakdown voltage vs temperature



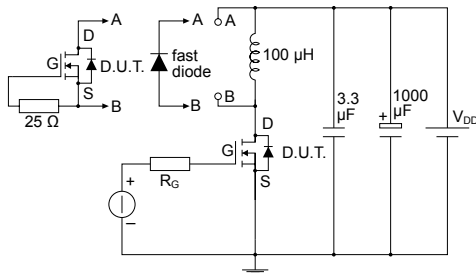
3 Test circuits

Figure 12. Test circuit for resistive load switching times


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Figure 13. Test circuit for gate charge behavior


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Figure 14. Test circuit for inductive load switching and diode recovery times


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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform

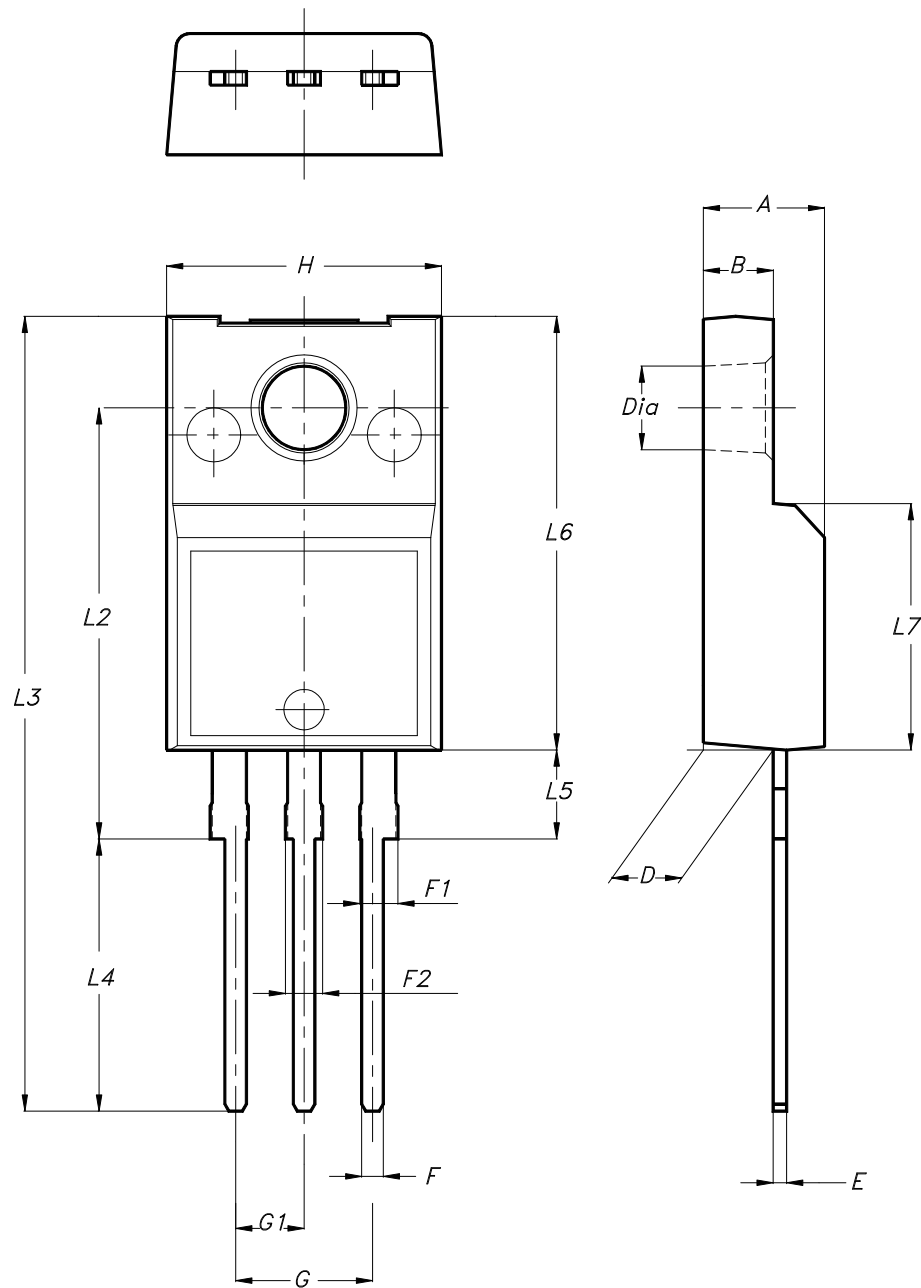

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 18. TO-220FP type B package outline



7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. Document revision history

Date	Revision	Changes
25-May-2023	1	First release. The part number STF13NM60ND was previously inserted in the DS9668.

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