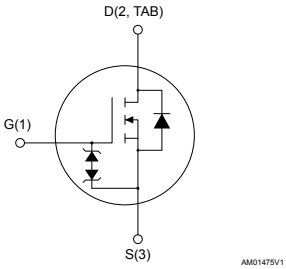
Datasheet

N-channel 525 V, 0.72 Ω typ., 6 A, MDmesh™ K3 Power MOSFETs in D²PAK and TO-220FP packages

D²PAK TO-220FP



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB7N52K3	525 V	0.85 Ω	6 A	90 W
STF7N52K3				25 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These MDmesh™ K3 Power MOSFETs are the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Product status links
STB7N52K3
STF7N52K3

Product summary	
STB7N52K3	
Order code	STB7N52K3
Marking	7N52K3
Package	D²PAK
Packing	Tape and reel
STF7N52K3	
Order code	STF7N52K3
Marking	7N52K3
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK	TO-220FP	
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	6	6(1)	A
	Drain current (continuous) at T_C = 100 °C	3.8	3.8(1)	A
I_{DM}(2)	Drain current (pulsed)	24	24(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	25	W
I_{AR}(3)	Avalanche current, repetitive or non-repetitive (pulse width is limited by T_J max.)	3		A
E_{AS}(4)	Single pulse avalanche energy	100		mJ
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	2.5		kV
dv/dt(5)	Peak diode recovery voltage slope	12		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)		2.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range			

1. *This value is limited by maximun junction temperature.*
2. *Pulse width is limited by safe operating area.*
3. *Pulse width is limited by Tj max.*
4. *Starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V*
5. *I_{SD} ≤ 6 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39	5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	30		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.		62.5	°C/W

1. *When mounted on an 1-inch² FR-4, 2oz Cu board.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			1	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		0.72	0.85	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	870	-	pF
C_{oss}	Output capacitance			70		
C_{rss}	Reverse transfer capacitance			13		
$C_{oss(tr)}$(1)	Equivalent output capacitance	V_{DS} = 0 to 420 V, V_{GS} = 0 V,	-	53	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 420 V, I_D = 6 A, V_{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	33	-	nC
Q_{gs}	Gate-source charge			6		
Q_{gd}	Gate-drain charge			21		

1. *$C_{oss(tr)}$ is defined as the constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 420 V.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	13	-	ns
t_r	Rise time			11		
$t_{d(off)}$	Turn-off delay time			36		
t_f	Fall time			19		

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}(1)	Source-drain current (pulsed)				24	
V_{SD}(2)	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	220		ns
Q_{rr}	Reverse recovery charge			1.8		µC
I_{RRM}	Reverse recovery current			16		A
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	250		ns
Q_{rr}	Reverse recovery charge			2.2		µC
I_{RRM}	Reverse recovery current			18		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK

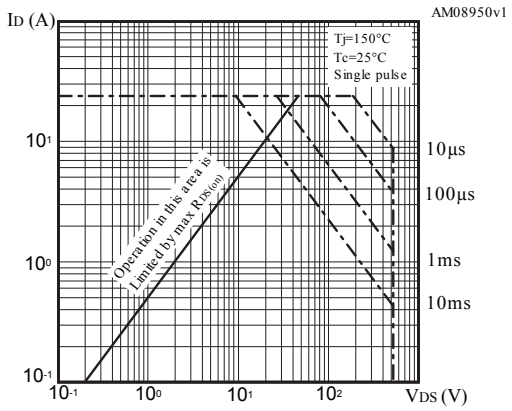


Figure 2. Thermal impedance for D²PAK

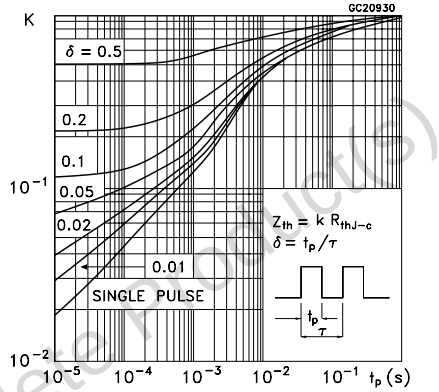


Figure 3. Safe operating area for TO-220FP

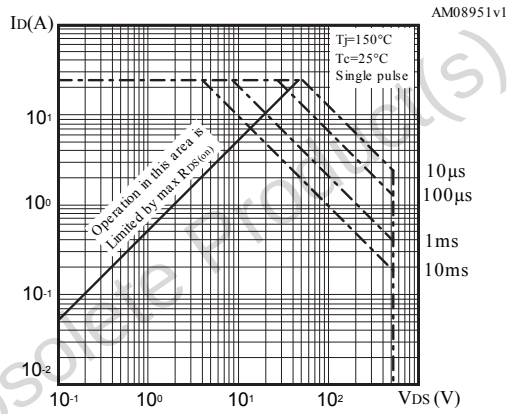


Figure 4. Thermal impedance for TO-220FP

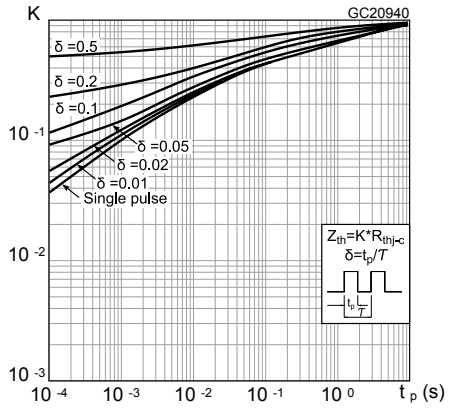


Figure 5. Output characteristics

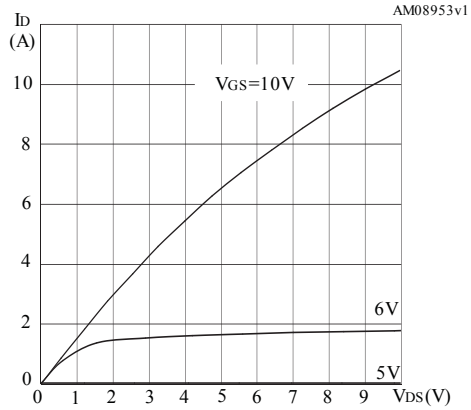


Figure 6. Transfer characteristics

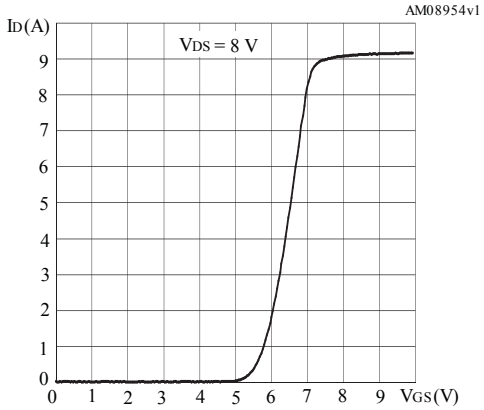


Figure 7. Normalized B_{VDSS} vs temperature

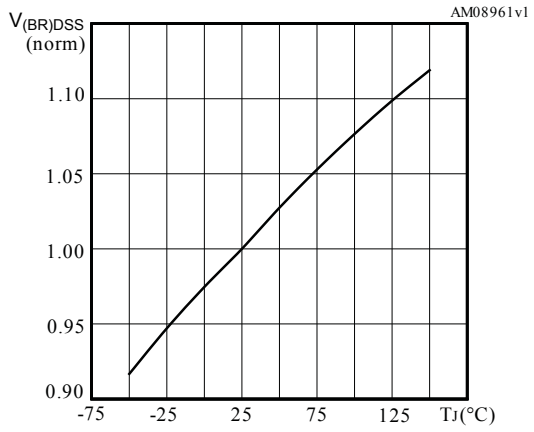


Figure 8. Static drain-source on-resistance

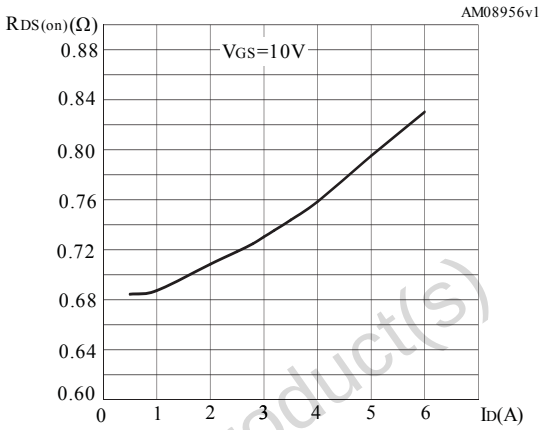


Figure 9. Output capacitance stored energy

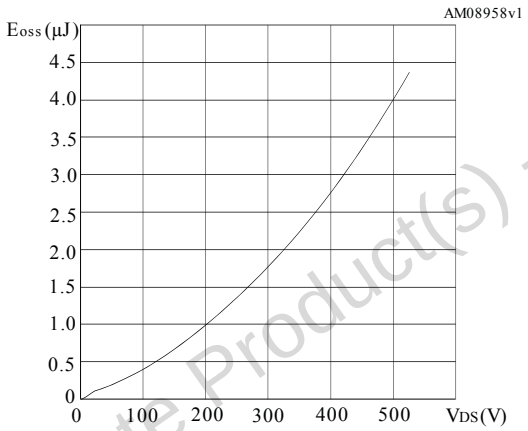


Figure 10. Capacitance variations

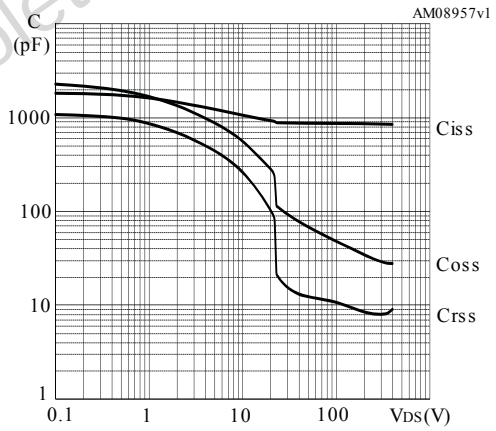


Figure 11. Gate charge vs gate-source voltage

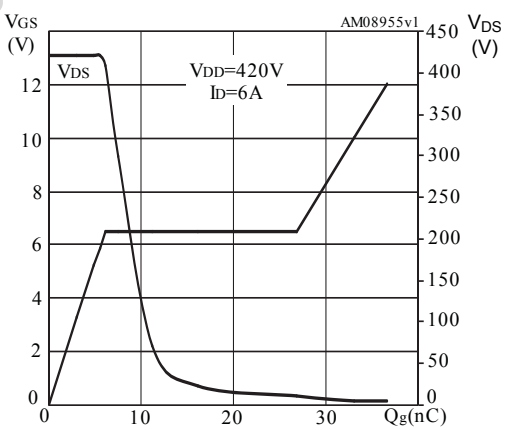


Figure 12. Normalized on-resistance vs temperature

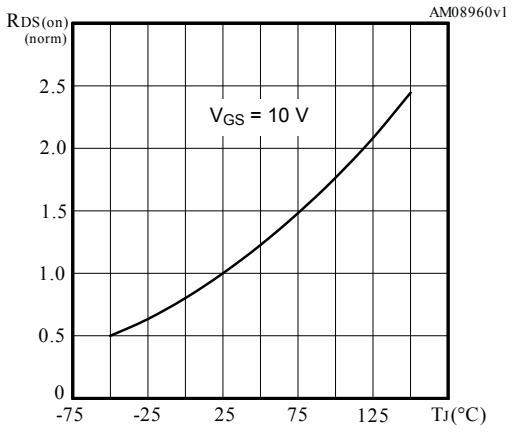


Figure 13. Normalized gate threshold voltage vs temperature

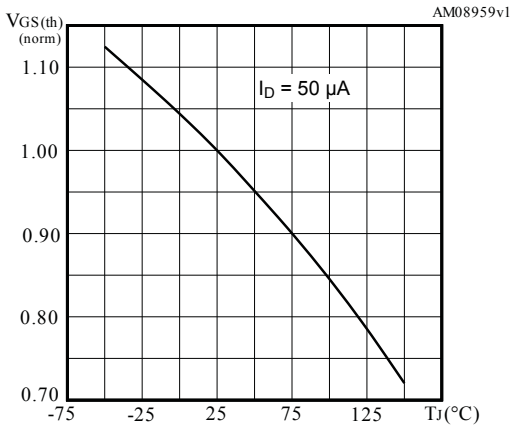


Figure 14. Maximum avalanche energy vs temperature

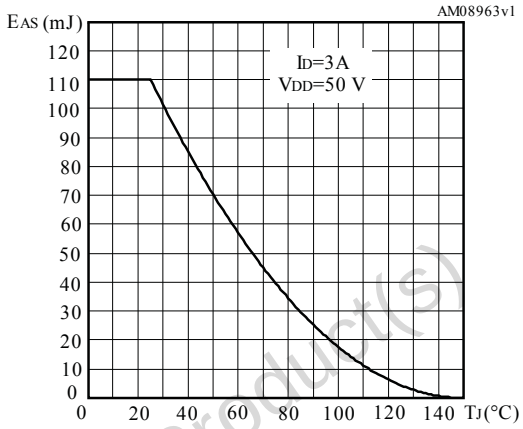
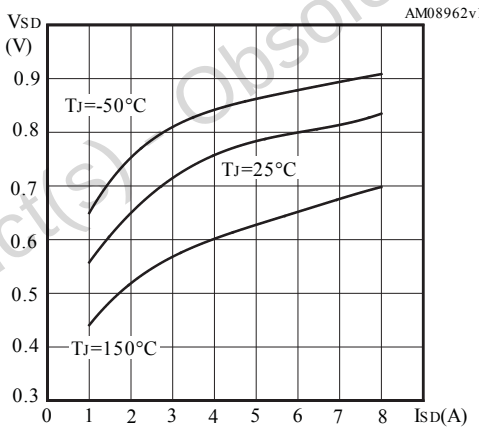


Figure 15. Source-drain diode forward characteristics



3 Test circuits

Figure 16. Test circuit for resistive load switching times

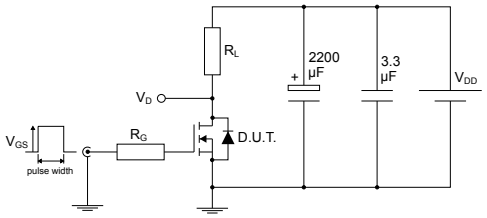


Figure 17. Test circuit for gate charge behavior

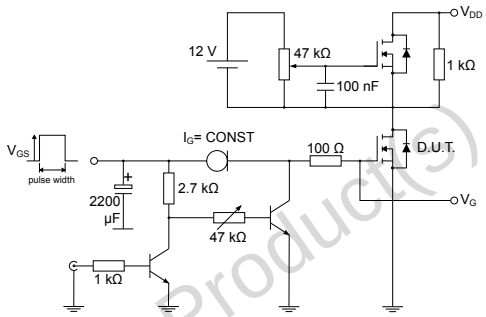


Figure 18. Test circuit for inductive load switching and diode recovery times

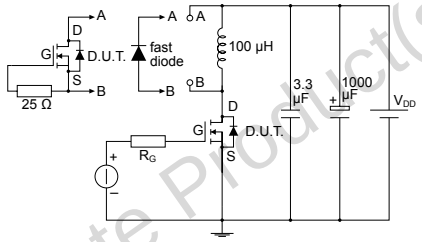


Figure 19. Unclamped inductive load test circuit

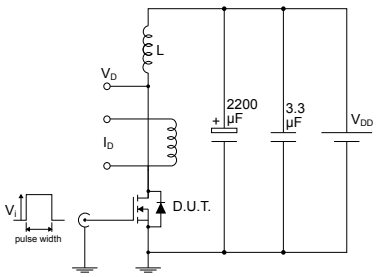


Figure 20. Unclamped inductive waveform

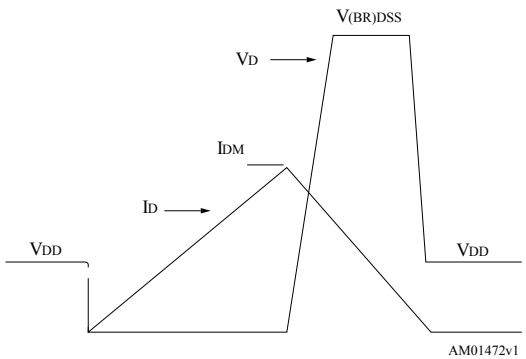
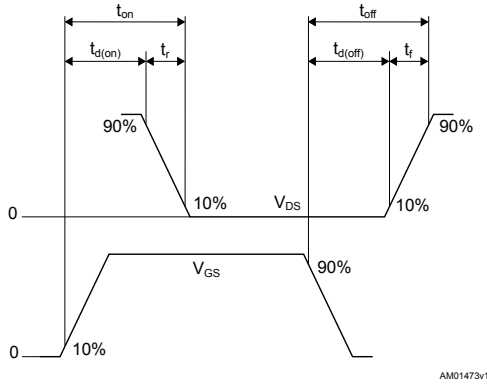


Figure 21. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 22. D²PAK (TO-263) type A package outline

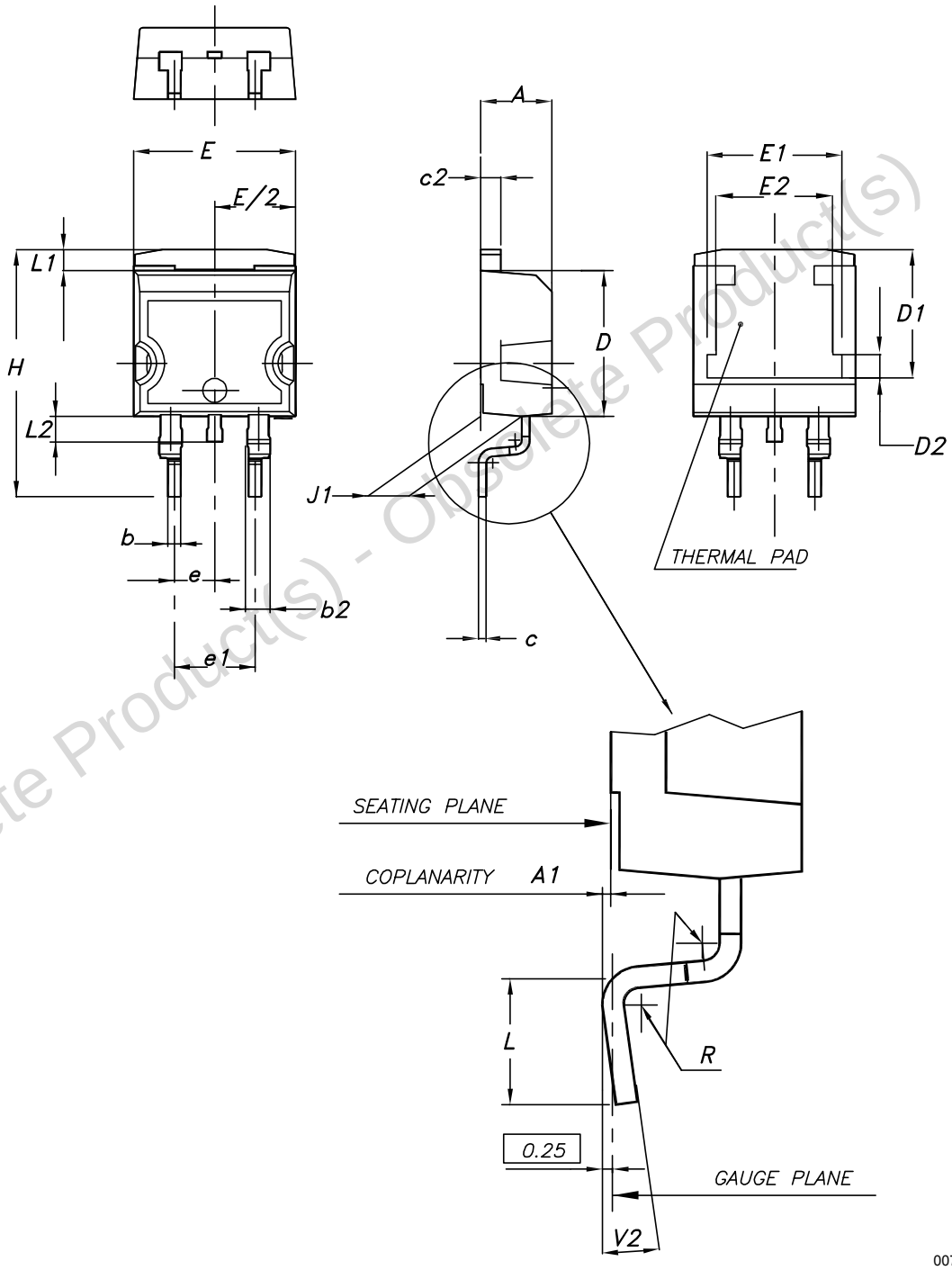
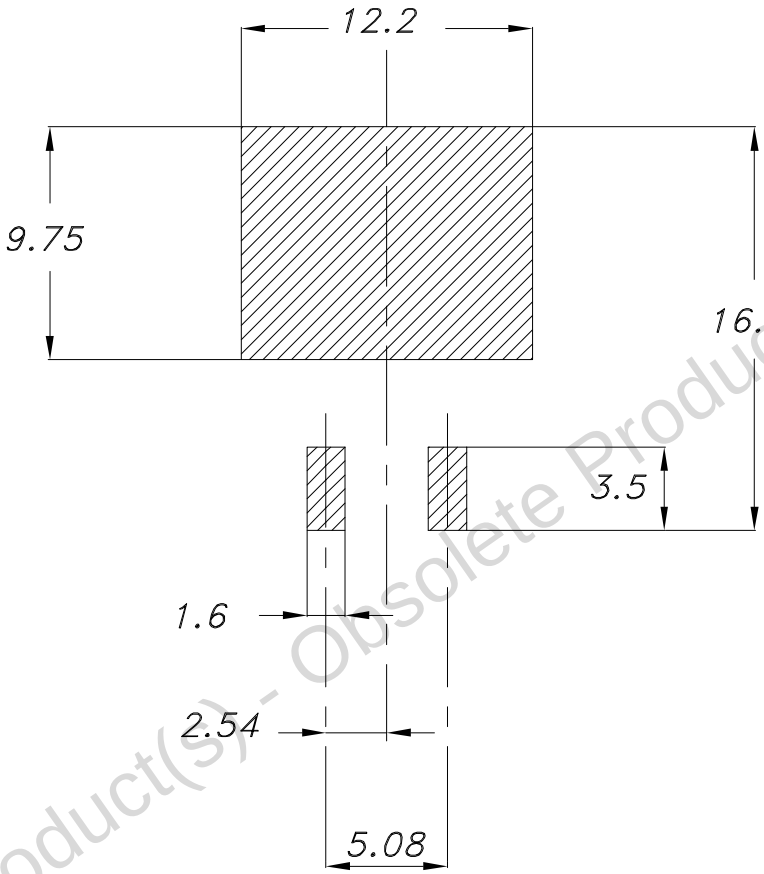


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 23. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

4.2 D²PAK packing information

Figure 24. D²PAK tape outline

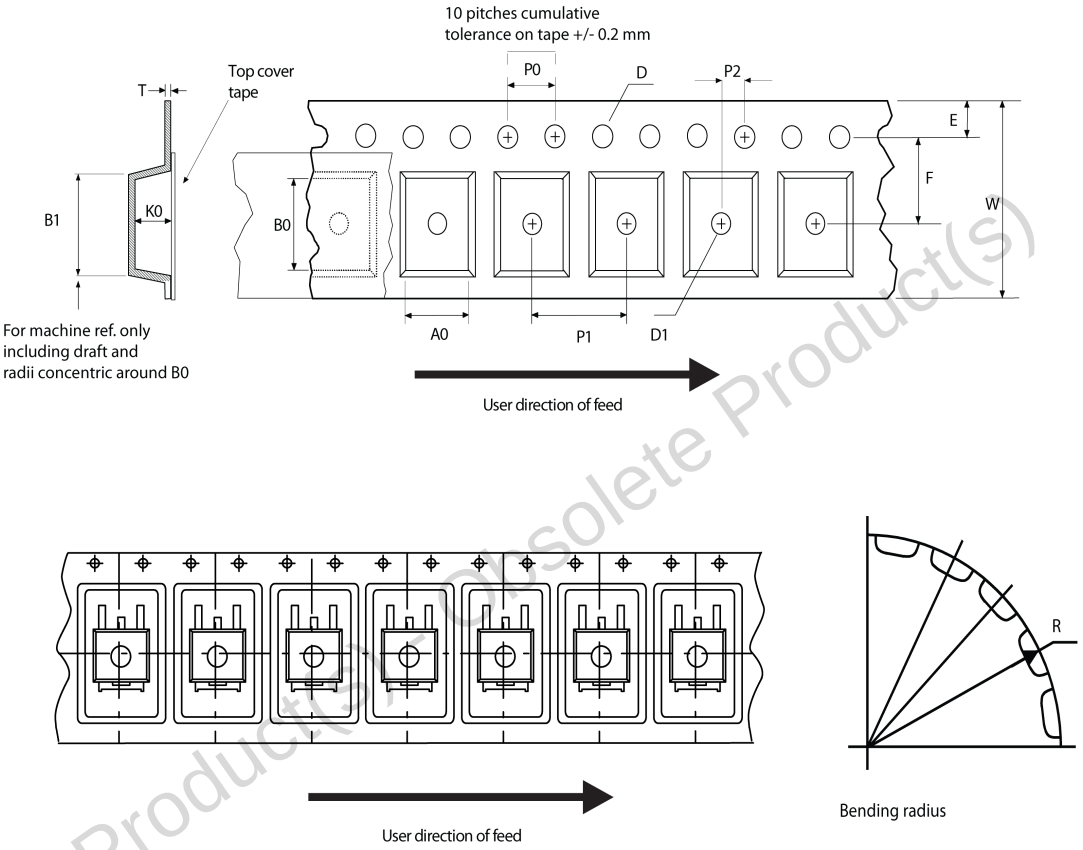


Figure 25. D²PAK reel outline

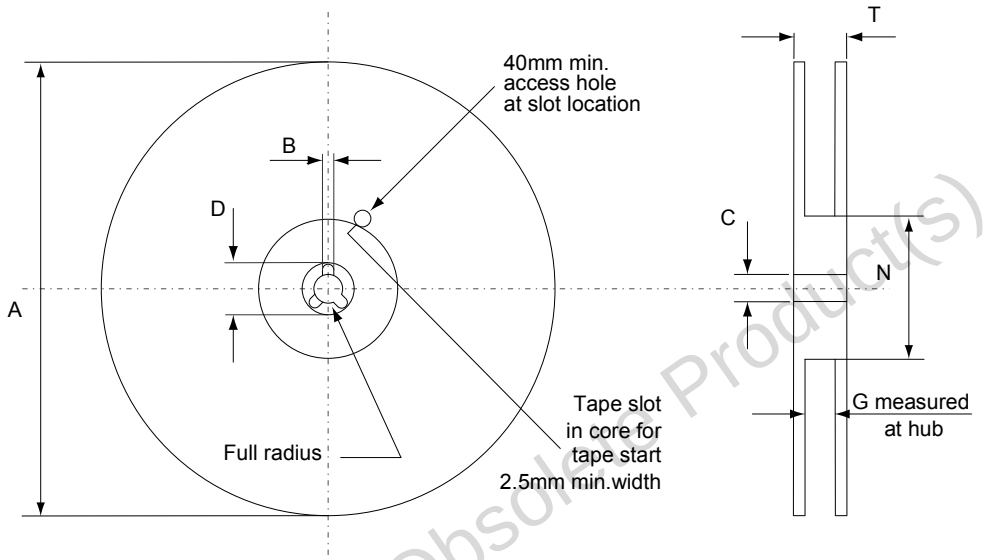


Table 9. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 TO-220FP package information

Figure 26. **TO-220FP package outline**

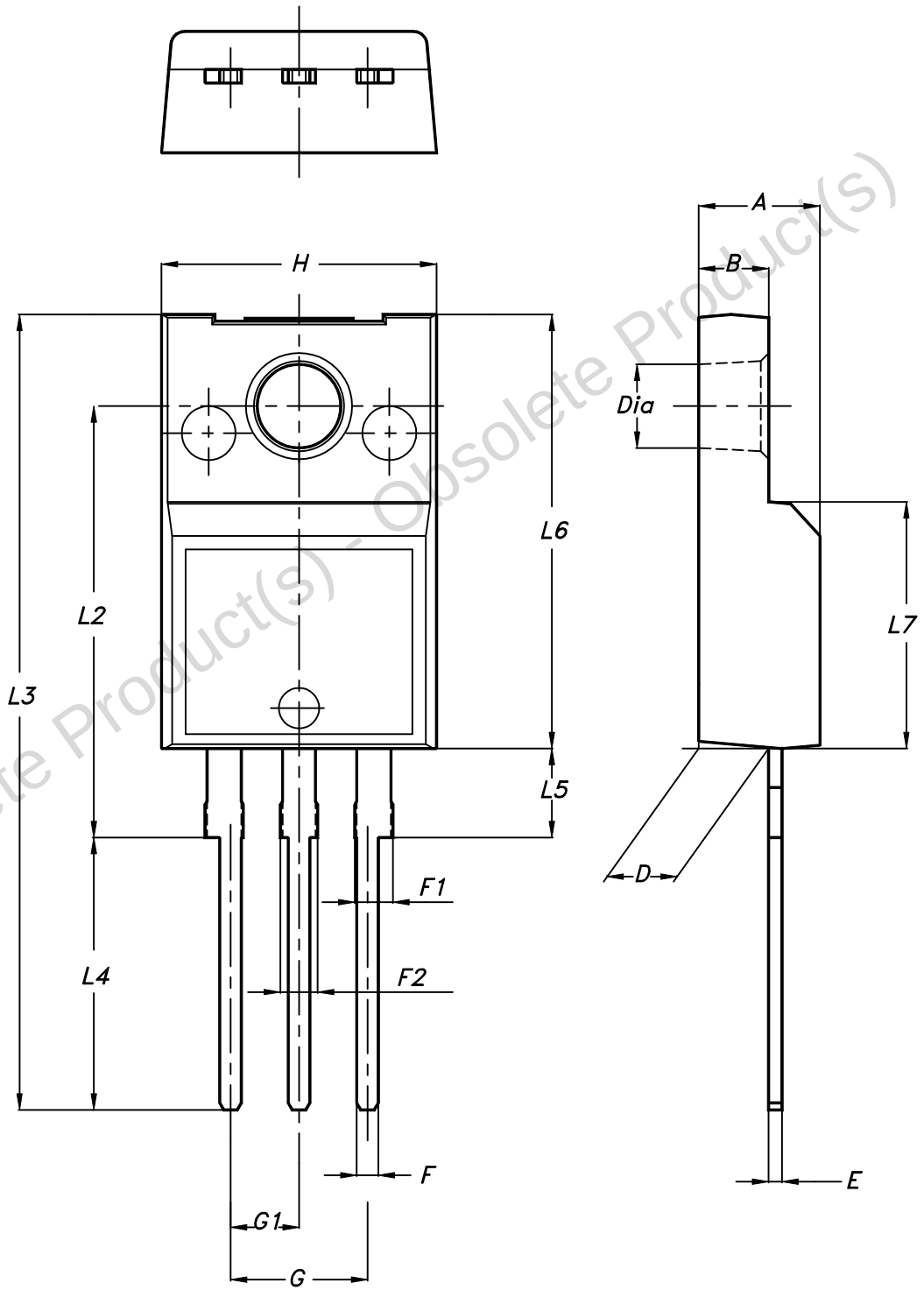


Table 10. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 11. **Document revision history**

Date	Version	Changes
06-Aug-2018	1	Initial release. These part numbers were previously included in datasheet DS5889.

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