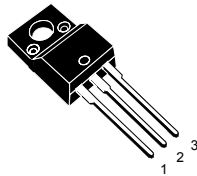
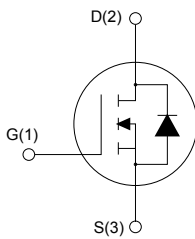


N-channel 600 V, 800 mΩ typ., 5 A MDmesh II Power MOSFET in a TO-220FP package



TO-220FP



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF7NM60N	600 V	900 mΩ	5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.



Product status link

[STF7NM60N](#)

Product summary

Order code	STF7NM60N
Marking	7NM60N
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	
$I_{DM}^{(2)}$	Drain current pulsed	20	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	20	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^\circ\text{C}$)	2.5	kV
T_J	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		$^\circ\text{C}$

1. This value is limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 80\%V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	6.25	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	2	A
E_{AS}	Single-pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	119	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		800	900	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	363	-	pF
C_{oss}	Output capacitance		-	24.6	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	130	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 12. Test circuit for gate charge behavior)	-	14	-	nC
Q_{gs}	Gate-source charge		-	2.7	-	nC
Q_{gd}	Gate-drain charge		-	7.7	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	7	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	26	-	ns
t_f	Fall time		-	12	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	213		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1.5		μC
I_{RRM}	Reverse recovery current	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	14		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	265		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	1.8		μC
I_{RRM}	Reverse recovery current	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	14		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

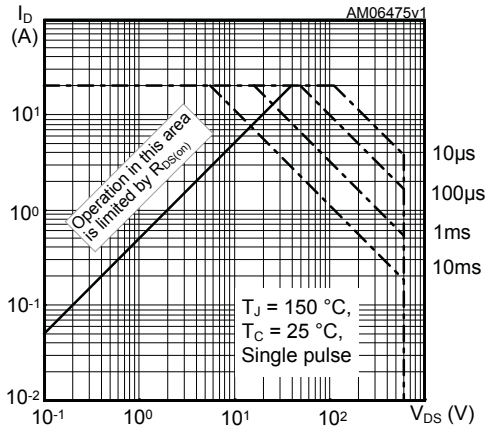


Figure 2. Thermal impedance

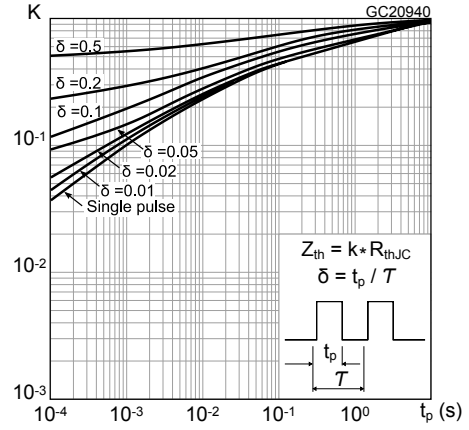


Figure 3. Output characteristics

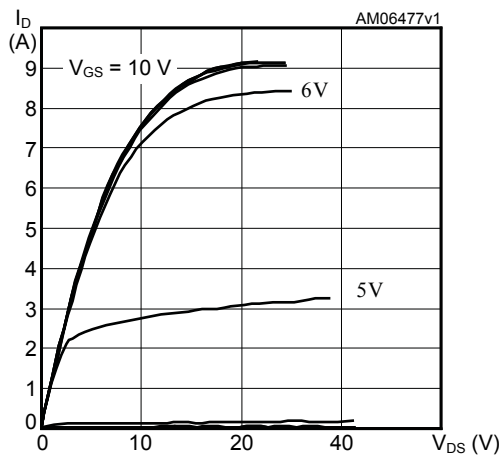


Figure 4. Transfer characteristics

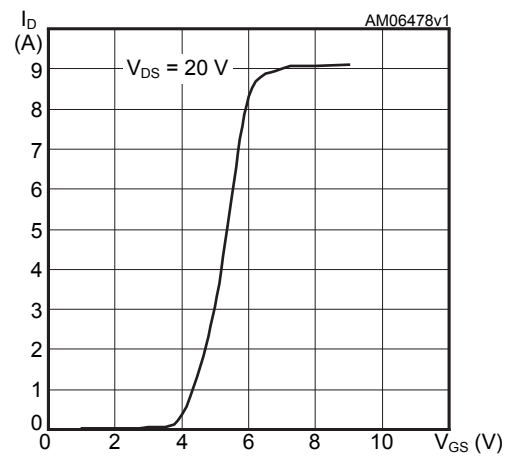


Figure 5. Gate charge vs gate-source voltage

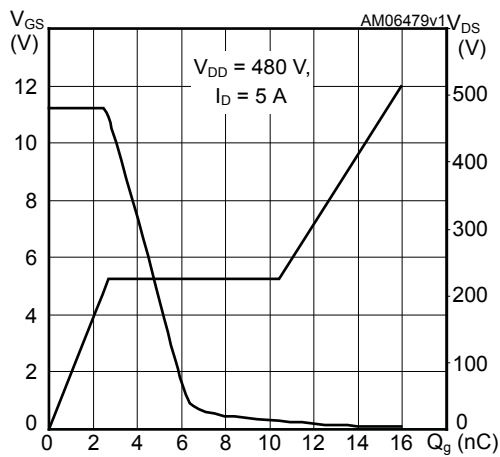


Figure 6. Static drain-source on-resistance

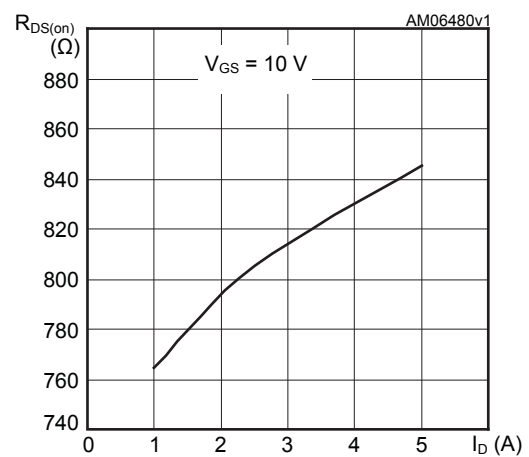


Figure 7. Capacitance variations

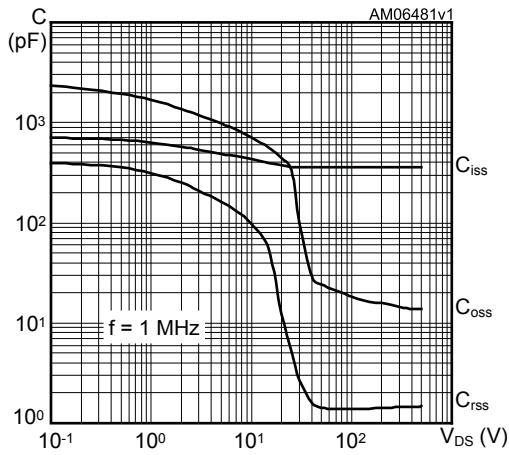


Figure 8. Normalized gate threshold voltage vs temperature

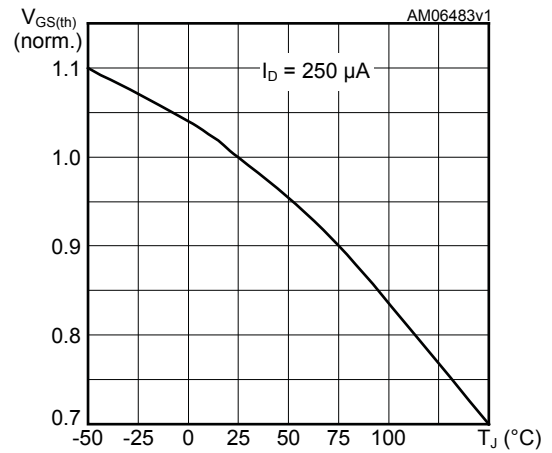


Figure 9. Normalized on-resistance vs temperature

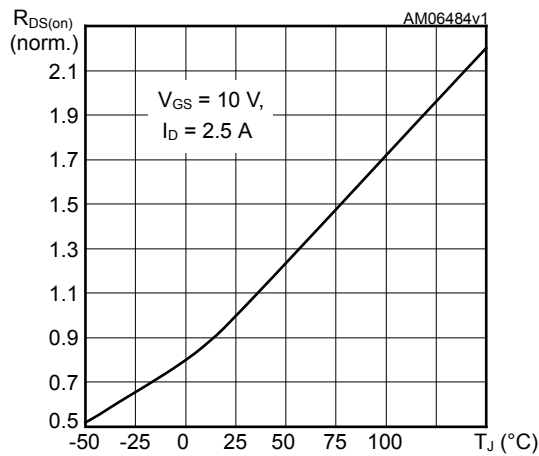
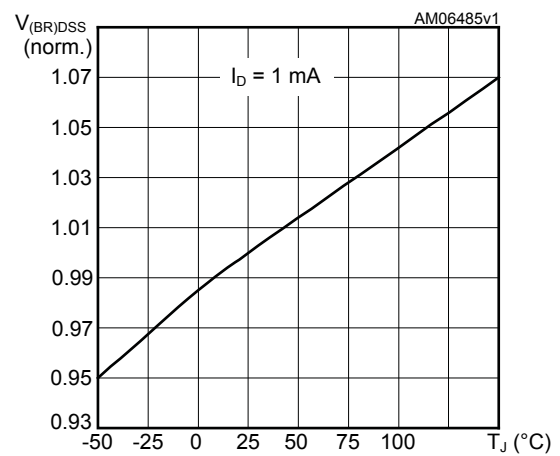


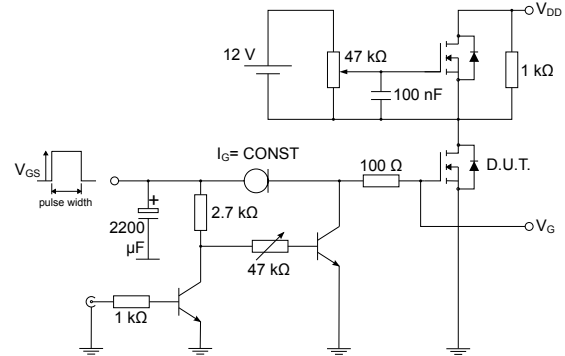
Figure 10. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 11. Test circuit for resistive load switching times


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Figure 12. Test circuit for gate charge behavior


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Figure 13. Test circuit for inductive load switching and diode recovery times


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Figure 14. Unclamped inductive load test circuit


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Figure 15. Unclamped inductive waveform


AM01472v1

Figure 16. Switching time waveform

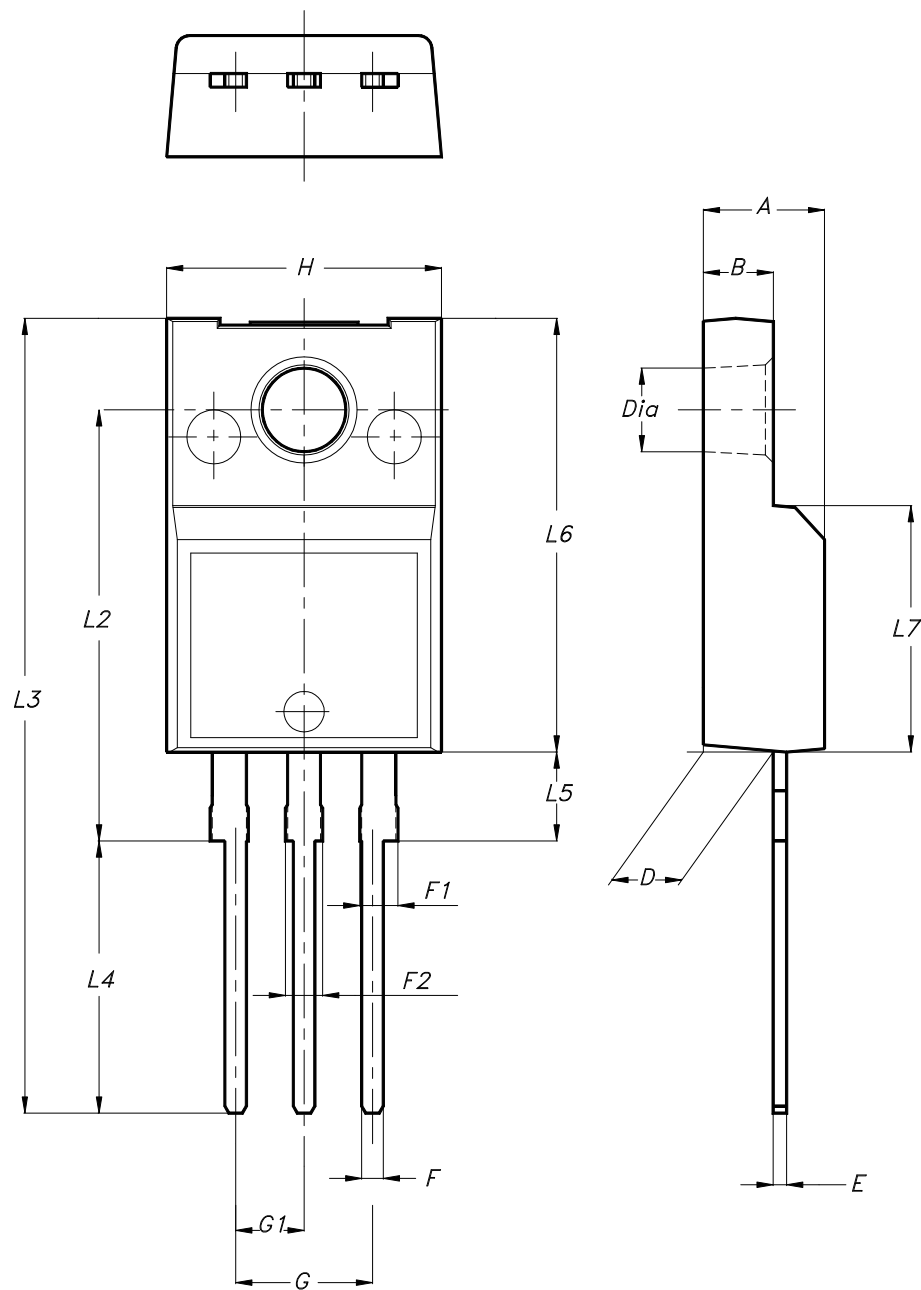

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 17. TO-220FP type B package outline



7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Oct-2023	1	First release. The part number STF7NM60N previously included in datasheet DS6523.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	TO-220FP type B package information	8
	Revision history	10

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