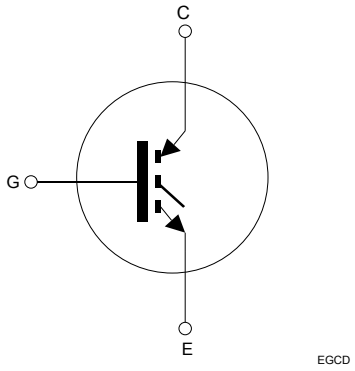
STG200M65F2D11AG

Datasheet

Automotive-grade 650 V, 200 A trench gate field-stop M series low-loss IGBT die in D11 packing



Features

- AEC-Q101 qualified
- Low-loss series IGBT
- Low $V_{CE(sat)}$ = 1.55 V (typ.) at I_C = 200 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: T_J = 175 °C
- 6 µs minimum short-circuit withstanding time at T_J = 150 °C

Applications

- Main inverter (electric traction)

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.

Product status link
STG200M65F2D11AG

Product summary	
Order code	STG200M65F2D11AG
V_{CE}	650 V
I_{CN}	200 A
Die size	9.73 x 10.23 mm
Packing	D11

1 Mechanical parameters

Table 1. Mechanical parameters

Parameter		Value	Unit
Die size including scribe line		9.73 x 10.23	mm
Die thickness		70	µm
Front side passivation		Silicon nitride	
Emitter pad size	x4	4.26 x 1.94	mm
	including gate pad (x4)	4.26 x 2.18	mm
Gate pad size		1.66 x 0.83	mm
Front side metallization	Composition	AlCu	
	Thickness	4.5	µm
Back side metallization	Composition	Al/Ti/NiV/Ag	
	Thickness	0.80	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤ 500	µm

2 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	650	V
V_{GE}	Gate-emitter voltage	±20	V
I_{CN}	Continuous collector current at T = 100 °C	200	A
I_{CP}[(1)(2)]	Pulsed collector current	600	A
t_{sc}[(3)]	Short-circuit withstand time V_{CC} = 360 V, V_{GE} = 15 V, V_{CE} (peak) ≤ 650 V, T_{Jstart} ≤ 150 °C	6	µs
T_J	Operating junction temperature range	-40 to 175	°C

1. *Depending on thermal properties of assembly.*
2. *Pulse width limited by maximum junction temperature.*
3. *Not tested at chip level, verified by design/characterization. Allowed number of short-circuits < 1000; time between short-circuits > 1 s.*

3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 250 µA, V_{GE} = 0 V	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 200 A		1.55		V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 3 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{CE} = 650 V, V_{GE} = 0 V			100	µA
I_{GES}	Gate-emitter leakage current	V_{GE} = ±20 V, V_{CE} = 0 V			±600	nA
R_G	Intrinsic gate resistance	f = 1 MHz		2.5		Ω

Table 4. Electrical characteristics (specified by design and evaluated by characterization, not tested in production)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 200 A	-	1.55	2.3	V
		V_{GE} = 15 V, I_C = 200 A T_J = 175 °C	-	1.95		V
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz V_{GE} = 0 V	-	17.8		nF
C_{oes}	Output capacitance		-	0.7		nF
C_{res}	Reverse transfer capacitance		-	0.37		nF
Q_g	Total gate charge	V_{CC} = 400 V, I_C = 200 A, V_{GE} = 0 to 15 V	-	650		nC
Q_{ge}	Gate-emitter charge		-	130		nC
Q_{gc}	Gate collector charge		-	240		nC

Table 5. Switching characteristics on inductive load (specified by design and evaluated by characterization, not tested in production)

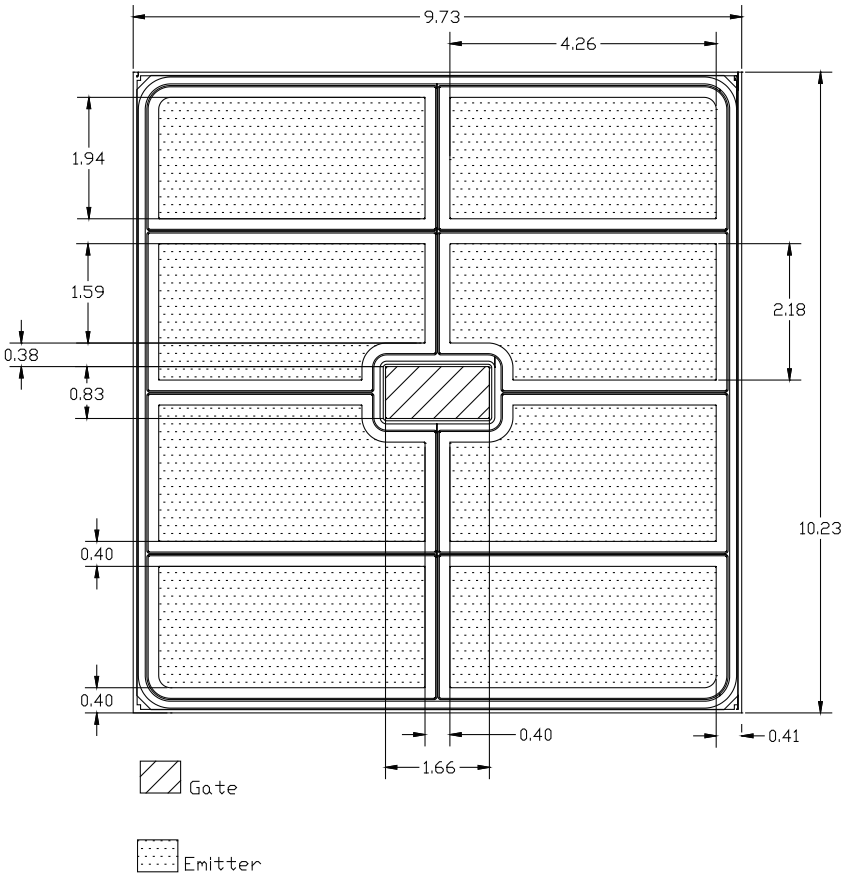
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 300 V, I_C = 200 A, V_{GE} = -15 to 15 V, R_G = 2 Ω	-	134	-	ns
t_r	Current rise time		-	41	-	ns
$t_{d(off)}$	Turn-off delay time		-	151	-	ns
t_f	Current fall time		-	88	-	ns
E_{off} (1)	Turn-off switching energy		-	5.5	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 300 V, I_C = 200 A, V_{GE} = -15 to 15 V, R_G = 2 Ω, T_J = 175 °C	-	173	-	ns
t_f	Current rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	58	-	ns
t_f	Current fall time		-	110	-	ns
E_{off} (1)	Turn-off switching energy		-	7.0	-	mJ

1. *Including the tail of the collector current.*

Note: Switching characteristics and thermal properties are strongly dependent on module design and mounting technology. These results are obtained using an ST custom package.

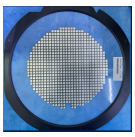
4 Die layout

Figure 1. **Die drawing (dimensions are in mm)**



4.1 Packing information

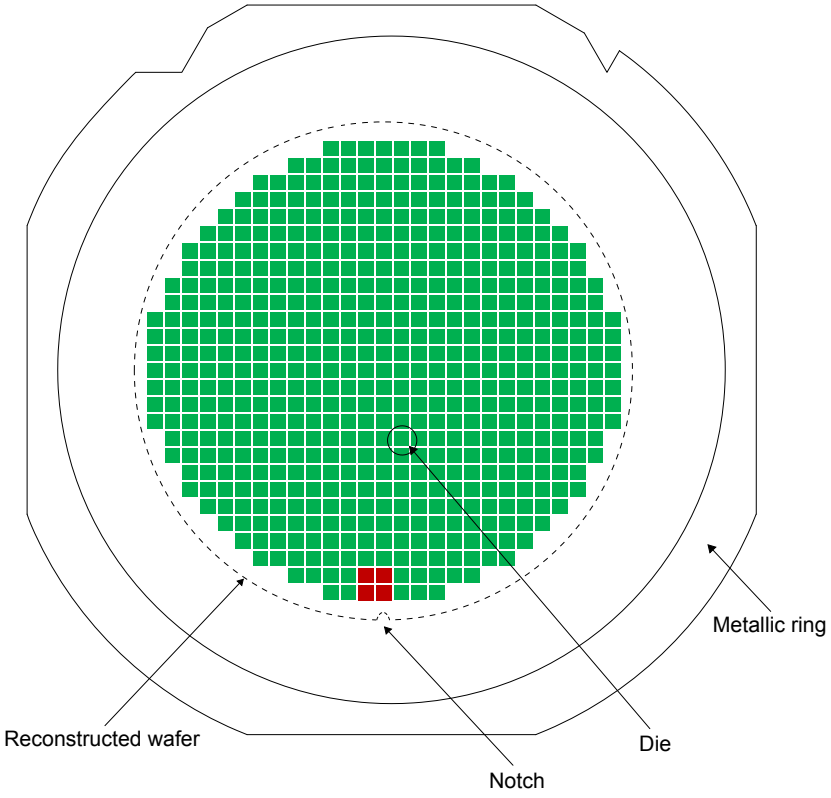
Table 6. **Die delivery**

Package option	Description	Picture
D11	Known good dice (KGD) 100% tested in UV cured reconstructed wafer, supported by metallic ring frame. Reconstructed wafers are packed into a black box sealed under vacuum in a moisture barrier bag, with oxygen absorber, oxygen indicator, desiccant dry and HIC card. Some inked dice can be present after final QA visual inspection.	

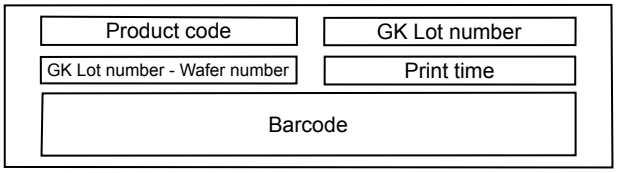
The wafers on frames are shipped inside a black box containing 25 wafers maximum.

Figure 2. **Black box wafers**

Figure 3. **Notch orientation and label**



Label



Picture not in scale,
used for demonstration purposes only.

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5 Additional information

5.1 Handling

- Products should only be handled in ESD-safe workstations. Standard ESD precautions and safe work environments are defined in MIL-HDBK-263.
- Products must be handled in a class 1000 clean room or higher.
- The single die should not be handled with tweezers. A vacuum wand with a non-metallic tip protected against electrostatic discharge must be used.

5.2 Wafer storage

To avoid contamination and/or degradation of the product after shipment, proper storage conditions are required.

- The recommended storage temperature is between 15 °C and 35 °C maximum.
- The recommended ambient humidity is between 10% and 70% maximum.
- The maximum storage time after the date of shipment from ST is 6 months.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
07-Dec-2023	1	First release.

Contents

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