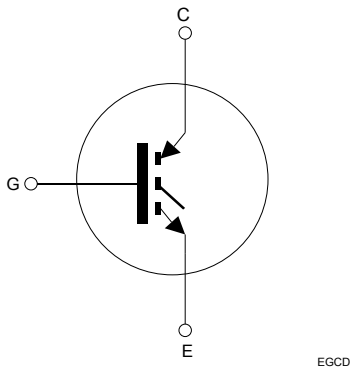



Automotive-grade 650 V, 200 A trench gate field-stop M series low-loss IGBT die in D8 packing



Features

- AEC-Q101 qualified 
- Low-loss series IGBT
- Low $V_{CE(sat)} = 1.55$ V (typ.) at $I_C = 200$ A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: $T_J = 175$ °C
- 6 μ s minimum short-circuit withstanding time at $T_J = 150$ °C

Applications

- Traction inverter for EV/HEV

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.



Product status link

[STG200M65F2D8AG](#)

Product summary

Order code	STG200M65F2D8AG
V_{CE}	650 V
I_{CN}	200 A
Die size	9.73 x 10.23 mm ²
Packing	D8

1 Mechanical parameters

Table 1. Mechanical parameters

Parameter		Value	Unit
Die size including scribe line		9.73 x 10.23	mm ²
Die thickness		70	µm
Front side passivation		Silicon nitride	
Emitter pad size	x4	4.26 x 1.94	mm ²
	including gate pad (x4)	4.26 x 2.18	mm ²
Gate pad size		1.66 x 0.83	mm ²
Front side metallization	Composition	AlCu	
	Thickness	4.5	µm
Back side metallization	Composition	Al/Ti/NiV/Ag	
	Thickness	0.80	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤ 500	µm

2 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$ V)	650	V
V_{GE}	Gate-emitter voltage	± 20	V
I_{CN}	Continuous collector current at $T = 100$ °C	200	A
I_{CP} ^{(1) (2)}	Pulsed collector current	600	A
t_{sc} ⁽³⁾	Short-circuit withstand time $V_{CC} = 360$ V, $V_{GE} = 15$ V, $V_{CE(peak)} \leq 650$ V, $T_{Jstart} \leq 150$ °C	6	μ s
T_J	Operating junction temperature range	-40 to 175	°C

1. Depending on thermal properties of assembly.

2. Pulse width limited by maximum junction temperature.

3. Not tested at chip level, verified by design/characterization. Allowed number of short-circuits < 1000; time between short-circuits > 1 s.

3 Electrical characteristics

($T_J = 25\text{ °C}$ unless otherwise specified)

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 250\ \mu\text{A}$, $V_{GE} = 0\ \text{V}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\ \text{V}$, $I_C = 200\ \text{A}$		1.55		V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 3\ \text{mA}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{CE} = 650\ \text{V}$, $V_{GE} = 0\ \text{V}$			100	μA
I_{GES}	Gate-emitter leakage current	$V_{GE} = \pm 20\ \text{V}$, $V_{CE} = 0\ \text{V}$			± 600	nA
R_G	Intrinsic gate resistance	$f = 1\ \text{MHz}$		2.5		Ω

Table 4. Electrical characteristics (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\ \text{V}$, $I_C = 200\ \text{A}$	-	1.55	2.3	V
		$V_{GE} = 15\ \text{V}$, $I_C = 200\ \text{A}$, $T_J = 175\text{ °C}$	-	1.95		V
C_{ies}	Input capacitance	$V_{CE} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GE} = 0\ \text{V}$	-	17.8		nF
C_{oes}	Output capacitance		-	0.7		nF
C_{res}	Reverse transfer capacitance		-	0.37		nF
Q_g	Total gate charge	$V_{CC} = 400\ \text{V}$, $I_C = 200\ \text{A}$, $V_{GE} = 0\ \text{to}\ 15\ \text{V}$	-	650		nC
Q_{ge}	Gate-emitter charge		-	130		nC
Q_{gc}	Gate collector charge		-	240		nC

Table 5. Switching characteristics on inductive load (not tested at chip level, verified by design/ characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 300\text{ V}$, $I_c = 200\text{ A}$, $V_{GE} = 15/-15\text{ V}$, $R_G = 2\ \Omega$	-	134	-	ns
t_r	Current rise time		-	41	-	ns
$t_{d(off)}$	Turn-off delay time		-	151	-	ns
t_f	Current fall time		-	88	-	ns
$E_{off}^{(1)}$	Turn-off switching energy		-	5.5	-	mJ
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 300\text{ V}$, $I_c = 200\text{ A}$, $V_{GE} = 15/-15\text{ V}$, $R_G = 2\ \Omega$, $T_J = 175\text{ }^\circ\text{C}$	-	173	-	ns
t_r	Current rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	58	-	ns
t_f	Current fall time		-	110	-	ns
$E_{off}^{(1)}$	Turn-off switching energy		-	7.0	-	mJ

1. Including the tail of the collector current.

Note: Switching characteristics and thermal properties are strongly dependent on module design and mounting technology. These results are obtained using an ST custom package.

4 Die layout

Figure 1. Die drawing (dimensions are in mm)

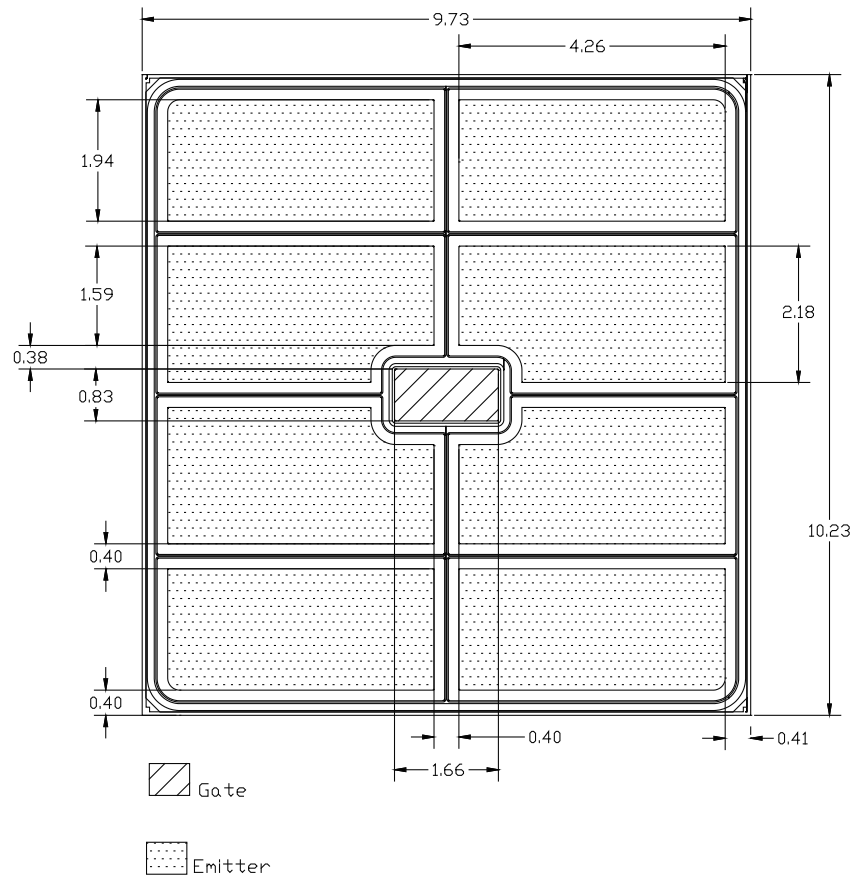


Table 6. Die delivery

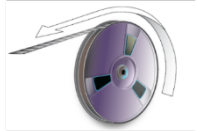
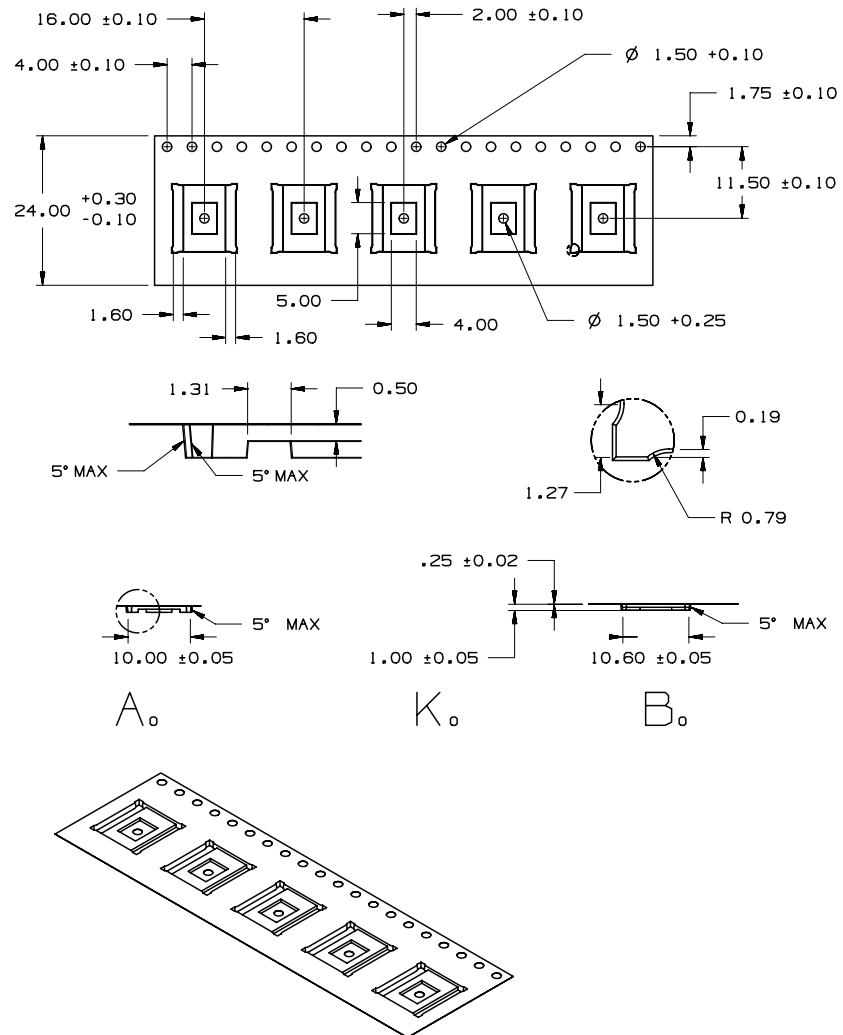
Package option	Description	Picture
D8	Wafer tested, inked, cut; die is picked up and submitted to automatic visual inspection on the back side. Each die is tested and submitted again to visual inspection on both top and back sides. Finally, each die is placed inside the reel pocket, submitted once again to a top-side visual inspection and sealed with a cover tape.	

Figure 2. Tape drawing (dimensions are in mm)


5 Additional information

5.1 Additional testing and screening

For customers requiring products supplied as KGD (known good die) or requiring specific die level testing, please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

5.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

5.3 Handling

- Products must be handled at ESD safe workstations only. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263
- Products must be handled in a class 1000 only or better designated clean room environment
- Singular die is not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used

5.4 Wafer/die and storage

Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.

Revision history

Table 7. Document revision history

Date	Revision	Changes
11-Aug-2015	1	First release.
02-Feb-2017	2	Updated: features in cover page, <i>Section 1: "Mechanical parameters"</i> . Minor text changes.
03-Jul-2017	3	Updated features, applications and description in cover page. Minor text changes in <i>Section 2: "Electrical ratings"</i> and <i>Section 4: "Additional information"</i> .
04-May-2021	4	Modified Table 1. Mechanical parameters . Minor text changes.

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