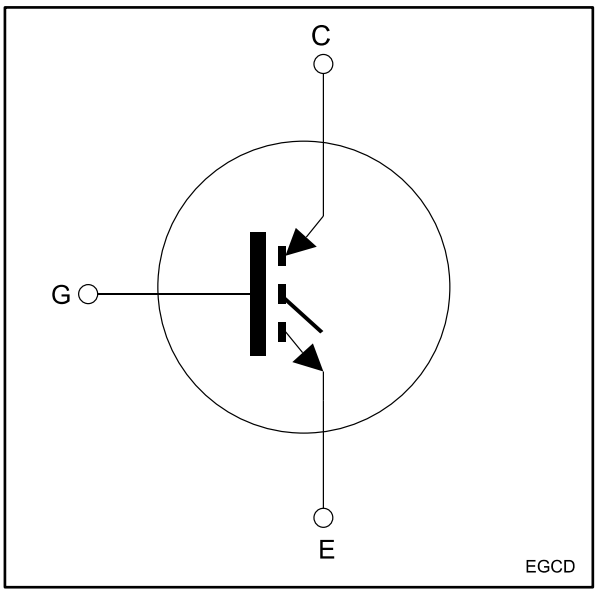
STG35M120F3D8

1200 V, 35 A trench gate field-stop M series low-loss IGBT die in D8 packing

Datasheet - production data



Features

- 10 µs of short-circuit withstand time
- Low $V_{CE(sat)}$ = 1.85 V (typ.) @ I_C = 35 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: T_J = 175 °C

Applications

- Motor control
- Industrial drives
- PFC
- UPS
- Solar
- General purpose inverter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where low-loss and short-circuit functionality are essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and tight parameter distribution result in safer paralleling operation.

Table 1: Device summary

Order code	V_{CE}	I_{CN}	Die size	Packing
STG35M120F3D8	1200 V	35 A	6.44 x 5.74 mm²	D8

Contents

1 Mechanical parameters

Table 2: Mechanical parameters

Parameter		Value	Unit
Die size		6.44 x 5.74	mm²
Die thickness		110	µm
Front side passivation		Silicon nitride	
Emitter pad size including gate pad	x2	5.42 x 2.22	mm²
Gate pad size		0.82 x 1.20	mm²
Front side metallization	Composition	AlCu	
	Thickness	4.5	µm
Back side metallization	Composition	Al/Ti/NiV/Ag	
	Thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤ 500	µm

2 Electrical ratings

Table 3: Absolute maximum ratings (TJ = 25 °C, unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	1200	V
V_{GE}	Gate-emitter voltage	±20	V
I_{CN}(1)	Continuous collector current at T = 100 °C	35	A
I_{CP}(1)(2)	Pulsed collector current	105	A
t_{sc}(3)	Short-circuit withstand time, V_{CC}= 600 V,V_{GE}= 15 V, $V_{CE(peak)}$ ≤ 1200 V,T_{Jstart} ≤ 150 °C	10	µs
T_J	Operating junction temperature range	-55 to 175	°C

Notes:

(1)Nominal collector current for die packaged in ST power module solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.

(2)Pulse width limited by maximum junction temperature.

(3)Not tested at chip level, verified by design/characterization.

Table 4: Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C = 1 mA, V_{GE} = 0 V	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 15 A			1.9	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{CE} = 1200 V, V_{GE} = 0 V			100	µA
I_{GES}	Gate-emitter leakage current	V_{GE} = ±20 V, V_{CE} = 0 V			±500	nA

Table 5: Electrical characteristics (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 35 A	-	1.95	-	V
		V_{GE} = 15 V, I_C = 35 A, T_J = 150 °C	-	2.3	-	V
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	2154	-	nF
C_{oes}	Output capacitance		-	164	-	nF
C_{res}	Reverse transfer capacitance		-	86	-	nF
Q_g	Total gate charge	V_{CC} = 960 V, I_C = 35 A, V_{GE} = -15 to 15 V	-	163	-	nC

Table 6: Switching characteristics on inductive load (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CE} = 600 V, I_c = 35 A, V_{GE} = ±15 V, R_G = 10 Ω	-	127	-	ns
t_r	Current rise time		-	18.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	135	-	ns
t_f	Current fall time		-	133	-	ns
E_{off}(1)	Turn-off switching energy		-	1.83	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, I_c = 35 A, V_{GE} = ±15 V, R_G = 10 Ω, T_J = 150 °C	-	125	-	ns
t_f	Current rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	140	-	ns
t_f	Current fall time		-	2.84	-	ns
E_{off}(1)	Turn-off switching energy		-	2.85	-	mJ

Notes:

(1)Including the tail of the collector current.

Switching characteristics and thermal properties are strongly dependent on module design and mounting technology.

3 Chip layout

Figure 1: Die outline and dimensions (in mm)

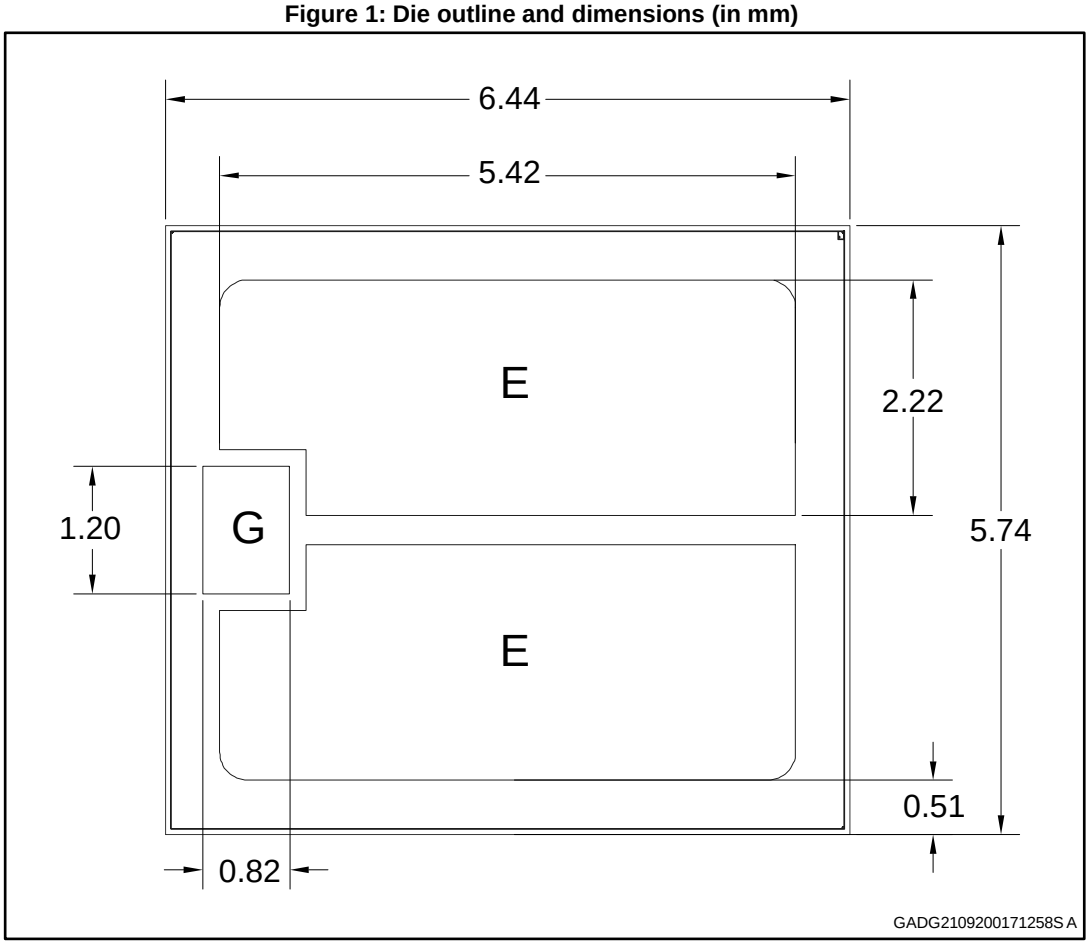


Table 7: Die delivery

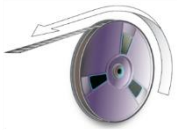
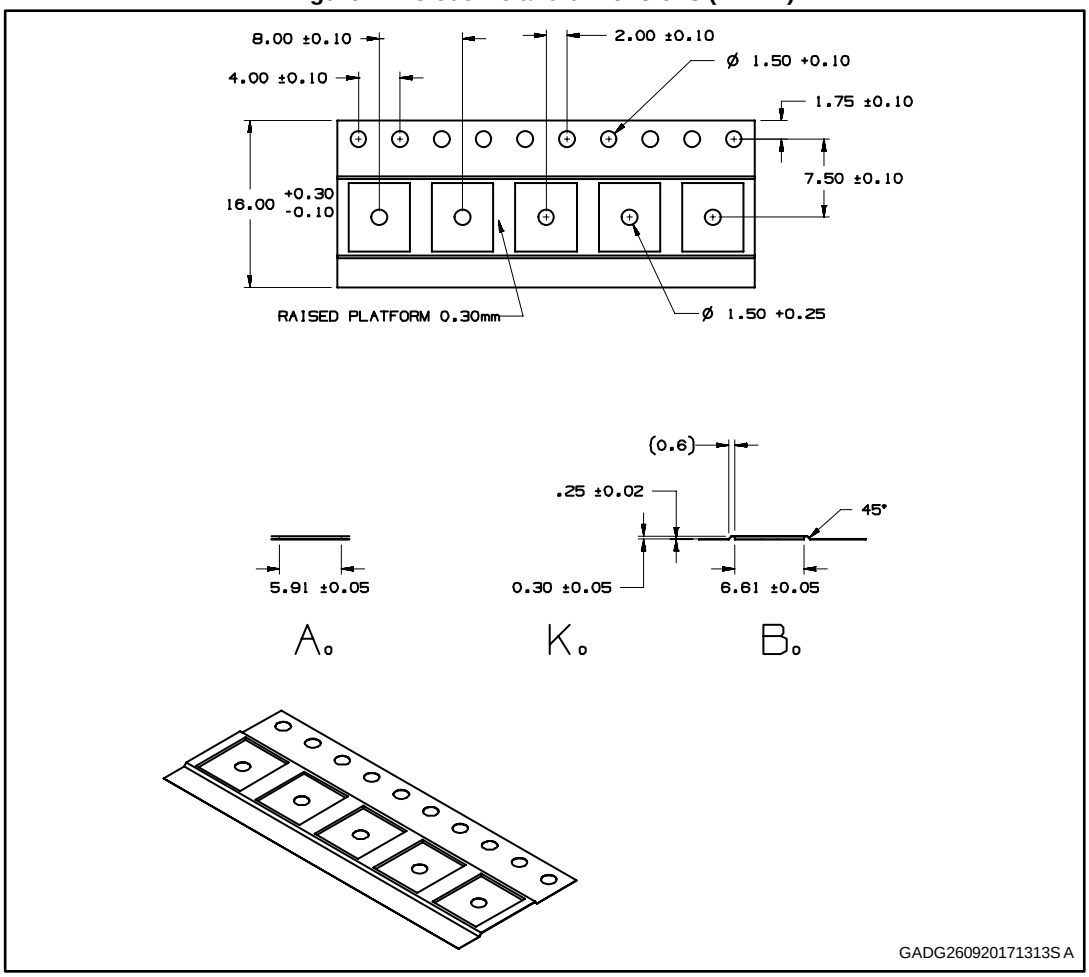
Package option	Test conditions	Details
D8	Wafer (8 inches) tested, inked, cut and each die is picked up and submitted to an automatic visual inspection on back side. Each die is tested and again submitted to visual inspection on both top and back side. Finally each die is placed inside reel pocket, again submitted to a top side visual inspection and sealed with a cover tape	

Figure 2: D8 outline and dimensions (in mm)



4 Additional information

4.1 Additional testing and screening

For customers requiring products supplied as known good die (KGD) or requiring specific die level testing, please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

4.3 Handling

- Products must be handled at ESD safe workstations only. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263
- Products must be handled in a class 1000 only or better designated clean room environment
- Singular die is not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used

4.4 Wafer/die storage

Once packaging is opened, it can be stored at 21 °C ±3 °C for 1 year after shipment and dice must be stored in a dry, inert atmosphere, such as nitrogen. After the customer opens the package, the customer is responsible for the products. The above storage conditions come from "JEDEC Standard JESD 49 Procurement Standard for Known Good Die”.

5 Revision history

Table 8: Document revision history

Date	Revision	Changes
23-Jan-2015	1	Initial release.
07-Sep-2016	2	Updated features in cover page. Updated *Table 3.: Absolute maximum ratings (T_J = 25 °C, unless otherwise specified)* and *Table 5.: Electrical characteristics.* Minor text changes.
21-Sep-2017	3	Modified title, features and description. Modified *Table 2: "Mechanical parameters"*, *Table 3: "Absolute maximum ratings (T_J = 25 °C, unless otherwise specified)"*, *Table 4: "Static characteristics (tested on wafer unless otherwise specified)"*, *Table 5: "Electrical characteristics (not tested at chip level, verified by design/characterization)"* and *Table 6: "Switching characteristics on inductive load (not tested at chip level, verified by design/characterization)".* Modified *Figure 1: "Die outline and dimensions (in mm)"*. Added *Figure 2: "D8 outline and dimensions (in mm)"*. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.